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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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TLE7242-2G

4 Channel Fixed Frequency Constant Current Control IC

Automotive Power

Never stop thinking

Table of Contents

4 Channel Fixed Frequency Constant Current Control IC **TLE7242-2G**

1 Overview

PG-DSO-28

1.1 Features

- Low side constant current control pre-driver integrated circuit
- Four independent channels
- Output current programmable with 11 bit resolution
  - Current range = 0 to 1.2A (typ) with a 0.2 Ω sense resistor
  - Resolution = 0.78125 mA/bit (typ) with a 0.2 Ω sense resistor
  - +/- 2% full scale error over temperature when autozero is used
- Programmable PWM frequency via SPI from approximately 50 Hz to 4 KHz (typ)
- Programmable KP and KI coefficients for the PI controller for each channel
- Programmable Transient Mode of operation to reduce settling time when large changes in the current set point are commanded.
- Programmable superimposed dither.
  - Dither programmed by setting a dither step size and the number of PWM periods in each dither period
  - Programmed via the SPI interface
  - The dither for each channel can be enabled and programmed independently
- Programmable synchronization of the PWM control signals.
  - Phase delay time set via the SPI interface
  - Synchronization initiated via signal at the PHASE_SYNC input pin.
  - Channels within one device and between multiple devices can be synchronized.
- Each channel can be configured to function as a simple on/off predriver or a constant current predriver via SPI
- Interface and Control
  - 32 Bit SPI (Serial Peripheral Interface) - Slave only
  - ENABLE pin to disable all channels or freeze all channels
  - Active low RESET_B pin resets internal registers to their default state and disables all channels.
  - Open drain FAULT pin can be programmed to transition low when various faults are detected.
  - 5.0V and 3.3V logic compatible I/O
- Protection
  - Over current shutdown - monitored at POSx pin.
  - Programmable over current threshold
  - Programmable over current delay time
  - Programmable over current retry time
  - Battery pin (BAT) overvoltage shutdown.
- Diagnostics
  - Over current

Type	Package	Marking
TLE7242-2G	PG-DSO-28	TLE7242-2G

  - Open load in on state
  - Open load in off state
  - Short to ground
  - Test complete bit - indicates that fault detection test has completed
- Control loop monitor capabilities
  - The average current measurement over the last completed PWM cycle of each channel can be accessed via SPI.
  - The PWM duty cycle of each channel can be accessed via SPI
  - The auto zero values used to null the offsets of the input amplifiers can be accessed via SPI
- Required External Components:
  - N-Channel Logic level (5V) MOSFET transistor with typical Ron ≤ 100 mΩ (e.g. BSO604NS2)
  - Recirculation diode (ultrafast)
  - Sense resistor (0.2Ω for 1.2A average output current range)
- Green Product (RoHS compliant)
- AEC Qualified

1.2 Applications

- Variable Force Solenoids (e.g. automatic transmission solenoids)
- Other constant current solenoids
  - Idle Air Control
  - Exhaust Gas Recirculation
  - Vapor Management Valve
  - Suspension Control

1.3 General Description

The TLE7242 2G IC is a four channel low-side constant current control predriver IC. Each channel can be configured to function either in on/off mode or in constant current mode by setting the appropriate MODE bit in SPI message #7.

1.3.1 On / Off Mode Operation

For On/Off operation, the POSx and NEGx pins must be connected to the circuit in either of the configurations shown in **Figure 1**. If the sense resistor is included, the load current can be monitored by the microcontroller via a SPI command. The open load in on state fault detection feature is disabled in on/off mode.

Note: An external flyback clamp is required in this configuration otherwise the IC may be damaged.

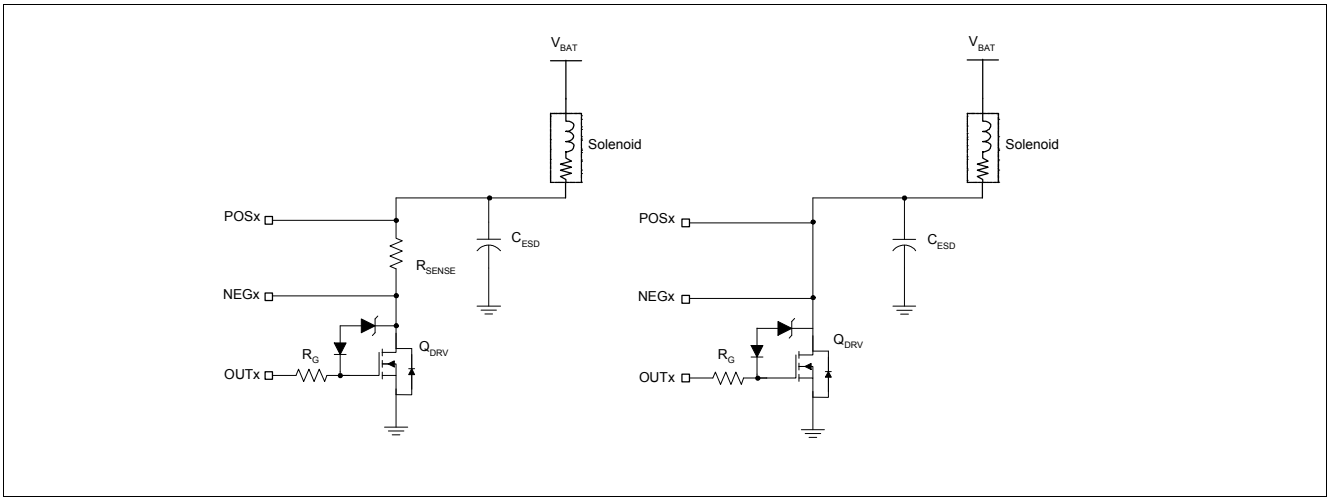

Figure 1 External Circuit Diagram for On/Off Mode Operation

1.3.2 Constant Current Mode Operation

During constant current operation, the POSx and NEGx pins must be connected to the circuit in the configuration shown in **Figure 2**.

Note: An external recirculation diode is required in this configuration otherwise the IC may be damaged.

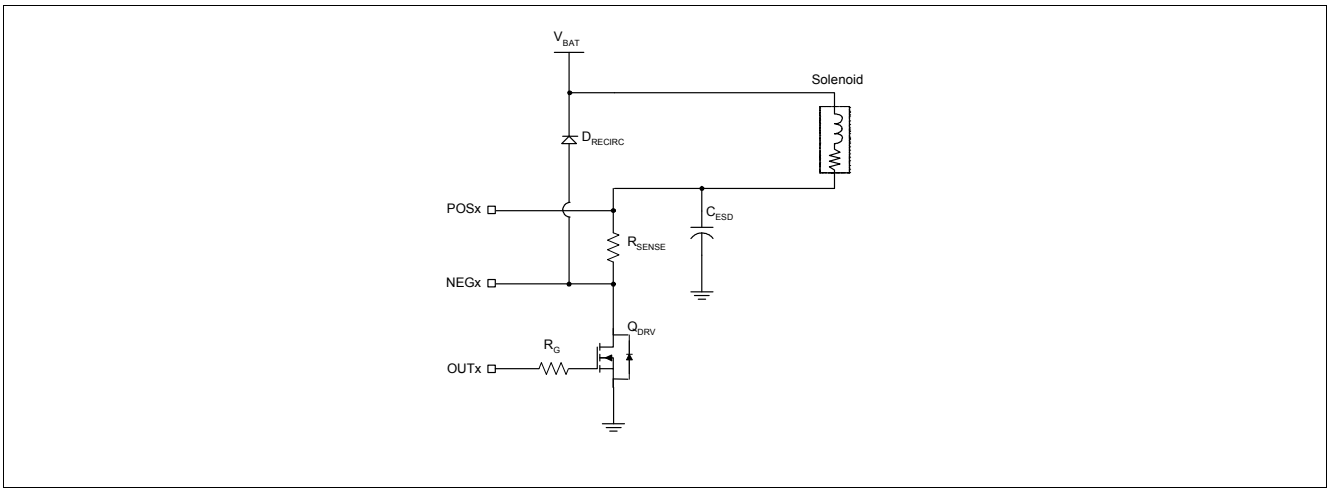

Figure 2 External Circuit Diagram for Constant Current Mode Operation

The constant current control circuit can operate in two modes; steady state mode and transient mode.

Steady-State Mode

During steady-state operation, the PWM control signal driven at the OUTx pin is controlled by the control loop shown in **Figure 3**. The PWM Frequency is programmed via the SPI message # 1. In this message the main period divider, N, can be set to any value between 79 and 2^{14} -1. The equation for calculating the PWM frequency is:

$$F_{PWM} = \frac{F_{CLK}}{32 * N}$$

The 11 bit Current Set Point is programmed via the SPI message #3. The equation for calculating the current setpoint is:

$$Current_{setpoint}\,[mA] = \frac{setpoint(11bit)}{2^{11}} * \frac{320}{R_{SENSE}}$$

The Proportional coefficient (KP) and the Integral coefficient (KI) of the control loop are programmed in SPI message #5. The KP and KI values should be set to values that result in the desired transient response of the control loop. The duty cycle of the OUTx pin can be calculated from the difference equations:

$$DutyCycle\ (k) = KP * \frac{Rsense}{1.28 * N} * error\ (k-1) + INT\ (k)$$

$$INT\ (k) = KI * \frac{Rsense}{1.28 * N} * error\ (k-1) + INT\ (k-1)$$

where error is the difference between the commanded average current and measured average current in units of Amps.

where k indicates the integral number of PWM periods that have elapsed since current regulation was initiated.

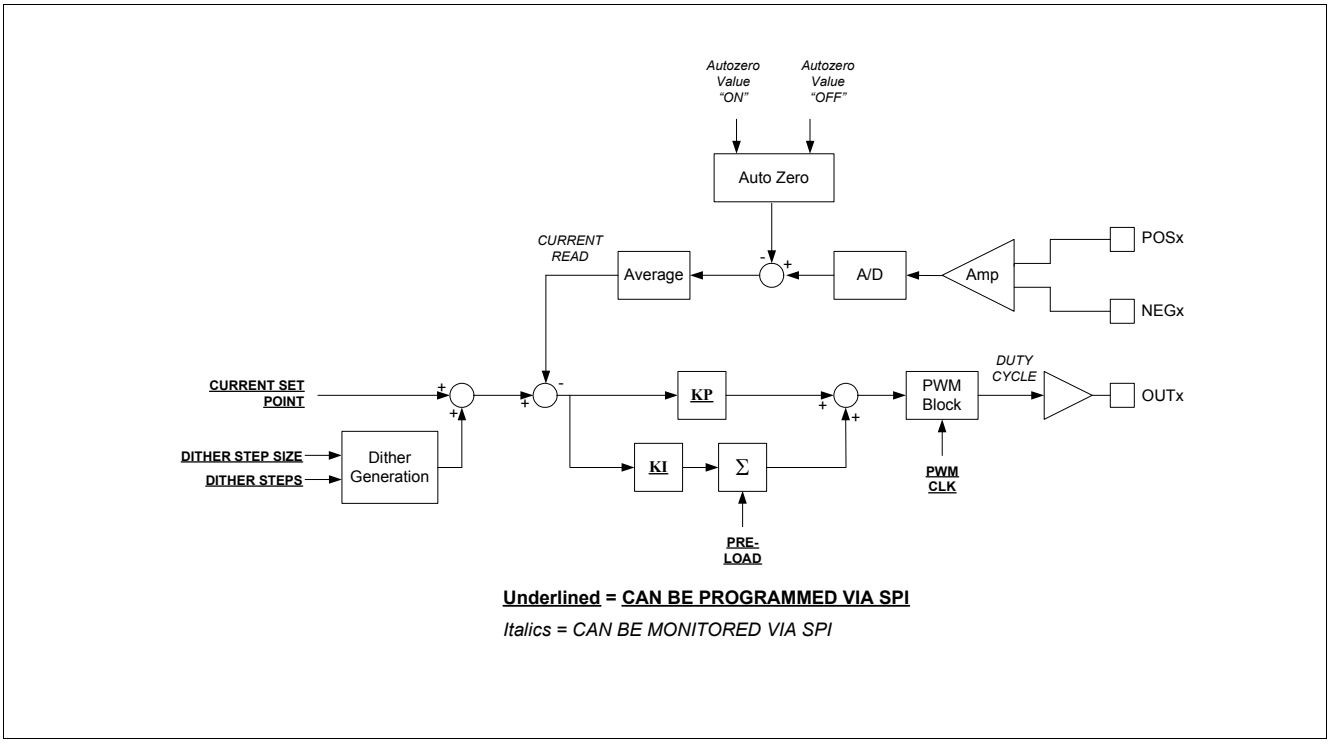

Figure 3 Control Loop - Steady-State Mode

Auto Zero

When a channel is configured for constant current operation and the current set point is 000h for 256 consecutive PWM periods, an autozero sequence is initiated. The autozero sequence will measure the offset of the current

measurement amplifiers. If the autozero function is enabled in SPI message #7, then the measured offset will be subtracted from the A/D converter output as shown in **Figure 3** when the current set point is greater than 0.

Dither

A triangular dither waveform can be superimposed on the current set point by setting the Dither Enable bit in SPI message #3. The amplitude and frequency of the dither waveform are programmed for each channel via SPI messages #3 and #4. See the SPI message section for details.

The first programmed value is the step size of the dither waveform which is the number of bits added or subtracted from the setpoint per PWM period. One LSb of the dither step size is 1/16 the magnitude of the nominal setpoint current value. The second programmed value is the number of steps in one quarter of the dither waveform.

When dither is enabled, a new dither amplitude setting, a new dither frequency setting, or a dither disable command will not be activated until the current dither cycle has completed - see **Figure 4**. The dither cycle is completed on the positive zero crossing of the dither waveform. A change in the setpoint current, however, is activated at the start of the next PWM period.

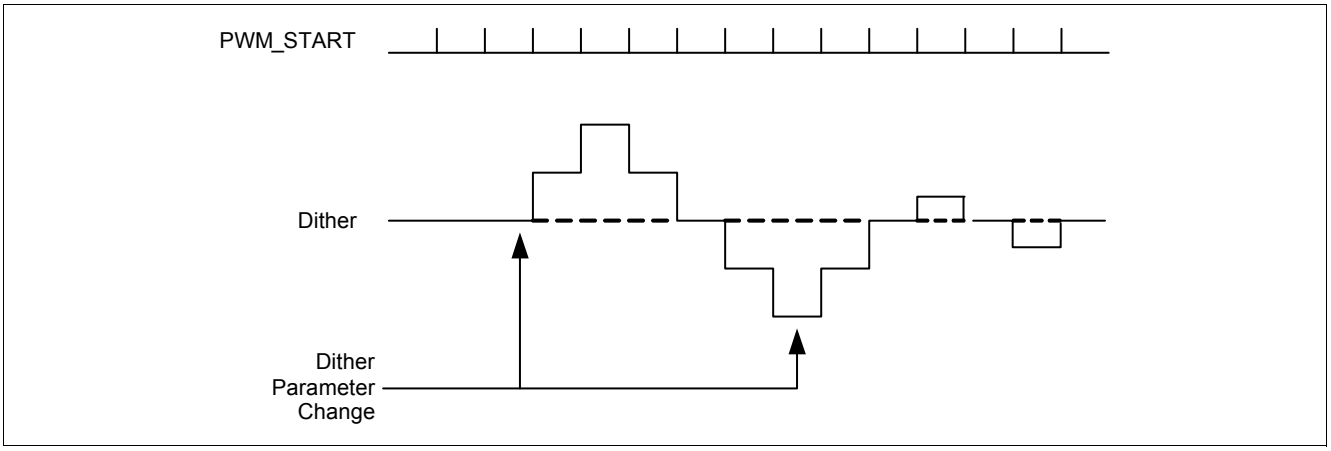

Figure 4 New Dither Values Programmed and the Resultant Waveform Timing

Note: the actual dither waveform is attenuated and phase shifted according to the frequency response of the control loop.

If a channel enters transient mode operation while the dither waveform is active, the dither wave-form will pause until transient mode is exited.

Transient Mode

When a large change in the current set point occurs, the device can be programmed to enter transient mode of operation. The setpoint change threshold required to initiate transient mode can be programmed in SPI message #6. The purpose of this mode of operation is to reduce the transition time of the load current after a large change in setpoint. In this mode of operation the OUTx pin signal is controlled by the state machine shown in **Figure 5**. The control method in this mode is similar to hysteretic control, the OUTx signal transitions high or low based on the immediate value of the measured output current. The PWM frequency is not fixed in this mode of operation. The device will automatically switch from transient mode of operation to steady state operation at the start of the first PWM period after the new set point has been reached.

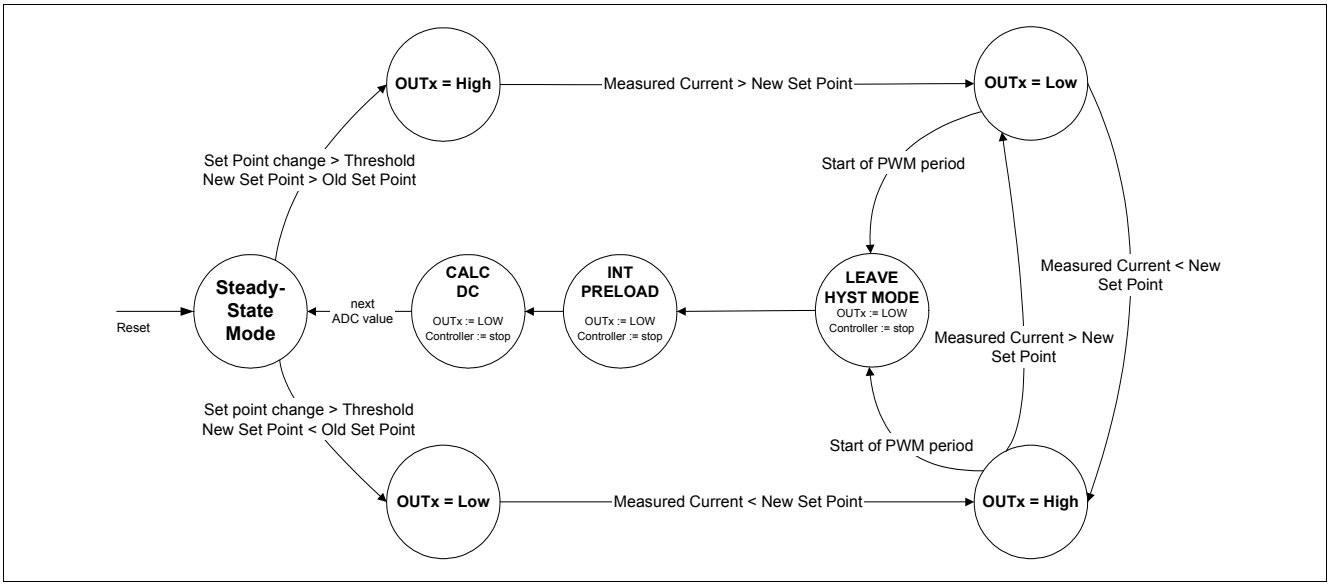

Figure 5 Transient Mode State Diagram

A typical current waveform during transient mode operation is shown in **Figure 6**. Starting from a set point I, the new set point II is accepted a short time after the rising edge on CS_B. The OUTx pin remains high until the measured load current has reached the new set point. The OUTx pin is then toggled on and off to maintain the load current near the new set point until the next PWM period begins. The device will then switch back to steady state control and the OUTx pin will be controlled by the control loop shown in **Figure 3**.

During the transition from transient mode operation to steady state operation, the integrator is pre-loaded with a SPI programmable value. This value should be chosen to give an initial PWM duty cycle approximately equal to the duty cycle required to regulate the load current at the new set point.

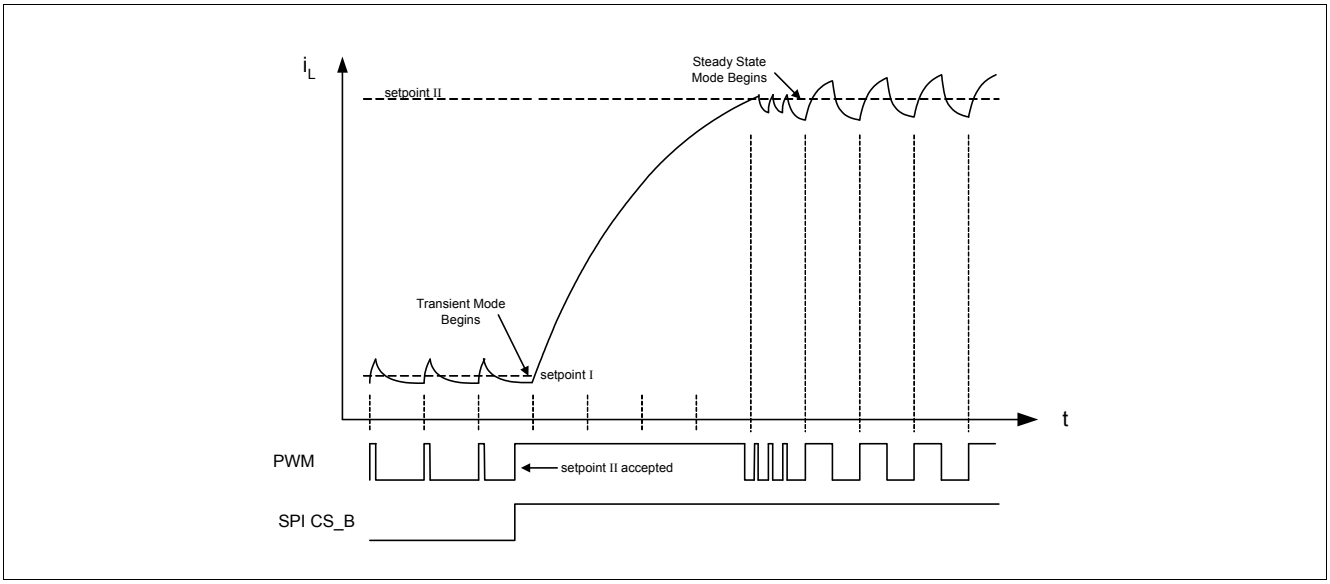

Figure 6 Transient Mode Timing Diagram

2 Block Diagram

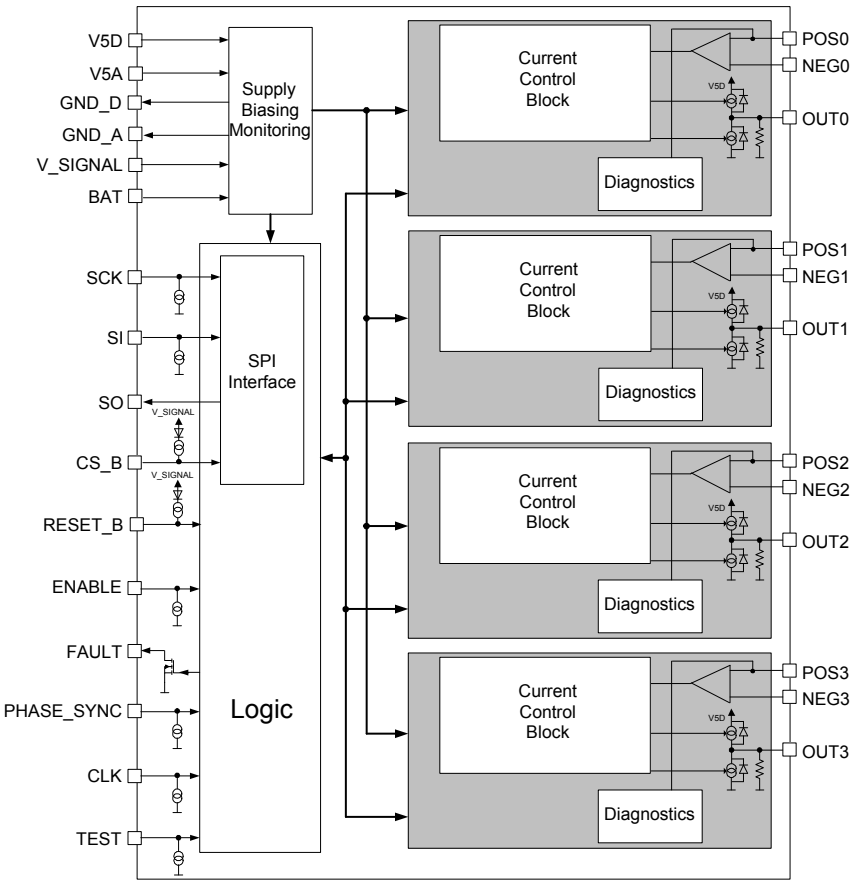

Figure 7 Block Diagram

3 Pin Configuration

3.1 Pin Assignment

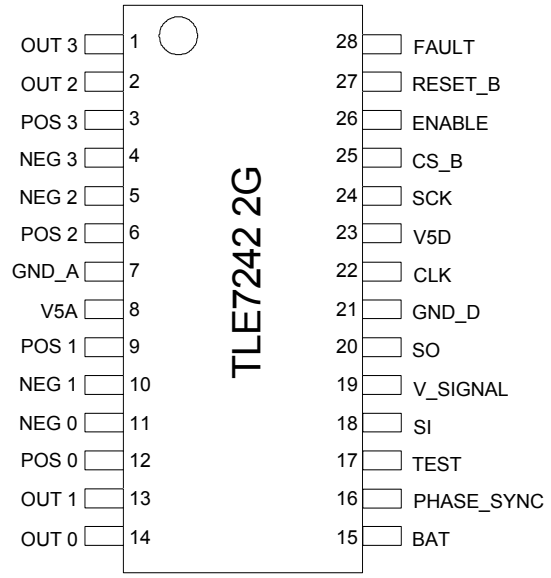

Figure 8 Pin Configuration

3.2 Pin Definitions and Functions

Pin	Symbol	I/O	Analog /Digital	Function
1	OUT3	O	A	Gate driver output for channel #3. Connect to the gate of the external MOSFET.
2	OUT2	O	A	Gate driver output for channel #2. Connect to the gate of the external MOSFET.
3	POS3	I	A	Channel #3 Positive sense pin. Connect to the "load" side of the external sense resistor.
4	NEG3	I	A	Channel #3 Negative sense pin. Connect to the "FET" side of the external sense resistor.
5	NEG2	I	A	Channel #2 Negative sense pin. Connect to the "FET" side of the external sense resistor.
6	POS2	I	A	Channel #2 Positive sense pin. Connect to the "load" side of the external sense resistor.
7	GND_A	-	-	Analog Ground
8	V5A	-	-	5V supply pin for analog. An external capacitor is to be connected between this pin and GND_A near this pin.
9	POS1	I	A	Channel #1 Positive sense pin. Connect to the "load" side of the external sense resistor.

Pin	Symbol	I/O	Analog /Digital	Function
10	NEG1	I	A	Channel #1 Negative sense pin. Connect to the "FET" side of the external sense resistor.
11	NEG0	I	A	Channel #0 Negative sense pin. Connect to the "FET" side of the external sense resistor.
12	POS0	I	A	Channel #0 Positive sense pin. Connect to the "load" side of the external sense resistor.
13	OUT1	O	A	Gate driver output for channel #1. Connect to the gate of the external MOSFET.
14	OUT0	O	A	Gate driver output for channel #0. Connect to the gate of the external MOSFET.
15	BAT	I	A	Battery sense input for over voltage detection. Connect through a series resistor (e.g. 1 Kohm) to the solenoid supply voltage. A large electrolytic capacitor (e.g. 47uF) should be placed between the BAT supply and ground.
16	PHASE_SYNC	I	D	Used to synchronize the rising edges of the PWM signal on the OUTx pins for each channel.
17	TEST	I	D	Used for IC Test. Must be connected to GND_D for specified operation of the IC.
18	SI	I	D	SPI Serial data in
19	V_SIGNAL	I	-	Supply pin for the SPI SO output and the pull-ups of the digital inputs CS_B and RESET_B. An external capacitor must be connected between this pin and GND_D near this pin.
20	SO	O	D	SPI Serial data out
21	GND_D	-	-	GND pin for digital and driver circuitry.
22	CLK	I	D	Main clock input for the IC. A clock input of 20 MHz to 40 MHz is required.
23	V5D	-	-	5V supply pin for the digital circuit blocks and the OUT pin driver circuits. A pair of external capacitors is to be connected between this pin and GND_D very near this pin. Example values of the external capacitors are 100nF and 100pF.
24	SCK	I	D	SPI Clock input
25	CS_B	I	D	SPI Chip Select Bar (low active signal)
26	ENABLE	I	D	When this input pin is low all channels are turned off (zero current) or remain in their last state, depending on how the channel is programmed to respond
27	RESET_B	I	D	When this input pin is low all channels are turned off and all internal registers are reset to their default state. The part must be held in reset by an external source until all supplies are stable and within tolerance.
28	FAULT	O	D	This open drain output pin is pulled low when a fault condition is detected. Certain faults can be masked via SPI.

4 General Product Characteristics

4.1 Maximum Ratings

Absolute Maximum Ratings [1)]

T_j = -40 ·C to +150 ·C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
Voltages						
4.1.1	Battery Input (VBAT)	V_{BAT}	-13	50	V	–
4.1.2	Supply Voltage (logic)	$V_{5D}, V_{5A}, V_{signal}$	-0.3	6.0	V	–
4.1.3	POSx, NEGx	V_{pos}, V_{neg}	-0.3	50	V	–
4.1.4	POSx-NEGx	V_{pos}-V_{neg}	-0.2	13	V	–
4.1.5	OUTx	V_{out}	-0.3	min(V_{5D}+ 0.3; 6)	V	–
4.1.6	RESET_B, SI, SCK, CS_B, CLK, TEST, PHASE_SYNC, ENABLE	V_{io}	-0.3	min(V_{5D}+ 0.3; 6)	V	–
4.1.7	SO, FAULT	V_{io}	-0.3	min(V_{signal} + 0.3; 6)	V	–
4.1.8	Maximum difference between V5D and V5A		-500	500	mV	–
Currents						
4.1.9	Input Clamp Current	I_{CLAMP}	5	–5	mA	–
Temperatures						
4.1.10	Storage Temperature	T_{stg}	-65	150	°C	–
4.1.11	Junction Temperature	T_j	-40	150	°C	–
ESD Susceptibility						
4.1.12	HBM	–	-2	2	kV	2)
4.1.13	CDM all pins	–	-500	500	V	3)
4.1.14	CDM corner pins	–	-750	750	V	3)

1) Not subject to production test, specified by design.

2) ESD Susceptability HBM according to EIA/JESD 22-A 114B

3) ESD Susceptability CDM according to EIA/JESD22-C101

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

4.2 Functional Range

T_j = -40 ·C to +150 ·C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
4.2.1	Supply Voltage (VBAT) - Full Parametric Operation on all functions except FET Pre-drivers	V_{BAT}	5.5	42	V	–
4.2.2	Supply Voltage (V5D)	V_{V5D}	4.75	5.25	V	–
4.2.3	Supply Voltage (V5A)	V_{V5A}	4.75	5.25	V	–
4.2.4	V_SIGNAL	V_{V_SIGNAL}	3.0	5.25	V	–
4.2.5	Clock Frequency	f_{CLK}	20	40	MHz	
4.2.6	PWM Frequency	f_{PWM}	50	4000	Hz	
4.2.7	Common Mode Voltage on POSx, NEGx pins	V_{pos} , V_{neg}	–	42	V	–

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

4.3 Thermal Resistance

T_j = -40 ·C to +150 ·C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
4.3.1	Junction to Ambient	R_{thJA}	–	50	–	K/W	1)

1) Specified R_{thJA} value according to natural convestion on FR4 2s0p board; The Product (Chip + Package) was simulated on a 60.0 X 45.0 X1.5 mm board (2 X 70um).

5 Functional Description and Electrical Characteristics

Note: The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at T_A = 25 °C and the given supply voltage.

5.1 Supply and Reference

The device includes a power-on reset circuit. This feature will disable the channels and reset the internal registers to their default values when the voltage on V5A and/or V5D are below their respective reset thresholds.

The V5D pin and GND_D pin are the supply and ground pins for the digital circuit blocks and the OUTx pin driver circuits. The current through these pins contain high frequency components. Decoupling with ceramic capacitors and careful PCB layout are required to obtain good EMC performance.

The V5A pin and GND_A pin are the supply and ground pins for the analog circuit blocks.

The V_SIGNAL pin supplies the SPI output pin (SO) and is the source voltage for the pull up currents on the CS_B and RESET_B pins. V_SIGNAL should be connected to the I/O supply of the microcontroller (3.3V or 5.0V).

The BAT pin is an input pin used to detect over voltage faults. This pin is not a power supply input. A series resistor should be connected between this pin and the solenoid supply voltage for transient protection.

Electrical Characteristics:

V5D = 4.75V to 5.25V, Vbat = 5.5V to 42V, T_j = -40 ·C to +150 ·C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.1.1	Undervoltage reset (internally triggered)	V_{V5A}	3.5	–	4.5	V	Internal reset occurs if V5A is under the undervoltage limit
5.1.2	Undervoltage reset (internally triggered)	V_{V5D}	1.0	–	4.5	V	Internal reset occurs if V5D is under the undervoltage limit
5.1.3	V5D supply current	I_{V5D}	–	–	30 50	mA mA	f_{CLK}=20MHz f_{CLK}=40MHz
5.1.4	V5A supply current	I_{V5A}	–	–	25	mA	
5.1.5	V_SIGNAL supply current	I_{V_SIGNAL}	–	–	1.0	mA	SO pin in hi-Z state, digital inputs in default state
5.1.6	VBAT current	I_{VBAT}	–	–	150 50 5	µA µA µA	full operating range V5A=5V, BAT=14V[1)] V5A=0V, BAT=14V[1)]

1) Not subject to production test, specified by design.

5.2 Input / Output

All digital inputs are compatible with 3.3 V and 5 V I/O logic levels. The supply voltage for the SPI output SO is the V_SIGNAL pin. All digital inputs are pulled to a known state by a weak internal current source or current sink when not connected. However, unused digital input pins should be connected to ground or to V_SIGNAL (according to the desired functionality) by an external connection or resistor. All input pin weak internal current sources are supplied by the V_SIGNAL pin.

The RESET_B pin is an active low input pin. When this pin is low, all channels are off, and all internal registers are reset to their default states. The device must be held in reset by an external source until all the power supplies have stabilized. The IC contains an internal power on and undervoltage reset which becomes active when V5D or V5A fall below the undervoltage reset threshold (VUVA, VUVD).

The ENABLE pin is an active high input pin which must be held high for normal operation of the device. When this pin is held low all channels are either turned off or will remain in the last state, depending on how the enable behavior of the channel is programmed via SPI. The default condition is that all channels are turned off when the ENABLE pin is low.

The CLK pin is the main clock input for the device. The input thresholds are compatible with 3.3 V and 5.0 V logic levels. No synchronization is required between the clock signal connected to the CLK pin and the SPI clock signal (SCK). All frequencies of operation (PWM signals, A/D sampling, diagnostics, etc.) are based on this clock input. Also, this clock is required in order for the device to accept and respond to SPI messages.

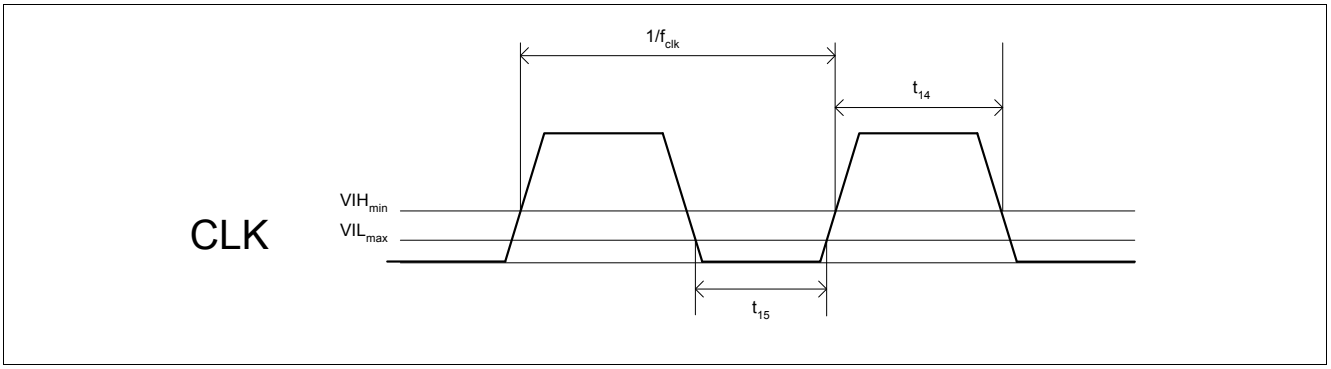

Figure 9 CLK Timing Diagram

The PHASE_SYNC pin is an input pin that can be used by the microcontroller to synchronize the PWM control signals of multiple channels. The desired phase delay between the rising edge of the signal applied to the PHASE_SYNC pin and the rising edge of the PWM signal of each channel can be programmed independently via SPI message #2. The equation for calculating the offset is:

$$T_{offset} = \frac{PhaseSynchOffset}{32 * F_{PWM}}$$

Each time the phase sequence occurs, the IC will latch a bit which is reported via the response to SPI message #11. (See SPI interface section for bit/message location.) This latch is cleared when the message is read.

Note: The PWM periods are restarted when a rising edge is detected on the PHASE_SYNC pin. A periodic pulse train on this pin will disturb the current regulation.

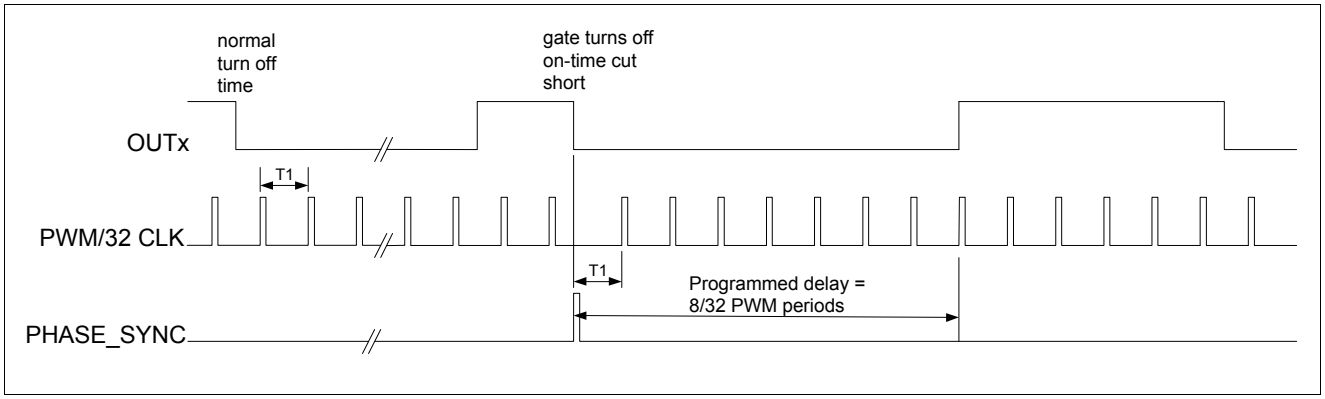

Figure 10 Phase Synchronization Diagram

The TEST pin is an input pin that is used during IC level test. This pin should be connected directly to ground for normal device operation.

The FAULT pin is an open drain output pin. This pin will be pulled low by the device when an unmasked fault has been detected. The fault masks are programmed via SPI message #7.

Electrical Characteristics:

V5D = 4.75V to 5.25V, Vbat = 5.5V to 42V, T_j = -40 ·C to +150 ·C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.2.1	Logic input low voltage	V_{ILMAX}	–	–	0.8	V	
5.2.2	Logic input high voltage	V_{IHMIN}	2.0	–	–	V	
5.2.3	Logic output low voltage	V_{OLMAX}	–	–	0.2	V	I_L=200µA
5.2.4	Logic output high voltage	V_{OHMIN}	0.8*V_ SIGNAL	–	–	V	I_L=-200µA
5.2.5	Pull down digital input (SI, CLK, SCK, PHASE_SYNC, ENABLE, TEST)	I_{pd}	10	–	50	µA	V_{in}=V_SIGNAL (current drain to ground)
5.2.6	Pull up digital input (CS_B, RESET_B)	I_{pu}	-10	–	-50	µA	V_{in}=0V (Current drain from V_SIGNAL)
5.2.7	Fault Pin voltage	V_{fault}	–	–	0.4	V	Active state; I_{fault}=2mA
5.2.8	CLK high time (rise 2.0V to fall 2.0V)	t_{14}	8	–	–	ns	
5.2.9	CLK low time (fall 0.8V to rise 0.8V)	t_{15}	8	–	–	ns	

5.3 Diagnostics

The TLE7242 2G includes both on-state and off-state diagnostics. On-state diagnostics are active when the OUTx pin is driven high and off-state diagnostics are active when the OUTx pin is driven low. A detected fault can be used to activate the open drain FAULT pin on the IC. This pin can be used to interrupt the microcontroller when a

fault is detected. Certain faults can be prevented from activating the FAULT pin by setting the fault mask register in SPI message #7.

Once a fault is detected it is latched into the FAULT register. The microcontroller can access the FAULT register by sending SPI message #9.

If the RESET_B line transitions high-to-low, a RL bit is latched into the FAULT register. The register is cleared after it is read from the SPI. The RL bit in the FAULT register will not be set again until the next high-to-low transition occurs on the RESET_B pin.

If the ENABLE pin voltage is low, the ENL bit is latched in the FAULT register. The ENL bit is cleared when the ENABLE pin returns to a high state and the FAULT register is accessed by SPI message #9.

The diagnostic delay timers for the on-state and off-state diagnostic functions are derived from the master clock signal applied to the pin CLK using a programmable predivider. This predivider is programmable by the DT1 and DT0 bits in SPI message #7.

Table 1 Timebase for Diagnostics

DT1	DT0	Pre-divider	Tested Timer and Fault Detection Timer Period.	
			F_{CLK}=20 MHz	F_{CLK}=40 MHz
0	0	128	64 µsec	32 µsec
0	1	192	96 µsec	48 µsec
1	0	192	96 µsec	48 µsec
1	1	256	128 µsec	64 µsec

$$t_{DIAG\_PERIOD} = \frac{n_{fault} * predivider}{F_{CLK}} \qquad 9 \le n_{fault} \le 10$$

Three fault types in 4 different fault bits are defined:

The fault bit is 1 if the fault is detected.

Table 2 Diagnostic Flags / Bits

Fault Type	Abr.	Gate is ON	Gate is OFF
Short to Ground Fault	SG	OL-ON-F reported (=0 in ON/OFF mode)	Bit SG-F
Short to Battery Fault	SB	Bit SB-F	
Open Load Fault	OL	BIT OL-ON-F (=0 in ON/OFF mode)	Bit OL-OFF-F

Note: In order to differentiate between a Short to Ground Failure and an Open Load Failure, the channel must be turned off (setpoint = 0ma).

Tested Diagnostic Bits

The tested bits allow the distinction between a true No Fault and a No Fault due to an untested state (the detection interval has yet to occur). For instance when the calculated duty cycle is too low to complete the short to battery test.

Two fault tested bits are defined:

The tested bit is set to 1 when the fault test has completed successfully.

Table 3 Diagnostics Tested Bits / Flags

Tested Type	OUTx High	OUTx Low
Short to Ground and Open load OFF tested		Bit OFF-T
Short to Battery tested	Bit SB-T	

Each fault type can be described by the two bits: FAULT and TESTED.

Table 4 FAULT vs. TESTED Bits Matrix and Interpretation

FAULT	TESTED	Interpretation by microcontroller
0	0	This fault type has not been tested
0	1	No Fault - The fault type has been tested and no fault is present
1	0	This combination cannot occur
1	1	Fault - This particular fault type has occurred

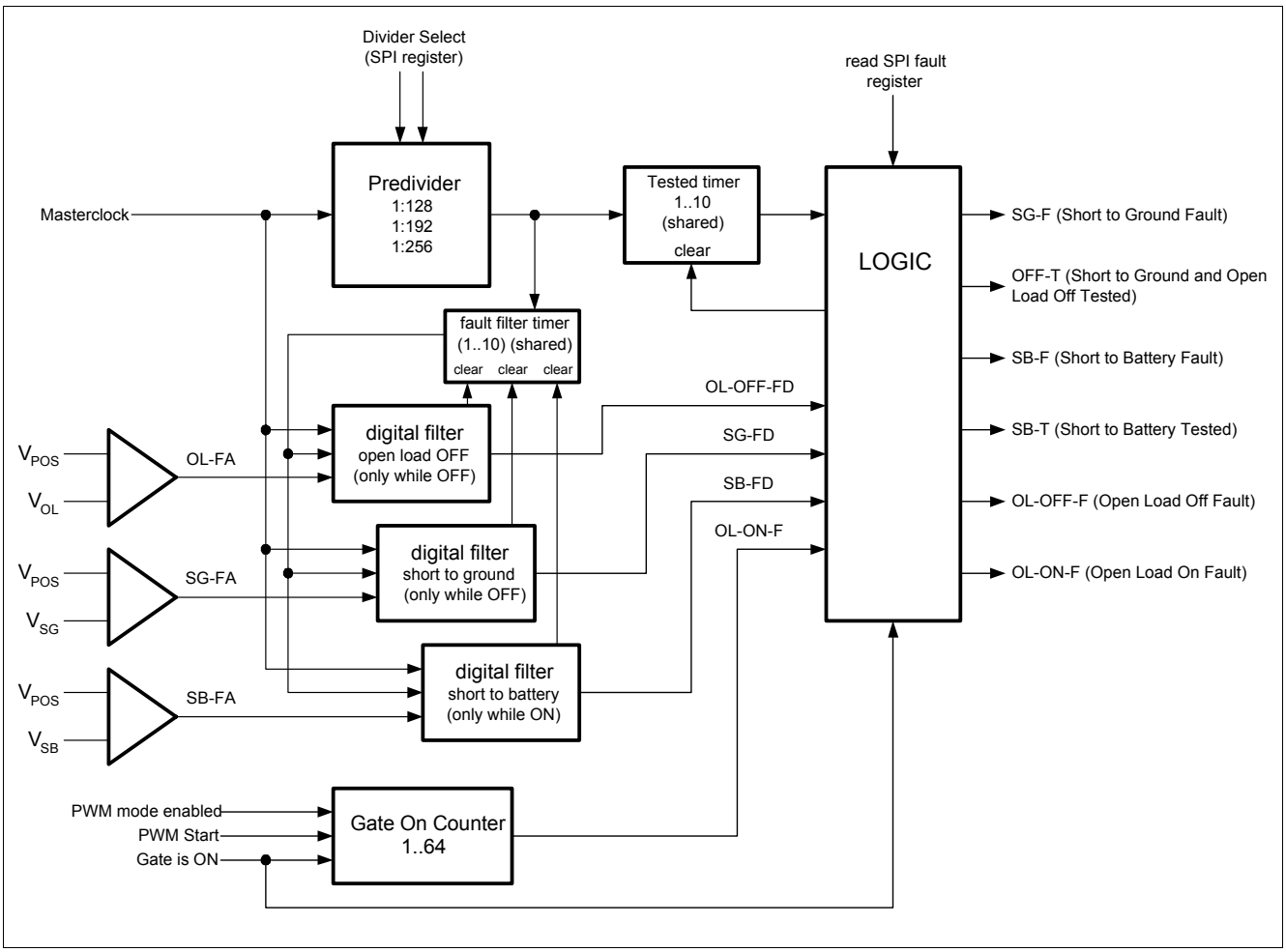

Figure 11 Diagnostic Block Diagram

5.3.1 On-State Diagnostics

When the OUTx pin transitions high, the fault timers are cleared to 0 and the tested timer starts. If the tested timer expires, the Bit SB-T (in the SPI register #9) is set to 1. If the OUTx pin transitions low, the tested timer is cleared and then used for the off-state diagnostics.

If the analog SB fault signal (SB-FA) changes to 1, the fault filter timer starts. If the fault filter timer expires, the digitally filtered SB fault signal (SB-FD) is set to one. If SB-FA changes to 0, SB-FD changes immediately to 0 and the filter timer is cleared to 0.

A SB-FD=1 and SB-T=1 switches off the OUTx signal and the SB-F bit in the FAULT register will be set. The OUTx pin remains in the off state until the fault retry PWM period counter expires.

If the SPI fault register is read, then the SB-F bit and the SB-FT bit in the FAULT register are cleared. Also, the tested timer is cleared to 0.

The Short to Battery (SB) detection functions in both on/off and constant current mode. The SG-FD and OL-OFF-FD signals are held to 0 while the OUTx pin is high.

If the TLE7242 2G IC is in ON/OFF mode, Open Load ON detection is disabled (OL-ON-F = 0).

If the TLE7242 2G IC is not in ON/OFF mode and the OUTx pin is high for 64 PWM periods, then open load fault ON mode is detected and the OL-ON-F bit in the FAULT register is set. This bit will be cleared when a SPI fault read occurs. If the OUTx pin remains in a high state, then the open load - on fault condition is detected again after another 64 PWM cycles.

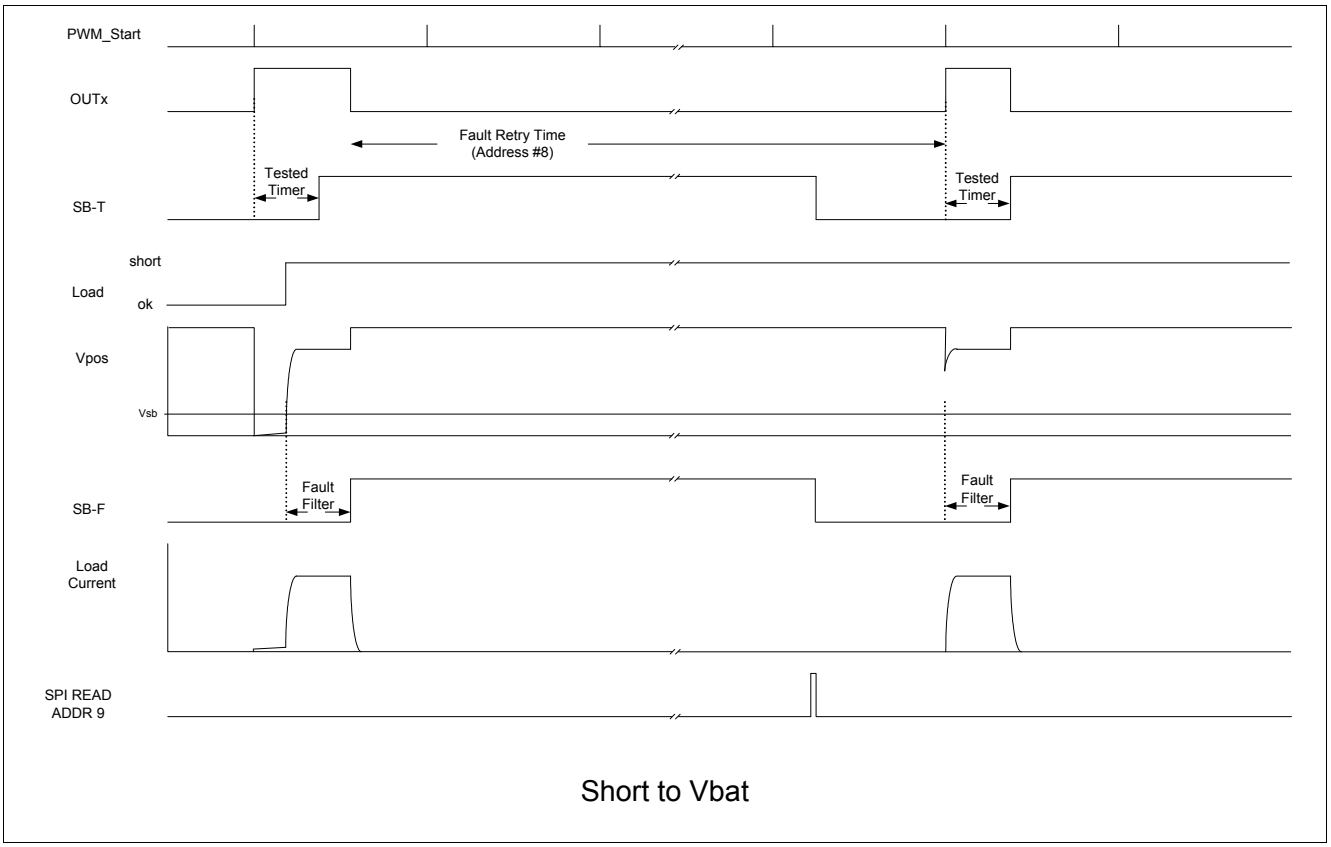

Figure 12 On-State Diagnostic Timing - Short to Vbat

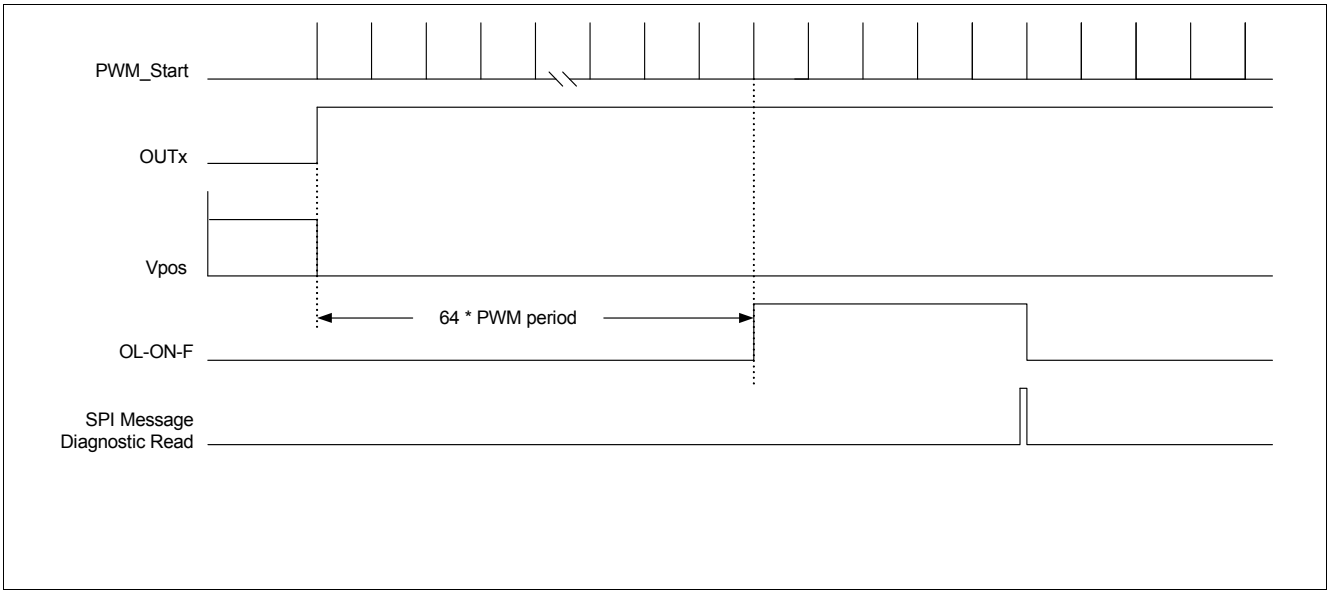

Figure 13 Open - On

5.3.2 Off-State Diagnostics

The off-state diagnostics function in both constant current mode and in on/off mode.

When the OUTx pin transitions low, the fault timers are cleared to 0 and the tested timer starts to count up. If the tested timer expires, the Bit OFF-T in the FAULT register is set. If a SPI fault register read occurs, the tested timer is cleared to 0 and starts again to count up. If the OUTx pin transitions high, the tested-timer is cleared to zero and then used for on-state diagnostics.

If the analog OL fault signal (OL-FA) changes to 1, the fault filter timer starts to count up. If the fault filter timer expires, the digitally filtered OL fault signal (OL-ON-FD) is set to one.

If OL-FA changes to 0, OL-FD changes immediately to 0 and the fault filter timer is cleared to 0.

If the analog SG fault signal (SG-FA) changes to 1, the fault filter timer is cleared to 0 and starts to count up. If the fault filter timer expires, the digitally filtered SG fault signal (SG-FD) is set to one. If SG-FA changes to 0, SG-FD changes immediately to 0 and the fault filter timer is cleared to 0.

If SG-FD = 1 and the tested timer is expired then the SG-F bit in the FAULT register is set and the OL-OFF-F bit in the FAULT register remains unchanged (independently from OL-OFF-FD).

If SG-FD = 0 and OL-OFF-FD = 1 then the OL-F Bit in the FAULT register is set.

If a SPI fault read occurs, the OFF-T Bit, the SG-F Bit and the OL-F Bit in the SPI registers are cleared to zero (and the timers are cleared to 0).

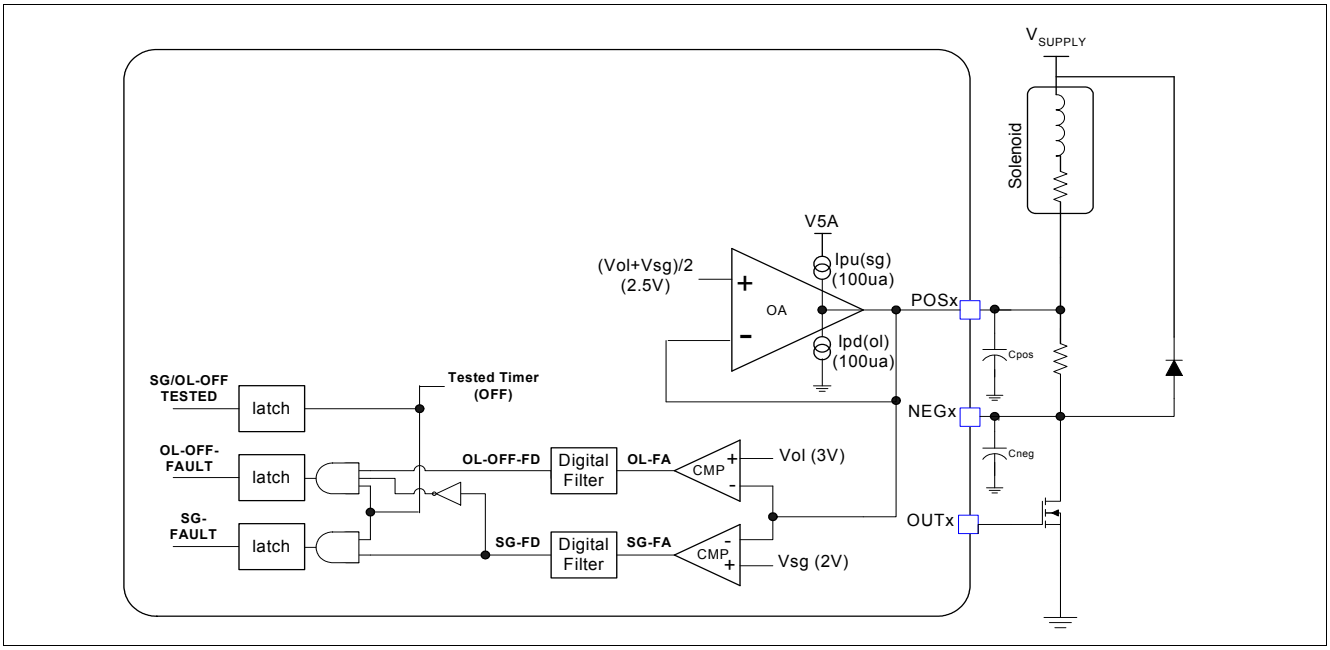

Figure 14 Off-State Diagnostics

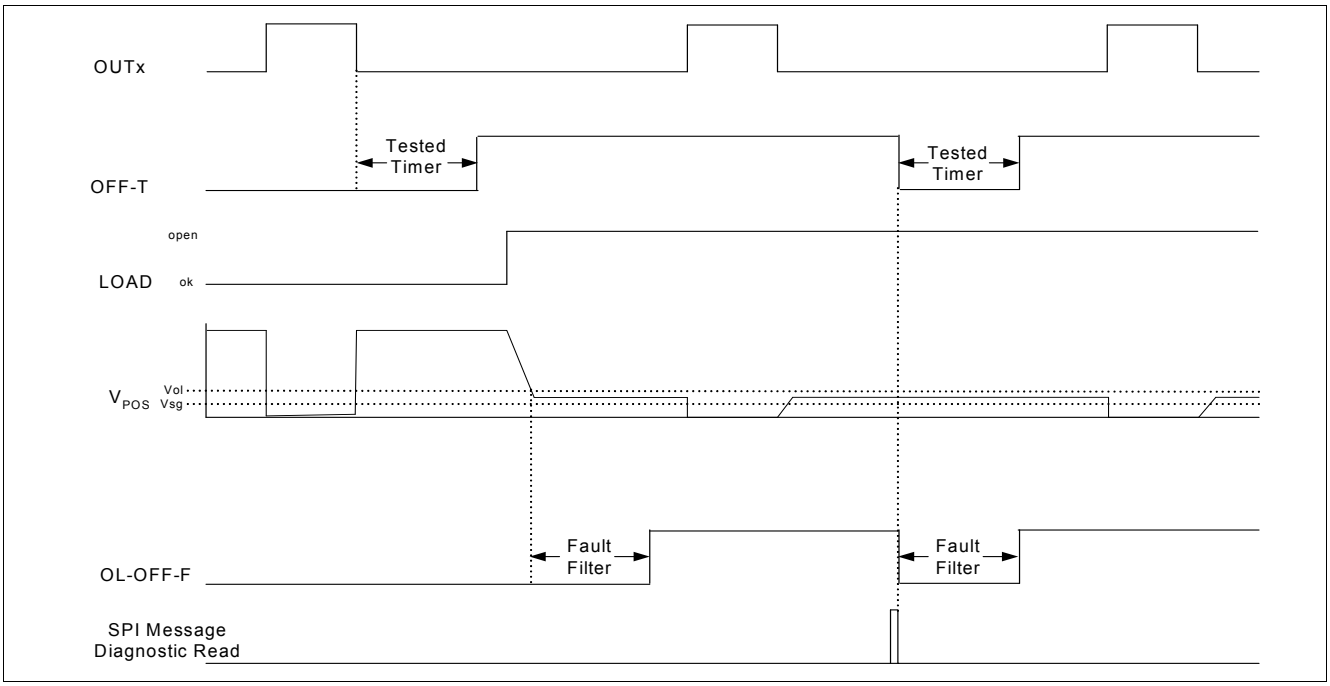

Figure 15 Off-State Diagnostics Timing Diagram - open

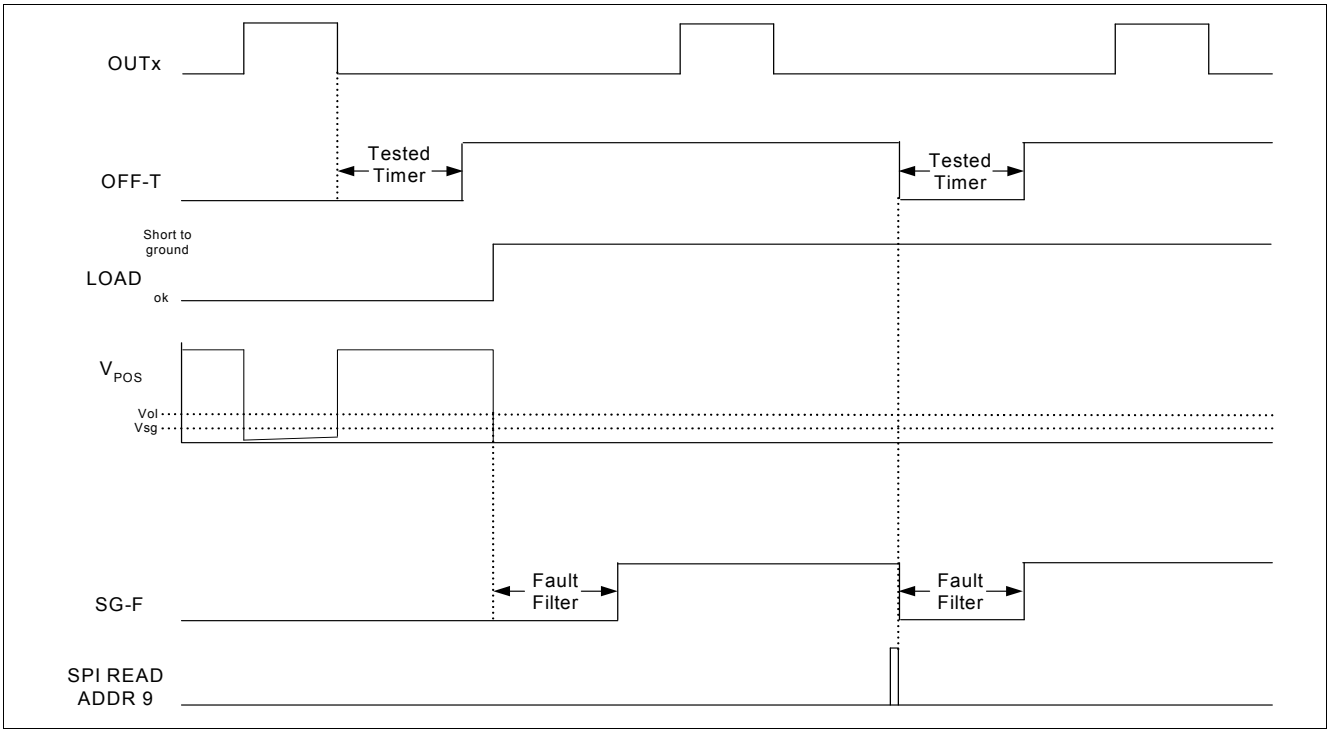

Figure 16 Off-State Diagnostics Timing Diagram - short to ground

Over voltage Shutdown and Diagnostics

If the voltage at the BAT pin is above $VBAT_{OV}$, the output drivers set all OUTx pins to low, and a diagnostic bit is set (SPI Message +11 bit OVL). During over voltage condition the integrator of the steady state current control is halted (actual value of the duty cycle is not changed during over voltage). All other functions operate normally (e.g. ADC, Dithering, Auto zero, Filters, …).

Electrical Characteristics:

V5D = 4.75V to 5.25V, Vbat = 5.5V to 42V, T_j = -40 ·C to +150 ·C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.3.1	Over voltage shutdown	V_{BATOV}	42	–	–	V	Raise VBAT until all outputs shut down
5.3.2	Open load detection voltage	$V_{POS(OL)}$	V5A-2.5	–	V5A-1.5	V	
5.3.3	POS pin OL pull down current	$I_{PD(OL)}$	60	100	150	µA	V5A=5V, V_{POS}=V_{NEG}=V5A
5.3.4	Short to GND detection voltage	$V_{POS(SHG)}$	V5A-3.5	–	V5A-2.5	V	
5.3.5	POS pin SG pull-up current	$I_{PD(SHG)}$	-60	-100	-150	µA	V5A=5V, V_{POS}=V_{NEG}=0V
5.3.6	NEG bias current - Low common mode	$I_{NEG(L)}$	-40	–	10	µA	V5A=5V, V_{POS}=V_{NEG}=0V
5.3.7	NEG bias current - High common mode	$I_{NEG(H)}$	0	–	60	µA	V5A=5V, V_{POS}=V_{NEG}=V5A

Functional Description and Electrical Characteristics

V5D = 4.75V to 5.25V, Vbat = 5.5V to 42V, T_j = -40 ·C to +150 ·C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.3.8	POS Fault Threshold Voltage	V_{FLT}	0.6	0.7	0.8	V	POS voltage required to trigger a short to battery fault: config bits = 00
5.3.9	POS Fault Threshold Voltage	V_{FLT}	0.8	0.9	1.0	V	POS voltage required to trigger a short to battery fault: config bits = 01
5.3.10	POS Fault Threshold Voltage	V_{FLT}	1.0	1.1	1.2	V	POS voltage required to trigger a short to battery fault: config bits = 10
5.3.11	POS Fault Threshold Voltage	V_{FLT}	1.2	1.3	1.4	V	POS voltage required to trigger a short to battery fault: config bits = 11
5.3.12	Fault Filter Timer	n_{fault}	9		10	clocks	
5.3.13	Fault Filter Time	T_{ff}	$\frac{n_{fault} \cdot predivider}{f_{CLK}}$				Clock Divider (SPI Message 7) 00 - Predivider 128 01, 10 - Predivider 192 11 - Predivider 256
5.3.14	Tested Timer Time	T_{tt}	$\frac{n_{fault} \cdot predivider}{f_{CLK}}$				Clock Divider (SPI Message 7) 00 - Predivider 128 01, 10 - Predivider 192 11 - Predivider 256

5.4 Output Driver

The OUTx pins of the device are connected to the gates of the external MOSFET transistors. The OUTx pin driver circuits charge and discharge the MOSFET gate capacitance with a constant current source and sink. The supply for the current source is the V5D pin. Internal resistors to ground are included on the OUTx pins so that the external MOSFET is held in the off state when power is not applied to the device.

An external resistor is typically placed between the OUTx pin and the gate of the external MOSFET in order to set the MOSFET turn-on and turn-off times. The value of the resistor must be chosen such that the turn-on and turn-off times of the MOSFET are no longer than 1/(Fpwm*32).

Electrical Characteristics:

V5D = 4.75V to 5.25V, Vbat = 5.5V to 42V, T_j = -40 ·C to +150 ·C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.4.1	Passive Gate Pull Down Resistance	R_{PD}	50	–	200	kΩ	Internal pull down resistor present at each OUTx pin
5.4.2	OUTx source current	I_{O_SRC}	-15	–	-30	mA	V_{OUT} = V5D-2V
5.4.3	OUTx sink current	I_{O_SNK}	15	–	30	mA	V_{OUT} = 2V

5.5 Current Control

Electrical Characteristics:

V5D = 4.75V to 5.25V, Vbat = 5.5V to 42V, T_j = -40 ·C to +150 ·C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.5.1	Offset Error Output from Average block in **Figure 3**. 1 count = 320/Rsense * 2^{-14} mA		0	–	240	counts	Autozero disabled.Vpos-Vneg=0mV Vpos, Vneg ≤ 30V
5.5.2	Gain Error		-2%	–	2%	%	Autozero Enabled.Vpos-Vneg=300mV Vpos, Vneg ≤ 30V

5.6 Serial Peripheral Interface (SPI)

SPI messages for the TLE7242 2G IC are 32-bit values broken down into the following fields.

Bit 31: Read/Write Bit - 0 = Read 1 = Write

Bits 30-26: Message Identifier

Bits 25-24: Channel Number (00, 01, 10, 11)

Bits 23-0: Message Data

The message from the microcontroller must be sent MSB first. The data from the SO pin is sent MSB first. The TLE7242 2G will sample data from the SI pin on the rising edge of SCK and will shift data out of the SO pin on the rising edge of SCK.

All SPI messages must be exactly 32-bits long, otherwise the SPI message is discarded. The response to an invalid message (returned in the next SPI message) is the message with identifier 00000 (Manufacturer ID).

When the ENABLE pin is low, all SPI writes commands are executed as read commands.

When RESET_B pin is low, the SPI port is disabled. No SPI messages are received and no responses are sent. The SO pin remains in a high impedance state.

There is a one message delay in the response to each message (i.e. the response for message N will be returned during message N+1).

Read/Write operation is referenced from the SPI master. The TLE7242 2G IC is the slave device.

Some messages, such as diagnostic information, do not use the channel number field. In these cases the channel number is not part of the response.

When bit 31 is = 0 to denote a read operation to the IC, the message data in bits 23-0 of the sent message are ignored, but will contain valid data in the response message.

All response data (either from a read or write operation) is the direct contents of the addressed internal register, and is not an echo of the data sent in the previous SPI message.

The response to the first SPI message after a reset is message #0 (IC Version / Manufacturer).