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TLE7250GVIO

High Speed CAN Transceiver

Data Sheet

Rev. 1.1, 2014-05-07

Automotive Power

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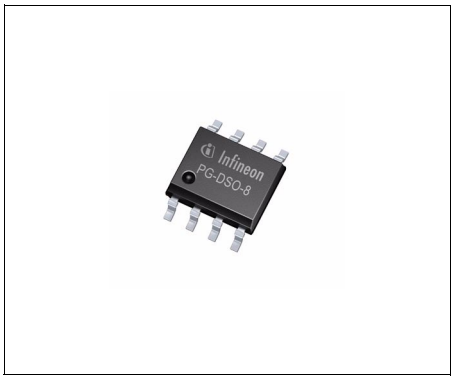
1 Overview



PG-DSO-8

Features

- Fully compliant with ISO 11898-2
- Wide common mode range for electromagnetic immunity (EMI)
- Very low electromagnetic emission (EME)
- Excellent ESD immunity
- Extended supply range at V_{CC} and V_{IO}
- Suitable for 5V and 3.3V microcontroller I/O voltages
- CAN short-circuit proof to ground, battery and V_{CC}
- TxD time-out function
- Low CAN bus leakage current in power-down state
- Overtemperature protection
- Protected against automotive transients
- CAN data transmission rate up to 1 Mbps
- V_{IO} input for voltage adaptation to the micro controller supply
- Green Product (RoHS-compliant)
- AEC Qualified

Description

The TLE7250GVIO is a transceiver designed for CAN networks in automotive and industrial applications. As an interface between the physical bus layer and the CAN protocol controller, the TLE7250GVIO drives the signals to the bus and protects the microcontroller against interferences generated within the network. Based on the high symmetry of the CANH and CANL signals, the TLE7250GVIO provides a very low level of electromagnetic emission (EME) within a wide frequency range. The TLE7250GVIO is integrated in a RoHS-compliant PG-DSO-8 package and fulfills or exceeds the requirements of ISO11898-2.

As a successor to the first generation of HS CAN transceivers, the pin assignment and function of the TLE7250GVIO is fully compatible with its predecessor model, the TLE6250GV33. The TLE7250GVIO is optimized to provide an excellent passive behavior in the power-down state. This feature makes the TLE7250GVIO extremely suitable for mixed supply CAN networks.

Based on the Infineon Smart Power Technology SPT, the TLE7250GVIO provides excellent ESD immunity together with a very high electromagnetic immunity (EMI). The Infineon Smart Power Technology SPT allows bipolar and CMOS control circuitry in accordance with DMOS power devices to exist on the same monolithic circuit. The TLE7250GVIO and the Infineon SPT technology are AEC qualified and tailored to withstand the harsh conditions of the Automotive Environment.

Two different operating modes, additional fail-safe features like TxD time-out and the optimized output slew rates on the CANH and CANL signals make the TLE7250GVIO the ideal choice for large CAN networks with high data transmission rates.

Type	Package	Marking
TLE7250GVIO	PG-DSO-8	7250GVIO

2 Block Diagram

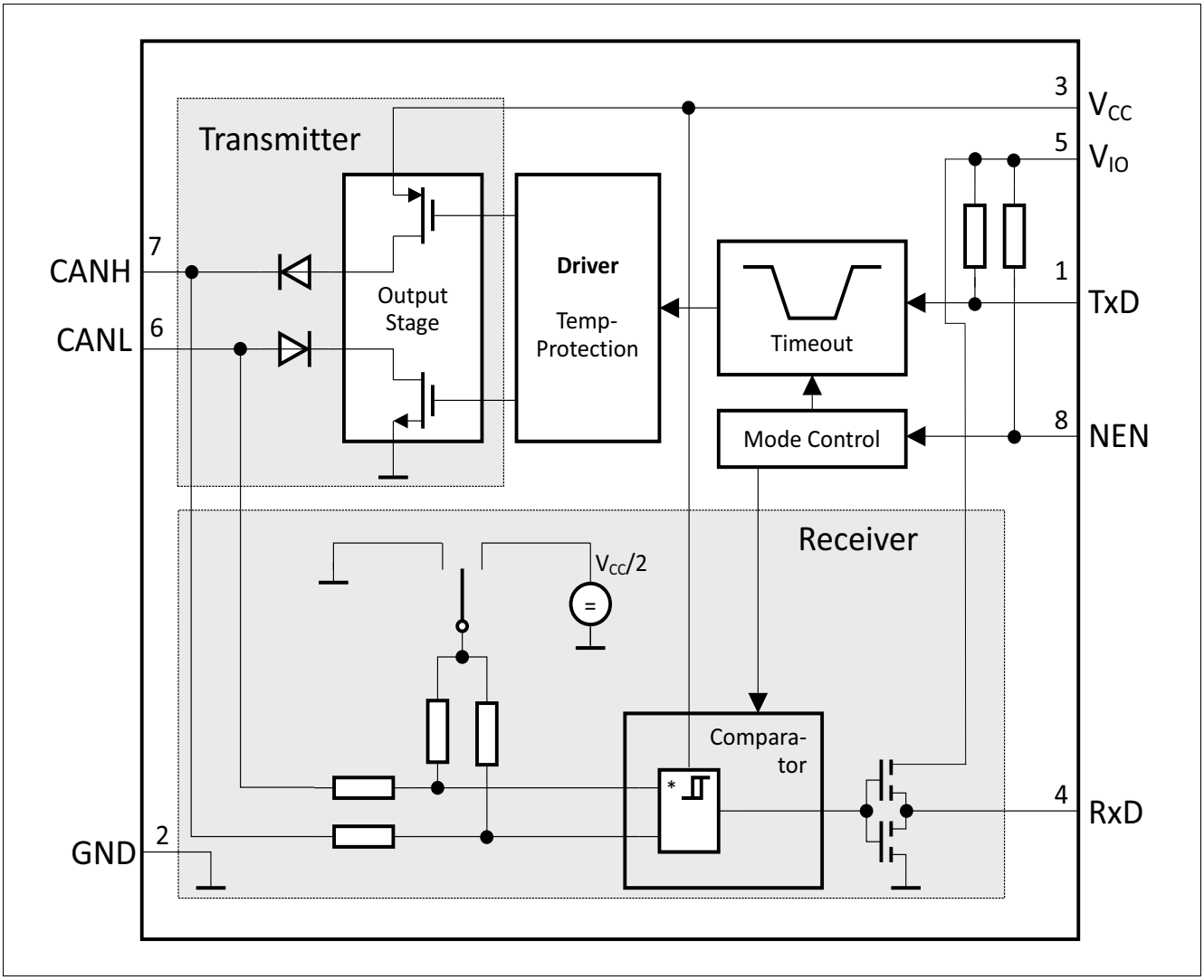


Figure 1 Block diagram

Note: In comparison with the TLE6250GV33, the pin 8 (INH) was renamed as NEN, but the function remains unchanged. NEN stands for Not ENable.

3 Pin Configuration

3.1 Pin Assignment

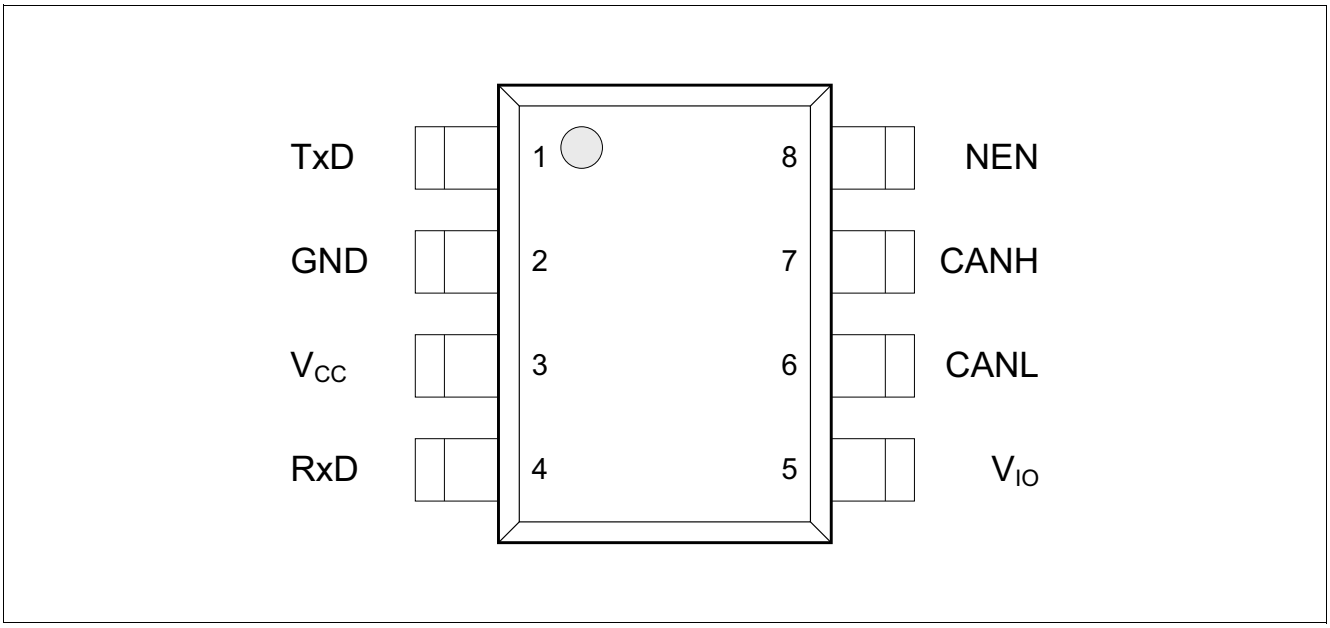


Figure 2 Pin configuration

3.2 Pin Definitions and Functions

Table 1 Pin Definition and Functions

Pin	Symbol	Function
1	TxD	**Transmit Data Input;** internal pull-up to V_{IO}, “low” for “dominant” state.
2	GND	**Ground**
3	V_{CC}	**Transceiver Supply Voltage;** 100 nF decoupling capacitor to GND required.
4	RxD	**Receive Data Output;** “low” in “dominant” state.
5	V_{IO}	**Digital Supply Voltage Input;** supply voltage input to adapt the logical input and output voltage levels of the transceiver to the microcontroller supply. 100 nF decoupling capacitor to GND required.
6	CANL	**CAN Bus Low Level I/O;** “low” in “dominant” state.
7	CANH	**CAN Bus High Level I/O;** “high” in “dominant” state.
8	NEN	**Not Enable Input**[1)]**;** internal pull-up to V_{IO}, “low” for normal-operating mode.

1) The designation of pin 8 is different in the TLE7250GVIO and its predecessor, the TLE6250GV33. The function of pin 8 remains the same.

4 Functional Description

CAN is a serial bus system that connects microcontrollers, sensors and actuators for real-time control applications. The use of the **C**ontrol **A**rea **N**etwork (abbreviated CAN) within road vehicles is described by the international standard ISO 11898. According to the 7-layer OSI reference model, the physical layer of a CAN bus system specifies the data transmission from one CAN node to all other available CAN nodes within the network. The physical layer specification of a CAN bus system includes all electrical and mechanical specifications of a CAN network. The CAN transceiver is part of the physical layer specification. Several different physical layer standards of CAN networks have been developed in recent years. The TLE7250GVIO is a High Speed CAN transceiver without a dedicated wake-up function. High-speed CAN transceivers without a wake-up function are defined by the international standard ISO 11898-2.

4.1 High Speed CAN Physical Layer

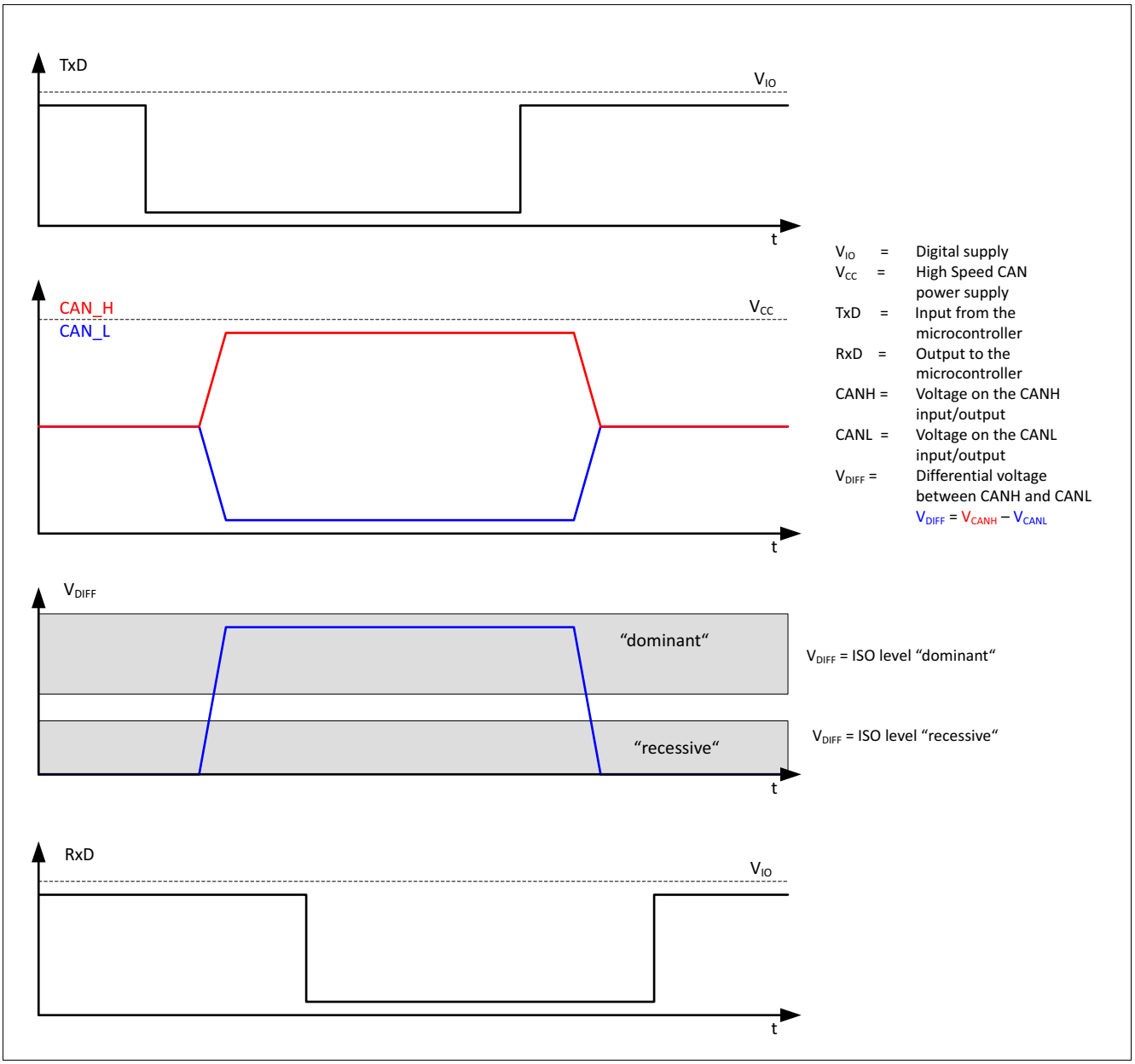


Figure 3 High Speed CAN bus signals and logic signals

The TLE7250GVIO is a High Speed CAN transceiver, operating as an interface between the CAN controller and the physical bus medium. A HS CAN network is a two-wire, differential network, which allows data transmission rates up to 1 Mbps. The characteristics of a HS CAN network are the two signal states on the CAN bus: “dominant” and “recessive” (see **Figure 3**).

The CANH and CANL pins are the interface to the CAN bus and both pins operate as an input and output. The RxD and TxD pins are the interface to the microcontroller. The TxD pin is the serial data input from the CAN controller, and the RxD pin is the serial data output to the CAN controller. As shown in **Figure 1**, the HS CAN transceiver TLE7250GVIO includes a receiver and a transmitter unit, allowing the transceiver to send data to the bus medium and monitor the data from the bus medium at the same time. The HS CAN transceiver TLE7250GVIO converts the serial data stream available on the transmit data input TxD, into a differential output signal on the CAN bus, provided by the CANH and CANL pins. The receiver stage of the TLE7250GVIO monitors the data on the CAN bus and converts them to a serial, single-ended signal on the RxD output pin. A logical “low” signal on the TxD pin creates a “dominant” signal on the CAN bus, followed by a logical “low” signal on the RxD pin (see **Figure 3**). The feature of broadcasting data to the CAN bus and listening to the data traffic on the CAN bus simultaneously is essential to support the bit-to-bit arbitration within CAN networks.

The voltage levels for HS CAN transceivers are defined by the ISO 11898-2 and the ISO 11898-5 standards. Whether a data bit is “dominant” or “recessive” depends on the voltage difference between the CANH and CANL pins: $V_{DIFF} = V_{CANH} - V_{CANL}$.

In comparison with other differential network protocols, the differential signal on a CAN network can only be larger than or equal to 0 V. To transmit a “dominant” signal to the CAN bus, the differential signal V_{DIFF} is larger than or equal to 1.5 V. To receive a “recessive” signal from the CAN bus, the differential V_{DIFF} is smaller than or equal to 0.5 V.

“Partially-supplied” High Speed CAN networks are those where the CAN bus nodes of one common network have different power supply conditions. Some nodes are connected to the common power supply, while other nodes are disconnected from the power supply and in power-down state. Regardless of whether the CAN bus subscriber is supplied or not, each subscriber connected to the common bus media must not interfere with the communication. The TLE7250GVIO is designed to support “partially-supplied” networks. In the power-down state, the receiver input resistors are switched off and the transceiver input has a high resistance.

The voltage level at the digital input TxD and the digital output RxD is determined by the power supply level at the V_{IO} pin. Depending on the voltage level at the V_{IO} pin, the signal levels on the logic pins (NEN, TxD and RxD) are compatible with microcontrollers having 5 V or 3.3 V I/O supply. Usually, the V_{IO} power supply of the transceiver is connected to same power supply as the I/O power supply of the microcontroller.

4.2 Modes of Operation

Two different modes of operation are available on the TLE7250GVIO. Each mode has specific characteristics in terms of quiescent current or data transmission. The digital input pin NEN is used for mode selection. **Figure 4** illustrates the different mode changes depending on the status of the NEN pin. After supplying V_{CC} and V_{IO} to the HS CAN transceiver, the TLE7250GVIO starts in stand-by mode. The internal pull-up resistor at the NEN pin sets the TLE7250GVIO to stand-by mode by default. If the microcontroller is up and running, the TLE7250GVIO can switch to any mode of operation within the time period for mode change t_{Mode}.

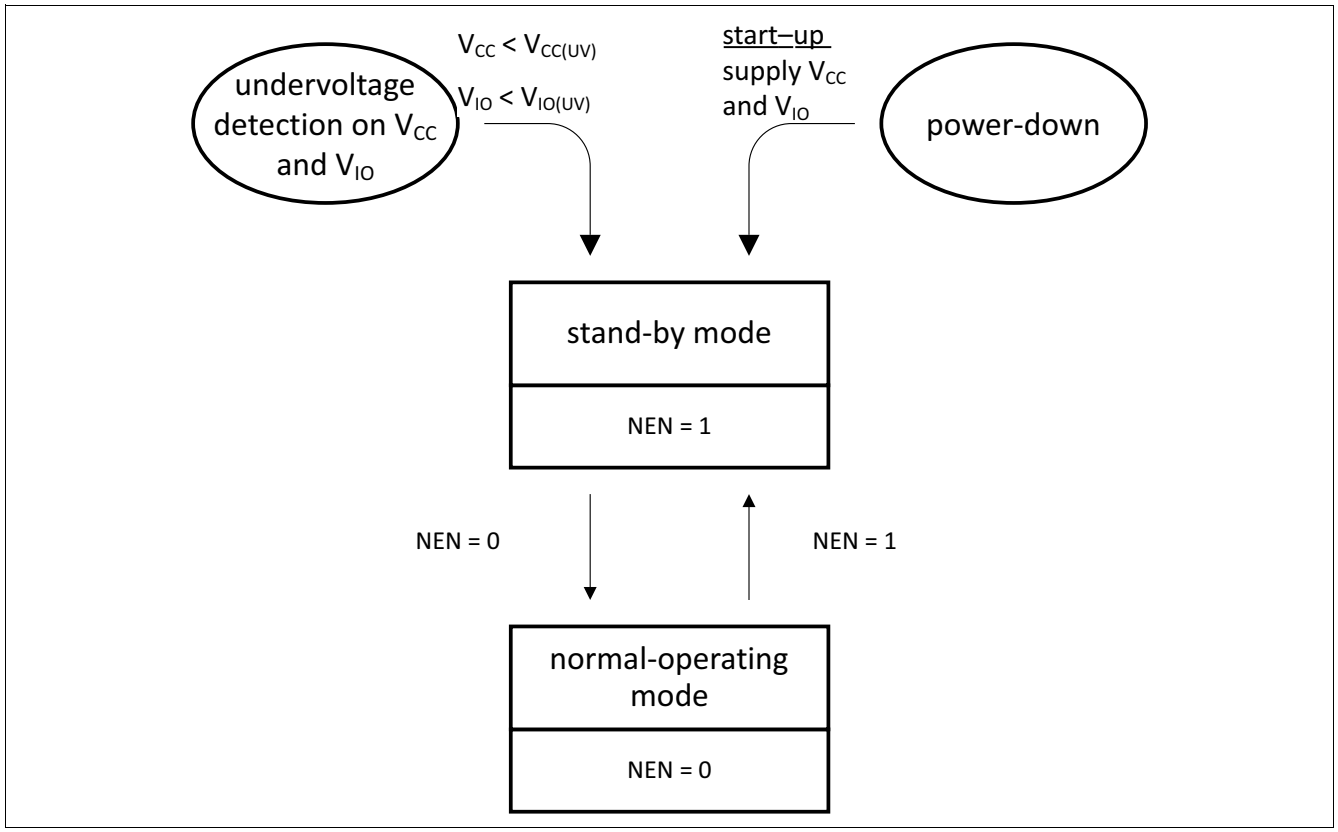


Figure 4 Modes of operation

The TLE7250GVIO has 2 major modes of operation:

- Stand-by mode
- Normal-operating mode

Table 2 Modes of Operation

Mode	NEN	Bus Bias	Comments
Normal-operating mode	“low”	V_{CC}/2	The transmitter is active. The receiver is active.
Stand-by	“high”	GND	The transmitter is disabled. The receiver is disabled.
V_{CC} off	“low” or “high”	floating	The transmitter is disabled. The receiver is disabled.

4.3 Normal-operating Mode

In the normal-operating mode, the HS CAN transceiver TLE7250GVIO sends the serial data stream on the TxD pin to the CAN bus. The data on the CAN bus is displayed at the RxD pin simultaneously. In normal-operating mode, all functions of the TLE7250GVIO are active:

- The transmitter is active and drives data from the TxD to the CAN bus.
- The receiver is active and provides the data from the CAN bus to the RxD pin.
- The bus biasing is set to V_{CC}/2.
- The undervoltage monitoring at the power supply V_{CC} and at the power supply V_{IO} is active.

To enter the normal-operating mode, set the NEN pin to logical “low” (see **Table 2** or **Figure 4**). The NEN pin has an internal pull-up resistor to the power-supply V_{IO}.

4.4 Stand-by Mode

The stand-by mode is an idle mode of the TLE7250GVIO with optimized power consumption. In the stand-by mode, the TLE7250GVIO can not send or receive any data. The transmitter and the receiver unit are disabled. Both CAN bus pins, CANH and CANL are connected to GND via the input resistors.

- The transmitter is disabled.
- The receiver is disabled.
- The input resistors of the receiver are connected to GND.
- The undervoltage monitoring at the power supply V_{CC} and at the power supply V_{IO} is active.

To enter the stand-by mode, set the pin NEN to logical “high” (see **Table 2** or **Figure 4**). The NEN pin has an internal pull-up resistor to the power-supply V_{IO}. If the stand-by mode is not used in the final application, the NEN pin needs to be connected to GND.

4.5 Power-down State

The power-down state means that the TLE7250GVIO is not supplied. In power-down state, the differential input resistors of the receiver are switched off. The CANH and CANL bus interface of the TLE7250GVIO act as high-impedance input with a very small leakage current. The high-ohmic input does not influence the “recessive” level of the CAN network and allows an optimized EME performance of the entire CAN network.

5 Fail-safe Functions

5.1 Short-circuit Protection

The CANH and CANL bus outputs are short-circuit proof, either against GND or a positive supply voltage. A current limiting circuit protects the transceiver against damage. If the device heats up due to a continuous short on the CANH or CANL, the internal overtemperature protection switches off the bus transmitter.

5.2 Unconnected Logic Pins

All logic input pins have an internal pull-up resistor to V_{IO}. In case the V_{IO} supply is activated and the logical pins are open or floating, the TLE7250GVIO enters the stand-by mode by default. In stand-by mode, the transmitter of the TLE7250GVIO is disabled, the bus bias is connected to GND and the HS CAN TLE7250G transceiver does not influence the data on the CAN bus.

5.3 TxD Time-out Function

The TxD time-out feature protects the CAN bus against permanent blocking in case the logical signal on the TxD pin is continuously “low”. A continuous “low” signal on the TxD pin can have its root cause in a locked-up microcontroller or in a short on the printed circuit board for example. In the normal-operating mode, a logical “low” signal on the TxD pin for the time t > t_{TxD} enables the TxD time-out feature and the TLE7250GVIO disables the transmitter (see **Figure 5**). The receiver is still active and the data on the bus continues to be monitored by the RxD output pin.

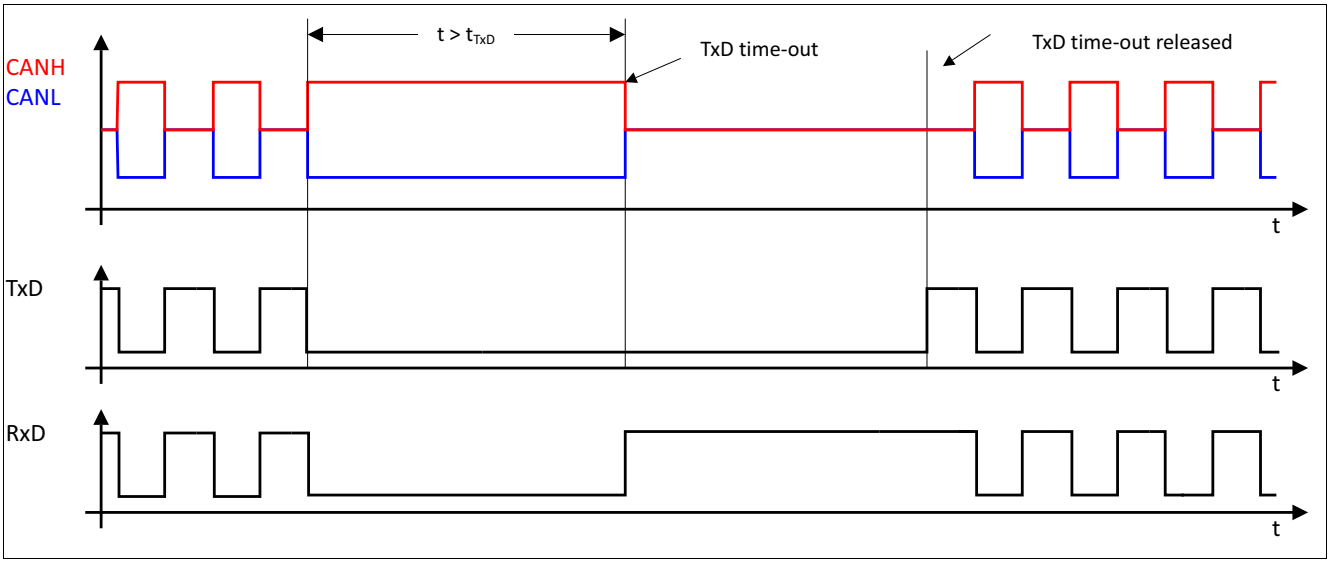
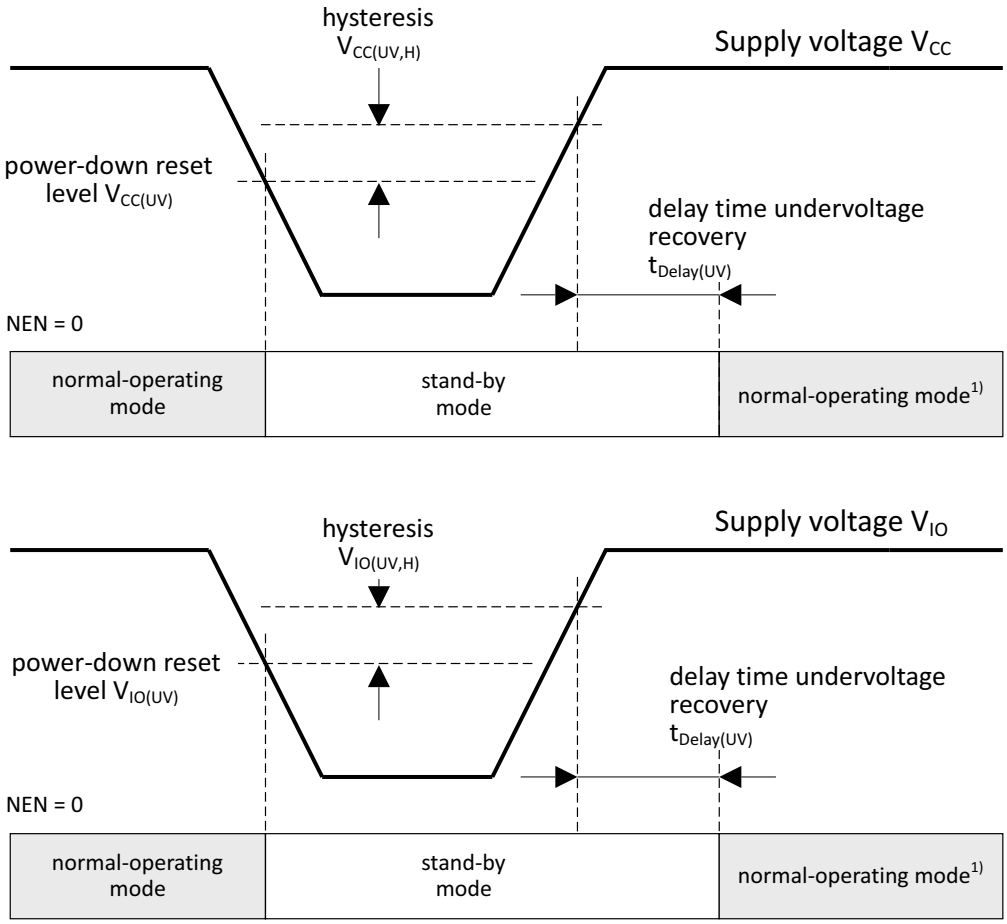


Figure 5 TxD Time-out function

Figure 5 illustrates how the transmitter is deactivated and activated again. A permanent “low” signal on the TxD input pin activates the TxD time-out function and deactivates the transmitter. To release the transmitter after a TxD time-out event, the TLE7250GVIO requires a signal change on the TxD input pin from logical “low” to logical “high”.

5.4 Undervoltage Detection

The HS CAN transceiver TLE7250GVIO is provided with undervoltage detection at the power supply V_{CC} and at the power supply V_{IO}. In case of undervoltage at V_{CC} or V_{IO}, the undervoltage detection changes the operating mode of TLE7250GVIO to the stand-by mode, regardless of the logical signal on the NEN pin (see **Figure 6**). If the transceiver TLE7250GVIO recovers from the undervoltage condition, the operating mode is restored to the programmed mode by the NEN pin.



1) Assuming the logical signal on the pin NEN keeps its values during the undervoltage event. In this case NEN remains “low“.

Figure 6 Undervoltage detection at the V_{CC} or V_{IO} Pins

5.5 Overtemperature Protection

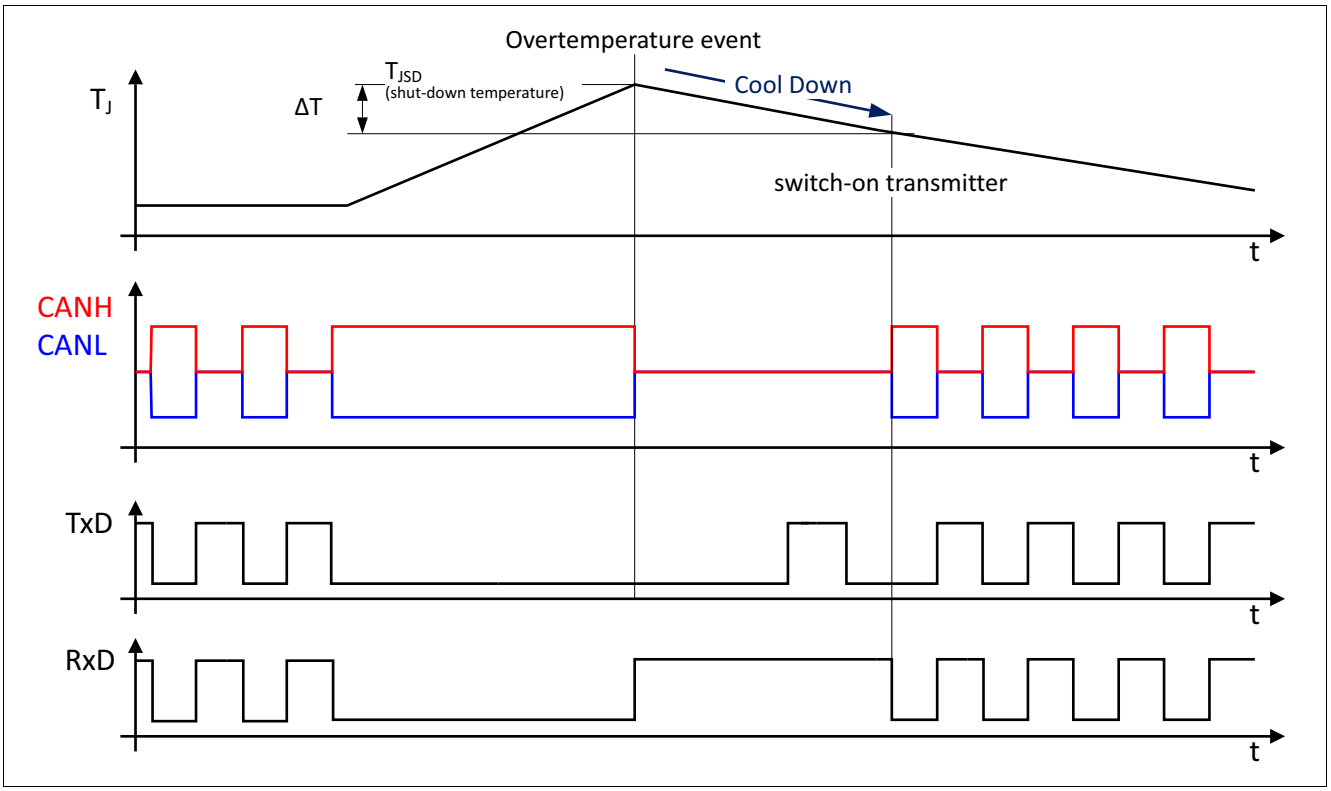


Figure 7 Overtemperature protection

The TLE7250GVIO has an integrated overtemperature detection circuit to protect the device against thermal overstress of the transmitter. In case of an overtemperature condition, the temperature sensor will disable the transmitter (see **Figure 1**). After the device cools down, the transmitter is activated again (see **Figure 7**).
A hysteresis is implemented within the temperature sensor.

6 General Product Characteristics

6.1 Absolute Maximum Ratings

Table 3 Absolute Maximum Ratings of Voltage, Current and Temperatures[1)]

All voltages with respect to ground; positive current flowing into the pin;

(unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Remarks
			Min.	Max.		
Voltage						
6.1.1	Supply voltage	V_{CC}	-0.3	6.0	V	–
6.1.2	Logic supply voltage	V_{IO}	-0.3	6.0	V	–
6.1.3	CANH DC voltage against GND	V_{CANH}	-40	40	V	–
6.1.4	CANL DC voltage against GND	V_{CANL}	-40	40	V	–
6.1.5	Differential voltage between CANH and CANL	$V_{CAN\ diff}$	-40	40	V	–
6.1.6	Logic voltage at logic input pins NEN, TxD	V_{Max_In}	-0.3	6.0	V	–
6.1.7	Logic voltage at logic output pin RxD	V_{Max_Out}	-0.3	V_{IO}	V	–
Temperature						
6.1.8	Junction temperature	T_j	-40	150	°C	–
6.1.9	Storage temperature	T_S	-55	150	°C	–
ESD Immunity						
6.1.10	ESD immunity at CANH, CANL against GND	$V_{ESD\_HBM\_CAN}$	-8	8	kV	HBM (100pF via 1.5 kΩ)[2)]
6.1.11	ESD immunity at all other pins	$V_{ESD\_HBM\_All}$	-2	2	kV	HBM (100pF via 1.5 kΩ)[2)]
6.1.12	ESD immunity to GND (all pins)	V_{ESD_CDM}	-750	750	V	CDM[3)]

1) Not subject to production test, specified by design

2) ESD susceptibility Human Body Model “HBM” according to ANSI/ESDA/JEDEC JS-001

3) ESD susceptibility, Charge Device Model “CDM” according to EIA/JESD22-C101 or ESDA STM5.3.1

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the associated electrical characteristics table.

6.2 Functional Range

Table 4 Operating Range

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
Supply Voltage						
6.2.1	Transceiver supply voltage	V_{CC}	4.5	5.5	V	–
6.2.2	Logical supply voltage	V_{IO}	3.0	5.5	V	–
Thermal Parameter						
6.2.3	Junction temperature	T_j	-40	150	°C	1)

1) Not subject to production test, specified by design

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the associated electrical characteristics table.

6.3 Thermal Characteristics

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, please visit **www.jedec.org**.*

Table 5 Thermal Resistance[1)]

Pos.	Parameter	Symbol	Limit Values			Unit	Remarks
			Min.	Typ.	Max.		
Thermal Resistance							
6.3.1	Junction to ambient[1)]	R_{thJA}	–	130	–	K/W	2)
Thermal Shut-down Junction Temperature							
6.3.2	Thermal shut-down temperature	T_{JSD}	150	175	200	°C	–
6.3.3	Thermal shut-down hysteresis	ΔT	–	10	–	K	–

1) Not subject to production test, specified by design

2) The R_{thJA} value specified, is according to Jedec JESD51-2,-7 at natural convection on the FR4 2s2p board; The product (TLE7250GVIO) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70 µm Cu, 2 x 35 µm Cu).

7 Electrical Characteristics

7.1 Functional Device Characteristics

Table 6 Electrical Characteristics

4.5 V < V_{CC} < 5.5 V; 3.0 V < V_{IO} < 5.5 V; R_L = 60 Ω; -40 °C < T_j < +150 °C; all voltages with respect to ground; positive current flowing into the pin; unless otherwise specified.

Pos.	Parameter	Symbol	Limit Values			Unit	Remarks
			Min.	Typ.	Max.		
Current Consumption							
7.1.1	Current consumption at V_{CC}	I_{CC}	–	2	6	mA	“recessive” state; $V_{TxD} = V_{IO}$
7.1.2	Current consumption at V_{CC}	I_{CC}	–	35	60	mA	“dominant” state; V_{TxD} = “low”
7.1.3	Current consumption at V_{IO}	I_{IO}	–	0.2	1	mA	normal-operating mode; NEN = “low”
7.1.4	Current consumption stand-by mode	$I_{CC(STB)}$	–	4	15	µA	$V_{CC} = V_{IO}$ = 5 V, TxD = V_{IO}, NEN = V_{IO}
7.1.5	Current consumption stand-by mode	$I_{IO(STB)}$	–	2	10	µA	$V_{CC} = V_{IO}$ = 5 V, TxD = V_{IO}, NEN = V_{IO}
Supply Reset							
7.1.6	V_{CC} undervoltage monitor	$V_{CC(UV)}$	1.3	3.2	4.3	V	–
7.1.7	V_{CC} undervoltage monitor hysteresis	$V_{CC(UV,H)}$	–	400	–	mV	1)
7.1.8	V_{IO} undervoltage monitor	$V_{IO(UV)}$	1.0	2.4	3.0	V	–
7.1.9	V_{IO} undervoltage monitor hysteresis	$V_{IO(UV,H)}$	–	200	–	mV	1)
7.1.10	V_{CC} and V_{IO} undervoltage delay time	$t_{Delay(UV)}$	–	–	50	µs	1) (see **Figure 6**)
Receiver Output: RxD							
7.1.11	“High” level output current	$I_{RD,H}$	–	-4	-2	mA	$V_{RxD} = V_{IO}$ - 0.4 V, V_{DIFF} < 0.5 V
7.1.12	“Low” level output current	$I_{RD,L}$	2	4	–	mA	V_{RxD} = 0.4 V, V_{DIFF} > 0.9 V
Transmission Input: TxD							
7.1.13	“High” level input voltage threshold	$V_{TD,H}$	–	0.5 × V_{IO}	0.7 × V_{IO}	V	“recessive” state
7.1.14	“Low” level input voltage threshold	$V_{TD,L}$	0.3 × V_{IO}	0.4 × V_{IO}	–	V	“dominant” state
7.1.15	TxD pull-up resistance	R_{TD}	10	25	50	kΩ	–
7.1.16	TxD input hysteresis	$V_{HYS(TxD)}$	–	800	–	mV	1)
7.1.17	TxD permanent “dominant” disable time	t_{TxD}	0.3	–	1.0	ms	–

Table 6 Electrical Characteristics (cont'd)

4.5 V < V_{CC} < 5.5 V; 3.0 V < V_{IO} < 5.5 V; R_L = 60 Ω; -40 °C < T_j < +150 °C; all voltages with respect to ground; positive current flowing into the pin; unless otherwise specified.

Pos.	Parameter	Symbol	Limit Values			Unit	Remarks
			Min.	Typ.	Max.		
Not Enable Input NEN							
7.1.18	"High" level input voltage threshold	$V_{NEN,H}$	–	0.5 × V_{IO}	0.7 × V_{IO}	V	stand-by mode
7.1.19	"Low" level input voltage threshold	$V_{NEN,L}$	0.3 × V_{IO}	0.4 × V_{IO}	–	V	normal-operating mode
7.1.20	NEN pull-up resistance	R_{NEN}	10	25	50	kΩ	–
7.1.21	NEN input hysteresis	$V_{HYS(NEN)}$	–	200	–	mV	1)
Bus Receiver							
7.1.22	Differential receiver threshold "dominant"	$V_{DIFF,(D)}$	–	0.75	0.9	V	normal-operating mode
7.1.23	Differential receiver threshold "recessive"	$V_{DIFF,(R)}$	0.5	0.65	–		normal-operating mode
7.1.24	Differential receiver input range "dominant"	$V_{diff,rdN}$	0.9	–	5.0	V	1) normal-operating mode
7.1.25	Differential receiver input range "recessive"	$V_{diff,drN}$	-1.0	–	0.5	V	1) normal-operating mode
7.1.26	Common mode range	CMR	-12	–	12	V	V_{CC} = 5 V
7.1.27	Differential receiver hysteresis	$V_{diff,hys}$	–	100	–	mV	1)
7.1.28	CANH, CANL input resistance	R_i	10	20	30	kΩ	"recessive" state
7.1.29	Differential input resistance	R_{diff}	20	40	60	kΩ	"recessive" state
7.1.30	Input resistance deviation between CANH and CANL	ΔR_i	-3	–	3	%	1) "recessive" state
7.1.31	Input capacitance CANH, CANL versus GND	C_{IN}	–	20	40	pF	1) V_{TxD} = V_{IO}
7.1.32	Differential input capacitance	C_{InDiff}	–	10	20	pF	1) V_{TxD} = V_{IO}
Bus Transmitter							
7.1.33	CANL/CANH "recessive" output voltage	$V_{CANL/H}$	2.0	2.5	3.0	V	no load; V_{TxD} = V_{IO}
7.1.34	CANH, CANL "recessive" output voltage difference	V_{diff}	-500	–	50	mV	no load; V_{TxD} = V_{IO}
7.1.35	CANL "dominant" output voltage	V_{CANL}	0.5	–	2.25	V	4.75 V ≤ V_{CC} ≤ 5.25 V, V_{TxD} = 0 V, 50 Ω < R_L < 65 Ω
7.1.36	CANH "dominant" output voltage	V_{CANH}	2.75	–	4.5	V	4.75 V ≤ V_{CC} ≤ 5.25 V, V_{TxD} = 0 V, 50 Ω < R_L < 65 Ω
7.1.37	CANH, CANL "dominant" output voltage difference V_{diff} = V_{CANH} - V_{CANL}	V_{diff}	1.5	–	3.0	V	4.75 V ≤ V_{CC} ≤ 5.25 V, V_{TxD} = 0 V, 50 Ω < R_L < 65 Ω
7.1.38	Driver symmetry V_{SYM} = V_{CANH} + V_{CANL}	V_{SYM}	4.5	–	5.5	V	V_{TxD} = 0 V, V_{CC} = 5 V, 50 Ω < R_L < 65 Ω

Table 6 Electrical Characteristics (cont'd)

4.5 V < V_{CC} < 5.5 V; 3.0 V < V_{IO} < 5.5 V; R_L = 60 Ω; -40 °C < T_j < +150 °C; all voltages with respect to ground; positive current flowing into the pin; unless otherwise specified.

Pos.	Parameter	Symbol	Limit Values			Unit	Remarks
			Min.	Typ.	Max.		
7.1.39	CANL short-circuit current	I_{CANLsc}	40	80	100	mA	V_{TxD} = 0 V, V_{CC} = 5 V, t < t_{TxD}, $V_{CANLshort}$ = 18 V
7.1.40	CANH short-circuit current	I_{CANHsc}	-100	-80	-40	mA	V_{TxD} = 0 V, V_{CC} = 5 V, t < t_{TxD}, $V_{CANHshort}$ = 0 V
7.1.41	Leakage current CANH	$I_{CANH,lk}$	-5	0	5	µA	V_{CC} = 0 V, V_{CANH} = V_{CANL}, 0 V < V_{CANH} < 5 V
7.1.42	Leakage current CANL	$I_{CANL,lk}$	-5	0	5	µA	V_{CC} = 0 V, V_{CANH} = V_{CANL}, 0 V < V_{CANL} < 5 V
Dynamic CAN Transceiver Characteristics							
7.1.43	Propagation delay TxD-to-RxD "low" ("recessive" to "dominant")	$t_{d(L),TR}$	30	180	255	ns	C_L = 100 pF, V_{CC} = 5 V, C_{RxD} = 15 pF
7.1.44	Propagation delay TxD-to-RxD "high" ("dominant" to "recessive")	$t_{d(H),TR}$	30	200	255	ns	C_L = 100 pF, V_{CC} = 5 V, C_{RxD} = 15 pF
7.1.45	Propagation delay TxD "low" to bus "dominant"	$t_{d(L),T}$	–	100	–	ns	1) C_L = 100 pF, V_{CC} = 5 V, C_{RxD} = 15 pF
7.1.46	Propagation delay TxD "high" to bus "recessive"	$t_{d(H),T}$	–	90	–	ns	1) C_L = 100 pF, V_{CC} = 5 V, C_{RxD} = 15 pF
7.1.47	Propagation delay bus "dominant" to RxD "low"	$t_{d(L),R}$	–	80	–	ns	1) C_L = 100 pF, V_{CC} = 5 V, C_{RxD} = 15 pF
7.1.48	Propagation delay bus "recessive" to RxD "high"	$t_{d(H),R}$	–	110	–	ns	1) C_L = 100 pF, V_{CC} = 5 V, C_{RxD} = 15 pF
7.1.49	Time for mode change	t_{Mode}	–	–	10	µs	1)

1) Not subject to production test, specified by design

7.2 Diagrams

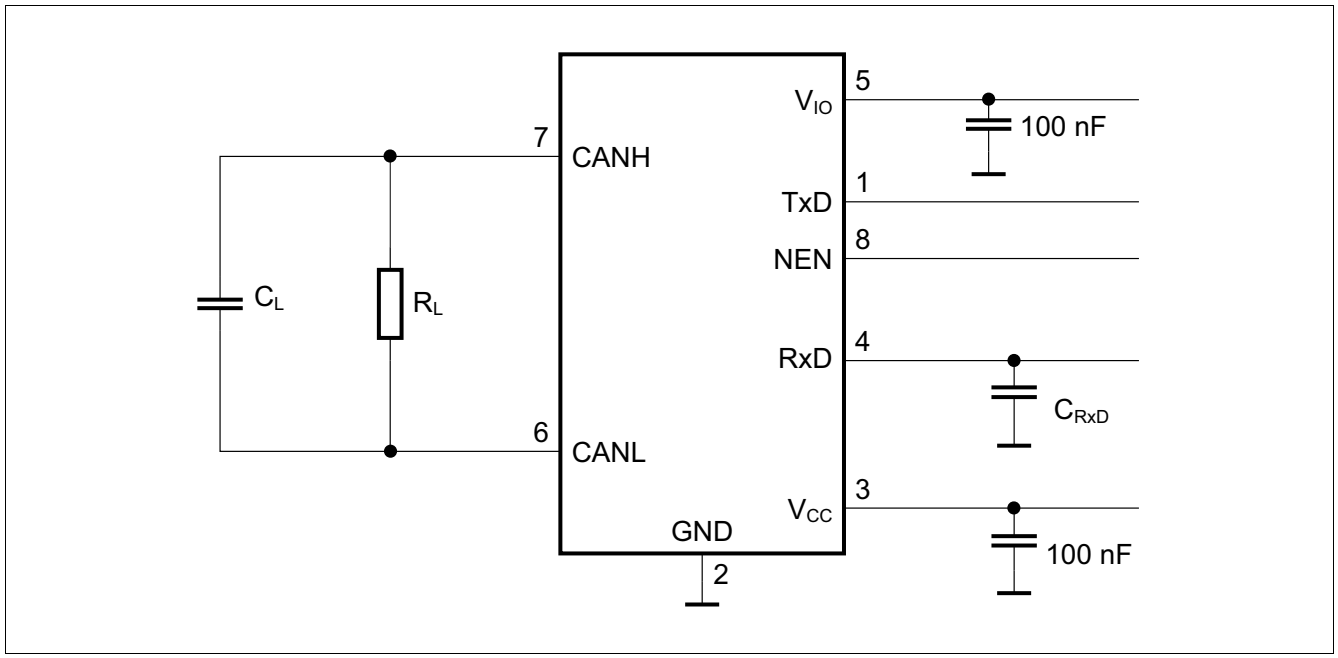


Figure 8 Simplified test circuit

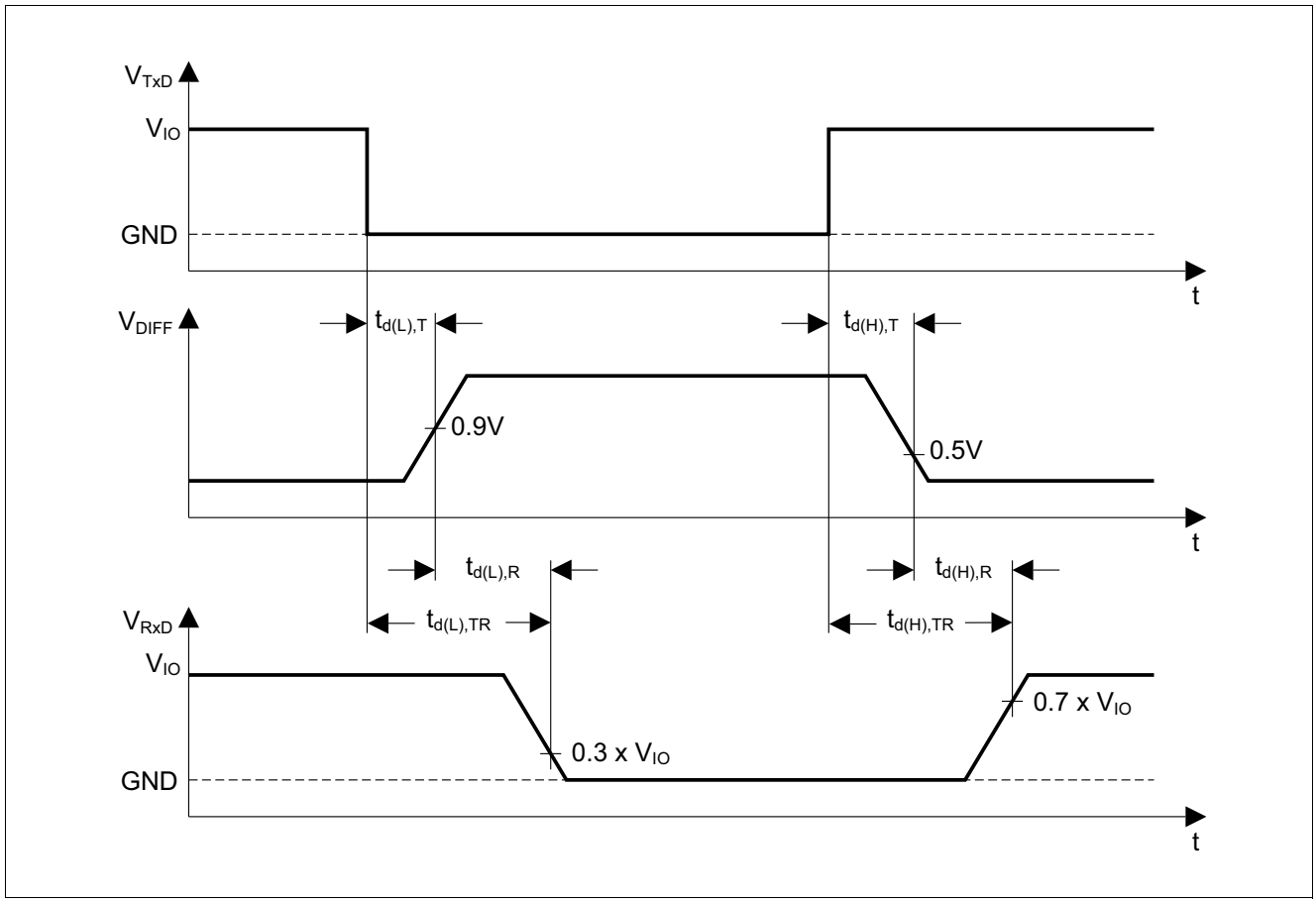


Figure 9 Timing diagram for dynamic characteristics

8 Application Information

8.1 ESD Immunity According to IEC61000-4-2

Tests for ESD immunity according to IEC61000-4-2, “GUN test” (150 pF, 330 Ω), have been performed. The results and test conditions are available in a separate test report.

Table 7 ESD Immunity according to IEC61000-4-2

Test performed	Result	Unit	Remarks
Electrostatic discharge voltage at CANH and CANL pins against GND	≥ +8	kV	[1)]Positive pulse
Electrostatic discharge voltage at CANH and CANL pins against GND	≤ -8	kV	[1)]Negative pulse

1) ESD susceptibility “ESD GUN” according to GIFT / ICT paper: “EMC Evaluation of CAN Transceivers, version 03/02/ IEC TS 62228”, section 4.3. (DIN EN 61000-4-2)
Tested by external test house (IBEE Zwickau, EMC test report no.: 05-12-11).

8.2 Application Example

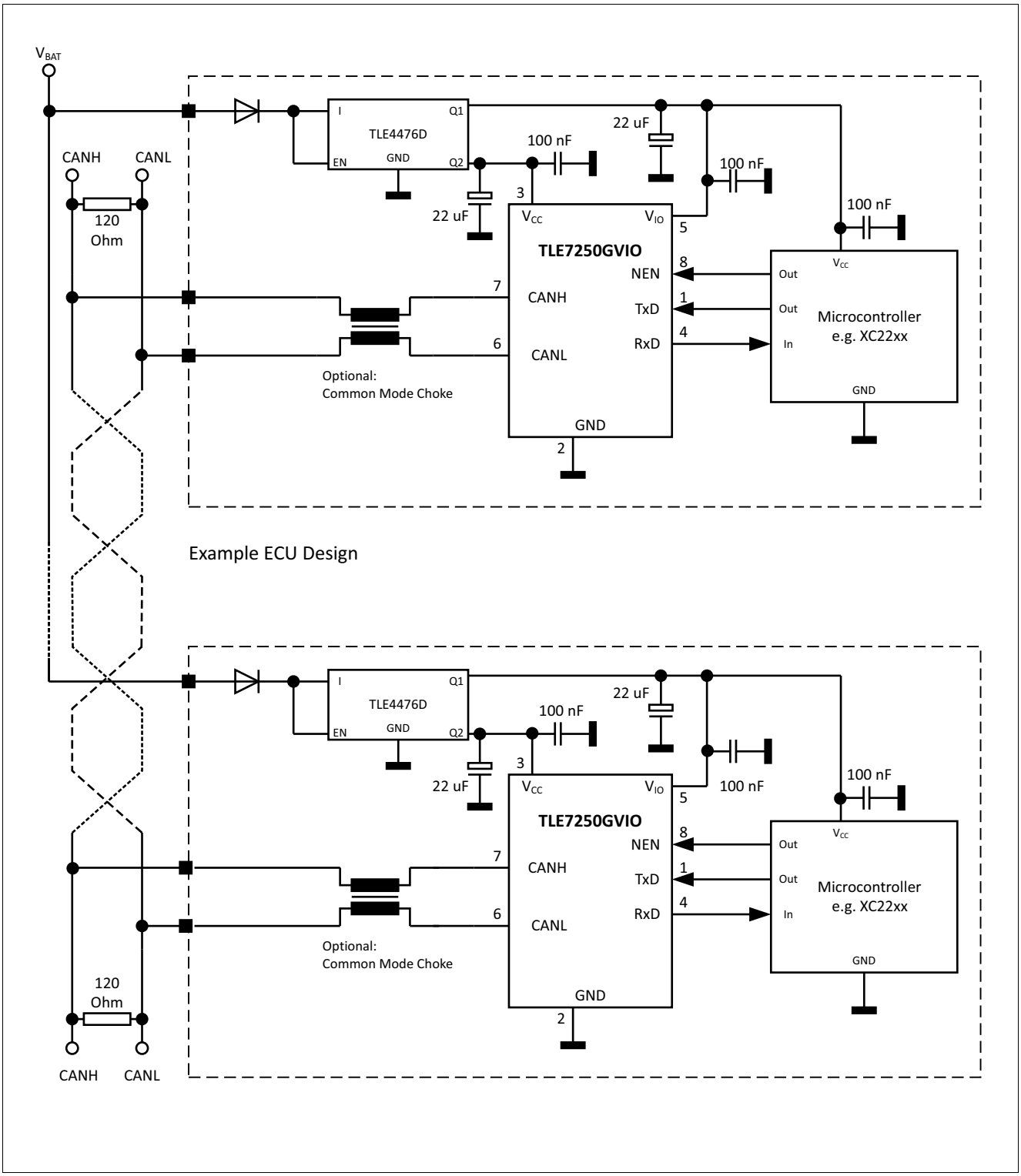


Figure 10 Simplified application for the TLE7250GVIO

8.3 Further Application Information

- Please contact us for information regarding the FMEA pin.
- For further information you may visit **http://www.infineon.com/transceiver**

9 Package Outlines

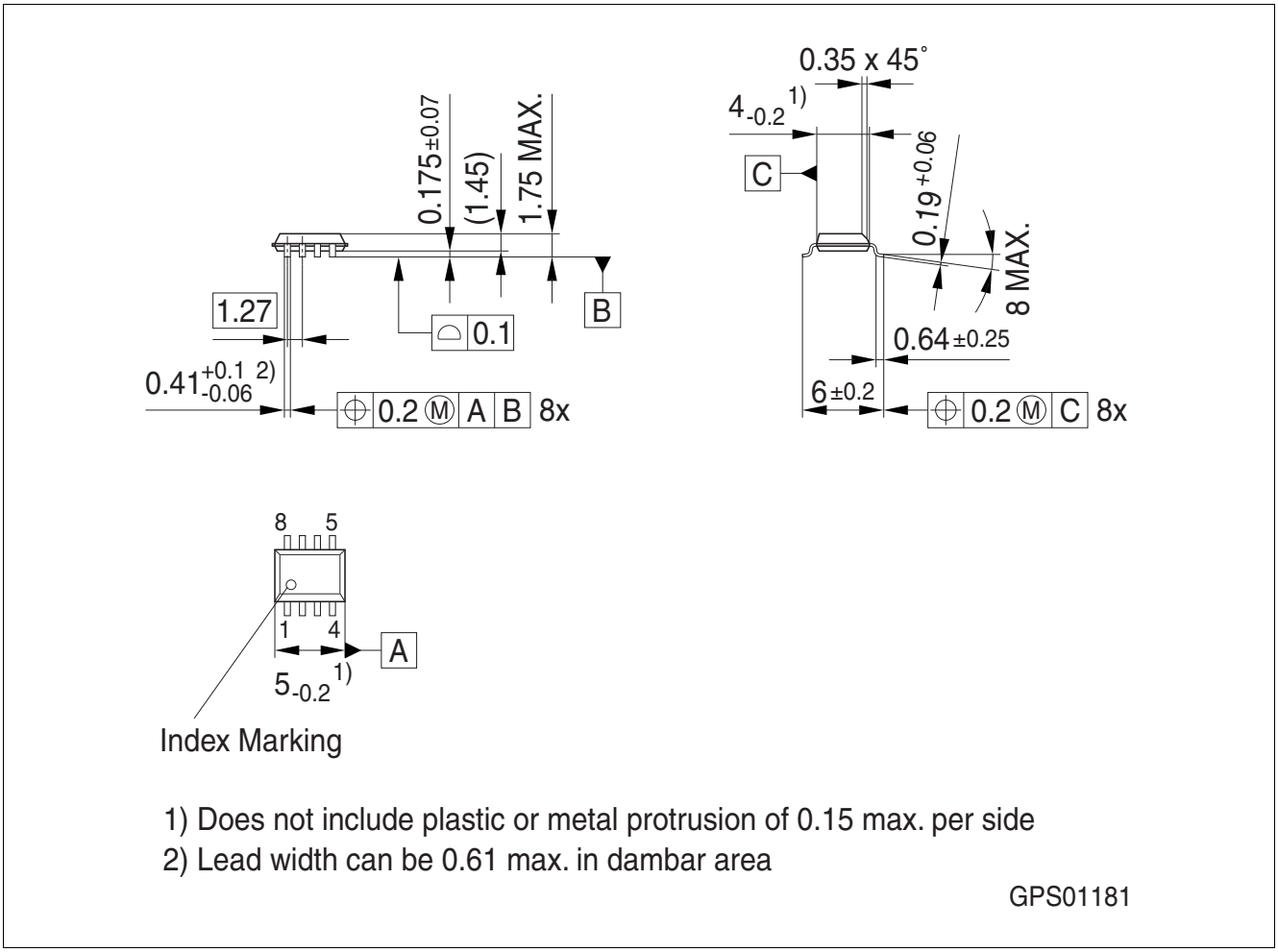


Figure 11 **PG-DSO-8** (Plastic dual small outline PG-DSO-8-16)

Green Product (RoHS-compliant)

The device has been designed as a green product to meet the world-wide customer requirements for environment-friendly products and to be compliant with government regulations. Green products are RoHS-compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website:
http://www.infineon.com/packages.

Dimensions in mm

10 Revision History

Revision	Date	Changes
1.1	2014-05-07	Update from Data Sheet Rev.: 1.0. • All pages: Revision and date update • **Page 3**, Overview: Feature list updated (“Extended supply range at V_{CC} and V_{IO}”). • **Page 14**, **Table 4**, **Parameter 6.2.1**, Supply range updated (4.5 V < V_{CC} < 5.5 V). • **Page 14**, **Table 4**, **Parameter 6.2.2**: Supply range updated (3.0 V < V_{IO} < 5.5 V). • **Page 15**, **Table 6**: Table header updated (4.5 V < V_{CC} < 5.5 V, 3.0 V < V_{IO} < 5.5 V). • **Page 16**, **Table 6**, **Parameter 7.1.35**: Remark added (“4.75 V≤V_{CC}≤5.25 V”). • **Page 16**, **Table 6**, **Parameter 7.1.36**: Remark added (“4.75 V≤V_{CC}≤5.25 V”). • **Page 16**, **Table 6**, **Parameter 7.1.37**: Remark added (“4.75 V≤V_{CC}≤5.25 V”). • **Page 20**, **Figure 10**: Picture updated. • **Page 22**: Revision history updated.
1.0	2012-03-01	Data Sheet Rev. 1.0 created

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