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TLE7250V

High Speed CAN-Transceiver

TLE7250VLE
TLE7250VSJ

Data Sheet

Rev. 1.0, 2015-08-12

Automotive Power

Table of Contents

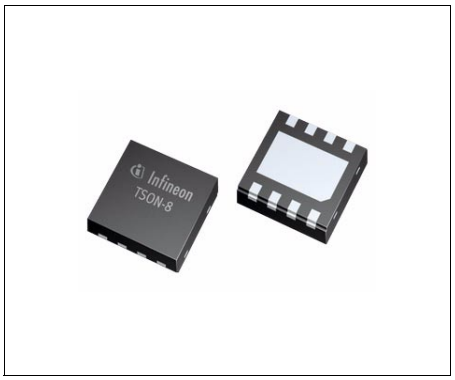
High Speed CAN-Transceiver

TLE7250VLE
TLE7250VSJ

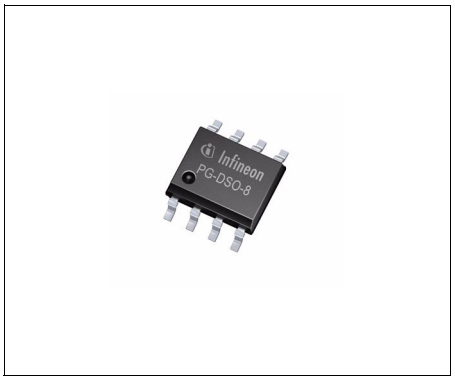
1 Overview

Features

- Fully compatible to ISO 11898-2
- Wide common mode range for electromagnetic immunity (EMI)
- Very low electromagnetic emission (EME)
- Excellent ESD robustness
- Guaranteed loop delay symmetry to support CAN FD data frames up to 2 MBit/s
- V_{IO} input for voltage adaption to the microcontroller supply
- Extended supply range on V_{CC} and V_{IO} supply
- CAN short circuit proof to ground, battery and V_{CC}
- TxD time-out function
- Low CAN bus leakage current in power-down state
- Overtemperature protection
- Protected against automotive transients
- Power-save mode
- Transmitter supply V_{CC} can be turned off in power-save mode
- Green Product (RoHS compliant)
- Two package variants: PG-TSON-8 and PG-DSO-8
- AEC Qualified



PG-TSON-8



PG-DSO-8

Description

The TLE7250V is a transceiver designed for HS CAN networks in automotive and industrial applications. As an interface between the physical bus layer and the CAN protocol controller, the TLE7250V drives the signals to the bus and protects the microcontroller against interferences generated within the network. Based on the high symmetry of the CANH and CANL signals, the TLE7250V provides a very low level of electromagnetic emission (EME) within a wide frequency range.

The TLE7250V is available in a small, leadless PG-TSON-8 package and in a PG-DSO-8 package. Both packages are RoHS compliant and halogen free. Additionally the PG-TSON-8 package supports the solder joint requirements for automated optical inspection (AOI). The TLE7250VLE and the TLE7250VSJ are fulfilling or exceeding the requirements of the ISO11898-2.

The TLE7250V provides a digital supply input V_{IO} and a power-save mode. It is designed to fulfill the enhanced physical layer requirements for CAN FD and supports data rates up to 2 MBit/s.

On the basis of a very low leakage current on the HS CAN bus interface the TLE7250V provides an excellent passive behavior in power-down state. These and other features make the TLE7250V exceptionally suitable for

Type	Package	Marking
TLE7250VLE	PG-TSON-8	7250V
TLE7250VSJ	PG-DSO-8	7250V

mixed supply HS CAN networks.
Based on the Infineon Smart Power Technology SPT, the TLE7250V provides excellent ESD immunity together with a very high electromagnetic immunity (EMI). The TLE7250V and the Infineon SPT technology are AEC qualified and tailored to withstand the harsh conditions of the automotive environment.

Two different operating modes, additional fail-safe features like a TxD time-out and the optimized output slew rates on the CANH and CANL signals, make the TLE7250V the ideal choice for large HS CAN networks with high data transmission rates.

2 Block Diagram

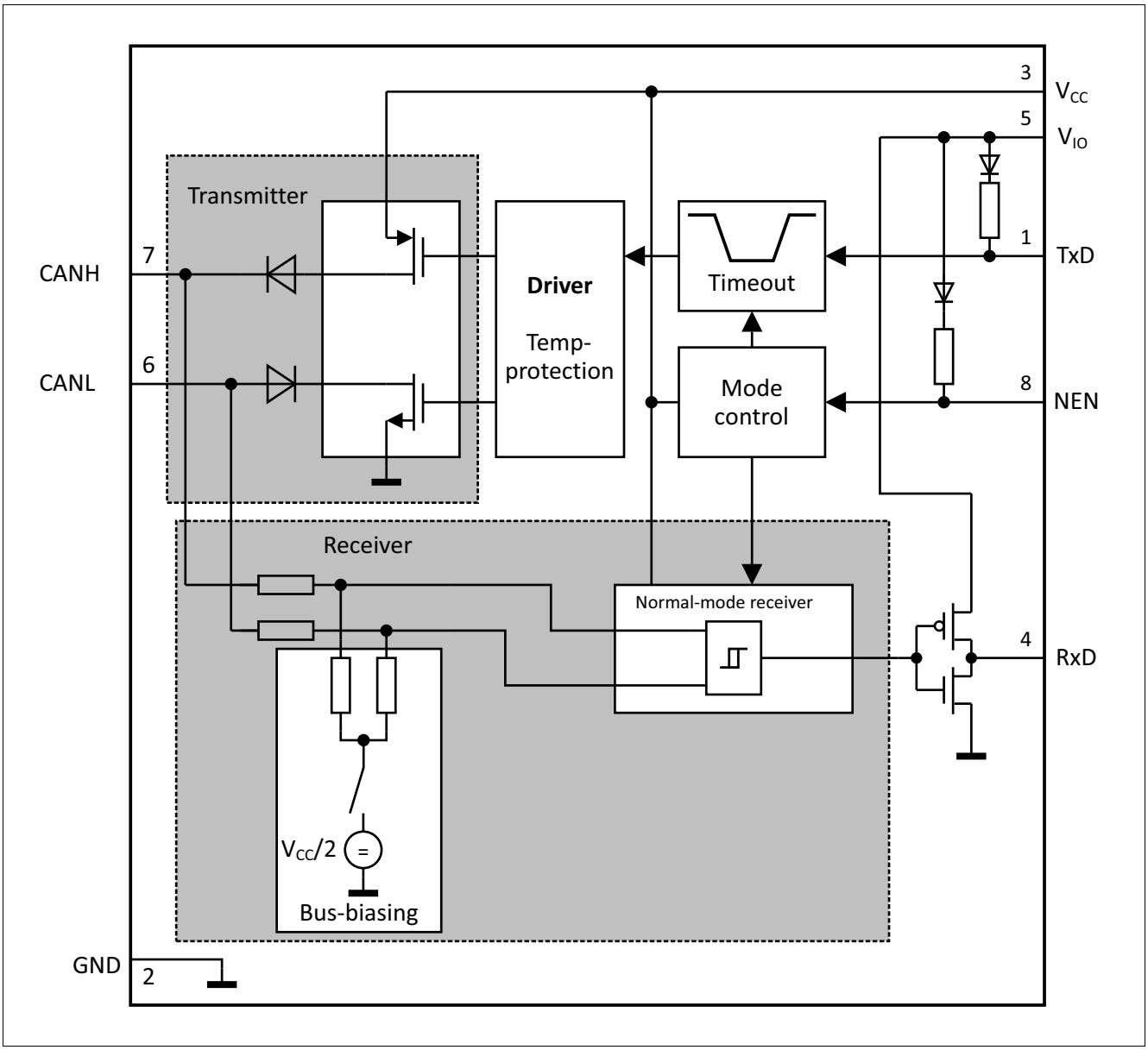


Figure 1 Functional block diagram

3 Pin Configuration

3.1 Pin Assignment

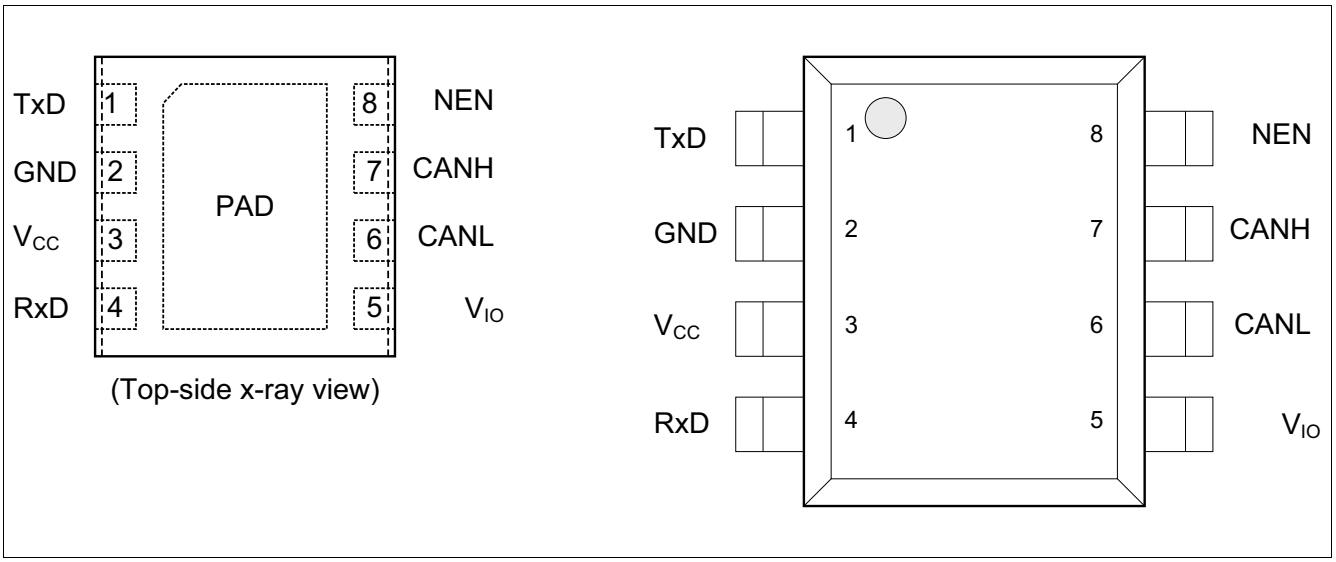


Figure 2 Pin configuration

3.2 Pin Definitions

Table 1 Pin definitions and functions

Pin No.	Symbol	Function
1	TxD	**Transmit Data Input;** internal pull-up to V_{IO}, “low” for “dominant” state.
2	GND	**Ground**
3	V_{CC}	**Transmitter Supply Voltage;** 100 nF decoupling capacitor to GND required, V_{CC} can be turned off in power-save mode.
4	RxD	**Receive Data Output;** “low” in “dominant” state.
5	V_{IO}	**Digital Supply Voltage;** supply voltage input to adapt the logical input and output voltage levels of the transceiver to the microcontroller supply, 100 nF decoupling capacitor to GND required.
6	CANL	**CAN Bus Low Level I/O;** “low” in “dominant” state.
7	CANH	**CAN Bus High Level I/O;** “high” in “dominant” state.

Table 1 Pin definitions and functions (cont'd)

Pin No.	Symbol	Function
8	NEN	**Not Enable Input;** internal pull-up to V_{IO}, "low" for normal-operating mode.
PAD	–	Connect to PCB heat sink area. Do not connect to other potential than GND.

4 Functional Description

HS CAN is a serial bus system that connects microcontrollers, sensors and actuators for real-time control applications. The use of the Controller Area Network (abbreviated CAN) within road vehicles is described by the international standard ISO 11898. According to the 7-layer OSI reference model the physical layer of a HS CAN bus system specifies the data transmission from one CAN node to all other available CAN nodes within the network. The physical layer specification of a CAN bus system includes all electrical and mechanical specifications of a CAN network. The CAN transceiver is part of the physical layer specification. Several different physical layer standards of CAN networks have been developed in recent years. The TLE7250V is a High Speed CAN transceiver without a wake-up function and defined by the international standard ISO 11898-2.

4.1 High Speed CAN Physical Layer

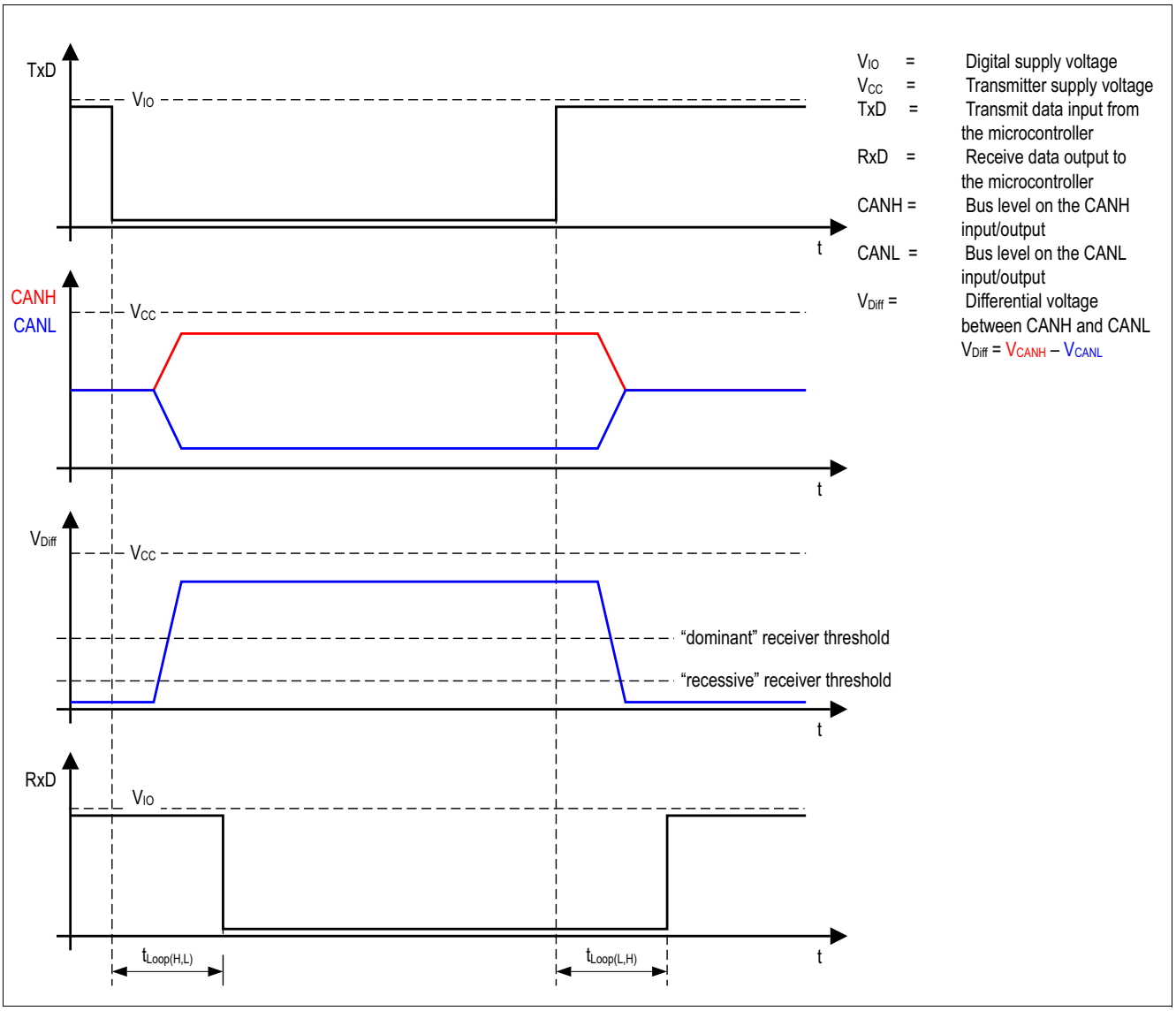


Figure 3 High speed CAN bus signals and logic signals

The TLE7250V is a High-Speed CAN transceiver, operating as an interface between the CAN controller and the physical bus medium. A HS CAN network is a two wire, differential network which allows data transmission rates for CAN FD frames up to 2 MBit/s. Characteristic for HS CAN networks are the two signal states on the HS CAN bus: “dominant” and “recessive” (see **Figure 3**).

V_{CC}, V_{IO} and GND are the supply pins for the TLE7250V. The pins CANH and CANL are the interface to the HS CAN bus and operate in both directions, as an input and as an output. RxD and TxD pins are the interface to the CAN controller, the TxD pin is an input pin and the RxD pin is an output pin. The NEN pin is the input pin for the mode selection (see **Figure 4**).

By setting the TxD input pin to logical “low” the transmitter of the TLE7250V drives a “dominant” signal to the CANH and CANL pins. Setting TxD input to logical “high” turns off the transmitter and the output voltage on CANH and CANL discharges towards the “recessive” level. The “recessive” output voltage is provided by the bus biasing (see **Figure 1**). The output of the transmitter is considered to be “dominant”, when the voltage difference between CANH and CANL is at least higher than 1.5 V (V_{Diff} = V_{CANH} - V_{CANL}).

Parallel to the transmitter the normal-mode receiver monitors the signal on the CANH and CANL pins and indicates it on the RxD output pin. A “dominant” signal on the CANH and CANL pins sets the RxD output pin to logical “low”, vice versa a “recessive” signal sets the RxD output to logical “high”. The normal-mode receiver considers a voltage difference (V_{Diff}) between CANH and CANL above 0.9 V as “dominant” and below 0.5 V as “recessive”.

To be conform with HS CAN features, like the bit to bit arbitration, the signal on the RxD output has to follow the signal on the TxD input within a defined loop delay t_{Loop} ≤ 255 ns.

The thresholds of the digital inputs (TxD and NEN) and also the RxD output voltage are adapted to the digital power supply V_{IO}.

4.2 Modes of Operation

The TLE7250V supports two different modes of operation, power-save mode and normal-operating mode while the transceiver is supplied according to the specified functional range. The mode of operation is selected by the NEN input pin (see **Figure 4**).

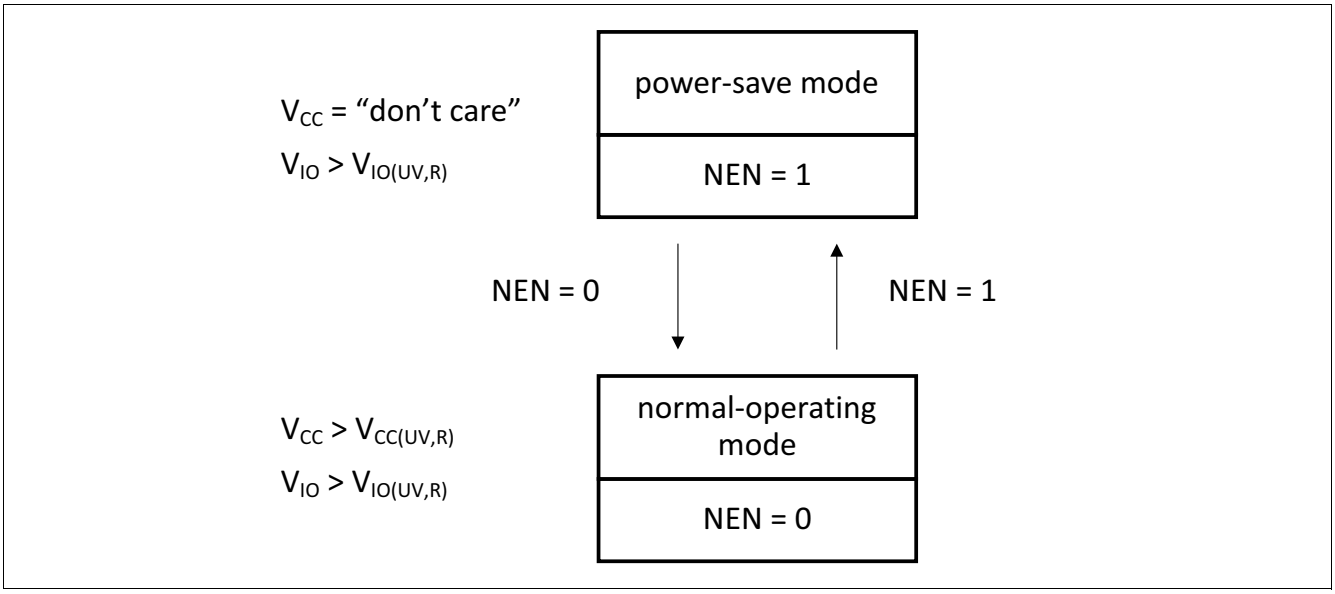


Figure 4 Mode state diagram

4.2.1 Normal-operating Mode

In normal-operating mode the transmitter and the receiver of the HS CAN transceiver TLE7250V are active (see **Figure 1**). The HS CAN transceiver sends the serial data stream on the TxD input pin to the CAN bus. The data on the CAN bus is displayed at the RxD pin simultaneously. A logical “low” signal on the NEN pin selects the normal-operating mode, while the transceiver is supplied by V_{CC} and V_{IO} (see **Table 2** for details).

4.2.2 Power-save Mode

The power-save mode is an idle mode of the TLE7250V with optimized power consumption. In power-save mode the transmitter and the normal-mode receiver are turned off. The TLE7250V can not send any data to the CAN bus nor receive any data from the CAN bus.

The RxD output pin is permanently “high” in the power-save mode.

A logical “high” signal on the NEN pin selects the power-save mode, while the transceiver is supplied by the digital supply V_{IO} (see **Table 2** for details).

In power-save mode the bus input pins are not biased. Therefore the CANH and CANL input pins are floating and the HS CAN bus interface has a high resistance.
The undervoltage detection on the transmitter supply V_{CC} is turned off, allowing to switch off the V_{CC} supply in power-save mode.

4.3 Power-up and Undervoltage Condition

By detecting an undervoltage event, either on the transmitter supply V_{CC} or the digital supply V_{IO}, the transceiver TLE7250V changes the mode of operation. Turning off the digital power supply V_{IO}, the transceiver powers down and remains in the power-down state. While switching off the transmitter supply V_{CC}, the transceiver either changes to the forced power-save mode, or remains in power-save mode (details see **Figure 5**).

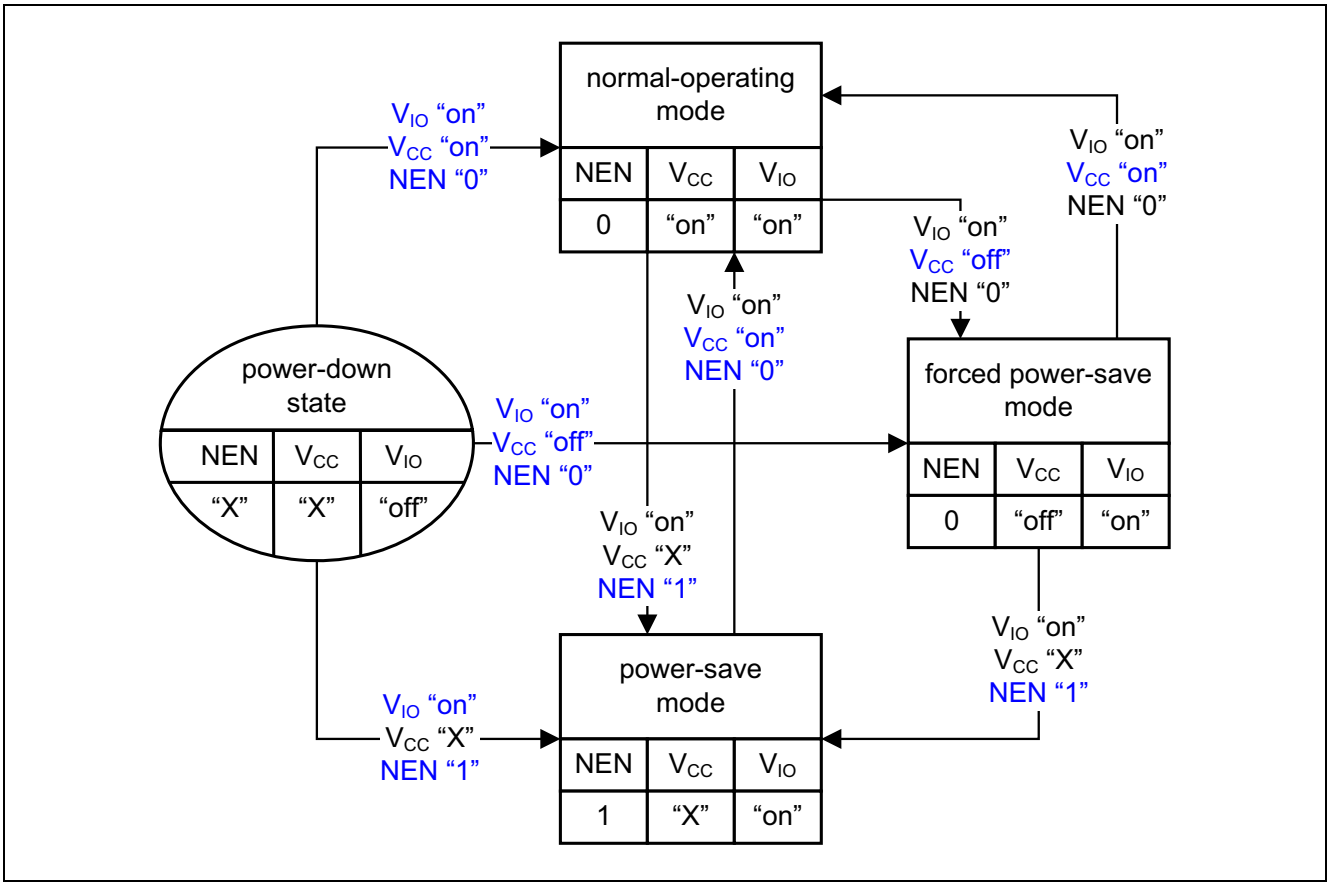


Figure 5 Power-up and undervoltage

Table 2 Modes of operation

Mode	NEN	V_{IO}	V_{CC}	Bus Bias	Transmitter	Normal-mode Receiver	Low-power Receiver
Normal-operating	“low”	“on”	“on”	$V_{CC}/2$	“on”	“on”	not available
Power-save	“high”	“on”	“X”	floating	“off”	“off”	not available
Forced power-save	“low”	“on”	“off”	floating	“off”	“off”	not available
Power-down state	“X”	“off”	“X”	floating	“off”	“off”	not available

4.3.1 Power-down State

Independent of the transmitter supply V_{CC} and of the NEN input pin, the TLE7250V is in power-down state when the digital supply voltage V_{IO} is turned off (see **Figure 5**).

In the power-down state the input resistors of the receiver are disconnected from the bus biasing V_{CC}/2. The CANH and CANL bus interface of the TLE7250V is floating and acts as a high-impedance input with a very small leakage current. The high-ohmic input does not influence the “recessive” level of the CAN network and allows an optimized EME performance of the entire HS CAN network (see also **Table 2**).

4.3.2 Forced Power-save Mode

The forced power-save mode is a fail-safe mode to avoid any disturbance on the HS CAN bus, while the TLE7250V faces a loss of the transmitter supply V_{CC}.
In forced power-save mode, the transmitter and the normal-mode receiver are turned off and therefore the transceiver TLE7250V can not disturb the bus media.
The RxD output pin is permanently set to logical “high”. The bus biasing is floating (details see **Table 2**).

The forced power-save mode can only be entered when the transmitter supply V_{CC} is not available, either by powering up the digital supply V_{IO} only or by turning off the transmitter supply in normal-operating mode. While the transceiver TLE7250V is in forced power-save mode, switching the NEN input to logical “high” triggers a mode change to power-save mode (see **Figure 5**).

4.3.3 Power-up

The HS CAN transceiver TLE7250V powers up if at least the digital supply V_{IO} is connected to the device. By default the device powers up in power-save mode, due to the internal pull-up resistor on the NEN pin to V_{IO}.

In case the device needs to power-up to normal-operating mode, the NEN pin needs to be pulled active to logical “low” and the supplies V_{IO} and V_{CC} have to be connected.

By supplying only the digital power supply V_{IO} the TLE7250V powers up either in forced power-save mode or in power-save mode, depending on the signal of the NEN input pin (see **Figure 5**).

4.3.4 Undervoltage on the Digital Supply V_{IO}

If the voltage on V_{IO} supply input falls below the threshold $V_{IO} < V_{IO(UV,F)}$, the transceiver TLE7250V powers down and changes to the power-down state.

The undervoltage detection on the digital supply V_{IO} has the highest priority. It is independent of the transmitter supply V_{CC} and also independent of the currently selected operating mode. An undervoltage event on V_{IO} always powers down the TLE7250V.

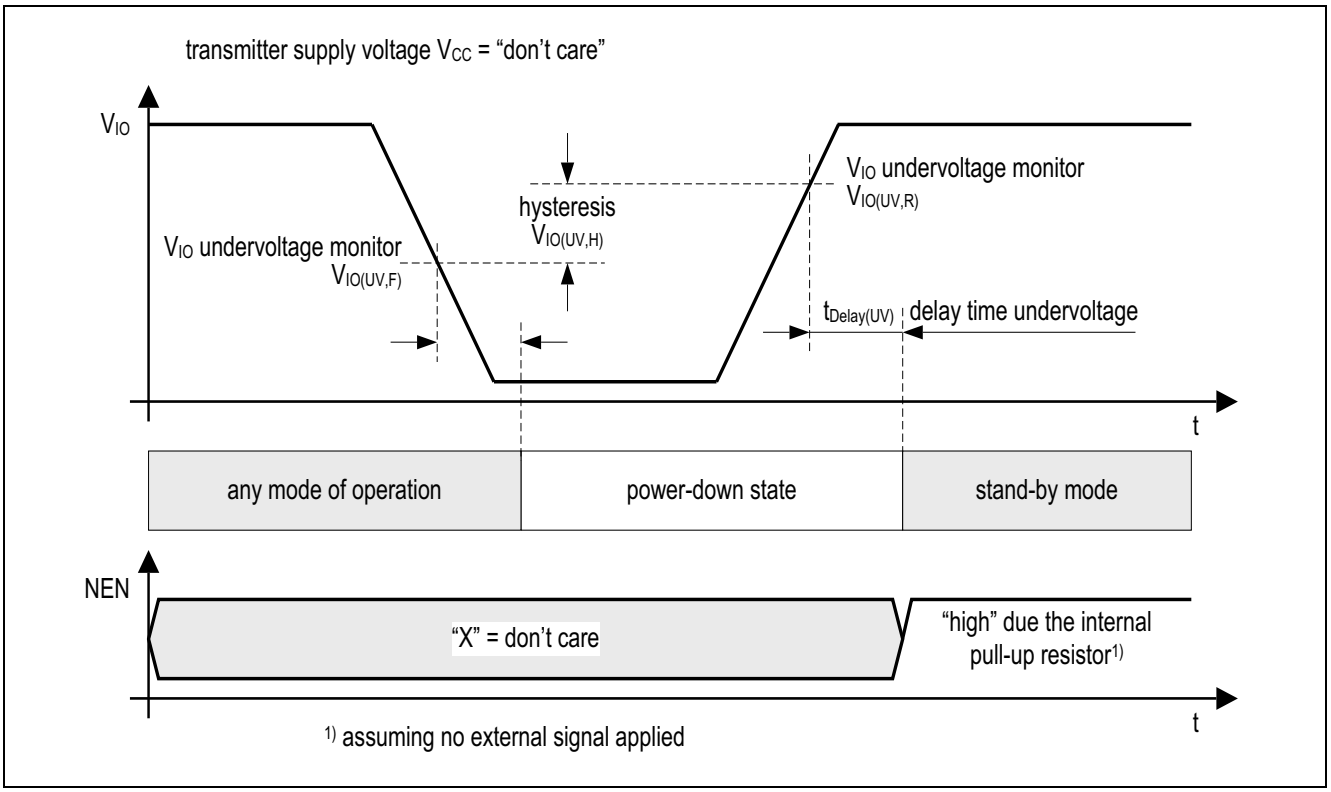


Figure 6 Undervoltage on the digital supply V_{IO}

4.3.5 Undervoltage on the Transmitter Supply V_{CC}

In case the transmitter supply V_{CC} falls below the threshold $V_{CC} < V_{CC(UV,F)}$, the transceiver TLE7250V changes the mode of operation to forced power-save mode. The transmitter and also the normal-mode receiver of the TLE7250V are powered by the V_{CC} supply. In case of an insufficient V_{CC} supply, the TLE7250V can neither transmit the CANH and CANL signals correctly to the bus, nor can it receive them properly. Therefore the TLE7250V blocks the transmitter and the receiver in forced power-save mode (see **Figure 7**).

The undervoltage detection on the transmitter supply V_{CC} is only active in normal-operating mode (see **Figure 5**).

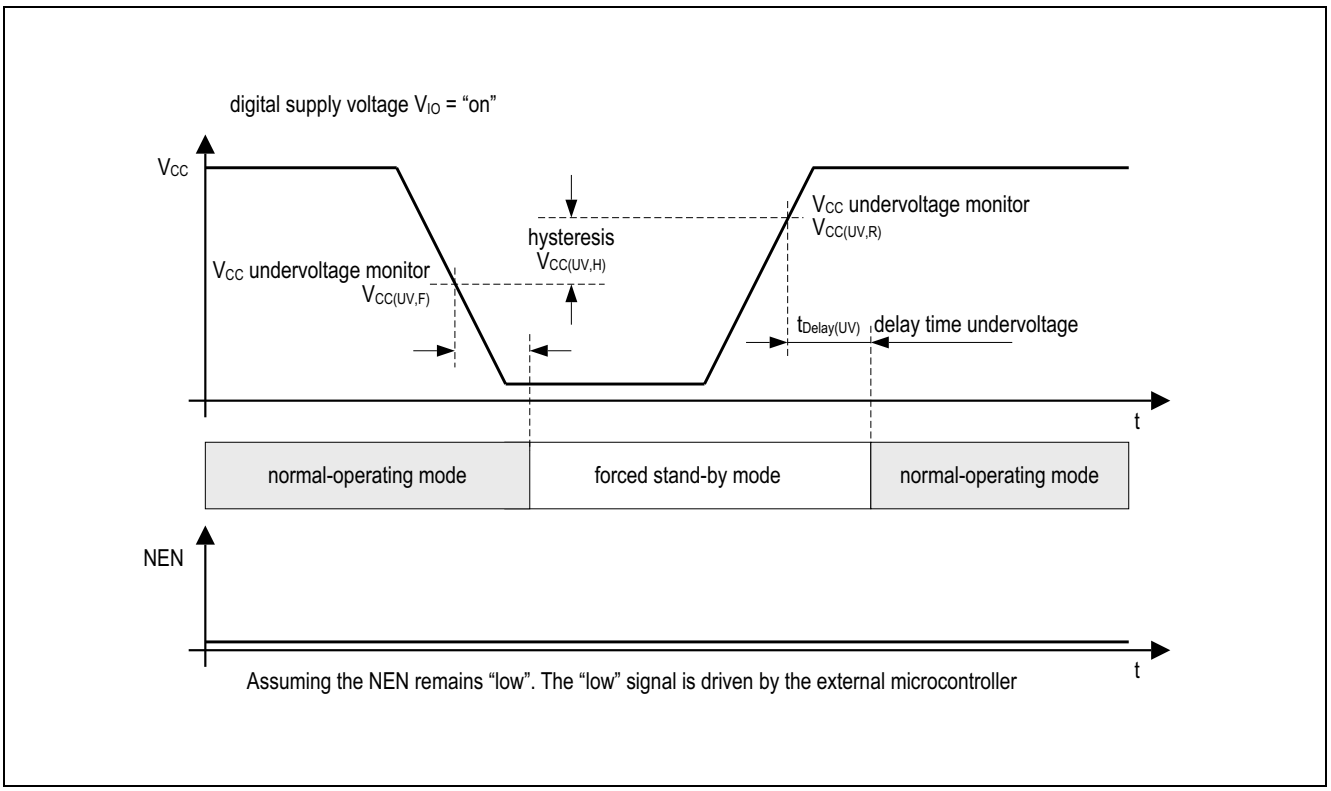


Figure 7 Undervoltage on the transmitter supply V_{CC}

4.3.6 Voltage Adaption to the Microcontroller Supply

The HS CAN transceiver TLE7250V has two different power supplies, V_{CC} and V_{IO}. The power supply V_{CC} supplies the transmitter and the normal-mode receiver. The power supply V_{IO} supplies the digital input and output buffers and it is also the main power domain for the internal logic.

To adjust the digital input and output levels of the TLE7250V to the I/O levels of the external microcontroller, connect the power supply V_{IO} to the microcontroller I/O supply voltage (see **Figure 13**).

Note: In case the digital supply voltage V_{IO} is not required in the application, connect the digital supply voltage V_{IO} to the transmitter supply V_{CC}.

5 Fail Safe Functions

5.1 Short Circuit Protection

The CANH and CANL bus outputs are short circuit proof, either against GND or a positive supply voltage. A current limiting circuit protects the transceiver against damages. If the device is heating up due to a continuous short on the CANH or CANL, the internal overtemperature protection switches off the bus transmitter.

5.2 Unconnected Logic Pins

All logic input pins have an internal pull-up resistor to V_{IO}. In case the V_{IO} supply is activated and the logical pins are open, the TLE7250V enters into the power-save mode by default. In power-save mode the transmitter of the TLE7250V is disabled and the bus bias is floating.

5.3 TxD Time-out Function

The TxD time-out feature protects the CAN bus against permanent blocking in case the logical signal on the TxD pin is continuously “low”. A continuous “low” signal on the TxD pin might have its root cause in a locked-up microcontroller or in a short circuit on the printed circuit board, for example. In normal-operating mode, a logical “low” signal on the TxD pin for the time $t > t_{TxD}$ enables the TxD time-out feature and the TLE7250V disables the transmitter (see **Figure 8**). The receiver is still active and the data on the bus continues to be monitored by the RxD output pin.

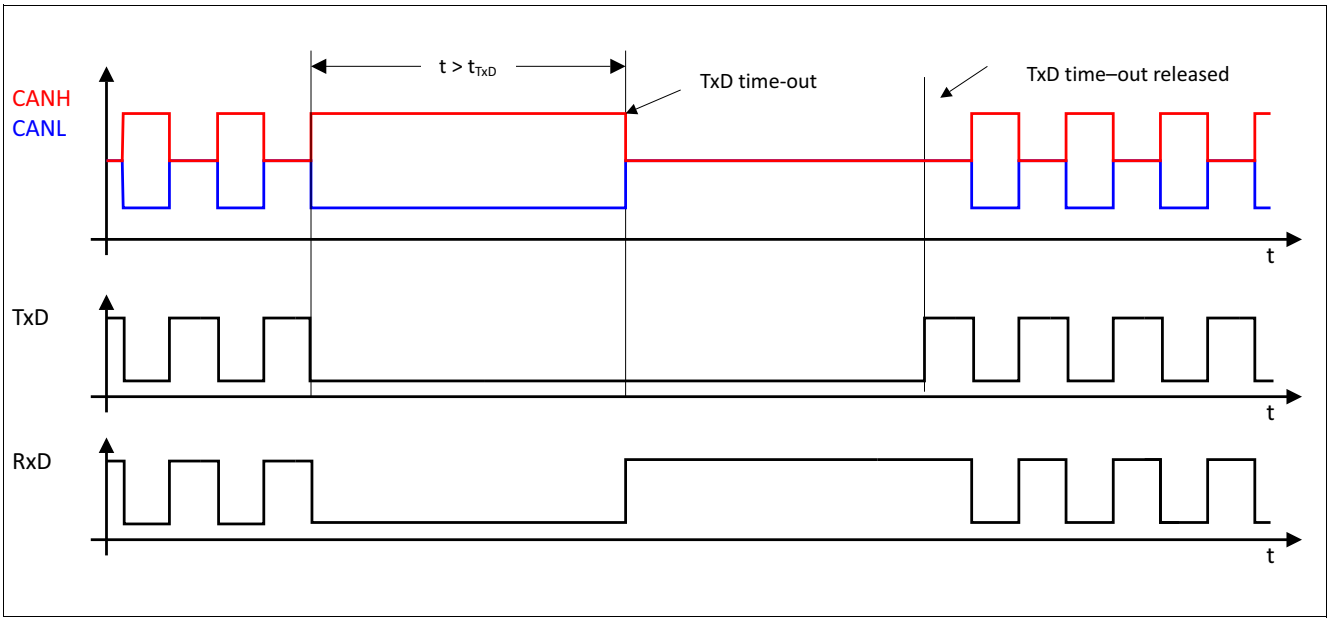


Figure 8 TxD time-out function

Figure 8 illustrates how the transmitter is deactivated and activated again. A permanent “low” signal on the TxD input pin activates the TxD time-out function and deactivates the transmitter. To release the transmitter after a TxD time-out event the TLE7250V requires a signal change on the TxD input pin from logical “low” to logical “high”.

5.4 Overtemperature Protection

The TLE7250V has an integrated overtemperature detection to protect the TLE7250V against thermal overstress of the transmitter. The overtemperature protection is active in normal-operating mode and disabled in power-save mode. In case of an overtemperature condition, the temperature sensor will disable the transmitter (see **Figure 1**) while the transceiver remains in normal-operating mode.

After the device has cooled down the transmitter is activated again (see **Figure 9**). A hysteresis is implemented within the temperature sensor.

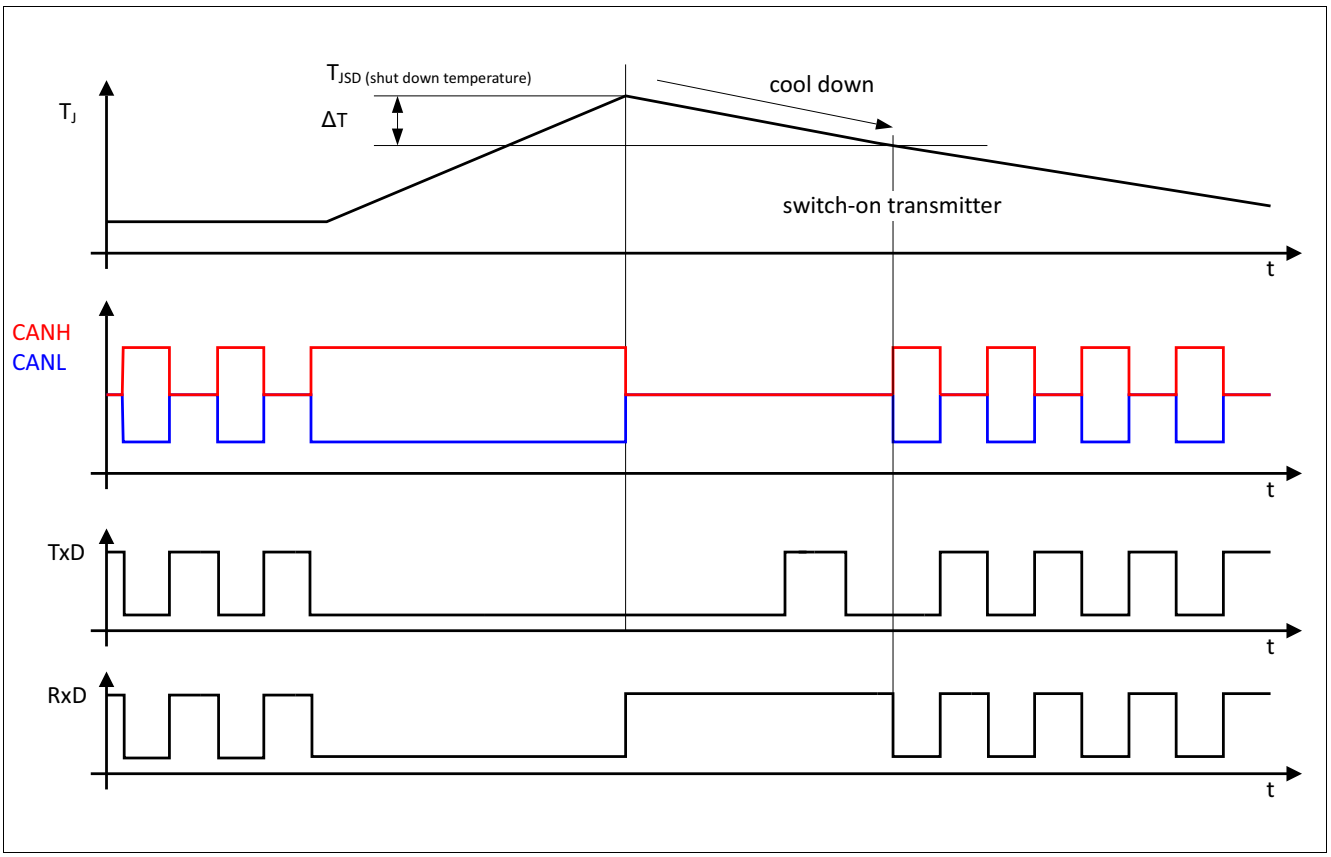


Figure 9 Overtemperature protection

5.5 Delay Time for Mode Change

The HS CAN transceiver TLE7250V changes the mode of operation within the time window t_{Mode}. During the mode change the RxD output pin is permanently set to logical “high” and does not reflect the status on the CANH and CANL input pins (see as an example **Figure 14** and **Figure 15**).

6 General Product Characteristics

6.1 Absolute Maximum Ratings

Table 3 Absolute maximum ratings voltages, currents and temperatures[1)]

All voltages with respect to ground; positive current flowing into pin;
(unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Voltages							
Transmitter supply voltage	V_{CC}	-0.3	–	6.0	V	–	P_6.1.1
Digital supply voltage	V_{IO}	-0.3	–	6.0	V	–	P_6.1.2
CANH DC voltage versus GND	V_{CANH}	-40	–	40	V	–	P_6.1.3
CANL DC voltage versus GND	V_{CANL}	-40	–	40	V	–	P_6.1.4
Differential voltage between CANH and CANL	V_{CAN_Diff}	-40	–	40	V	–	P_6.1.5
Voltages at the input pins: NEN, TxD	V_{MAX_IN}	-0.3	–	6.0	V	–	P_6.1.6
Voltages at the output pin: RxD	V_{MAX_OUT}	-0.3	–	V_{IO}	V	–	P_6.1.7
Currents							
RxD output current	I_{RxD}	-20	–	20	mA	–	P_6.1.8
Temperatures							
Junction temperature	T_j	-40	–	150	°C	–	P_6.1.9
Storage temperature	T_S	-55	–	150	°C	–	P_6.1.10
ESD Resistivity							
ESD immunity at CANH, CANL versus GND	$V_{ESD\_HBM\_CAN}$	-9	–	9	kV	HBM (100 pF via 1.5 kΩ)[2)]	P_6.1.11
ESD immunity at all other pins	$V_{ESD\_HBM\_ALL}$	-2	–	2	kV	HBM (100 pF via 1.5 kΩ)[2)]	P_6.1.12
ESD immunity to GND	V_{ESD_CDM}	-750	–	750	V	CDM[3)]	P_6.1.13

1) Not subject to production test, specified by design

2) ESD susceptibility, Human Body Model “HBM” according to ANSI/ESDA/JEDEC JS-001

3) ESD susceptibility, Charge Device Model “CDM” according to EIA/JESD22-C101 or ESDA STM5.3.1

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal-operating range. Protection functions are not designed for continuos repetitive operation.

6.2 Functional Range

Table 4 Functional range

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Supply Voltages							
Transmitter supply voltage	V_{CC}	4.5	–	5.5	V	–	P_6.2.1
Digital supply voltage	V_{IO}	3.0	–	5.5	V	–	P_6.2.2
Thermal Parameters							
Junction temperature	T_j	-40	–	150	°C	1)	P_6.2.3

1) Not subject to production test, specified by design.

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

6.3 Thermal Resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, please visit **www.jedec.org**.*

Table 5 Thermal resistance[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Thermal Resistances							
Junction to Ambient PG-TSON-8	R_{thJA}	–	55	–	K/W	2) TLE7250VLE	P_6.3.1
Junction to Ambient PG-DSO-8	R_{thJA}	–	130	–	K/W	2) TLE7250VSJ	P_6.3.2
Thermal Shutdown (junction temperature)							
Thermal shutdown temperature	T_{JSD}	150	175	200	°C	–	P_6.3.3
Thermal shutdown hysteresis	ΔT	–	10	–	K	–	P_6.3.4

1) Not subject to production test, specified by design

2) Specified R_{thJA} value is according to Jedec JESD51-2,-7 at natural convection on FR4 2s2p board. The product (TLE7250V) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70µm Cu, 2 x 35µm Cu).

7 Electrical Characteristics

7.1 Functional Device Characteristics

Table 6 Electrical characteristics

4.5 V < V_{CC} < 5.5 V; 3.0 V < V_{IO} < 5.5 V; R_L = 60 Ω; -40 °C < T_j < 150 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Current Consumption							
Current consumption at V_{CC} normal-operating mode	I_{CC}	–	2.6	4	mA	“recessive” state, V_{TxD} = V_{IO}, V_{NEN} = 0 V;	P_7.1.1
Current consumption at V_{CC} normal-operating mode	I_{CC}	–	38	60	mA	“dominant” state, V_{TxD} = V_{NEN} = 0 V;	P_7.1.2
Current consumption at V_{IO} normal-operating mode	I_{IO}	–	–	1	mA	V_{NEN} = 0 V;	P_7.1.3
Current consumption at V_{CC} power-save mode	$I_{CC(PSM)}$	–	–	5	µA	V_{TxD} = V_{NEN} = V_{IO};	P_7.1.4
Current consumption at V_{IO} power-save mode	$I_{IO(PSM)}$	–	5	8	µA	V_{TxD} = V_{NEN} = V_{IO}, 0 V < V_{CC} < 5.5 V;	P_7.1.5
Supply Resets							
V_{CC} undervoltage monitor rising edge	$V_{CC(UV,R)}$	3.8	4.0	4.3	V	–	P_7.1.6
V_{CC} undervoltage monitor falling edge	$V_{CC(UV,F)}$	3.65	3.85	4.3	V	–	P_7.1.7
V_{CC} undervoltage monitor hysteresis	$V_{CC(UV,H)}$	–	150	–	mV	1)	P_7.1.8
V_{IO} undervoltage monitor rising edge	$V_{IO(UV,R)}$	2.0	2.5	3.0	V	–	P_7.1.9
V_{IO} undervoltage monitor falling edge	$V_{IO(UV,F)}$	1.8	2.3	3.0	V	–	P_7.1.10
V_{IO} undervoltage monitor hysteresis	$V_{IO(UV,H)}$	–	200	–	mV	1)	P_7.1.11
V_{CC} and V_{IO} undervoltage delay time	$t_{Delay(UV)}$	–	–	100	µs	1) (see **Figure 6** and **Figure 7**);	P_7.1.12
Receiver Output RxD							
“High” level output current	$I_{RD,H}$	–	-4	-2	mA	V_{RxD} = V_{IO} - 0.4 V, V_{Diff} < 0.5 V;	P_7.1.13
“Low” level output current	$I_{RD,L}$	2	4	–	mA	V_{RxD} = 0.4 V, V_{Diff} > 0.9 V;	P_7.1.14

Table 6 Electrical characteristics (cont'd)

4.5 V < V_{CC} < 5.5 V; 3.0 V < V_{IO} < 5.5 V; R_L = 60 Ω; -40 °C < T_j < 150 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Transmission Input TxD							
"High" level input voltage threshold	$V_{TxD,H}$	–	0.5 × V_{IO}	0.7 × V_{IO}	V	"recessive" state;	P_7.1.15
"Low" level input voltage threshold	$V_{TxD,L}$	0.3 × V_{IO}	0.4 × V_{IO}	–	V	"dominant" state;	P_7.1.16
Pull-up resistance	R_{TxD}	10	25	50	kΩ	–	P_7.1.17
Input hysteresis	$V_{HYS(TxD)}$	–	450	–	mV	1)	P_7.1.18
Input capacitance	C_{TxD}	–	–	10	pF	1)	P_7.1.19
TxD permanent "dominant" time-out	t_{TxD}	4.5	–	16	ms	normal-operating mode;	P_7.1.20
Not Enable Input NEN							
"High" level input voltage threshold	$V_{NEN,H}$	–	0.5 × V_{IO}	0.7 × V_{IO}	V	power-save mode;	P_7.1.21
"Low" level input voltage threshold	$V_{NEN,L}$	0.3 × V_{IO}	0.4 × V_{IO}	–	V	normal-operating mode;	P_7.1.22
Pull-up resistance	R_{NEN}	10	25	50	kΩ	–	P_7.1.23
Input capacitance	C_{NEN}	–	–	10	pF	1)	P_7.1.24
Input hysteresis	$V_{HYS(NEN)}$	–	200	–	mV	1)	P_7.1.25
Bus Receiver							
Differential receiver threshold "dominant" normal-operating mode	V_{Diff_D}	–	0.75	0.9	V	2)	P_7.1.26
Differential receiver threshold "recessive" normal-operating mode	V_{Diff_R}	0.5	0.66	–	V	2)	P_7.1.27
Common mode range	CMR	-12	–	12	V	V_{CC} = 5 V;	P_7.1.28
Differential receiver hysteresis normal-operating mode	$V_{Diff,hys}$	–	90	–	mV	1)	P_7.1.29
CANH, CANL input resistance	R_i	10	20	30	kΩ	"recessive" state;	P_7.1.30
Differential input resistance	R_{Diff}	20	40	60	kΩ	"recessive" state;	P_7.1.31
Input resistance deviation between CANH and CANL	ΔR_i	- 1	–	1	%	1) "recessive" state;	P_7.1.32
Input capacitance CANH, CANL versus GND	C_{In}	–	20	40	pF	1) V_{TxD} = V_{IO};	P_7.1.33
Differential input capacitance	C_{In_Diff}	–	10	20	pF	1) V_{TxD} = V_{IO};	P_7.1.34

Table 6 Electrical characteristics (cont'd)

4.5 V < V_{CC} < 5.5 V; 3.0 V < V_{IO} < 5.5 V; R_L = 60 Ω; -40 °C < T_j < 150 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Bus Transmitter							
CANL/CANH "recessive" output voltage normal-operating mode	$V_{CANL/H}$	2.0	2.5	3.0	V	V_{TxD} = V_{IO}, no load;	P_7.1.35
CANH, CANL "recessive" output voltage difference normal-operating mode	V_{Diff_NM}	-500	–	50	mV	V_{TxD} = V_{IO}, no load;	P_7.1.36
CANL "dominant" output voltage normal-operating mode	V_{CANL}	0.5	–	2.25	V	V_{TxD} = 0 V;	P_7.1.37
CANH "dominant" output voltage normal-operating mode	V_{CANH}	2.75	–	4.5	V	V_{TxD} = 0 V;	P_7.1.38
CANH, CANL "dominant" output voltage difference normal-operating mode according to ISO 11898-2 V_{Diff} = V_{CANH} - V_{CANL}	V_{Diff}	1.5	–	3.0	V	V_{TxD} = 0 V, 50 Ω < R_L < 65 Ω, 4.75 < V_{CC} < 5.25 V;	P_7.1.39
CANH, CANL "dominant" output voltage difference normal-operating mode V_{Diff} = V_{CANH} - V_{CANL}	V_{Diff_R45}	1.4	–	3.0	V	V_{TxD} = 0 V, 45 Ω < R_L < 50 Ω, 4.75 < V_{CC} < 5.25 V;	P_7.1.40
Driver "dominant" symmetry normal-operating mode V_{SYM} = V_{CANH} + V_{CANL}	V_{SYM}	4.5	5	5.5	V	V_{CC} = 5.0 V, V_{TxD} = 0 V;	P_7.1.41
CANL short circuit current	I_{CANLsc}	40	75	100	mA	$V_{CANLshort}$ = 18 V, V_{CC} = 5.0 V, t < t_{TxD}, V_{TxD} = 0 V;	P_7.1.42
CANH short circuit current	I_{CANHsc}	-100	-75	-40	mA	$V_{CANHshort}$ = 0 V, V_{CC} = 5.0 V, t < t_{TxD}, V_{TxD} = 0 V;	P_7.1.43
Leakage current, CANH	$I_{CANH,lk}$	-5	–	5	µA	V_{CC} = V_{IO} = 0 V, 0 V < V_{CANH} < 5 V, V_{CANH} = V_{CANL};	P_7.1.44
Leakage current, CANL	$I_{CANL,lk}$	-5	–	5	µA	V_{CC} = V_{IO} = 0 V, 0 V < V_{CANL} < 5 V, V_{CANH} = V_{CANL};	P_7.1.45

Table 6 Electrical characteristics (cont'd)

4.5 V < V_{CC} < 5.5 V; 3.0 V < V_{IO} < 5.5 V; R_L = 60 Ω; -40 °C < T_j < 150 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Dynamic CAN-Transceiver Characteristics							
Propagation delay TxD-to-RxD "low" ("recessive to "dominant")	$t_{Loop(H,L)}$	–	180	255	ns	C_L = 100 pF, 4.75 V < V_{CC} < 5.25 V, C_{RxD} = 15 pF;	P_7.1.46
Propagation delay TxD-to-RxD "high" ("dominant" to "recessive")	$t_{Loop(L,H)}$	–	180	255	ns	C_L = 100 pF, 4.75 V < V_{CC} < 5.25 V, C_{RxD} = 15 pF;	P_7.1.47
Propagation delay extended load TxD-to-RxD "low" ("recessive to "dominant")	$t_{Loop\_Ext(H,L)}$	–	–	300	ns	[1] C_L = 200 pF, R_L = 120 Ω, 4.75 V < V_{CC} < 5.25 V, C_{RxD} = 15 pF;	P_7.1.53
Propagation delay extended load TxD-to-RxD "high" ("dominant" to "recessive")	$t_{Loop\_Ext(L,H)}$	–	–	300	ns	[1] C_L = 200 pF, R_L = 120 Ω, 4.75 V < V_{CC} < 5.25 V, C_{RxD} = 15 pF;	P_7.1.54
Propagation delay TxD "low" to bus "dominant"	$t_{d(L),T}$	–	90	140	ns	C_L = 100 pF, 4.75 V < V_{CC} < 5.25 V, C_{RxD} = 15 pF;	P_7.1.48
Propagation delay TxD "high" to bus "recessive"	$t_{d(H),T}$	–	90	140	ns	C_L = 100 pF, 4.75 V < V_{CC} < 5.25 V, C_{RxD} = 15 pF;	P_7.1.49
Propagation delay bus "dominant" to RxD "low"	$t_{d(L),R}$	–	90	140	ns	C_L = 100 pF, 4.75 V < V_{CC} < 5.25 V, C_{RxD} = 15 pF;	P_7.1.50
Propagation delay bus "recessive" to RxD "high"	$t_{d(H),R}$	–	90	140	ns	C_L = 100 pF, 4.75 V < V_{CC} < 5.25 V, C_{RxD} = 15 pF;	P_7.1.51
Delay Times							
Delay time for mode change	t_{Mode}	–	–	20	µs	[1] (see **Figure 14** and **Figure 15**);	P_7.1.52

Table 6 Electrical characteristics (cont'd)

4.5 V < V_{CC} < 5.5 V; 3.0 V < V_{IO} < 5.5 V; R_L = 60 Ω; -40 °C < T_j < 150 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
CAN FD Characteristics							
Received recessive bit width at 2 MBit/s	$t_{Bit(RxD)\_2MB}$	400	500	550	ns	C_L = 100 pF, 4.75 V < V_{CC} < 5.25 V, C_{RxD} = 15 pF, t_{Bit} = 500 ns, (see **Figure 12**);	P_7.1.55
Transmitted recessive bit width at 2 MBit/s	$t_{Bit(Bus)\_2MB}$	435	500	530	ns	C_L = 100 pF, 4.75 V < V_{CC} < 5.25 V, C_{RxD} = 15 pF, t_{Bit} = 500 ns, (see **Figure 12**);	P_7.1.56
Receiver timing symmetry at 2 MBit/s $\Delta t_{Rec} = t_{Bit(RxD)} - t_{Bit(Bus)}$	Δt_{Rec_2MB}	-65	–	40	ns	C_L = 100 pF, 4.75 V < V_{CC} < 5.25 V, C_{RxD} = 15 pF, t_{Bit} = 500 ns, (see **Figure 12**);	P_7.1.57

1) Not subject to production test, specified by design.

2) In respect to common mode range.

7.2 Diagrams

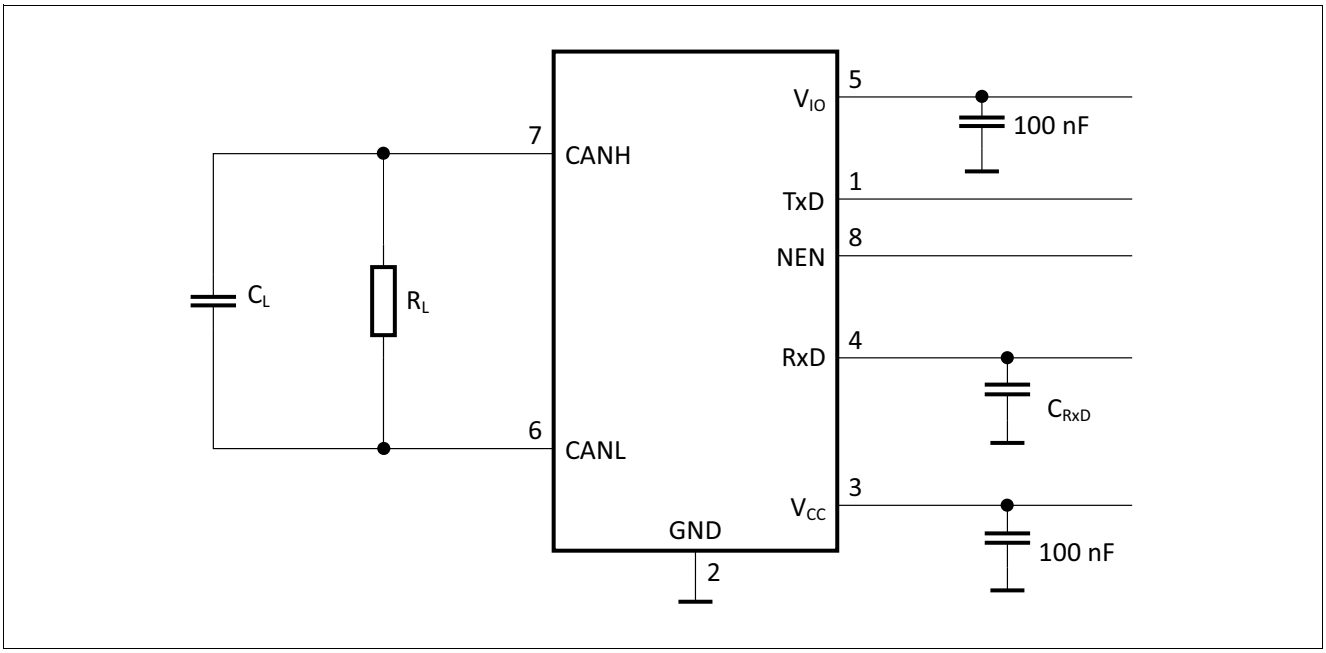


Figure 10 Test circuits for dynamic characteristics

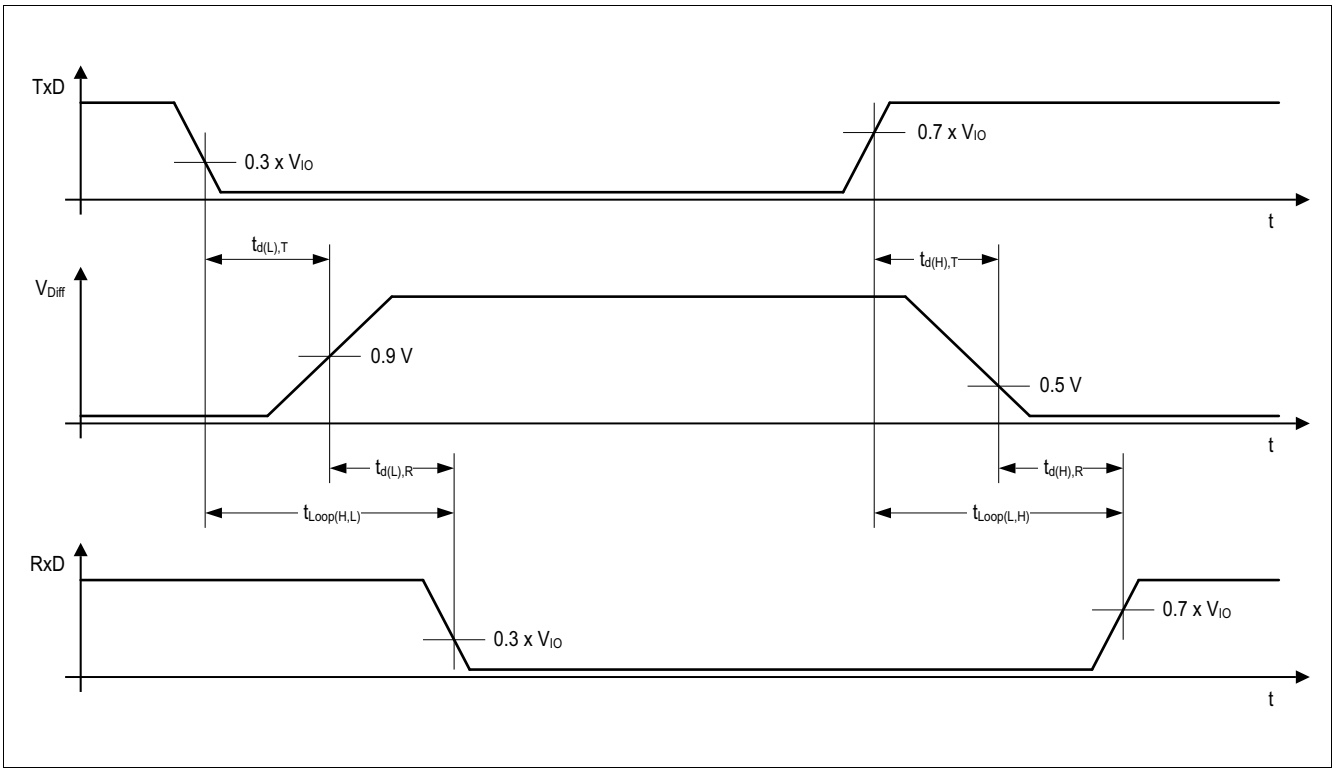


Figure 11 Timing diagrams for dynamic characteristics

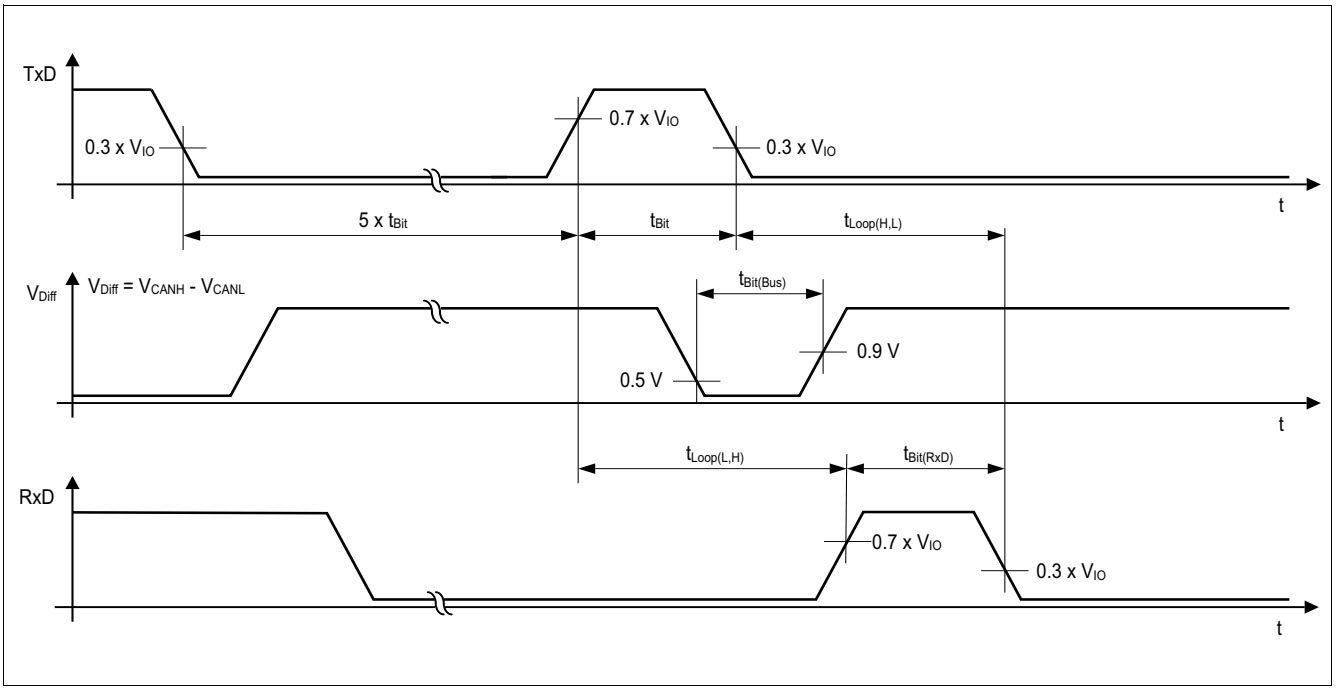


Figure 12 “Recessive” bit time - five “dominant” bits followed by one “recessive” bit