Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

TLE 7263E

Integrated HS-CAN, LIN, LDO and HS Switch

System Basis Chip

Automotive Power

Never stop thinking.

Integrated HS-CAN, LIN, LDO and HS Switch System Basis Chip **TLE 7263E**

AEC Qualified RoHS

1 Overview

PG-DSO-36-53

Features

- Two Low Drop Voltage Regulators
- Window watchdog
- Standard 16-bit SPI-interface
- Supports µController Stop Mode
- Sleep Mode (50µA)
- V_{BAT} Monitoring and fail-safe output
- Overtemperature and short circuit protection
- Power on and undervoltage reset generator
- High side switch, 150 mA
- 4 Monitoring / wake-up inputs
- Exposed Pad Package
- AEC Qualified
- Green (RoHS Compliant) product

HS CAN Transceiver

- CAN data transmission rate up to 1 MBaud
- Low power mode management
- Supports sleep and receive-only modes
- Bus wake-up capability via CAN message
- Bus pins are short circuit proof to ground and battery voltage

LIN Transceiver

- Single-wire transceiver
- Transmission rate up to 20 kBaud
- Compatible to LIN specification 1.3, 2.0, 2.1 and SAE J2602-2
- Very low current consumption in Sleep Mode
- Short circuit proof to GND and battery

Type	Package	Marking
TLE 7263E	PG-DSO-36-53	

Dual-Voltage Regulator

- Low-dropout voltage regulator, dual voltage-supply
- V1, 150 mA, 5 V ±2% for external devices, e.g. microcontrollers
- V2, 150 mA, 5 V ±2% for internal CAN module and external devices.

Description

The TLE 7263E is a monolithic integrated circuit in an enhanced power package. The IC is designed for CAN-LIN gateway applications.

To support these applications the TLE 7263E covers smart power functions such as HS-CAN transceiver and LIN transceiver for data transmission, dual low dropout voltage regulator (LDO) for external 5 V supply, and high-side switch as well as a 16-bit SPI (serial peripheral interface) to control and monitor the IC. There is also a window watchdog circuit with a reset feature, a fail-safe output, a voltage sensing input and a undervoltage reset feature implemented.

The device offer low power modes in order to support modules directly connected to the battery (KL. 30). A wake-up from the low power mode is possible via a message on the bus or via the bi level sensitive monitoring/wake-up inputs. The integrated High-Side switch can also be used to periodically supply an external wake-up circuitry in the low power mode, by choosing a special function. The integrated bus transceivers offer a receive-only mode for software diagnosis functions.

The IC is designed to withstand the severe conditions of automotive applications.

2 Pin Configuration

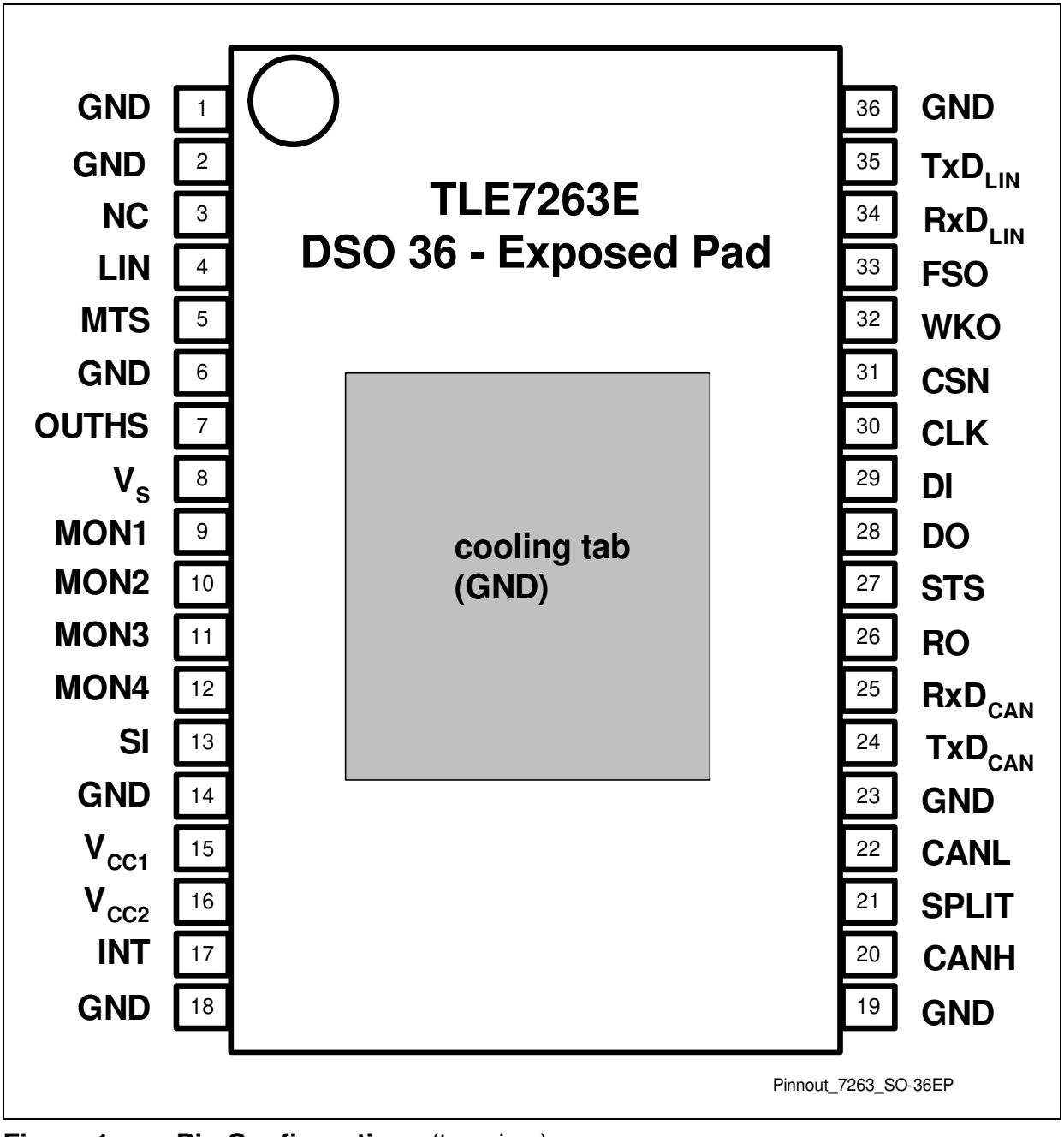

Figure 1 Pin Configuration (top view)

Table 1 Pin Definitions and Functions

Pin	Symbol	Function
9 10 11 12	MON1, MON2, MON3, MON4	**Monitoring / Wake-Up Inputs;** bi level sensitive inputs used to monitor signals coming from, for example, an external switch panel; also used as wake-up input during cyclic sensing in low power modes (MON4 is exempted from “cyclic sense” as this input is permanently active)
8	V_S	**Power Supply Input;** block to GND directly at the IC with ceramic capacitor; (ferrite recommended for better EMC behavior)
15	V_{CC1}	**Voltage Regulator Output (V1);** 5 V supply; to stabilize block to GND with an external capacitor $C_Q \geq 10$ µF, ESR < 6 Ω
16	V_{CC2}	**Voltage Regulator Output (V2);** 5 V supply; to stabilize block to GND with an external capacitor $C_Q \geq 10$ µF, ESR < 6 Ω
32	WKO	**Wake-Up Event Output;** indicates wake up via monitoring inputs, CAN or LIN during Sleep or Stop Mode; active low; wake up sets device to Standby Mode
33	FSO	**Fail Safe Output;** to supervise and control critical applications, high when watchdog is correctly served, low at any reset condition; active low
26	RO	**Reset Output;** open drain output, integrated pull-up, active low
13	SI	**Sense Comparator Input;** for monitoring of external voltages, to program the detection level connect external voltage divider
17	INT	**Interrupt Output;** output to monitor sense comparator input condition; input for enabling the Flash Programming Mode (voltage to be applied > 7 V)
5	MTS	**Master Termination Switch;** output used to turn-on the termination/pull-up resistor of a LIN master
34	RxD_{LIN}	**LIN Transceiver Data Output;** according to the ISO 9141 and LIN specification 1.3 and 2.0; push-pull output; LOW in dominant state
35	TxD_{LIN}	**LIN Transceiver Data Input;** according to ISO 9141 and LIN specification 1.3 and 2.0

Table 1 Pin Definitions and Functions (cont'd)

Pin	Symbol	Function
4	LIN	**LIN Bus;** Bus Line for the LIN interface, according to ISO 9141 and LIN specification 1.3 and 2.0
29	DI_{SPI}	**SPI Data Input;** receives serial data from the control device; serial data transmitted to DI is a 16-bit control word with the Least Significant Bit (LSB) transferred first: the input has a pull-down and requires CMOS logic level inputs; DI will accept data on the falling edge of CLK-signal
28	DO_{SPI}	**SPI Data Output;** this tri-state output transfers diagnosis data to the control device; the output will remain 3-stated unless the device is selected by a low on Chip-Select-Not (CSN)
30	CLK_{SPI}	**SPI Clock Input;** clock input for shift register; CLK has an internal pull-down and requires CMOS logic level inputs
31	CSN_{SPI}	**SPI Chip Select Not Input;** CSN is an active low input; serial communication is enabled by pulling the CSN terminal low; CSN input should only be transitioned when CLK is low; CSN has an internal pull-up and requires CMOS logic level inputs
7	OUTHS	**High Side Switch Output;** controlled via SPI, in SBC Sleep Mode controlled by internal cyclic sense function when selected
24	TxD_{CAN}	**CAN Transmit Data Input;** integrated pull-up
25	RxD_{CAN}	**CAN Receive Data Output**
21	SPLIT	**CAN Termination Output;** to support the recessive voltage level of the bus lines
20	CANH	**CAN High Line Output**
22	CANL	**CAN Low Line Input**
27	STS	**Send-to-Sleep;** to switch the SBC back into low current mode during cyclic wake
1, 2, 6,14, 18,19, 23,36	GND	**Ground**
3	NC	**Not Connected Internally;** leave open or connect to GND
EP	EP	**Exposed Pad;** internally connected to GND; connect to GND on board

3 Block Diagram

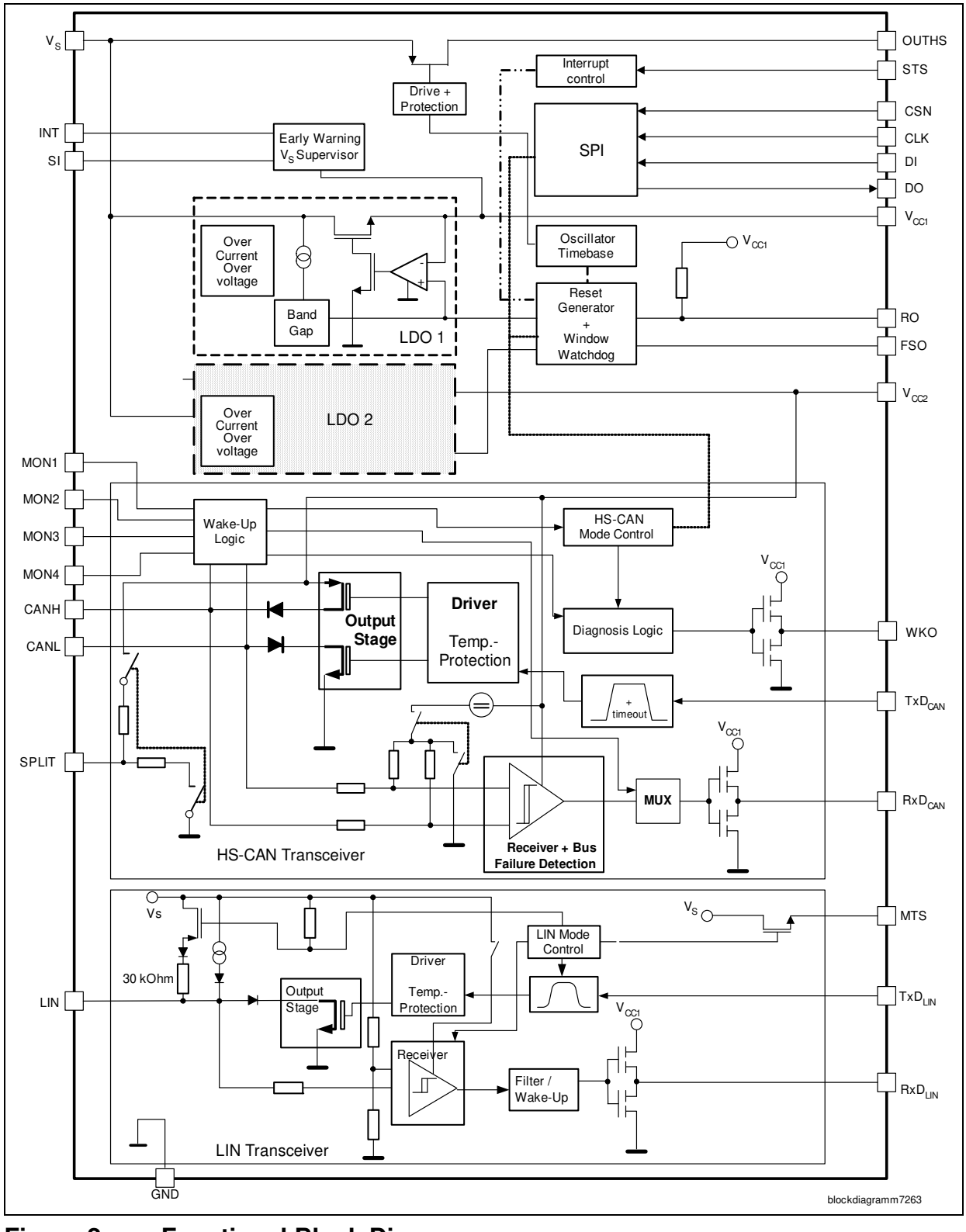

Figure 2 Functional Block Diagram

4 Features

The TLE 7263E incorporates a lot of features, that are listed in **Table 2** below. A short description of the features is given in **"Operation Modes" on Page 9**.

Table 2 Truth Table of the TLE 7263E

Feature	SBC Active Mode	SBC Standby Mode	SBC Stop Mode	SBC Sleep Mode	CAN RxD-only Mode
V_{CC}, V1, 5 V	ON	ON	ON	OFF	ON
V_{CC}, V2, 5 V	ON	ON/OFF	ON/OFF	OFF[1)]	ON
Reset RO	ON	ON	ON	OFF	ON
Window Watchdog	ON	ON	ON/OFF	OFF/[ON]	ON
Fail Safe Output	ON	ON	ON	OFF	ON
Sense input	ON	ON	ON	OFF	ON
Monitoring pins	ON	ON	ON	ON	ON
HS-switch	ON	ON	ON	OFF	ON
HS-cyclic-sense	OFF	OFF	ON	ON	OFF
16-bit SPI	ON	ON	ON	OFF	ON
CAN/LIN wake-up via bus message	OFF/"Sleep"	ON	ON	ON	OFF
CAN Transmit	ON/"Sleep"	OFF	OFF	OFF	OFF
CAN Receive	ON/"Sleep"	OFF	OFF	OFF	ON
LIN Transmit	ON/"Sleep"	OFF	OFF	OFF	ON
LIN Receive	ON/"Sleep"	OFF	OFF	OFF	ON
RxD_{LIN}	L/H	active low wake-up interrupt	active low wake-up interrupt	low	L/H
RxD_{CAN}	L/H	active low wake-up interrupt	active low wake-up interrupt	low	L/H
INT output	active low early warning	active low early warning	active low early warning	low	active low early warning
WKO output	OFF	active low wake-up	active low wake-up	low	OFF

1) In Sleep Mode the Vcc2 should be switched off. This is the default setting at the SPI

4.1 Operation Modes

This System Basis Chip (SBC) offers five main operation modes that are controlled via three mode select bits MS1, MS2 and MS3 within the SPI: SBC Active, Standby, Sleep and Stop mode, as well as CAN Receive-Only mode. After powering-up the SBC, it starts-up in **SBC Standby Mode**, waiting for the microcontroller to finish its startup and initialization sequences. From this transition mode the SBC can be switched via SPI command into the desired operating mode (The device should not be switched directly from Standby Mode to Sleep or Stop Mode). All modes are selected via SPI bits or certain operation conditions, e.g. external wake-up events.

The **SBC Active Mode**, that is used in order to transmit and receive CAN and LIN messages, supports two additional sub-modes, “CAN Sleep” and “LIN Sleep”. During these sub-modes the SBC remains its voltage regulators running in order to supply external devices. Also, the line termination of the “sleeping” bus transceiver is turned-off respectively.

During **SBC Sleep Mode**, the lowest power consumption is achieved, by having its main voltage regulator switched-off. As the microcontroller can not be supplied, the integrated window watchdog might be disabled in Sleep Mode via SPI bit. However, it can be turned-on for periodically waking-up the system, e.g. ECU, by generating a reset.

In case an external microcontroller needs to be supplied with its quiescent current, the **SBC Stop Mode** can be chosen. In this mode the main voltage regulator remains active. Optionally, the second voltage regulator can be turned-on or off via the SPI prior to entering one of the respective power saving modes. The integrated window watchdog remains active until the microcontroller enters its power saving mode (“Stop Mode”). This power saving mode is assumed to be reached once the current consumption is below a certain threshold (see **Watchdog current threshold**, **Table** and **“Window Watchdog, Reset” on Page 26**).

In both low power modes the internal bus transceivers, including the line termination, are turned off while the wake-up capabilities via bus message or monitoring pins are still active. The SBC offers Sleep and Stop Mode in conjunction **with** or **without** the Cyclic Sense/Wake feature. If the Cyclic Sense/Wake feature is selected, two possible states can be entered during Sleep/Stop Mode: **HS-On** and **HS-Off** (see text and respective state diagram).

The **Cyclic Sense** feature can be used to supply an external wake-up circuitry periodically, and is entered upon activation via SPI command. In cyclic sense HS-On state, the High-Side switch is activated for a certain “on-time” and provides supply voltage at its OUTHS pin. Within this on-time the SBC starts sampling of the monitoring/wake-up lines. On-time as well as time period are programmable via the SPI control word. A wake-up at the monitoring / wake-up pins during the on-time as well as a message at the CAN or LIN bus lines automatically sets the TLE 7263E into SBC Standby mode, and turns-on the main voltage regulator V_{CC1}. The digital RxD_{CAN}/RxD_{LIN} lines, that are monitored by the microcontroller during power saving, are pulled low with

respect to the wake-up source (CAN or LIN). Furthermore, the wake-up source is indicated within the SPI status word. Additionally, the wake-up capabilities of the monitoring / wake-up pins can be configured via SPI.

If **Cyclic Wake** is entered upon SPI command, the High-Side switch is turned-on immediately (HS-On state), providing supply voltage at the OUTHS pin. Once the HS-On state is entered, a transition to the HS-Off state can be triggered by a pulse with a minimum width at the STS pin (see **STS pulse width**, **Table**). The microcontroller fully controls the signal level at the STS pin, and this way determines the duration of the HS-On state. As of now the HS-Off state is automatically terminated according to the Cyclic Wake period selected via SPI, or by a CAN or LIN message.

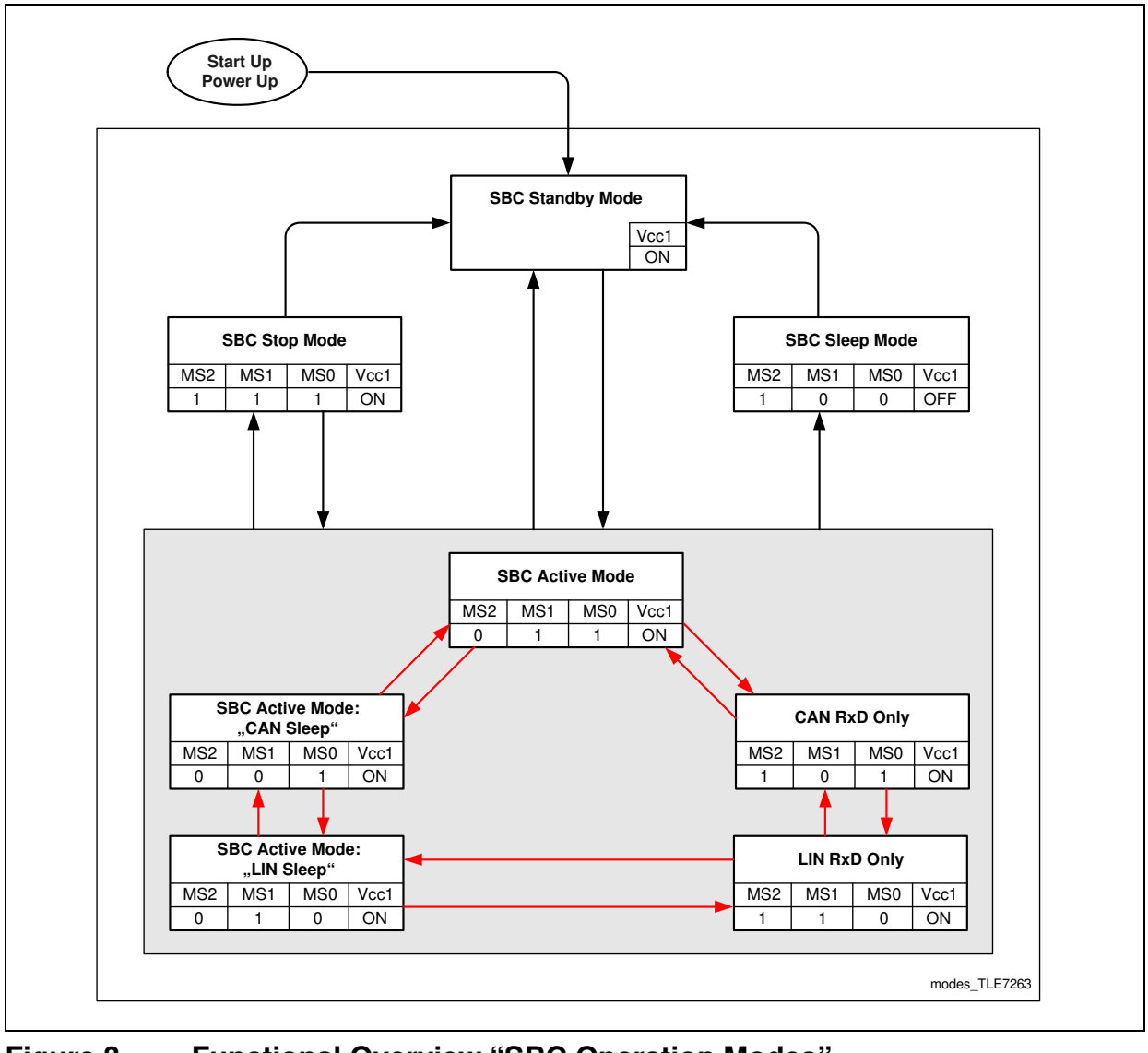

Figure 3 Functional Overview “SBC Operation Modes”

4.2 SBC Sleep Mode without Cyclic Sense

In order to reduce the current consumption to a minimum, the SBC offers a Sleep Mode without Cyclic Sense (see **Figure 4**). This mode is entered via SPI command, and turns-off the integrated bus transceivers and respective termination, main voltage regulator as well as the High-Side switch. Upon a voltage level change at the monitoring/wake-up pins or by a CAN or LIN message the SBC Sleep Mode will be terminated and the SBC Standby Mode will automatically be entered.

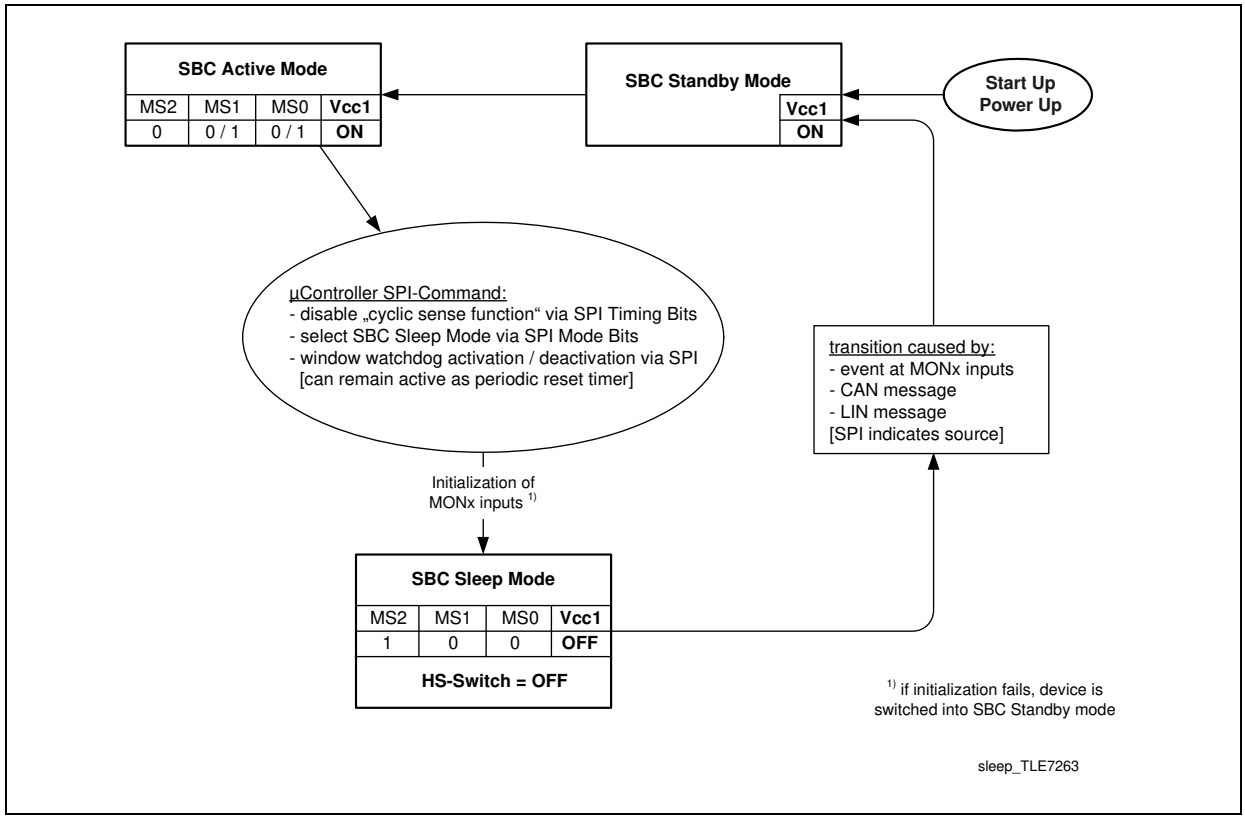

Figure 4 State Diagram “SBC Sleep Mode without Cyclic Sense”

Note: To switch into Low Power Mode from Standby Mode the device should be switched into Normal Mode first. This is required to reset the CAN and LIN transceiver to ensure correct wakeup as well as to ensure the correct function of the RO pin when going to Sleep Mode. The time the device is in Normal Mode before going to Low Power Mode should be long enough that the Vcc2 is up. This can be released by a wait time or by reading the status of Vcc2 via SPI (bit13).

4.3 SBC Sleep Mode with Cyclic Sense

In order to reduce the current consumption to a minimum, but still supply a wake-up circuit periodically, the SBC offers a Sleep Mode with Cyclic Sense (see **Figure 5**). This mode is entered via SPI command, and turns-off the integrated bus transceivers and respective termination, as well as the main voltage regulator. The High-Side switch is turned-on according to the SPI timings setting for cyclic sense, as there is the cyclic sense period and the on-time. Upon a voltage level change at the monitoring/wake-up pins or by a CAN or LIN message the SBC Sleep Mode will be terminated and the SBC Standby Mode will automatically be entered. The respective RxD pin of the transceiver that generated the wake-up will be pulled low.

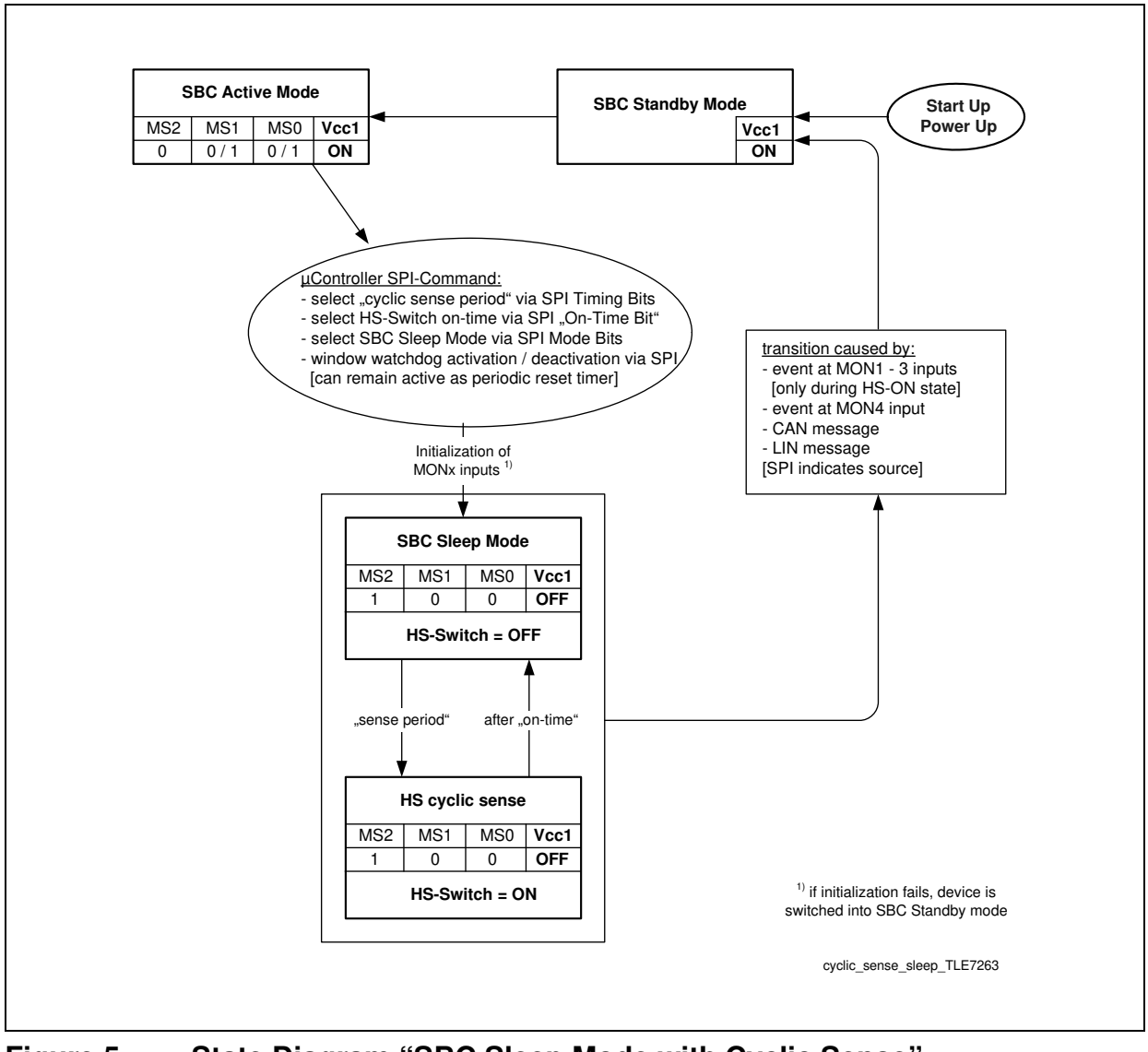

Figure 5 State Diagram “SBC Sleep Mode with Cyclic Sense”

4.4 SBC Sleep Mode with Cyclic Wake

The SBC Sleep Mode has the advantage of reducing the current consumption to a minimum. During this mode the integrated voltage regulator for external supply is turned off. In case the connected microcontroller needs to get activated periodically, the Cyclic Wake feature in combination with the SBC Sleep Mode can be activated (see **Figure 6**).

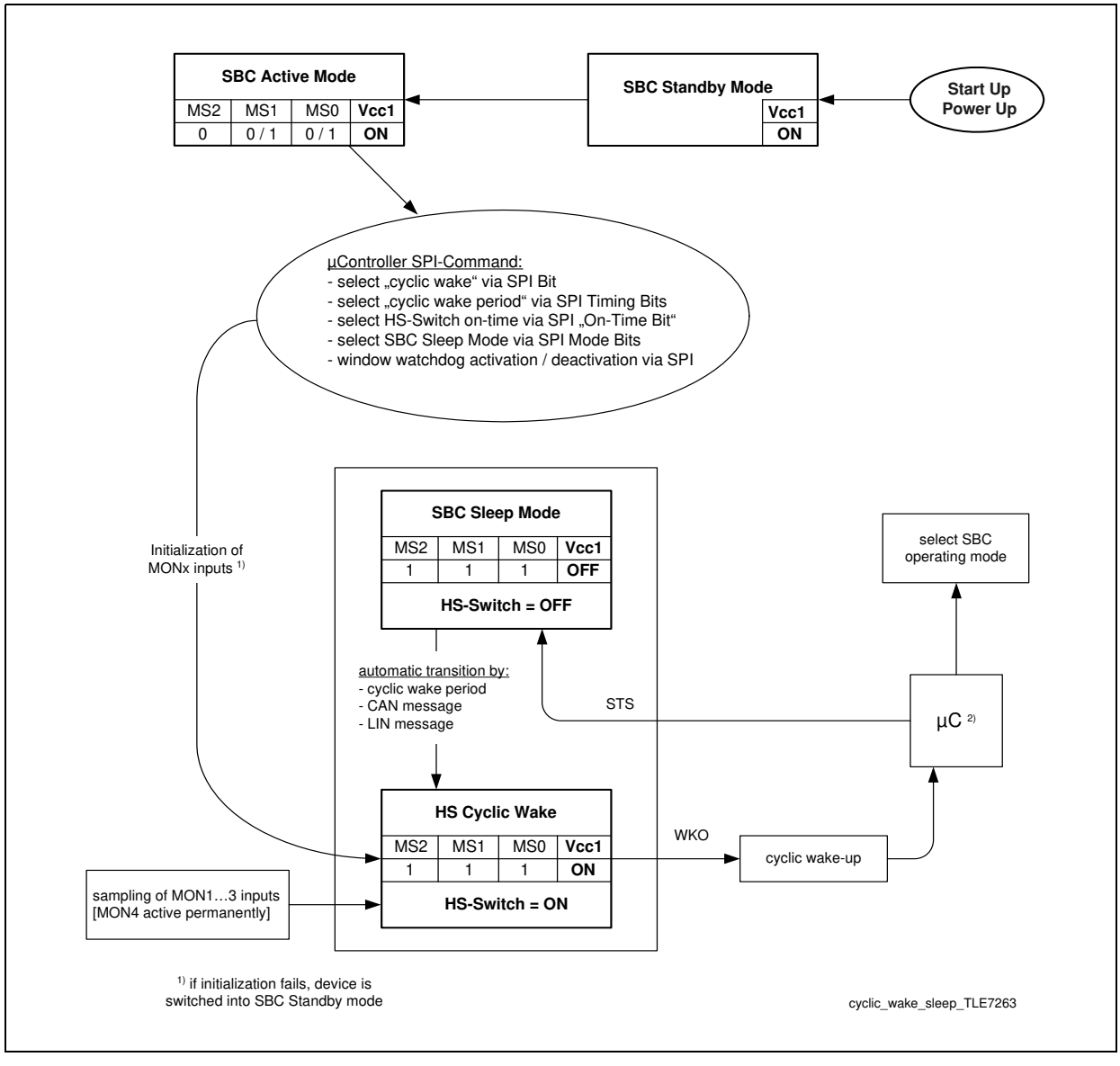

Figure 6 State Diagram “SBC Sleep Mode with Cyclic Wake”

4.5 SBC Stop Mode without Cyclic Sense

The SBC Stop Mode has the advantage of reducing the current consumption to a minimum, while supplying the microcontroller with its quiescent current during its power saving mode (“Stop”). This mode is entered via SPI command, and turns-off the integrated bus transceivers and respective termination, but the main voltage regulator remains active.

A voltage level change at the monitoring / wake-up pins will, in contrast to the behavior in Sleep Mode, generate a pulse at the WKO pin that is monitored by the microcontroller, e.g. at an external interrupt input. In case the wake-up event was a CAN or LIN message, the respective RxD pin will be pulled low. (The microcontroller itself has to take care of switching SBC modes after a wake-up event notification (see **Figure 7**).)

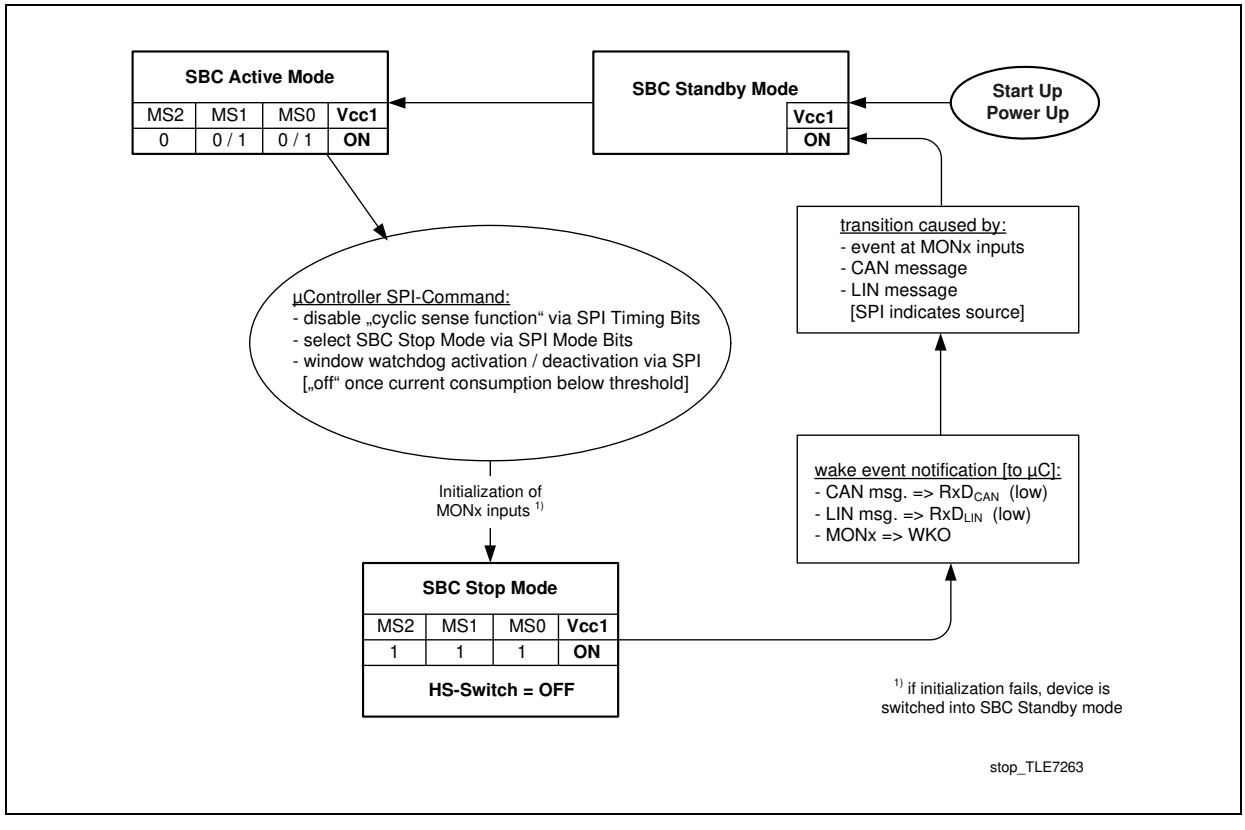

Figure 7 State Diagram “SBC Stop Mode without Cyclic Sense”

4.6 SBC Stop Mode with Cyclic Sense

The SBC Stop Mode has the advantage of reducing the current consumption to a minimum, while supplying the microcontroller with its quiescent current during its power saving mode (“Stop”). This mode is entered via SPI command, and turns-off the integrated bus transceivers and respective termination, but the main voltage regulator remains active. The High-Side switch is turned-on according to the SPI timings setting for cyclic sense, as there is the cyclic sense period and the on-time. A voltage level change at the monitoring/wake-up pins will, in contrast to the behavior in Sleep Mode, generate a pulse at the WKO pin that is monitored by the microcontroller, e.g. at an external interrupt input. In case the wake-up event was a CAN or LIN message, the respective RxD pin will be pulled low. (The microcontroller itself has to take care of switching SBC modes after a wake-up event notification (see **Figure 8**).)

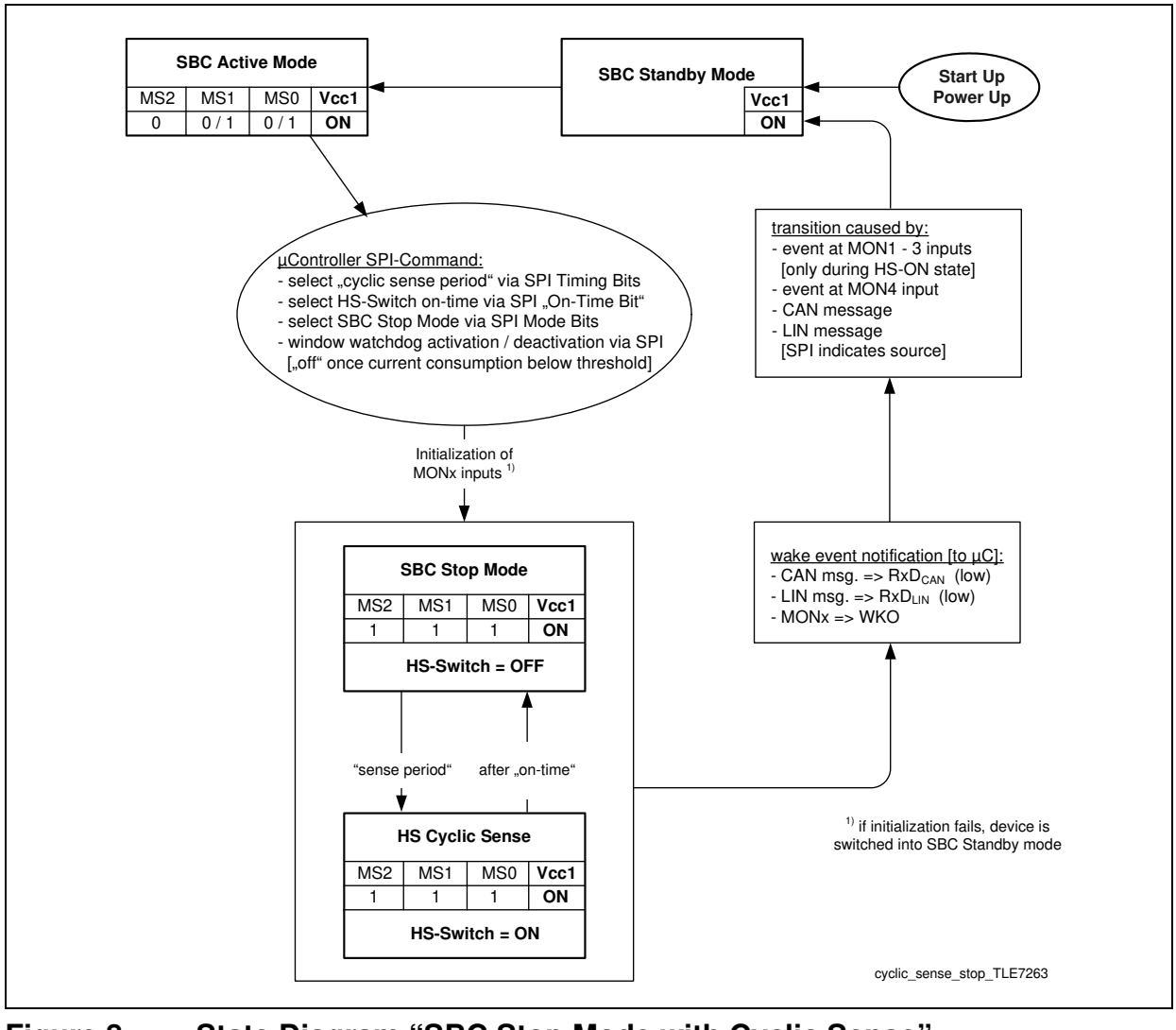

Figure 8 State Diagram “SBC Stop Mode with Cyclic Sense”

4.7 SBC Stop Mode with Cyclic Wake

The SBC Stop Mode has the advantage of reducing the current consumption to a minimum, while supplying the microcontroller with its quiescent current during its power saving mode (“Stop”). This mode is entered via SPI command, and turns-off the integrated bus transceivers and respective termination, but the main voltage regulator remains active. In contrast to Cyclic Sense the HS-On state is entered once Cyclic Wake is selected, immediately providing supply voltage at the OUTHS pin. The microcontroller determines the duration of the HS-On state via the STS input pin (see **Figure 9**). Further transitions from that HS-Off into the HS-On state are done by the selected cyclic wake period or by a bus message. The microcontroller is notified by the WKO (Wake-Up Output) that the HS-On state has been entered. Further notification is done in the same way as for Cyclic Sense in Stop Mode.

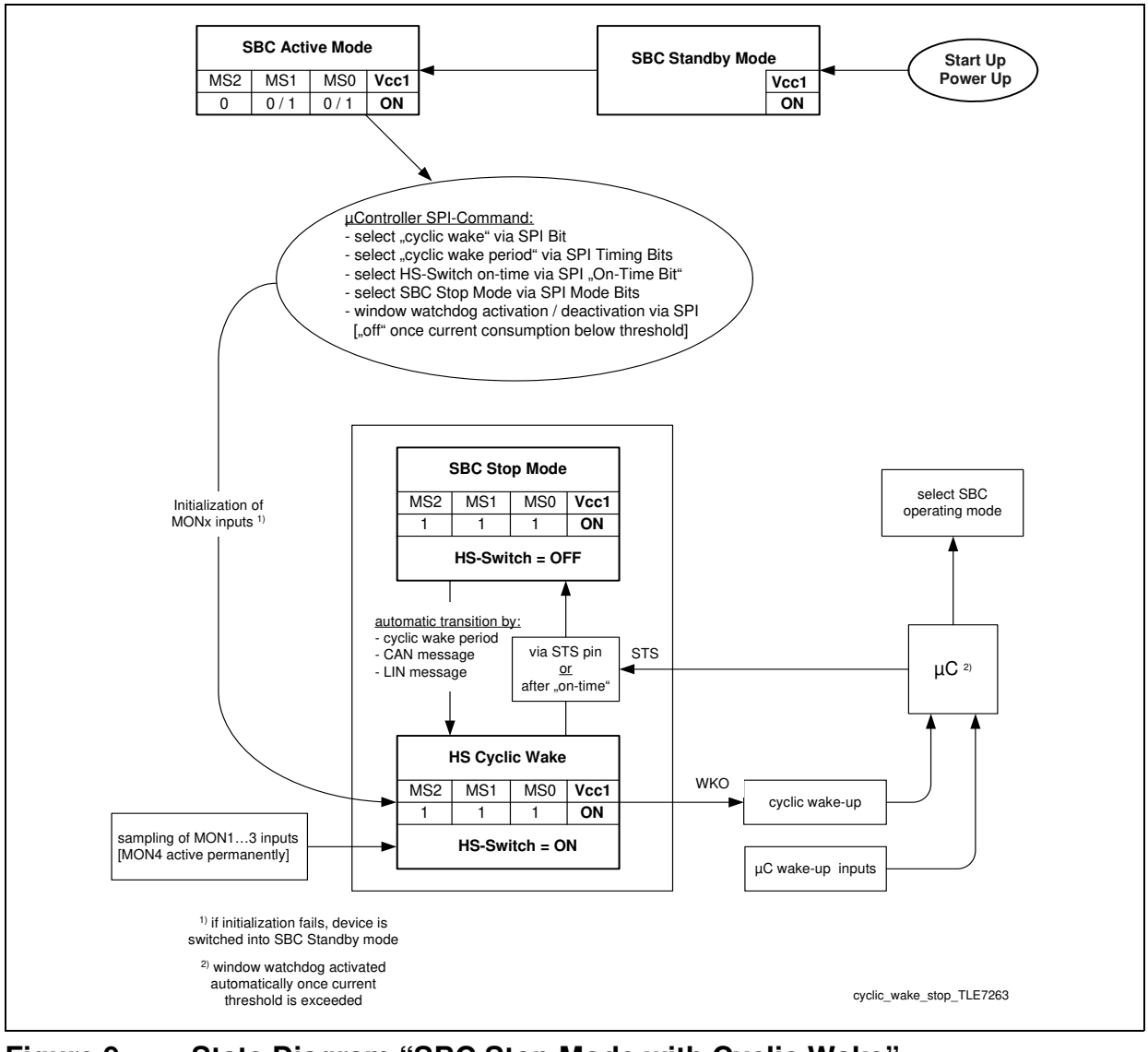

Figure 9 State Diagram “SBC Stop Mode with Cyclic Wake”

Continuous Timer Mode (CTM) for “Cyclic Wake Timer”

Upon start of the “cyclic wake timer” in Cyclic Wake Mode the operating mode might be changed to “SBC Active Mode” by the microcontroller, e.g. in order to transmit data via the CAN or LIN transceiver. In this case the timer continues running with the selected period started in Cyclic Wake Mode. This behavior guarantees the periodic generation of a wake-up signal at the WKO pin, even in case of a mode switch. However, this provides that the time spent in SBC Active Mode is not exceeding the selected period.

Should a time-out (end of selected period) occur in SBC Active Mode before the Cyclic Wake Mode is re-entered, the SBC will generate an interrupt signal at its WKO pin if the CTM feature is enabled via the respective SPI bit (see **Figure 11**).

When the CTM feature is set in the SPI, a wake-up event at the CAN bus in “SBC Active CAN Sleep” mode or at the LIN bus in the “SBC Active LIN Sleep” mode results in switching WKO “low” in addition to switching the RxD to “low”.

4.8 Dual Low Dropout Voltage Regulator

The dual low dropout voltage regulator integrated in the TLE 7263E is able to drive external as well as internal loads, e.g. CAN-circuit supplied via V_{CC2}, even in case of a bus short circuit. Its output voltage tolerance is better than ±2%. The maximum output current for external loads is limited to 150 mA (V_{CC1}), e.g. for microcontroller supply, and 150 mA (V_{CC2}) for internal CAN module and, e.g. for external sensor supply. The two voltage regulator outputs are protected against overload and overtemperature. The thermal pre-warning flag might be used by the microcontroller to reduce the power dissipation of the TLE 7263E by switching off functions of minor priority until the temperature threshold of the thermal shutdown is reached.

An external reverse current protection is required at the pin V_S to prevent the output capacitor from being discharged by negative transients or low input voltage.

A capacitor of 10 µF at the supply voltage input V_S buffers the input voltage. In combination with the required reverse polarity diode this prevents the device from detecting power down conditions in case of negative transients on the supply line. Stability of the output voltage is guaranteed for output capacitors $C_Q \geq 100$ nF, nevertheless it is recommended to use capacitors $C_Q \geq 10$ µF to buffer the output voltage and therefore improve the reset behavior at input voltage transients.

4.9 CAN Transceiver

The TLE 7263E is optimized for high speed data transmission up to 1 MBaud in automotive applications and is compatible to the ISO 11898 standard. It works as an interface between the CAN protocol controller and the physical bus lines.

This HS-CAN module also supports extended bus error detection via a general error flag as well as individual notification flags, e.g. temperature shutdown and TxD time-out flag, within the SPI.

To reduce EMI the dynamic slopes of the CANL and CANH signals both are limited and symmetric. This allows the use of an unshielded twisted or parallel pair of wires for the bus.

Furthermore there is implemented a time-out feature to prevent the bus from being blocked by a permanently dominant TxD input signal. Both, the CANL and CANH output stage are automatically disabled after the delay time t_{TxD}.

In order to protect the transceiver output stages from being damaged by shorts on the bus lines, current limiting circuits are integrated. The CANL and CANH output stage respectively are protected by an additional temperature sensor, that disables them as soon as the junction temperature exceeds the maximum value. During the temperature shut-down condition of the CAN output stages receiving messages from the bus lines is still possible.

Wake-Up Indication: A bus wake-up via a CAN message (minimum dominant time $t > t_{WU}$) from low power mode sets the RxD pin and the WKO pin to low. In addition, the V_{cc2}, which supplies the CAN output stage is switched ON.The CAN transceiver has to be enabled to reset the wake-up capability after a bus wake event and after power-up.

Bus Failure Flag: signalizes a bus line short circuit condition to GND, V_S or V_{CCx} via SPI bit 11 in the SPI Output Data “CAN Bus Failure”.

Remarks: Flag is set after four consecutive recessive to dominant cycles on pin TxD when trying to drive the bus dominant. The bus failure flag is cleared upon 4 recessive to dominant edges at TxD without failure condition.

Local Failure Flag: signalizes the local failure conditions listed in the text below via SPI bit 10 in the SPI Output Data “CAN Local Failure”.

Remark: Flag is cleared upon dominant level at RxD while TxD is recessive.

General: release of the transmitter stage only after transition into CAN RxD Only mode and transition back into SBC Active Mode.

TxD Dominant Failure Detection

At permanent dominant signal for $t > t_{TxD}$ at TxD the local failure flag is set and the transmitter stage is turned off.

Remarks: none

RxD Permanent Recessive Clamping

Internal RxD signal does not match signal at RxD pin because the RxD pin is pulled to HIGH (permanent HIGH). This results in setting the local failure flag and disabling of the receiver stage

Remark: the flag is cleared when RxD signal gets dominant.

TxD to RxD Short Circuit

Caused by a short circuit between RxD and TxD. The local failure flag is set and the transmitter stage is disabled.

Remark: the flag is cleared once the short circuit condition is removed.

Bus Dominant Clamping

At a permanent dominant signal at the CAN bus for $t > t_{BUS}$ the local failure flag is set.

Remark: none

Over Temperature Detection

Once the maximum junction temperature at the driving stages exceeded, the local failure flag is set and the transmitter stage is disabled.

Remark: the flag is cleared once RxD gets dominant. Bus only released after the next dominant bit in TxD.

Split Circuit

The split circuitry is activated during SBC Active and RxD Only Mode and deactivated (SPLIT pin high omic) during SBC Sleep, Stop and Standby Mode. The SPLIT pin is used to stabilize the recessive common mode signal in SBC Active Mode and RxD Only mode. This is realized with a stabilized voltage of 0.5 V_{CC2} at the SPLIT pin.

A correct application of the SPLIT pin is shown in **Figure 10**. The split termination for the left and right node is realized with two 60 Ohm resistances and one 10nF capacitor. The center node in this example is a stub node and the recommended value for the split resistances is 1.5 kOhm.

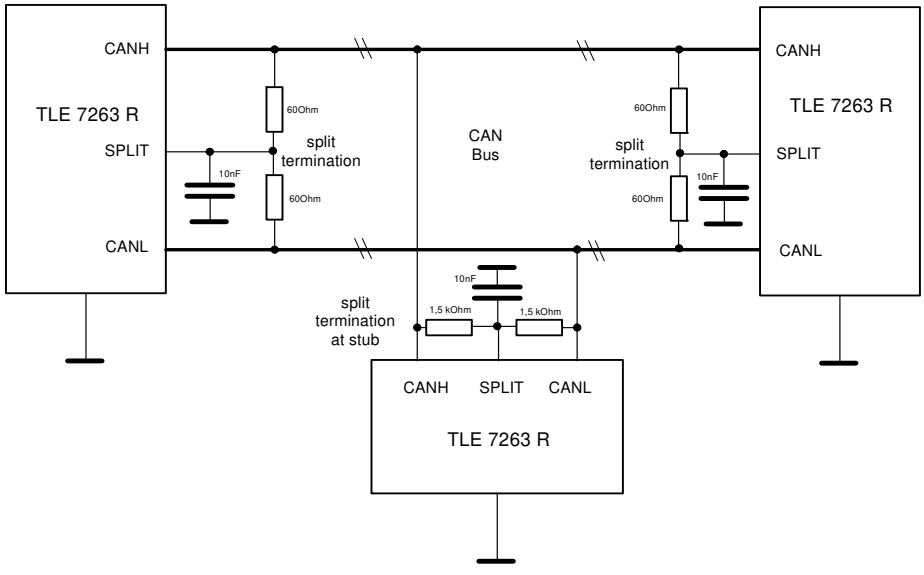

Figure 10 Application of the SPLIT pin for normal nodes and one stub node

4.10 LIN Transceiver

The TLE 7263E offers a transceiver, which is compatible to ISO 9141 and LIN specification 2.0. For fail safe reasons the transceiver already has a pull-up resistor of 30 kΩ implemented. In order to achieve the required timing for the dominant to recessive transition of the bus signal an additional external termination resistor of 1 kΩ is required, when the LIN node is used as a master. This termination resistor will automatically be turned off via the “Master Termination Switch” pin (MTS) once the LIN module enters LIN Sleep Mode or when the SBC enters Sleep Mode. The transceiver is protected against short to battery and short to GND.

For LIN automotive applications in the United States a dedicated mode by the name “Low Slope Mode” can be used. This mode limits the maximum data transmission rate to 10.4 kBaud by switching to a different slew rate. Operating with the default slew rate at up to 20 kBaud may cause interferences with the AM radio band.

A bus wake-up via a LIN message (minimum dominant time $t > t_{wake}$) from low power mode sets the RxD pin and the WKO pin to low. in addition the MTS is switched ON. The LIN transceiver has to be enabled to reset the wake-up capability after a bus wake event and after power-up.

In case of a “TxD dominant time out failure” or a “transmitter thermal shutdown” the SPI bit 9 is set. After a SPI read-out this bit will be reset unless one of the failure conditions is still present.

Note: In case of a short to GND on the LIN bus a RxD dominant signal is generated by the SBC. In the case that RxD is dominant the device can not go into low power mode from normal mode.

4.11 SPI (Serial Peripheral Interface)

The 16-bit wide Programming or Input Word (see **Table 3**) is read in via the data input DI, which is synchronized with the clock input CLK supplied by the µC. The Diagnosis or Output Word appears synchronously at the data output DO (see **Figure 10**).

The transmission cycle begins when the chip is selected by the Chip Select Not input CSN (“low” active). After the CSN input returns from L to H, the word that has been read in becomes the new control word. The DO output switches to tristate status at this point, thereby releasing the DO bus for other usage.

The state of DI is shifted into the input register with every falling edge on CLK. The state of DO is shifted out of the output register after every rising edge on CLK. The number of received input clocks is supervised by a modulo-16 operation and the Input / Control Word is discarded in case of a mismatch. This error is flagged by the WKO set to “low” and in the following SPI output by a “high” at the data output (DO pin) before the first rising edge of the clock is received.

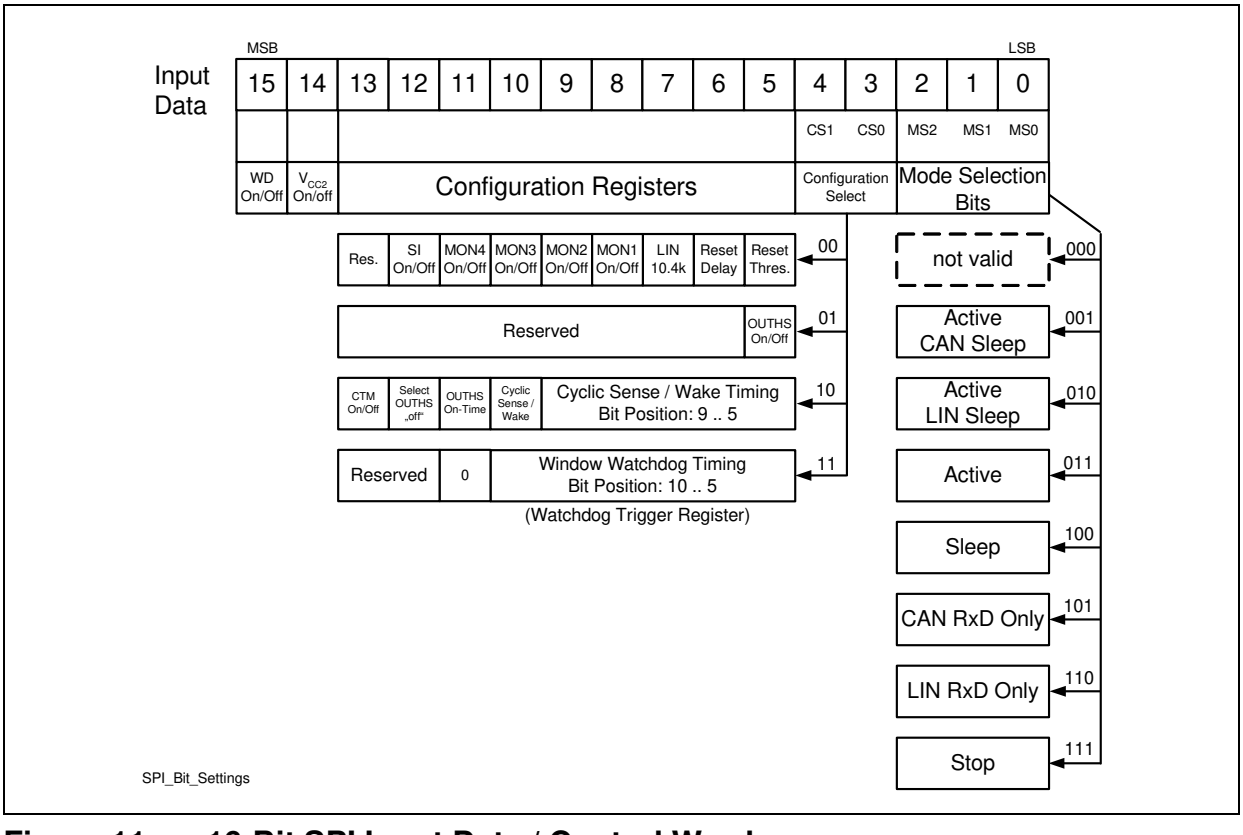

Figure 11 16-Bit SPI Input Data / Control Word

Table 3 SPI Input Data Bits

IBIT	Input Data
0 … 2	Mode Selection
3 … 4	Configuration Selection (determine meaning of “Configuration Setting Bits”)
5 … 13	Configuration Settings (meaning based on “Configuration Selection Bits”)
14	V_{CC2} Activation (power saving modes only)
15	Window Watchdog “on”/“off” (power saving modes only)

Table 4 Mode Selection Bits

MS2	MS1	MS0	Mode Selection: SBC Mode
0	0	0	“reserved” / not valid
0	0	1	SBC Active Mode: “CAN Sleep”
0	1	0	SBC Active Mode: “LIN Sleep”
0	1	1	SBC Active Mode (CAN & LIN “on”)
1	0	0	SBC Sleep (CAN, LIN & VReg “off”)
1	0	1	SBC Active mode : CAN Transceiver: RxD-Only
1	1	0	SBC Active mode : LIN Transceiver: RxD-Only
1	1	1	SBC Stop Mode (CAN & LIN “off”)

Table 5 Configuration Selection Bits

CS1	CS0	Configuration Selection
0	0	General Configuration
0	1	Integrated Switch Configuration
1	0	Cyclic Sense / Wake Configuration
1	1	Window Watchdog Configuration

Table 6 General & Integrated Switch Configuration

Pos.	General Configuration[1)]	Integrated Switch Configuration[2)]
5	Reset Threshold (see **Table** : “Reset Generator”, “0” = V_{RT1} / “1” = V_{RT2})	OUTHS “on” / “off”
6	Reset Delay (“0” = 5 ms / “1” = 0.5 ms)	“reserved” / not used
7	LIN “Low Slope Mode” (10.4 kBaud)	“reserved” / not used
8	MON1 Input Wake-Up Capability	“reserved” / not used
9	MON2 Input Wake-Up Capability	“reserved” / not used
10	MON3 Input Wake-Up Capability	“reserved” / not used
11	MON4 Input Wake-Up Capability	“reserved” / not used
12	Sense Input (SI) “on” / “off”	“reserved” / not used
13	“reserved” / not used	“reserved” / not used

1) “1” = ON (enable), “0” = OFF (disable)

2) “1” = ON, “0” = OFF

Table 7 Cyclic Sense / Wake & Window Watchdog Period Settings[1)]

Pos.	Cyclic Sense / Wake Configuration	Window Watchdog Configuration
5	Cyclic Period Bit 0 (T0)	Watchdog Period Bit 0 (T0)
6	Cyclic Period Bit 1 (T1)	Watchdog Period Bit 1 (T1)
7	Cyclic Period Bit 2 (T2)	Watchdog Period Bit 2 (T2)
8	Cyclic Period Bit 3 (T3)	Watchdog Period Bit 3 (T3)
9	Cyclic Period Bit 4 (T4)	Watchdog Period Bit 4 (T4)
10	Cyclic Sense / Wake Selection (“0” = Cyclic Sense / “1” = Cyclic Wake)	Watchdog Period Bit 5 (T5)
11	OUTHS On-Time Selection (“0” = 500 µs / “1” = 100 µs)	“0” [mandatory]
12	Cyclic Wake Mode only: Select OUTHS “off” via STS / On-Time (“0” = via STS / “1” = via HS On-Time)	“reserved” / not used
13	Continuous Timer Mode (incl. WKO) (“0” = “off” / “1” = “on”)	“reserved” / not used

1) “1” = ON, “0” = OFF

Table 8 Cyclic Sense / Wake Period Settings

T4	T3	T2	T1	T0	Cyclic Sense or Cyclic Wake Period
0	0	0	0	0	Cyclic Sense / Wake “off”
0	0	0	0	1	16 ms
0	0	0	1	0	32 ms
0	0	0	1	1	48 ms
0	0	1	0	0	64 ms
0	0	1	0	1	80 ms
0	0	1	1	0	96 ms
…	…	…	…	…	… ms
1	1	1	1	1	496 ms

Table 9 Window Watchdog Reset Period Settings

T5	T4	T3	T2	T1	T0	Window Watchdog Reset Period
0	0	0	0	0	0	“not a valid selection”
0	0	0	0	0	1	16 ms
0	0	0	0	1	0	32 ms
0	0	0	0	1	1	48 ms
0	0	0	1	0	0	64 ms
0	0	0	1	0	1	80 ms
0	0	0	1	1	0	96 ms
0	…	…	…	…	…	… ms
1	1	1	1	1	1	1008 ms

Table 10 SPI Output Data

Pos.	Output Data “active”[1]	Output Data “after wake-up”[2]
0	V_{CC1} Temperature Prewarning	V_{CC1} Temperature Prewarning
1	HS Overcurrent	HS Overcurrent
2	OUTHS UV / Temp. Shut-Down	OUTHS UV / Temp. Shut-Down
3	Window Watchdog Reset	Window Watchdog Reset
4	MON1 Logic Input Level	Wake-Up via MON1
5	MON2 Logic Input Level	Wake-Up via MON2
6	MON3 Logic Input Level	Wake-Up via MON3
7	MON4 Logic Input Level	Wake-Up via MON4
8	MONx Initialization Failure	MONx Initialization Failure
9	LIN Failure	Bus Wake-Up via LIN Msg.
10	CAN Local Failure	Bus Wake-Up via CAN Msg.
11	CAN Bus Failure	End of Cyclic Wake Period
12	V_{CC1} Fail (active low)	V_{CC1} Fail (active low)
13	V_{CC2} Fail (active low)	V_{CC2} Fail (active low)
14	V_{INT} Fail (active low)	V_{INT} Fail (active low)
15	“reserved” / not used	“reserved” / not used

1) “1” = ON (enable), “0” = OFF (disable)

2) “1” = ON, “0” = OFF