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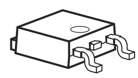
5-V Low Drop Voltage Regulator

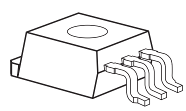
TLE 7274

Features

- Output voltage 5 V ±2%
- Ultra low current consumption: typ. 20µA
- 300 mA current capability
- Very low-drop voltage
- Short-circuit-proof
- Suitable for use in automotive electronics



P-TO252-3-1



P-TO263-3-1

Functional Description

The TLE 7274 is a monolithic integrated low-drop voltage regulator for load currents up to 300 mA. An input voltage up to 42 V is regulated to $V_{Q,nom}$ = 5.0 V with a precision of ±2%. The sophisticated design allows to achieve stable operation even with ceramic output capacitors down to 470 nF. The device is designed for the harsh environment of automotive applications. Therefore it is protected against overload, short circuit and over temperature conditions. Of course the TLE 7274 can be used also in all other applications, where a stabilized 5 V voltage is required. Due to its ultra low stand-by current consumption of typ. 20µA the TLE 7274 is dedicated for use in applications permanently connected to V_{BAT}. An integrated output sink current circuitry keeps the voltage at the Output pin Q below 5.5 V even when reverse currents are applied. Thus connected devices are protected from overvoltage damage.

For applications requiring extremely low noise levels the Infineon voltage regulator family TLE 42XY and TLE 44XY is more suited than the TLE 7274. A mV-range output noise on the TLE 7274 caused by the charge pump operation is unavoidable due to the ultra low quiescent current concept.

Type	Ordering Code	Package
TLE 7274 D	Q67006-A9728	P-TO252-3-1, P-TO252-3-11
TLE 7274 G	Q67006-A9731	P-TO263-3-1

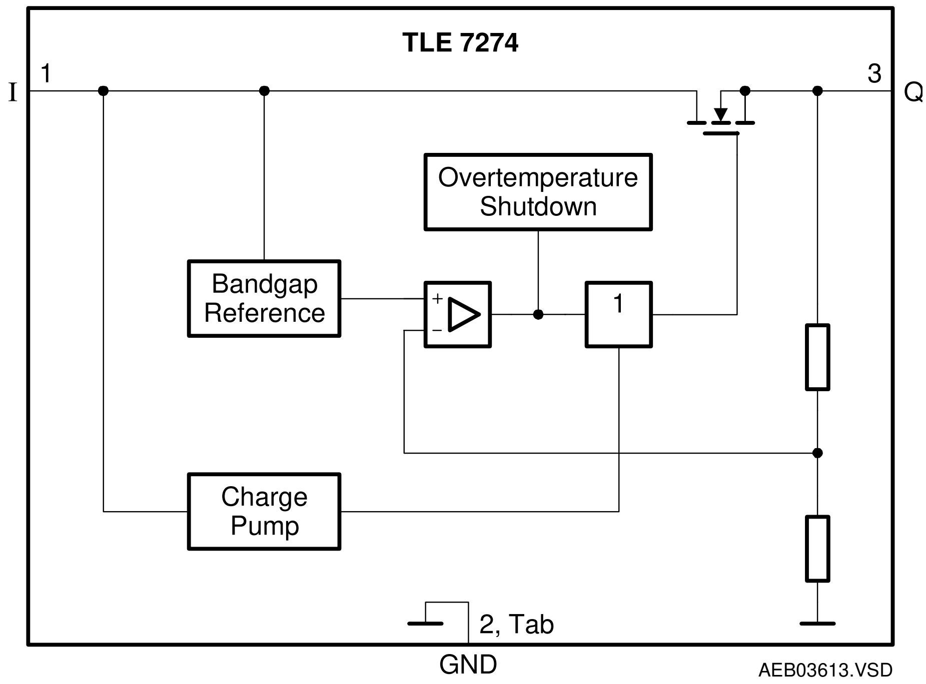


Figure 1 Block Diagram

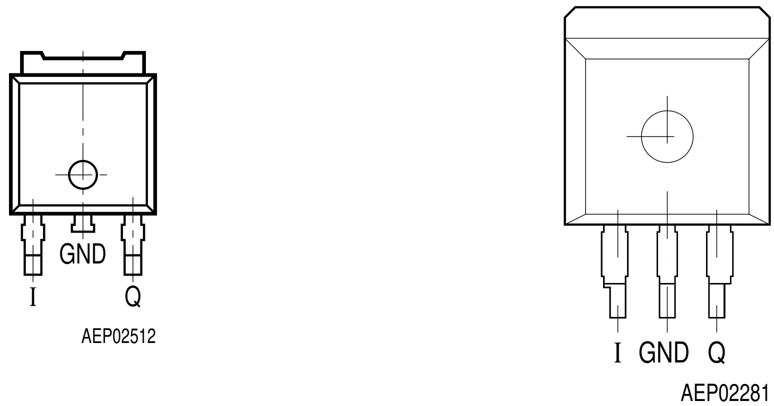


Figure 2 Pin Configuration P-TO252-3 (D-PAK), P-TO263-3 (D^2-PAK)(top view)

Table 1 Pin Definitions and Functions

Pin No.	Symbol	Function
1	I	**Input;** block to ground directly at the IC with a ceramic capacitor.
2	GND	**Ground;** Pin 2 internally connected to heatsink.
3	Q	**Output;** block to ground with a ceramic capacitor, $C \geq 470$ nF.

Table 2 Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Test Condition
		Min.	Max.		
Input I					
Voltage	V_I	-0.3	45	V	–
Current	I_I	-1	–	mA	–
Output Q					
Voltage	V_Q	-0.3	5.5	V	–
Voltage	V_Q	-0.3	6.2	V	t < 10 s[1)]
Current	I_Q	-1	–	mA	–
Temperature					
Junction temperature	T_j	-40	150	°C	–
Storage temperature	T_{stg}	-50	150	°C	–

1) Exposure to these absolute maximum ratings for extended periods (t > 10 s) may affect device reliability.

Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3 Operating Range

Parameter	Symbol	Limit Values		Unit	Remarks
		Min.	Max.		
Input voltage	V_I	5.5	42	V	–
Junction temperature	T_j	-40	150	°C	–

Note: In the operating range, the functions given in the circuit description are fulfilled.

Table 4 Thermal Resistance

Parameter	Symbol	Limit Values		Unit	Remarks
		Min.	Max.		
Junction case	R_{thj-c}	–	8	K/W	–
Junction ambient	R_{thj-a}	–	80	K/W	TO252[1)]
Junction ambient	R_{thj-a}	–	55	K/W	TO263[2)]

1) Worst case, regarding peak temperature; zero airflow; mounted on a PCB FR4, 80 × 80 × 1.5 mm^3, heat sink area 300 mm^2

2) Worst case, regarding peak temperature; zero airflow; mounted on a PCB FR4, 80 × 80 × 1.5 mm^3, heat sink area 300 mm^2

The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at T_a = 25 °C and the given supply voltage.

Table 1 Electrical Characteristics

V_I = 13.5 V; – 40 °C < T_j < 150 °C (unless otherwise specified)

Parameter	Symbol	Limit Values			Unit	Measuring Condition
		Min.	Typ.	Max.		
Output Q						
Output voltage	V_Q	4.9	5.0	5.1	V	0.1 mA < I_Q < 300 mA; 6 V < V_I < 16 V
Output voltage	V_Q	4.9	5.0	5.1	V	0.1 mA < I_Q < 100 mA; 6 V < V_I < 40 V
Output current limitation	I_Q	320	–	–	mA	[1]
Output current limitation	I_Q	–	–	800	mA	V_Q = 0V
Current consumption; $I_q = I_I - I_Q$	I_q	–	20	25	µA	I_Q = 0.1 mA; T_j = 25 °C
Current consumption; $I_q = I_I - I_Q$	I_q	–	–	35	µA	I_Q = 0.1 mA; $T_j \leq$ 80 °C
Drop voltage	V_{dr}	–	250	500	mV	I_Q = 200 mA; $V_{dr} = V_I - V_Q$ [1]
Load regulation	$\Delta V_{Q,lo}$	-40	15	40	mV	I_Q = 5 mA to 250 mA
Line regulation	$\Delta V_{Q,li}$	-20	5	20	mV	V_I = 10V to 32 V; I_Q = 5 mA
Power supply ripple rejection	$PSRR$	–	60	–	dB	f_r = 100 Hz; V_r = 0.5 Vpp
Temperature output voltage drift	dV_Q/dT	–	0.5	–	mV/K	–
Output Capacitor	C_Q	470	–	–	nF	ESR < 3 Ω

1) Measured when the output voltage V_Q has dropped 100 mV from the nominal value obtained at V_I = 13.5 V.

Application Information

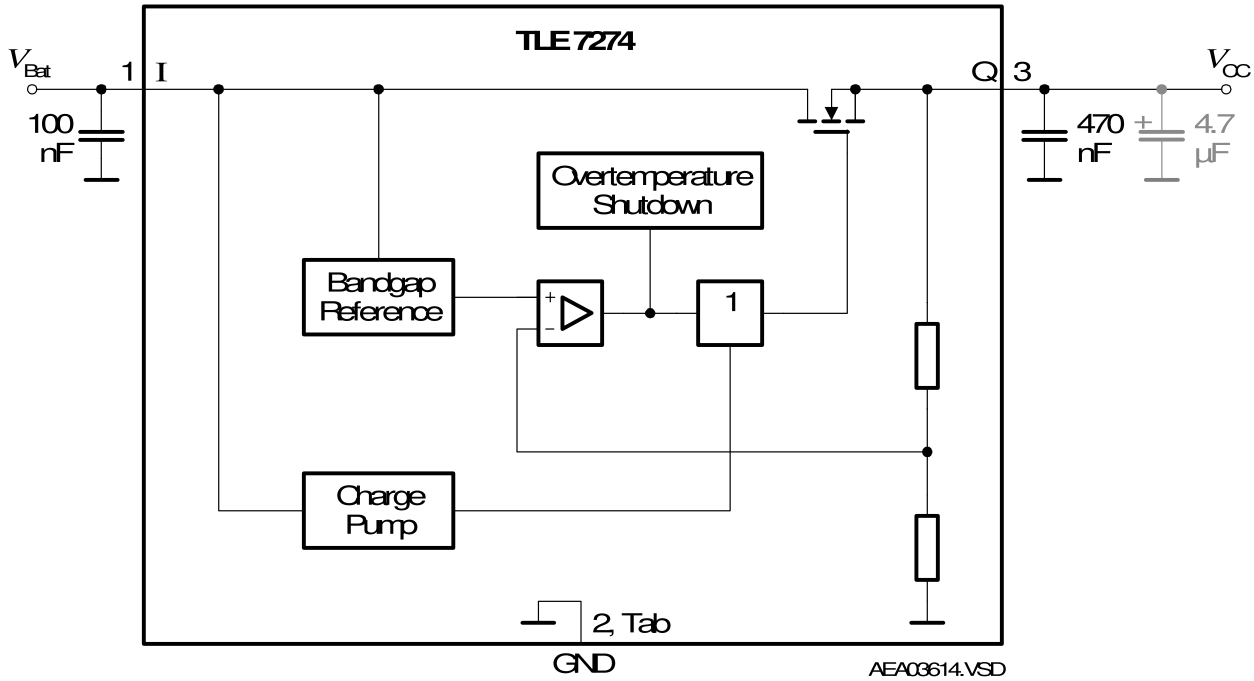


Figure 3 Application Diagram

Input, Output

An input capacitor is necessary for damping line influences. A resistor of approx. 1 Ω in series with C_I, can damp the LC of the input inductivity and the input capacitor.

In contrast to most low drop voltage regulators the TLE 7274 only needs moderate capacitance at the output to assure stability of the regulation loop. This offers more design flexibility to the circuit designer providing for cost efficient solutions.

The TLE 7274 requires a ceramic output capacitor of at least 470 nF. In order to damp influences resulting from load current surges it is recommended to add an additional electrolytic capacitor of 4.7 µF to 47 µF at the output as shown in **Figure 3**.

Additionally a buffer capacitor C_B of > 10µF should be used for the output to suppress influences from load surges to the voltage levels. This one can either be an aluminum electrolytic capacitor or a tantalum capacitor following the application requirements.

A general recommendation is to keep the drop over the equivalent serial resistor (ESR) together with the discharge of the blocking capacitor below the allowed Headroom of the Application to be supplied (e.g. typ. dV_Q = 350mV).

Since the regulator output current roughly rises linearly with time the discharge of the capacitor can be calculated as follows:

$$dVC_B = dI_Q*dt/C_B$$

The drop across the ESR calculates as:

$$dV_{ESR} = dI*ESR$$

To prevent a reset the following relationship must be fullfilled:

$$dV_C + dV_{ESR} < V_{RH} = 350mV$$

Example: Assuming a load current change of C_B = 100mA, a blocking capacitor of dI_Q = 22µF and a typical regulator reaction time under normal operating conditions of dt ~ 25µs and for special dynamic load conditions, such as load step from very low base load, a reaction time of dt ~ 75µs..

$$dV_C = dI_Q*dt/C_B = 100mA * 25µs/22µF = 113mV$$

So for the ESR we can allow

$$dV_{ESR} = V_{RH2} - dV_C = 350mV - 113mV = 236mV$$

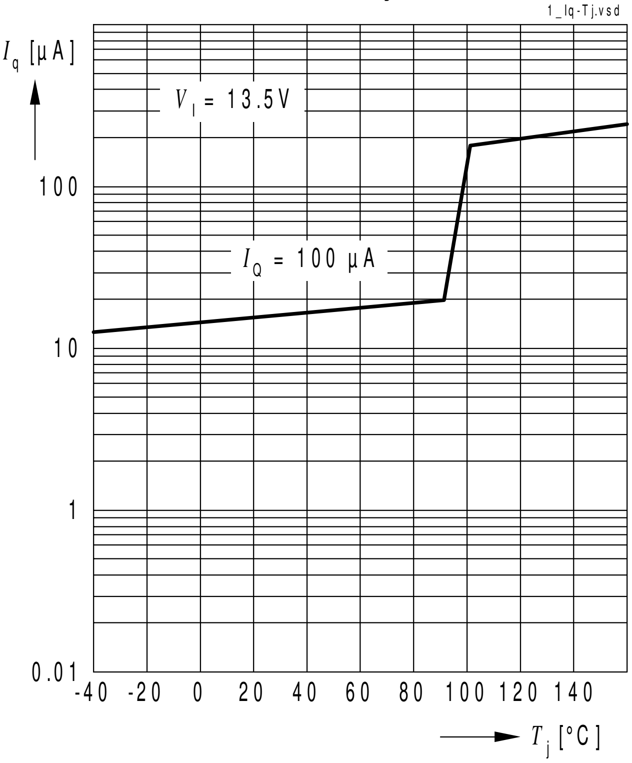
The permissible ESR becomes:

$$ESR = dV_{ESR} / dI_Q = 236mV/100mA = 2.36Ohm$$

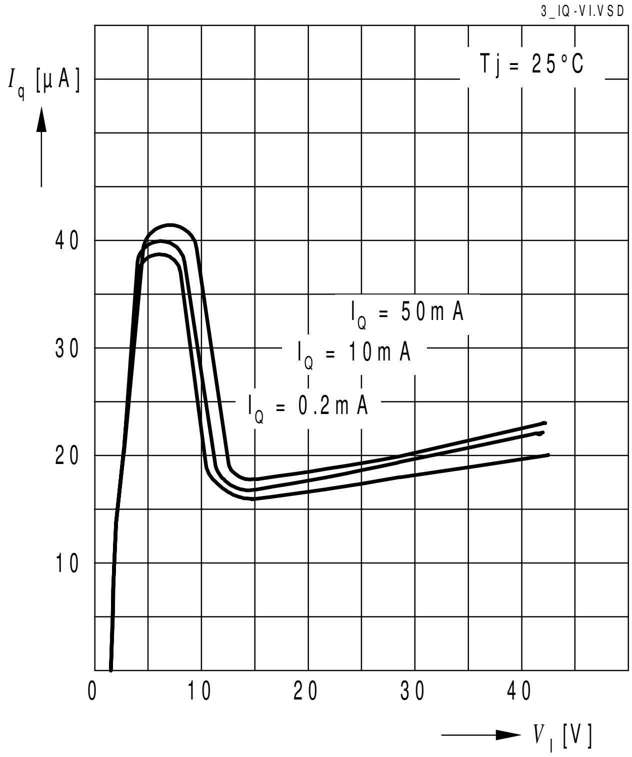
During design-in of the TLE7469 product family, special care needs to be taken with regards to the regulators reaction time to sudden load current changes starting from very low pre-load as well as cyclic load changes. The application note “*TLE7x Voltage Regulators - Application Note about Transient Response at ultra low quiescent current Voltage Regulators*” (see 3_cip05405.pdf) gives important hints for successful design-in of the Voltage Regulators of the TLE7x family.

Typical Performance Characteristics

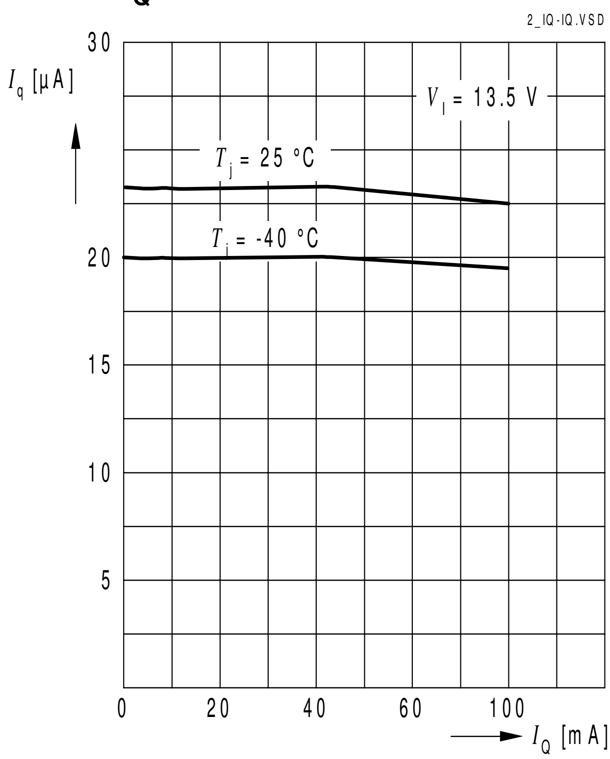
Current Consumption I_q versus Junction Temperature T_j



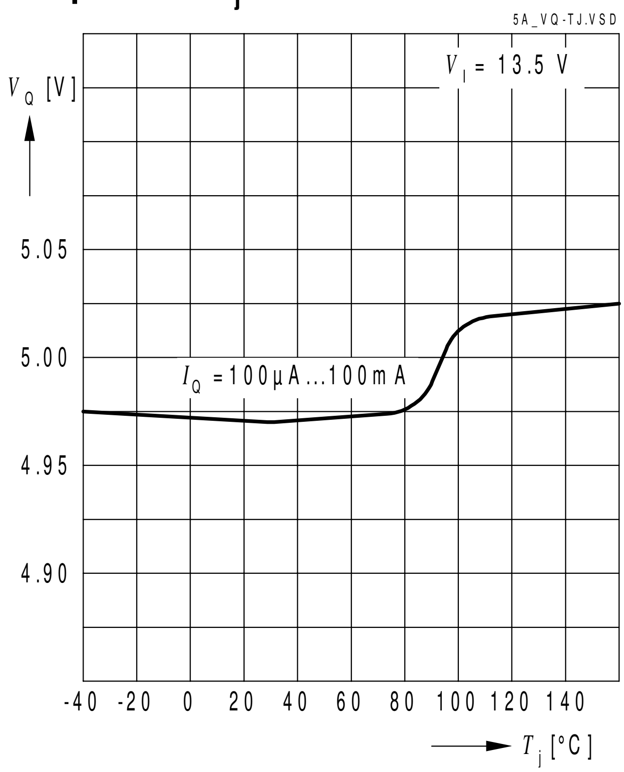
Current Consumption I_q versus Input Voltage V_I



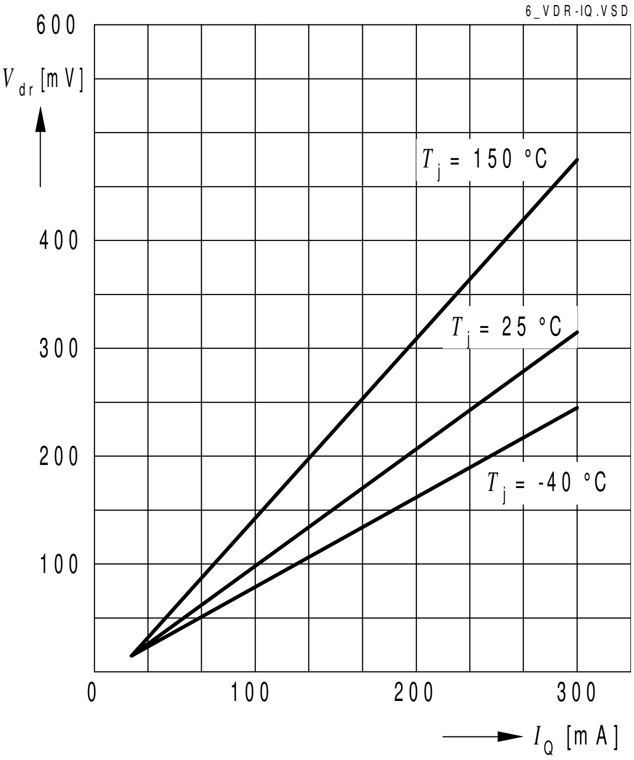
Current Consumption I_q versus Output Current I_Q



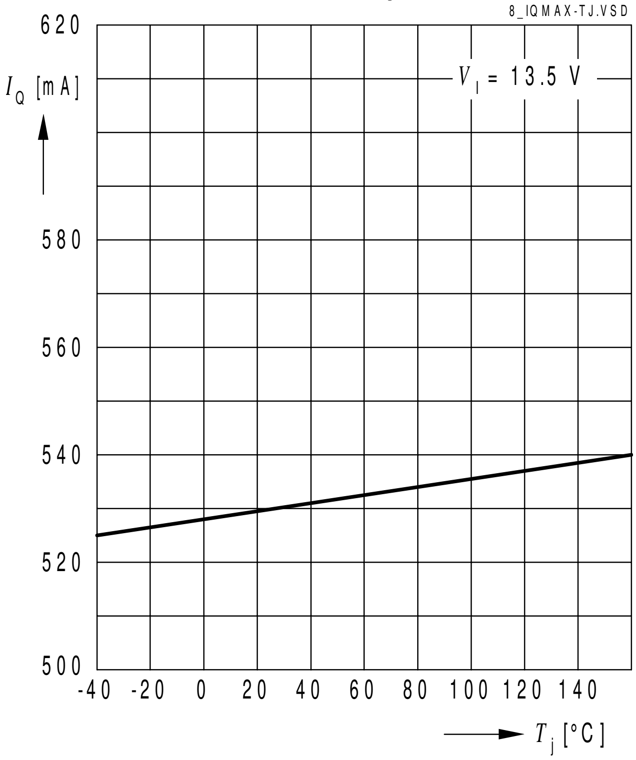
Output Voltage V_Q versus Junction Temperature T_j



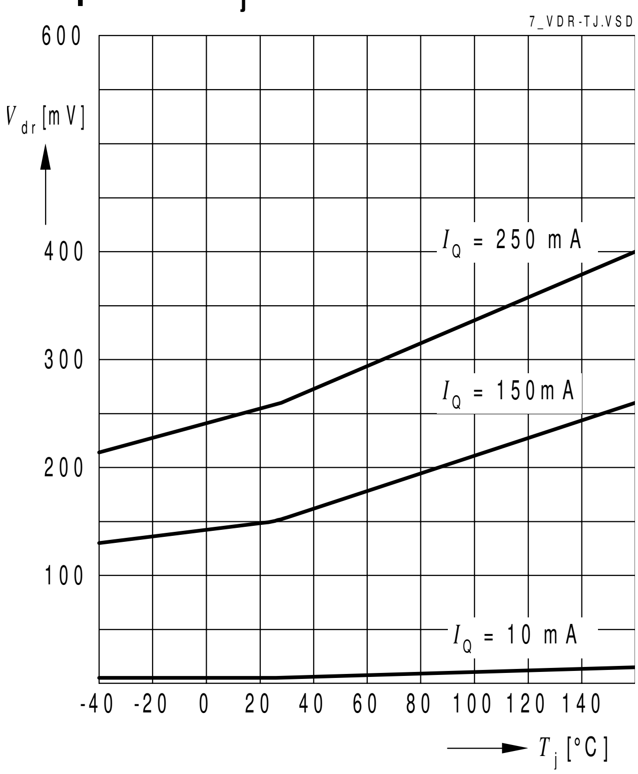
Dropout Voltage V_{dr} versus Output Current I_Q



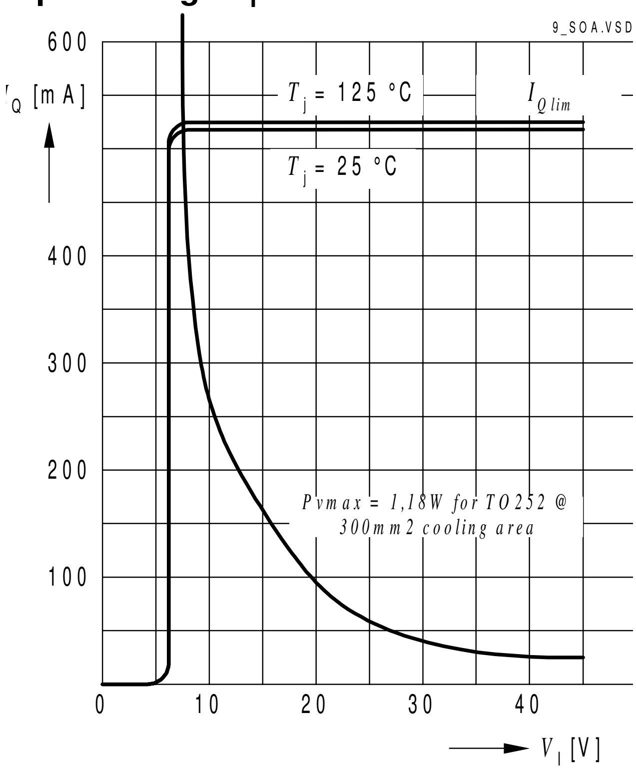
Maximum Output Current I_Q versus Junction Temperature T_j



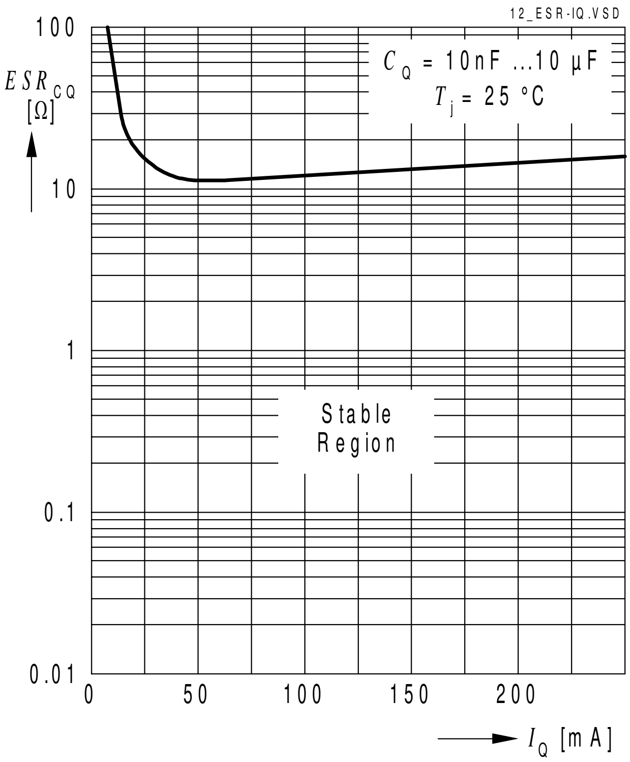
Dropout Voltage V_{dr} versus Junction Temperature T_j



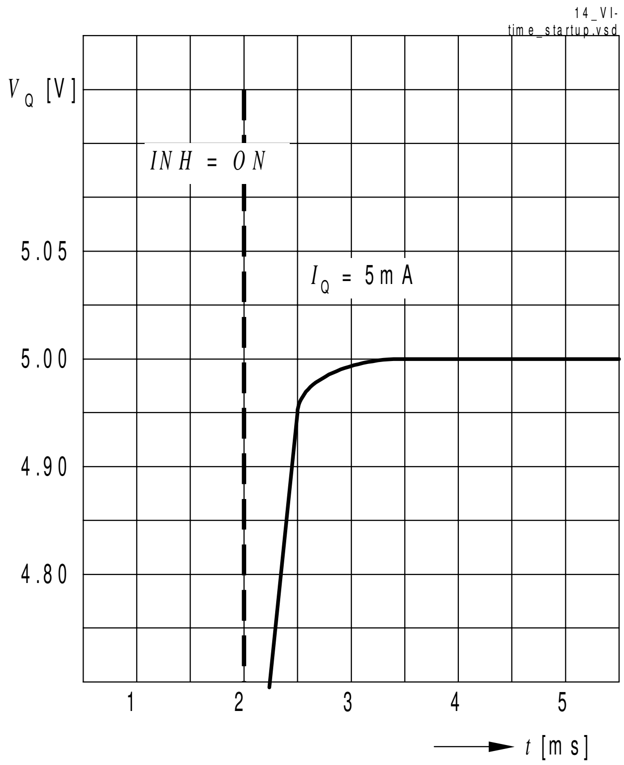
Maximum Output Current I_Q versus Input Voltage V_I



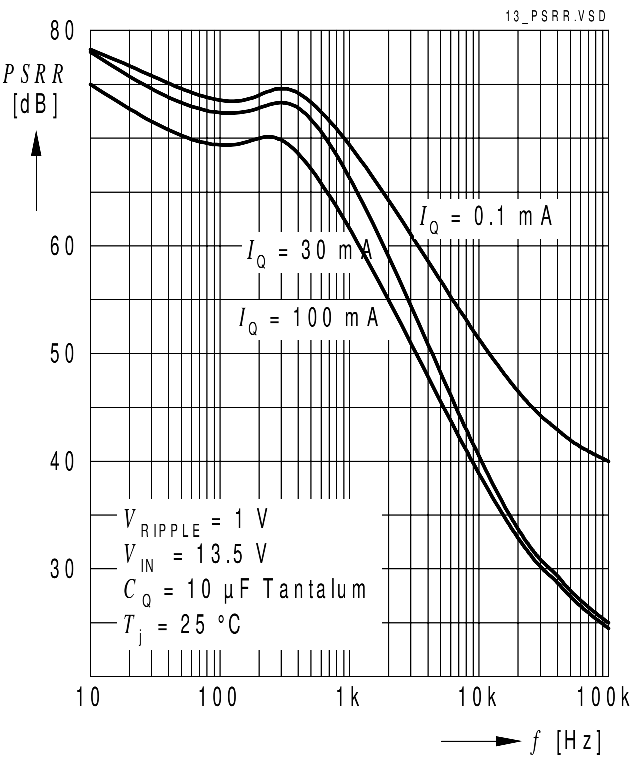
Region of Stability



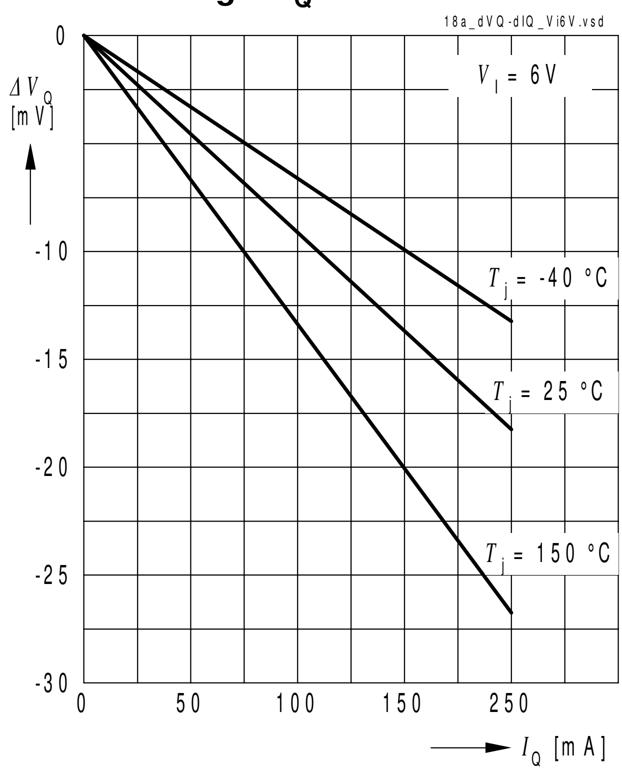
Output Voltage V_Q Start-up behaviour



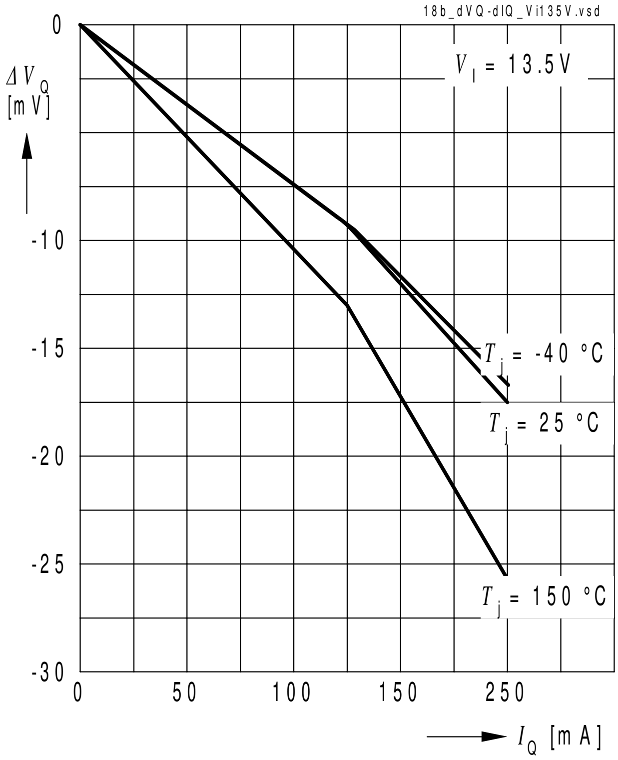
Power Supply Ripple Rejection PSRR versus Frequency f



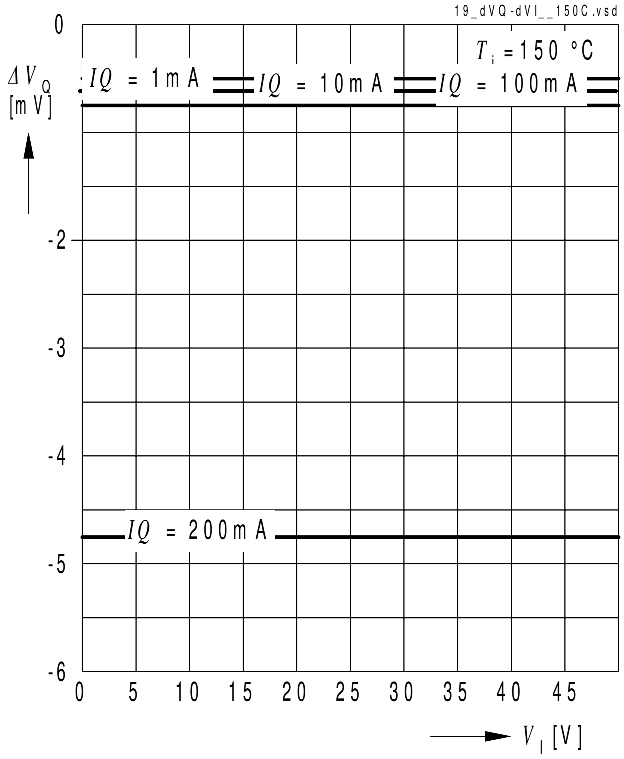
Load Regulation dV_Q versus Output Current Change dI_Q



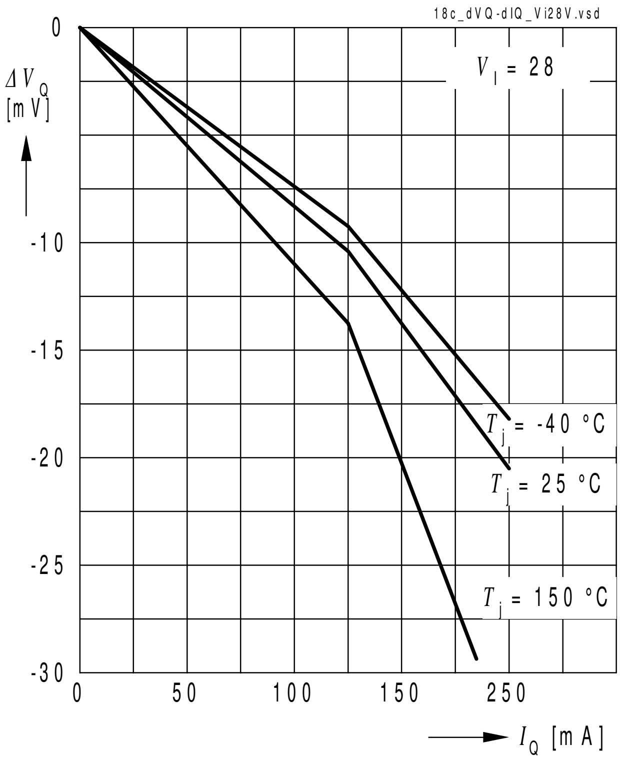
Load Regulation dV_Q versus Output Current Change dI_Q



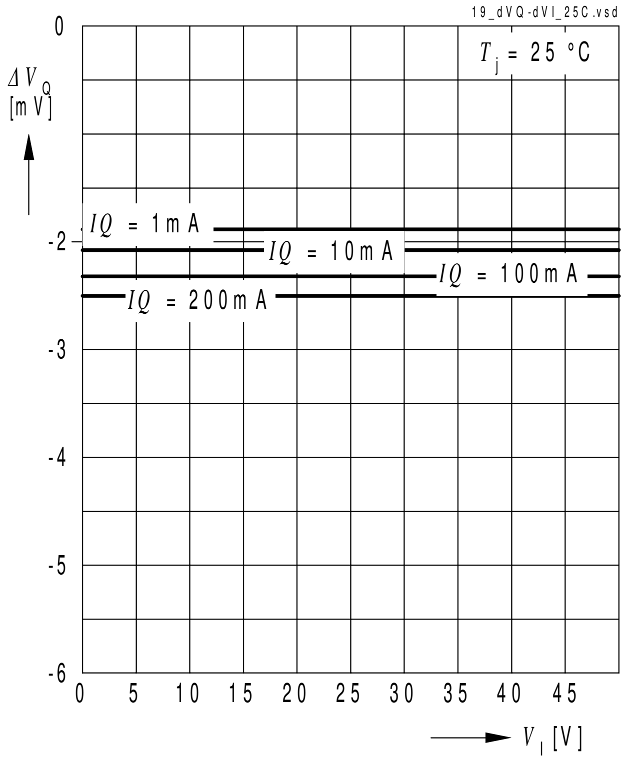
Line Regulation dV_Q versus Input Voltage ChangedV_I



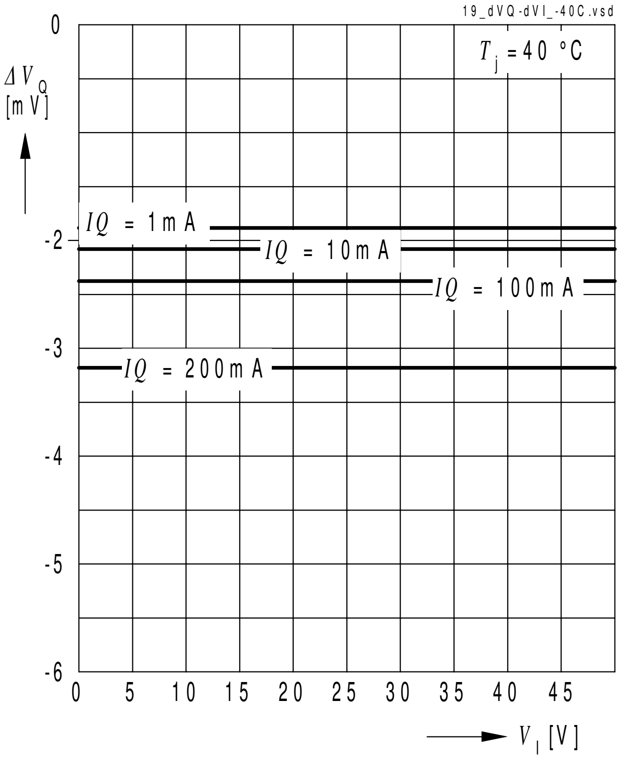
Load Regulation dV_Q versus Output Current Change dI_Q



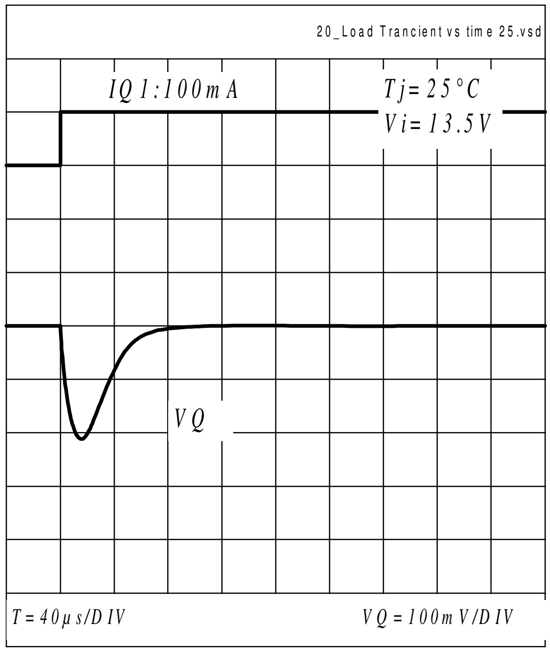
Line Regulation dV_Q versus Input Voltage ChangedV_I



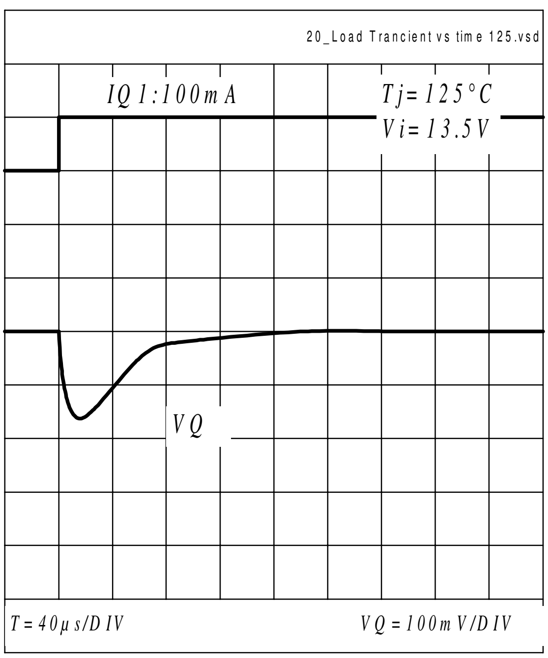
Line Regulation dV_Q versus Input Voltage Change dV_I



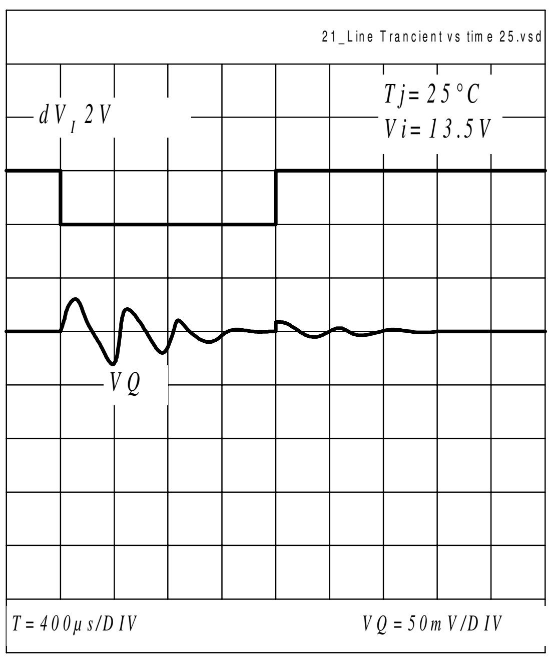
Load Transient Response Peak Voltage dV_Q



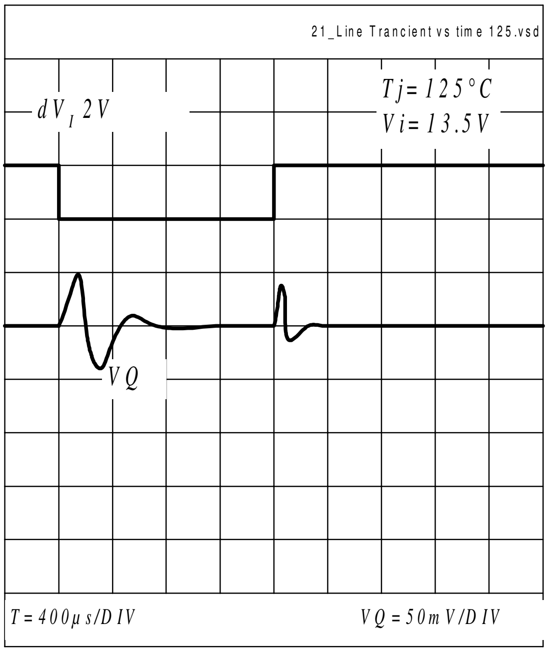
Load Transient Response Peak Voltage dV_Q



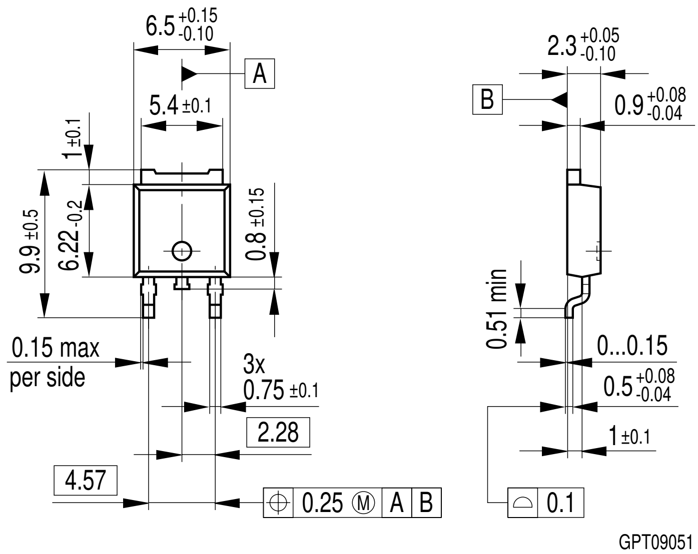
Line Transient Response Peak Voltage dV_Q



Line Transient Response Peak Voltage
dV_Q



Package Outlines



All metal surfaces tin plated, except area of cut.

Figure 4 **P-TO252-3-1** (Plastic Transistor Single Outline)

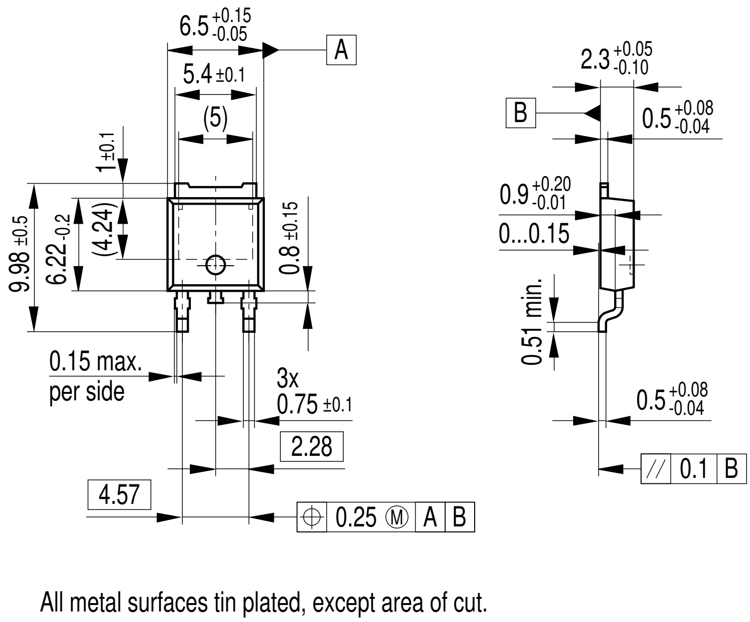


Figure 5 **P-TO252-3-11** (Plastic Transistor Single Outline)

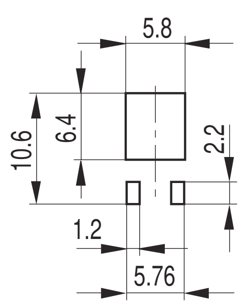


Figure 6 **Foot Print for P-TO-252-3-1 and P-TO-252-3-11** (Plastic Transistor Single Outline)

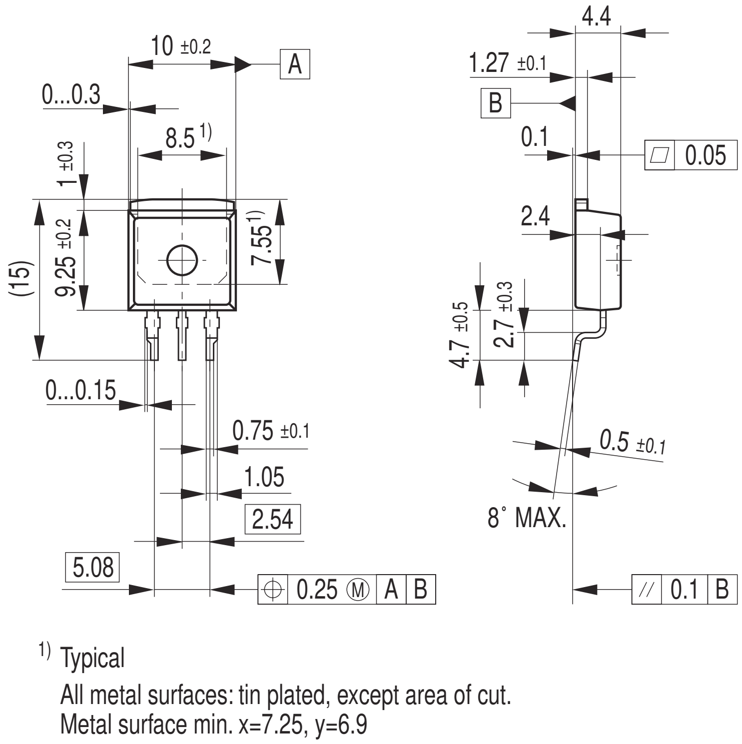


Figure 7 **P-TO263-3-1** (Plastic Transistor Single Outline)

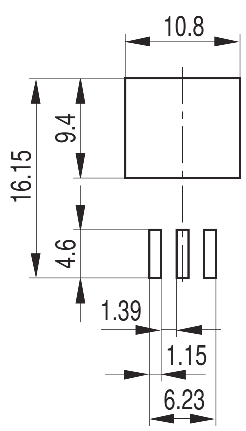


Figure 8 **Foot Print for P-TO263-3-1** (Plastic Transistor Single Outline)

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Dimensions in mm

Remarks

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