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TLE7368

Next Generation Micro Controller Supply

TLE7368G
TLE7368E
TLE7368-2E
TLE7368-3E

Data Sheet

Rev. 2.1, 2010-11-22

Automotive Power

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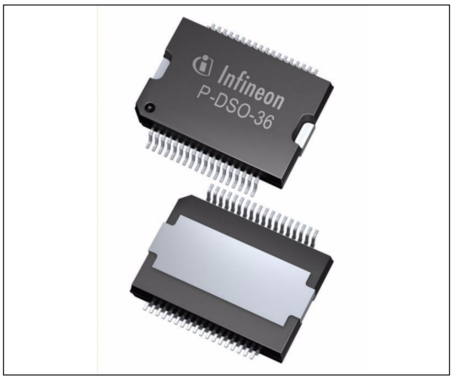
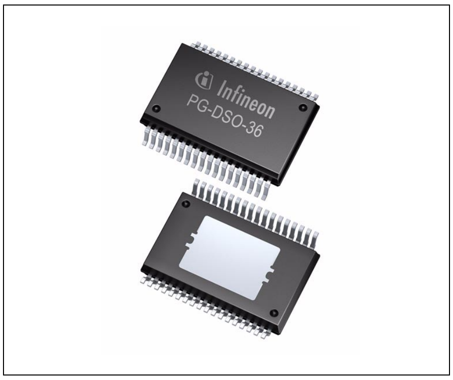
Next Generation Micro Controller Supply **TLE7368**

1 Overview



Power-P-DSO-36



PG-DSO-36

Features

- High efficient next generation microcontroller power supply system
- Wide battery input voltage range < 4.5 V up to 45 V
- Operating temperature range T_j = -40 °C to +150 °C
- Pre-regulator for low all over power loss:
  Integrated current mode Buck converter 5.5 V/2.5 A
- Post-regulators, e.g. for system and controller I/O supply:
  - LDO1: 5 V ±2%, 800 mA current limit
  - LDO2: 3.3 V ±2% or 2.6V ±2% (selectable output), 700 mA current limit
- Integrated linear regulator control circuit to supply controller cores:
  - LDO3 control for an external NPN power stage:
  - 1.5 V ±2% at TLE7368G and TLE7368E
  - 1.2 V ±2% at TLE7368-2E
  - 1.3 V ±2% at TLE7368-3E
- Post-regulators for off board supply:
  - 2 Tracking regulators following the main 5 V, 105 mA and 50 mA
- Stand-by regulator with lowest current consumption:
  - Linear voltage regulator as stand-by supply for e.g. memory circuits
  - Hardware selectable output voltages as 1.0 V or 2.6 V, 30 mA
  - Independent battery input, separated from Buck regulator input
- Hardware controlled on/off logic
- Undervoltage detection:
  - Undervoltage reset circuits with adjustable reset delay time at power up
  - Undervoltage monitoring circuit on stand-by supply
- Window watchdog circuit
- Overcurrent protection on all regulators
- Power sequencing on controller supplies
- Overtemperature shutdown
- Packages: Low R_{thja} Power-P-DSO-36; small exposed pad PG-DSO-36
- PG-DSO-36 only: Green Product (RoHS compliant)
- AEC Qualified

Type	Package	Marking	Remark
TLE7368G	Power-P-DSO-36	TLE7368 G	–
TLE7368E	PG-DSO-36	TLE7368 E	RoHS compliant
TLE7368-2E	PG-DSO-36	TLE7368-2 E	RoHS compliant
TLE7368-3E	PG-DSO-36	TLE7368-3 E	RoHS compliant

Description

The **TLE7368** device is a multifunctional power supply circuit especially designed for Automotive powertrain systems using a standard 12 V battery. The device is intended to supply and monitor next generation 32-bit microcontroller families (13 µm lithography) where voltage levels such as 5 V, 3.3 V or 1.5/1.2/1.3 V are required.

The regulator follows the concept of its predecessor TLE6368/SONIC, where the output of a pre-regulator feeds the inputs of the micro's linear supplies. In detail, the **TLE7368** cascades a Buck converter with linear regulators and voltage followers to achieve lowest power dissipation. This configuration allows to power the application even at high ambient temperatures.

The step-down converter delivers a pre-regulated voltage of 5.5 V with a minimum peak current capability of 2.5 A.

Supplied by this step down converter two low drop linear post-regulators offer 5 V and 3.3 V (2.6 V) with high accuracy. The current capability of the regulators is 800 mA and 700 mA. The 3.3 V (2.6 V) linear regulator does have its own input allowing to insert a dropper from the Buck output to reduce the on chip power dissipation if necessary. For the same reason, reduction of on chip power dissipation, the core supply (1.5 V, 1.2 V or 1.3 V) follows the concept of integrated control circuit with external power stage.

Implementing the on board and microcontroller supplies in this way described, allows operation even at high ambient temperatures.

The regulator system contains the so called power sequencing function which provides a controlled power up sequence of the three output voltages.

In addition to the main regulators the inputs of two voltage trackers are connected to the 5.5 V Buck converter output voltage. Their protected outputs follow the main 5 V linear regulator with high accuracy and are able to drive loads of 50 mA and 105 mA.

To monitor the output voltage levels of each of the linear regulators two independent undervoltage detection circuits are available. They can be used to implement the reset or an interrupt function.

For energy saving reasons, e.g. while the motor is turned off, the **TLE7368** offers a stand-by mode. The standby mode can be enabled and disabled either by battery or the microcontroller. In this stand-by mode just the stand-by regulator remains active and the current drawn from battery is reduced to a minimum for extended battery lifetime. A selection pin allows to configure the output voltages of the stand-by regulator to the application's needs. The input of the stand-by regulator is separated from the high power input of the pre-/post-regulator system.

The **TLE7368** is based on Infineon's Power technology SPT™ which allows bipolar, CMOS and power DMOS circuitry to be integrated on the same monolithic chip/circuitry.

2 Block Diagram

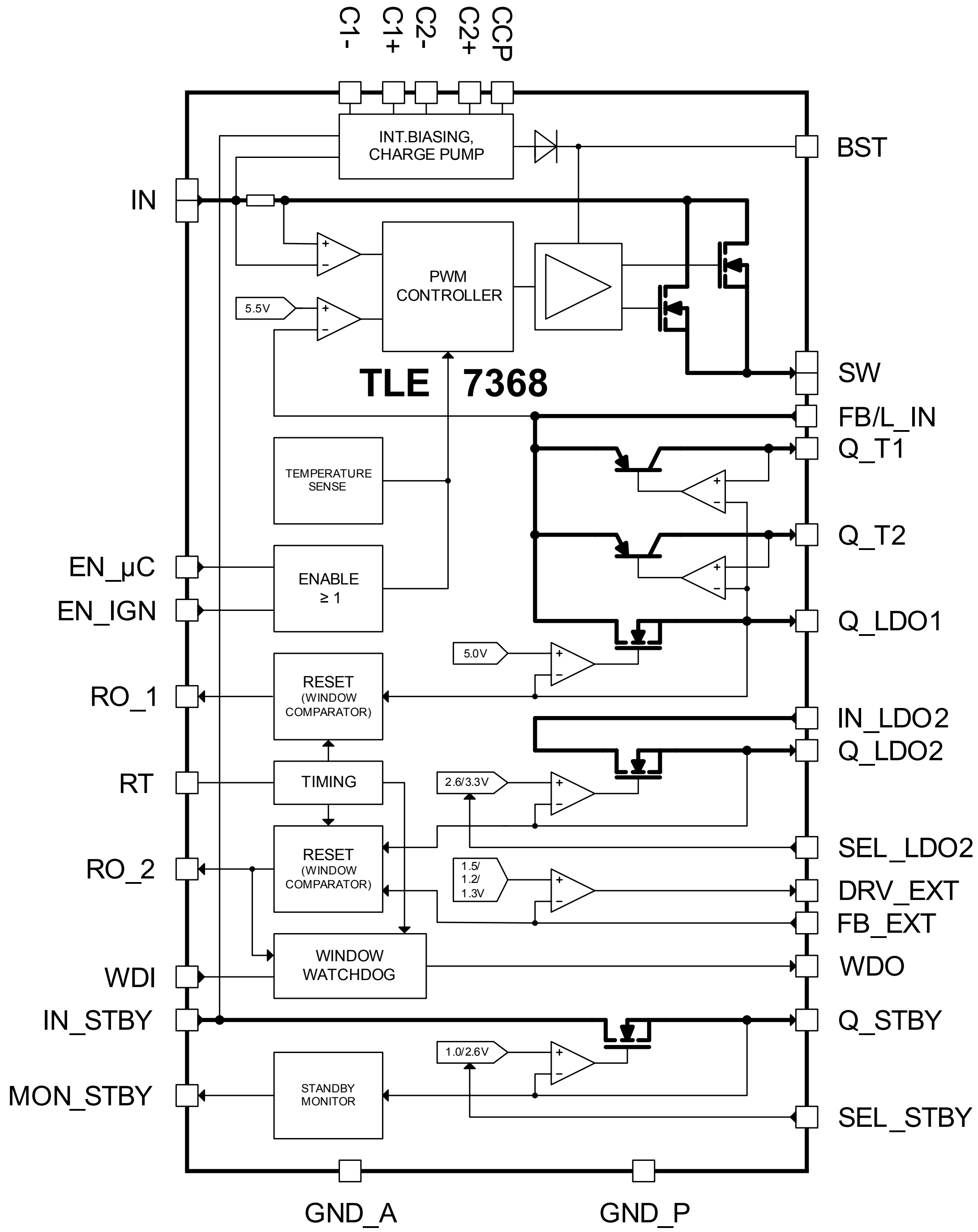


Figure 1 Block Diagram

3 Pin Configuration

3.1 Pin Assignment

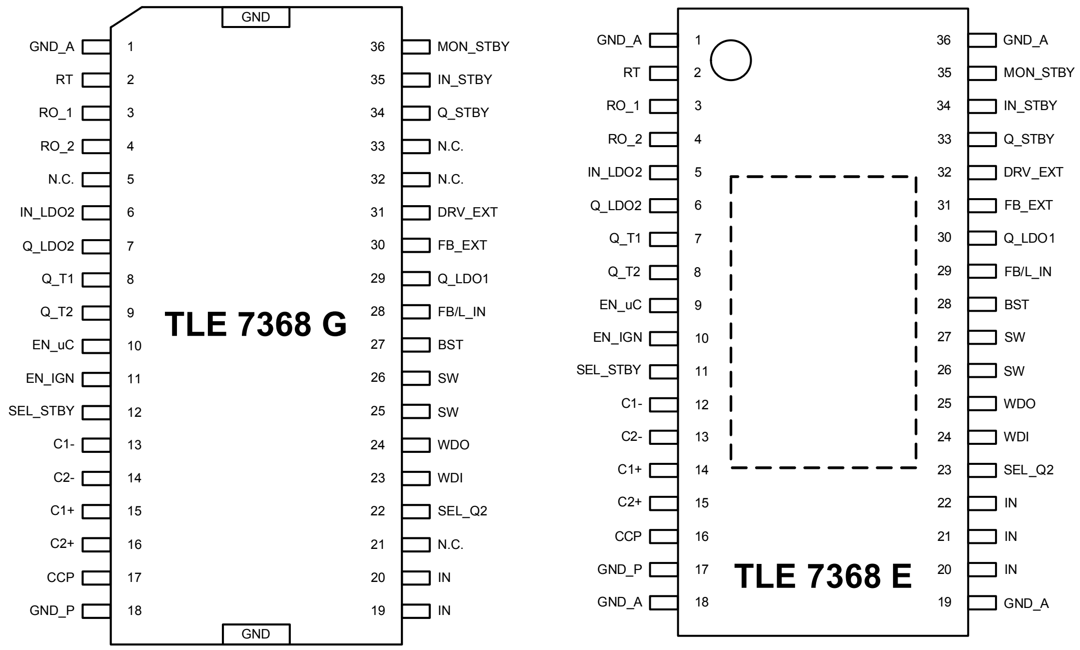


Figure 2 Pin Configuration

3.2 Pin Definitions and Functions TLE7368G

Pin (TLE7368G)	Pin (TLE7368E)	Symbol	Function
1	1	GND_A	**Analog ground connection;** Connect to heatslug resp. exposed pad.
2	2	RT	**Reset and watchdog timing pin;** Connect a ceramic capacitor to GND to determine the time base for the reset delay circuits and the watchdog cycle time
3	3	RO_1	**Reset output Q_LDO1;** Open drain output, active low. Connect an external 10 kΩ pull-up resistor to microcontroller I/O voltage.
4	4	RO_2	**Reset output Q_LDO2 and FB_EXT;** Open drain output, active low. Connect an external 10 kΩ pull-up resistor to microcontroller I/O voltage
5	–	N.C.	**Internally not connected;** Connect to GND_A

Pin (TLE7368G)	Pin (TLE7368E)	Symbol	Function
6	5	IN_LDO2	**LDO2 input;** Connect this pin straight to the Buck converter output or add a dropper in between to reduce power dissipation on the chip.
7	6	Q_LDO2	**Voltage regulator 2 output;** 3.3 V or 2.6 V, depending on the state of SEL_LDO2. Block to GND with capacitor for stable regulator operation; selection of capacitor C_{Q_LDO2} according to **Chapter 4.4** and **Chapter 6**.
8	7	Q_T1	**Tracking regulator 1 output;** Block to GND with capacitor for stable regulator operation; selection of capacitor C_{Q_T1} according to **Chapter 4.4** and **Chapter 6**.
9	8	Q_T2	**Tracking regulator 2 output;** Block to GND with capacitor for stable regulator operation; selection of capacitor C_{Q_T2} according to **Chapter 4.4** and **Chapter 6**.
10	9	EN_uC	**Enable input microcontroller;** High level enables / low level disables the IC except the stand-by regulators; Integrated pull-down resistor
11	10	EN_IGN	**Enable input ignition line;** High level enables / low level disables the IC except the stand-by regulators; Integrated pull-down resistor
12	11	SEL_STBY	**Selection input for stand-by regulator;** Connect to GND to select 2.6 V output voltage for Q_STBY; Connect straight to Q_STBY to select 1.0 V output voltage for Q_STBY
13	12	C1-	**Charge pump negative #1;** Connect a ceramic capacitor 100 nF, to C1+
14	13	C2-	**Charge pump negative #2;** Connect a ceramic capacitor 100 nF, toC2+
15	14	C1+	**Charge pump positive #1;** Connect a ceramic capacitor 100 nF, to C1-
16	15	C2+	**Charge pump positive #2;** Connect a ceramic capacitor 100 nF, to C2-
17	16	CCP	**Charge pump output;** Connect a ceramic capacitor, 220 nF, to GND; Used for internal IC supply, do not use for other circuitry.
18	17	GND_P	**Power ground;** Exclusive GND connection of charge pump; Connect this pin to the power ground star point on the PCB.
–	18, 19	GND_A	**Analog ground connection;** Connect to exposed pad.
19, 20	20, 21, 22	IN	**Buck regulator input;** Connect to a pi-filter (or if not used to battery) with short lines; connect filter capacitors in any case with short lines; connect a small ceramic directly at the pin; For details refer to **Chapter 6**. Interconnect the pins.
21	–	N.C.	**Internally not connected;** Connect to GND_A.

Pin (TLE7368G)	Pin (TLE7368E)	Symbol	Function
22	23	SEL_LDO2	**Selection input LDO2;** Connect to GND to select 2.6 V output voltage for LDO2; Connect straight to Q_LDO2 to select 3.3 V output voltage for LDO2.
23	24	WDI	**Window Watchdog input;** Apply a watchdog trigger signal to this pin
24	25	WDO	**Window Watchdog output;** Open drain output, active low, connect external 10 kΩ pull-up resistor to microcontroller I/O voltage
25, 26	26, 27	SW	**Buck power stage's output;** Connect both pins directly, on short lines, to the Buck converter circuit, i.e. the catch diode and the Buck inductance
27	28	BST	**Bootstrap driver supply input;** Connect the buck power stage's driver supply capacitor to the SW pins; For capacitor selection please refer to **Chapter 6**.
28	29	FB/L_IN	**Buck converter feedback input plus input for LDO1 and trackers;** Connect the output of the buck converter circuit with short lines to these pins; For Buck output capacitor selection please refer to **Chapter 6**.
29	30	Q_LDO1	**Voltage regulator 1 output;** 5 V output; Block to GND with capacitor for stable regulator operation; Selection of capacitor C_{Q_LDO1} according to **Chapter 4.4** and **Chapter 6**.
30	31	FB_EXT	**External regulator feedback input;** Feedback input of control loop for the external power stage regulator. Connect to the emitter of the regulating transistor; Block to GND with capacitor for stable regulator operation; Selection of capacitor $C_{Q\_FB\_EXT}$ according to **Chapter 4.4** and **Chapter 6**.
31	32	DRV_EXT	**Bipolar power stage driver output;** Connect the base of an external NPN transistor directly to this pin; Regarding choice of the external power stage refer to **Chapter 6**.
32, 33	–	N.C.	**Internally not connected;** Connect to GND_A.
34	33	Q_STBY	**Stand-by regulator output;** Output voltage depending on the state of SEL_STBY; Block to GND with capacitor for stable regulator operation; Selection of capacitor C_{Q_STBY} according to **Chapter 4.4** and **Chapter 6**.
35	34	IN_STBY	**Input to stand-by regulator;** Always connect the reverse polarity protected battery line to this pin; Input to all IC internal biasing circuits; Block to GND directly at the IC with ceramic capacitor; For proper choice of input capacitors please refer to **Chapter 6**.
36	35	MON_STBY	**Monitoring output for stand-by regulator;** power fail active low output with special timing, open drain, connect external pull-up resistor.
–	36	GND_A	**Analog ground connection;** Connect to exposed pad.

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Absolute Maximum Ratings [1)]

T_j = -40 °C to +150 °C; all voltages with respect to ground.

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
Stand-by Regulator Input IN_STBY						
4.1.1	Voltage	V_{IN_STBY}	-0.3	45	V	–
4.1.2	Current	I_{IN_STBY}	–	–	A	Limited internally
Selection Input SEL_STBY						
4.1.3	Voltage	V_{SEL_STBY}	-0.3	5.5	V	–
4.1.4	Voltage	V_{SEL_STBY}	-0.3	6.2	V	t < 10 s[2)]
4.1.5	Current	I_{SEL_STBY}	–	–	A	Limited internally
Buck Regulator Inputs IN						
4.1.6	Voltage	V_{IN}	V_{SW} - 0.3	45	V	–
4.1.7	Voltage	V_{IN}	-0.3	45	V	–
4.1.8	Current	I_{IN}	–	–	A	Limited internally
Watchdog Input WDI						
4.1.9	Voltage	V_{WDI}	-0.3	5.5	V	–
4.1.10	Voltage	V_{WDI}	-0.3	6.2	V	t < 10 s[2)]
4.1.11	Current	I_{WDI}	–	–	A	Limited internally
Watchdog Output WDO						
4.1.12	Voltage	V_{WDO}	-0.3	5.5	V	–
4.1.13	Voltage	V_{WDO}	-0.3	6.2	V	t < 10 s[2)]
4.1.14	Current	I_{WDO}	–	–	A	Limited internally
Charge Pump Positive C<1+, 2+>						
4.1.15	Voltage	$V_{C<1+, 2+>}$	-0.3	18	V	–
4.1.16	Current	$I_{C<1+, 2+>}$	–	–	mA	–
Charge Pump Negative C<1-, 2->						
4.1.17	Voltage	$V_{C<1-, 2->}$	-0.3	5.5	V	–
4.1.18	Current	$I_{C<1-, 2->}$	–	–	mA	–
Charge Pump Output CCP						
4.1.19	Voltage	V_{CCP}	-0.3	18	V	–
4.1.20	Current	I_{CCP}	–	–	mA	–
Reset Output RO_1						
4.1.21	Voltage	V_{RO_1}	-0.3	5.5	V	–
4.1.22	Voltage	V_{RO_1}	-0.3	6.2	V	t < 10 s[2)]
4.1.23	Current	I_{RO_1}	–	–	A	Limited internally

Absolute Maximum Ratings (cont'd)[1]

T_j = -40 °C to +150 °C; all voltages with respect to ground.

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
Reset Output RO_2						
4.1.24	Voltage	V_{RO_2}	-0.3	5.5	V	–
4.1.25	Voltage	V_{RO_2}	-0.3	6.2	V	t < 10 s[2]
4.1.26	Current	I_{RO_2}	–	–	A	Limited internally
Reset Timing RT						
4.1.27	Voltage	V_{RT}	-0.3	5.5	V	–
4.1.28	Voltage	V_{RT}	-0.3	6.2	V	t < 10 s[2]
4.1.29	Current	I_{RT}	–	–	A	Limited internally
Tracking Regulator Outputs Q_T<1..2>						
4.1.30	Voltage	$V_{Q\_T<1..2>}$	-5	40	V	V_{FB/L_IN} = 5.5V
4.1.31	Voltage	$V_{Q\_T<1..2>}$	-5	35	V	off mode; V_{FB/L_IN} = 0V
4.1.32	Current	$I_{Q\_T<1..2>}$	–	–	A	Limited internally
Enable Ignition EN_IGN						
4.1.33	Voltage	V_{EN_IGN}	-0.3	45	V	–
4.1.34	Current	I_{EN_IGN}	–	–	mA	–
Enable Micro EN_uC						
4.1.35	Voltage	V_{EN_uC}	-0.3	5.5	V	–
4.1.36	Voltage	V_{EN_uC}	-0.3	6.2	V	t < 10 s[2]
4.1.37	Current	I_{EN_uC}	-5	5	mA	–
Voltage Regulator Outputs Q_LDO<1..2>						
4.1.38	Voltage	V_{Q_LDO1}	-0.3	V_{FB/L_IN} + 0.3	V	–
4.1.39	Voltage	V_{Q_LDO2}	-0.3	V_{IN_LDO2} + 0.3	V	–
4.1.40	Voltage	$V_{Q\_LDO<1..2>}$	-0.3	5.5	V	–
4.1.41	Voltage	$V_{Q\_LDO<1..2>}$	-0.3	6.2	V	t < 10 s[2]
4.1.42	Current	$I_{Q\_LDO<1..2>}$	–	–	A	Limited internally
Selection Input SEL_LDO2						
4.1.43	Voltage	V_{SEL_LDO2}	-0.3	5.5	V	–
4.1.44	Voltage	V_{SEL_LDO2}	-0.3	6.2	V	t < 10 s[2]
4.1.45	Current	I_{SEL_LDO2}	–	–	A	Limited internally
External Driver Output DRV_EXT						
4.1.46	Voltage	V_{DRV_EXT}	-0.3	5.5	V	–
4.1.47	Voltage	V_{DRV_EXT}	-0.3	6.2	V	t < 10 s[2]
4.1.48	Current	I_{DRV_EXT}	–	–	A	Limited internally
External Regulator Feedback Input FB_EXT						
4.1.49	Voltage	V_{FB_EXT}	-0.3	5.5	V	–
4.1.50	Voltage	V_{FB_EXT}	-0.3	6.2	V	t < 10 s[2]
4.1.51	Current	I_{FB_EXT}	–	–	A	Limited internally

Absolute Maximum Ratings (cont'd)[1)]

T_j = -40 °C to +150 °C; all voltages with respect to ground.

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
Feedback and Post-Regulators Input FB/L_IN						
4.1.52	Voltage	V_{FB/L_IN}	V_{Q_LDO1} - 0.3	18	V	–
4.1.53	Voltage	V_{FB/L_IN}	-0.3	18	V	–
4.1.54	Current	I_{FB/L_IN}	–	–	A	Limited internally
Linear Regulator 2 Input IN_LDO2						
4.1.55	Voltage	V_{IN_LDO2}	V_{Q_LDO2} - 0.3	18	V	–
4.1.56	Voltage	V_{IN_LDO2}	-0.3	18	V	–
4.1.57	Current	I_{IN_LDO2}	–	–	A	Limited internally
Bootstrap Supply BST						
4.1.58	Voltage	V_{BST}	V_{SW} - 0.3	V_{SW} + 5.5	V	–
4.1.59	Voltage	V_{BST}	-0.3	51	V	–
4.1.60	Current	I_{BST}	–	–	A	Limited internally
Buck Power Stage SW						
4.1.61	Voltage	V_{SW}	-2	V_{IN} + 0.3	V	–
4.1.62	Voltage	V_{SW}	-2	45	V	–
4.1.63	Current	I_{SW}	–	–	A	Limited internally
Stand-by Regulator Output Q_STBY						
4.1.64	Voltage	V_{Q_STBY}	-0.3	5.5	V	–
4.1.65	Voltage	V_{Q_STBY}	-0.3	6.2	V	t < 10 s[2)]
4.1.66	Current	I_{Q_STBY}	–	–	A	Limited internally
Monitoring Output MON_STBY						
4.1.67	Voltage	V_{MON_STBY}	-0.3	5.5	V	–
4.1.68	Voltage	V_{MON_STBY}	-0.3	6.2	V	t < 10 s[2)]
4.1.69	Current	I_{MON_STBY}	–	–	A	Limited internally
Temperatures						
4.1.70	Junction Temperature	T_j	-40	150	°C	–
4.1.71	Storage Temperature	T_{stg}	-50	150	°C	–
ESD-Protection (Human Body Model)						
4.1.72	Electrostatic discharge voltage	V_{ESD}	-2	2	kV	Human Body Model (HBM)[3)]
ESD-Protection (Charged Device Model)						
4.1.73	Electrostatic discharge voltage to GND	V_{ESD}	-500	500	V	Charged Device Model (CDM)[4)]
4.1.74	Electrostatic discharge voltage, corner pins to GND	V_{ESD}	-750	750	V	Charged Device Model (CDM)[4)]

1) Not subject to production test, specified by design.
2) Exposure to those absolute maximum ratings for extended periods of time (t > 10 s) may affect device reliability.
3) According to JEDEC standard EIA/JESD22-A114-B (1.5 kΩ, 100 pF)
4) According to EIA/JESD22-C101 or ESDA STM5.3.1

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

4.2 Functional Range

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
4.2.1	Stand-by input voltage	V_{IN_STBY}	3.0	45	V	1)
4.2.2	Buck input voltage	V_{IN}	4.5	45	V	1)
4.2.3	Peak to peak ripple voltage at FB/L_IN	V_{FB/L_IN}	0	150	mVpp	–
4.2.4	Junction temperature	T_j	-40	150	°C	–

1) At minimum battery voltage regulators with higher nominal output voltage will not be able to provide the full output voltage. Their outputs follow the battery with certain drop.

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

4.3 Thermal Resistance

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Power-P-DSO-36							
4.3.1	Junction to ambient	R_{thJA}	–	49	–	K/W	Footprint only 1)
4.3.2	Junction to ambient	R_{thJA}	–	39	–	K/W	Heat sink area $300 mm^2$ 1)
4.3.3	Junction to ambient	R_{thJA}	–	32	–	K/W	Heat sink area $600 mm^2$ 1)
4.3.4	Junction to case	R_{thJC}	–	4.4	–	K/W	–
PG-DSO-36							
4.3.5	Junction to ambient	R_{thJA}	–	54	–	K/W	Footprint only 1)
4.3.6	Junction to ambient	R_{thJA}	–	42	–	K/W	Heat sink area $300 mm^2$ 1)
4.3.7	Junction to ambient	R_{thJA}	–	35	–	K/W	Heat sink area $600 mm^2$ 1)
4.3.8	Junction to case	R_{thJC}	–	5.6	–	K/W	–

1) Worst case regarding peak temperature; zero airflow; mounted on FR4; $80 \times 80 \times 1.5 mm^3$; 35µ Cu; 5µ Sn

4.4 Electrical Characteristics

Electrical Characteristics

V_{IN} = V_{IN_STBY} = 13.5 V, T_j = -40 °C to +150 °C,
V_{CCP} = 9.0 V; SEL_STBY = Q_STBY; all voltages with respect to ground.

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Buck Regulator							
4.4.1	Switching frequency	f	280	370	425	kHz	–
4.4.2	Current transition rise/fall time	$t_{r,I}$	–	50	–	ns	[1]; slope magnitude 1 A; fixed internally
4.4.3	Power stage on resistance	$R_{ON, Buck}$	–	–	280	mΩ	–
4.4.4	Power stage peak current limit	$I_{peak, SW}$	2.5	–	4.6	A	V_{IN} = 5.0 V; V_{SW} ramped down from 5.0 V to 3.7 V; V_{FB/L_IN} = 5.0 V
4.4.5	Buck converter output voltage	V_{FB/L_IN}	5.4	–	6.0	V	I_{Buck} = 2.0 A[2]
4.4.6	Buck converter output voltage	V_{FB/L_IN}	5.4	–	6.4	V	I_{Buck} = 100 mA[2]
4.4.7	Buck converter, turn on threshold	$V_{IN, on}$	–	–	4.5	V	V_{IN} increasing
4.4.8	Buck converter, turn off threshold	$V_{IN, off}$	3.5	–	–	V	V_{IN} decreasing
4.4.9	Buck converter On/off hysteresis	$V_{IN, hyst}$	450	500	550	mV	$V_{IN, hyst}$ = $V_{IN, on}$ - $V_{IN, off}$
4.4.10	Bootstrap undervoltage lockout, turn on threshold	$V_{BST\_UV, on}$	–	–	V_{SW} + 5.0	V	Bootstrap voltage increasing
4.4.11	Bootstrap undervoltage lockout, turn off threshold	$V_{BST\_UV, off}$	V_{SW} + 3.2	–	–	V	Bootstrap voltage decreasing
4.4.12	Bootstrap undervoltage lockout, hysteresis	$V_{BST\_UV, hyst}$	0.2	–	1	V	$V_{BST\_UV, hyst}$ = $V_{BST\_UV, on}$ - $V_{BST\_UV, off}$
Charge Pump							
4.4.13	Charge pump voltage	V_{CCP}	9	–	15	V	C_{C1} = 100 nF; C_{C2} = 100 nF; C_{CCP} = 220 nF
4.4.14	Charge pump voltage	V_{CCP}	9	–	13.5	V	V_{IN} = 4.5 V; C_{C1} = 100 nF; C_{C2} = 100 nF; C_{CCP} = 220 nF
4.4.15	Charge pump switching frequency	f_{CCP}	1.0	–	2.5	MHz	–

Electrical Characteristics (cont'd)

$V_{IN} = V_{IN\_STBY}$ = 13.5 V, T_j = -40 °C to +150 °C,
V_{CCP} = 9.0 V; SEL_STBY = Q_STBY; all voltages with respect to ground.

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Voltage Regulator Q_LDO1							
4.4.16	Output voltage	V_{Q_LDO1}	4.9	–	5.1	V	1 mA < I_{Q_LDO1} < 700 mA[3)]
4.4.17	Output current limitation	$I_{Q\_LDO1,\ lim}$	800	–	1600	mA	V_{Q_LDO1} = 4.0 V
4.4.18	Drop voltage	$V_{dr,\ Q\_LDO1}$	–	–	400	mV	I_{Q_LDO1} = 500 mA; V_{FB/L_IN} = 5.0 V;[3) 4)]
4.4.19			–	–	400	mV	I_{Q_LDO1} = 250 mA; V_{IN} = 4.5 V;[3) 4)]
4.4.20	Load regulation	ΔV_{Q_LDO1}	–	60	120	mV/A	–
4.4.21	Power supply ripple rejection	$PSRR_{Q\_LD\ O1}$	26	–	–	dB	V_{FB/L_IN} = 5.6 V; $V_{FB/L\_IN,\ ripple\ pp}$ = 150 mV; $f_{FB/L\_IN,\ ripple}$ = 370 kHz; I_{Q_LDO1} = 250 mA; C_{Q_LDO1} = 4.7 µF, X7R[1)]
4.4.22	Output capacitor	C_{Q_LDO1}	1	–	470	µF	[1) 5)]
4.4.23	Output capacitor	ESR C_{Q_LDO1}	0	–	2	Ω	at 10 kHz[1)]
Voltage Regulator Q_LDO2							
4.4.24	Output voltage	V_{Q_LDO2}	3.23	–	3.37	V	SEL_LDO2 = Q_LDO2; IN_LDO2 = FB/L_IN; 1 mA < I_{Q_LDO2} < 500 mA
4.4.25	Output current limitation	$I_{Q\_LDO2,\ lim}$	700	–	1400	mA	SEL_LDO2 = Q_LDO2; IN_LDO2 = FB/L_IN; V_{Q_LDO2} = 2.8 V
4.4.26	Drop voltage	$V_{dr,\ Q\_LDO2}$	–	–	400	mV	SEL_LDO2 = Q_LDO2; V_{CCP} = 9 V; I_{Q_LDO2} = 500 mA;[4) 6)]
4.4.27	Drop voltage	$V_{dr,\ Q\_LDO2}$	–	–	400	mV	SEL_LDO2 = Q_LDO2; V_{CCP} = 9 V; I_{Q_LDO2} = 250 mA; V_{IN} = 4.5 V;[4) 6)]
4.4.28	Load regulation	ΔV_{Q_LDO2}	–	–	80	mV/A	3.3 V mode 1 mA < I_{Q_LDO2} < 650 mA
4.4.29	Output voltage	V_{Q_LDO2}	2.56	–	2.67	V	SEL_LDO2 = GND; IN_LDO2 = FB/L_IN; 1 mA < I_{Q_LDO2} < 500 mA
4.4.30	Output current limitation	$I_{Q\_LDO2,\ lim}$	700	–	1400	mA	SEL_LDO2 = GND; IN_LDO2 = FB/L_IN; V_{Q_LDO2} = 2.0 V
4.4.31	Drop voltage	$V_{dr,\ Q\_LDO2}$	–	–	400	mV	SEL_LDO2 = GND; V_{CCP} = 9 V; I_{Q_LDO2} = 500 mA;[4)6)]

Electrical Characteristics (cont'd)

V_{IN} = V_{IN_STBY} = 13.5 V, T_j = -40 °C to +150 °C,
V_{CCP} = 9.0 V; SEL_STBY = Q_STBY; all voltages with respect to ground.

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
4.4.32	Drop voltage	V_{dr, Q_LDO2}	–	–	400	mV	SEL_LDO2 = GND; V_{CCP} = 9 V; I_{Q_LDO2} = 250 mA; V_{IN} = 4.5 V;[4)6)]
4.4.33	Load regulation	ΔV_{Q_LDO2}	–	–	65	mV/A	2.6 V mode 1 mA < I_{Q_LDO2} < 650 mA
4.4.34	Power supply ripple rejection	$PSRR_{Q\_LDO2}$	26	–	–	dB	V_{IN_LDO2} = 5.6 V; $V_{IN\_LDO2, ripple pp}$ = 150 mV; $f_{IN\_LDO2, ripple}$ = 370 kHz; I_{Q_LDO2} = 250mA; C_{Q_LDO2} = 4.7 µF ceramic X7R[1)]
4.4.35	Selector Pull-down resistor	R_{SEL_LDO2}	0.7	1.2	1.9	MΩ	–
4.4.36	Output capacitor	C_{Q_LDO2}	1	–	470	µF	[1)5)]
4.4.37	Output capacitor	ESR C_{Q_LDO2}	0	–	2	Ω	at 10 kHz;[1)]
External Voltage Regulator Control							
4.4.38	Driver current limit	$I_{DRV\_EXT, lim}$	75	–	150	mA	TLE7368G, TLE7368E V_{FB_EXT} = 1.2 V
4.4.39	Driver current limit	$I_{DRV\_EXT, lim}$	75	–	150	mA	TLE7368-2E V_{FB_EXT} = 0.9V
4.4.40	Driver current limit	$I_{DRV\_EXT, lim}$	75	–	150	mA	TLE7368-3E V_{FB_EXT} = 1.0V
4.4.41	Feedback voltage	V_{FB_EXT}	1.51	–	1.55	V	TLE7368G, TLE7368E
4.4.42	Feedback voltage	V_{FB_EXT}	1.19	–	1.23	V	TLE7368-2E
4.4.43	Feedback voltage	V_{FB_EXT}	1.30	–	1.34	V	TLE7368-3E
4.4.44	Feedback input current	I_{FB_EXT}	-250	–	–	µA	–
4.4.45	Load regulation	ΔV_{FB_EXT}	–	–	20	mV/A	V_{FB/L_IN} = 5.4 V; V_{CCP} = 9.0 V; I_{FB_EXT} = 100 µA to 1 A;[7)]
4.4.46	Output capacitor	C_{FB_EXT}	4.7	–	–	µF	[1)5)7)]
4.4.47	Output capacitor	ESR C_{FB_EXT}	0	–	0.1	Ω	at 10 kHz;[1)]
Voltage Tracker Q_T1							
4.4.48	Output voltage tracking accuracy to Q_LDO1	ΔV_{Q_T1}	-10	–	10	mV	0 mA < I_{Q_T1} < 105 mA
4.4.49	Output current limitation	I_{Q_T1}	120	–	240	mA	V_{Q_T1} = 4.0 V
4.4.50	Drop voltage	V_{dr, Q_T1}	–	–	400	mV	I_{Q_T1} = 105 mA; V_{FB/L_IN} = 5.3 V; V_{Q_LDO1} = 5.0 V[4)]

Electrical Characteristics (cont'd)

$V_{IN} = V_{IN\_STBY}$ = 13.5 V, T_j = -40 °C to +150 °C,
V_{CCP} = 9.0 V; SEL_STBY = Q_STBY; all voltages with respect to ground.

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
4.4.51	Power supply ripple rejection	$PSRR_{Q\_T1}$	26	–	–	dB	V_{FB/L_IN} = 5.6 V; $V_{FB/L\_IN,\ ripple\ pp}$ = 150 mV; $f_{FB/L\_IN,\ ripple}$ = 370 kHz; V_{Q_LDO1} = 5.0 V; I_{Q_T1} = 100 mA; C_{Q_T1} = 4.7µF ceramic X7R;[1]
4.4.52	Output capacitor	C_{Q_T1}	4.7	–	–	µF	[1)5)]
4.4.53	Output capacitor	ESR C_{Q_T1}	0	–	3	Ω	at 10 kHz;[1]
Voltage Tracker Q_T2							
4.4.54	Output voltage tracking accuracy to Q_LDO1	ΔV_{Q_T2}	-10	–	10	mV	0 mA < I_{Q_T2} < 50 mA;
4.4.55	Output current limitation	I_{Q_T2}	60	–	110	mA	V_{Q_T2} = 4.0 V
4.4.56	Drop voltage	$V_{dr,\ Q\_T2}$	–	–	400	mV	I_{Q_T2} = 50 mA; V_{FB/L_IN} = 5.3 V; V_{Q_LDO1} = 5.0 V[4]
4.4.57	Power supply ripple rejection	$PSRR_{Q\_T2}$	26	–	–	dB	V_{FB/L_IN} = 5.6 V; $V_{FB/L\_IN,\ ripple\ pp}$ = 150 mV; $f_{FB/L\_IN,\ ripple}$ = 370 kHz; V_{Q_LDO1} = 5.0 V; I_{Q_T2} = 40 mA; C_{Q_T2} = 4.7 µF ceramic X7R;[1]
4.4.58	Output capacitor	C_{Q_T2}	4.7	–	–	µF	[1)5)]
4.4.59	Output capacitor	ESR C_{Q_T2}	0	–	3	Ω	at 10 kHz;[1]
Stand-by Regulator							
4.4.60	Output voltage	V_{Q_STBY}	0.93	1.02	1.08	V	V_{IN_STBY} > 3 V; 100 µA < I_{Q_STBY} < 10 mA; SEL_STBY = Q_STBY
4.4.61	Output voltage	V_{Q_STBY}	0.93	1.02	1.08	V	V_{IN_STBY} > 4.5 V; I_{Q_STBY} = 30 mA; SEL_STBY = Q_STBY
4.4.62	Output voltage	V_{Q_STBY}	2.51	2.62	2.73	V	V_{IN_STBY} > 3.0 V; 100 µA < I_{Q_STBY} < 10 mA; SEL_STBY = GND
4.4.63	Selector pull-up current	I_{SEL_STBY}	-2	-5	-10	µA	SEL_STBY = GND
4.4.64	Output current limitation	$I_{Q\_STBY,\ lim}$	31	–	90	mA	V_{Q_STBY} = 0.5 V

Electrical Characteristics (cont'd)

V_{IN} = V_{IN_STBY} = 13.5 V, T_j = -40 °C to +150 °C,
V_{CCP} = 9.0 V; SEL_STBY = Q_STBY; all voltages with respect to ground.

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
4.4.65	Load regulation	ΔV_{Q_STBY}	–	–	5	V/A	I_{Q_STBY} = 100µA to 10 mA V_{IN_STBY} > 4.5 V; SEL_STBY = Q_STBY V_{Q_STBY} = 1.0V
			–	–	10	V/A	I_{Q_STBY} = 100µA to 10 mA V_{IN_STBY} > 4.5 V; SEL_STBY = GND V_{Q_STBY} = 2.6V
4.4.66	Line regulation	ΔV_{Q_STBY}	–	–	5	mV/V	–
4.4.67	Power supply ripple rejection	$PSRR_{Q\_STBY}$	60	–	–	dB	$V_{IN\_STBY, ripple\ pp}$ = 500 mV; $f_{IN\_STBY, ripple}$ = 100 Hz; I_{Q_STBY} = 5 mA; C_{Q_STBY} = 1 µF ceramic X7R;[1]
4.4.68	Output capacitor	C_{Q_STBY}	0.47	–	2	µF	[1) 5)]
4.4.69	Output capacitor	ESR C_{Q_STBY}	0	–	0.5	Ω	at 10 kHz;[1]
Device Enable Blocks and Quiescent Current							
4.4.70	Ignition turn on threshold	$V_{EN\_IGN, on}$	–	–	4.0	V	Device operating
4.4.71	Ignition turn off threshold	$V_{EN\_IGN, off}$	2.0	–	–	V	Only stand-by regulators are active if V_{EN_IGN} < $V_{EN\_IGN, off}$ and V_{EN_uC} < $V_{EN\_uC, off}$
4.4.72	Ignition pull-down resistor current	I_{EN_IGN}	-100	–	–	µA	V_{EN_IGN} = 13.5 V
4.4.73	Turn on threshold	$V_{EN\_uC, on}$	–	–	2.0	V	Device operating
4.4.74	Turn off threshold	$V_{EN\_uC, off}$	0.8	–	–	V	Only stand-by regulators are active if V_{EN_IGN} < $V_{EN\_IGN, off}$ and V_{EN_uC} < $V_{EN\_uC, off}$
4.4.75	Pull-down resistor current	I_{EN_uC}	-30	–	–	µA	V_{EN_uC} = 5 V
4.4.76	Quiescent current	$I_q = I_{IN\_STBY} - I_{Q\_STBY}$	-120	–	–	µA	V_{EN_uC} = V_{EN_IGN} = 0 V; SEL_STBY = Q_STBY; MON_STBY = H; I_{Q_STBY} = 100 µA; T_j < 125 °C
4.4.77	Quiescent current	$I_q = I_{IN\_STBY} - I_{Q\_STBY}$	-130	–	–	µA	V_{EN_uC} = V_{EN_IGN} = 0 V; SEL_STBY = GND; MON_STBY = H; I_{Q_STBY} = 100 µA; T_j < 125 °C
4.4.78	Quiescent current	$I_{q, IN}$	-10	–	–	µA	V_{EN_uC} = V_{EN_IGN} = 0 V; V_{IN_STBY} = 0 V; T_j < 125 °C
Reset Generator RO_1 Monitoring Q_LDO1							

Electrical Characteristics (cont'd)

V_{IN} = V_{IN_STBY} = 13.5 V, T_j = -40 °C to +150 °C,
V_{CCP} = 9.0 V; SEL_STBY = Q_STBY; all voltages with respect to ground.

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
4.4.79	Undervoltage Reset threshold on Q_LDO1	$V_{URT\ Q\_LDO1, de}$	4.50	–	4.75	V	V_{Q_LDO1} decreasing; V_{FB/L_IN} = open;
4.4.80	Undervoltage Reset threshold on Q_LDO1	$V_{URT\ Q\_LDO1, in}$	4.55	–	4.90	V	V_{Q_LDO1} increasing
4.4.81	Undervoltage Reset hysteresis	$V_{URO\_1, hyst}$	100	–	220	mV	–
4.4.82	Overvoltage Reset threshold on Q_LDO1	$V_{ORT\ Q\_LDO1, in}$	5.40	–	5.65	V	V_{Q_LDO1} increasing
4.4.83	Overvoltage Reset threshold on Q_LDO1	$V_{ORT\ Q\_LDO1, de}$	5.25	–	5.60	V	V_{Q_LDO1} decreasing
4.4.84	Overvoltage Reset hysteresis	$V_{ORO\_1, hyst}$	80	–	180	mV	–
4.4.85	RO_1, Reset output low voltage	$V_{RO\_1, low}$	–	–	0.4	V	I_{RO_1} = -10 mA; V_{Q_LDO1} > 2.5 V
4.4.86	RO_1, Reset output low voltage	$V_{RO\_1, low}$	–	–	0.25	V	V_{IN_STBY} = 3.0 V; V_{Q_LDO1} = 2.5V; I_{RO_1} = -500 µA;
4.4.87	RO_1, Reset output leakage	$I_{RO\_1, high}$	-1	–	1	µA	V_{RO_1} = 5.0 V
4.4.88	Reset delay time base	T_{cycle}	41.6	50	62.5	µs	C_{RT} = 1 nF
4.4.89	Reset timing capacitor range	C_{RT}	0.33	1.0	4.7	nF	–
4.4.90	Reset delay time RO_1	t_{RD, RO_1}	–	160	–	T_{cycle}	–
4.4.91	Undervoltage Reset reaction time	t_{UVRR, RO_1}	2	–	10	µs	Voltage step at Q_LDO1 from 5.00 V to 4.48 V
4.4.92	Overvoltage Reset reaction time	t_{OVRR, RO_1}	20	–	80	µs	Buck converter operating; Voltage step at Q_LDO1 from 5.00 V to 5.67 V
Reset Generator RO_2 Monitoring Q_LDO2 and FB_EXT							
4.4.93	Undervoltage Reset threshold on Q_LDO2	$V_{URT\ Q\_LDO2, de}$	3.135	–	3.230	V	SEL_LDO2 = Q_LDO2; V_{Q_LDO2} decreasing; V_{IN_LDO2} = open
4.4.94	Undervoltage Reset headroom on Q_LDO2	$V_{URT\ Q\_LDO2, head}$	55	117.5	–	mV	SEL_LDO2 = Q_LDO2; $V_{URT\ Q\_LDO2, head}$ = V_{Q_LDO2} - $V_{URT\ Q\_LDO2, de}$; V_{Q_LDO2} @ I_{Q_LDO2} = 500 mA
4.4.95	Undervoltage Reset hysteresis Q_LDO2	$V_{URO\_2, hyst}$	15	–	55	mV	SEL_LDO2 = Q_LDO2; $V_{URO\_2, hyst}$ = $V_{URT\ Q\_LDO2, in}$ - $V_{URT\ Q\_LDO2, de}$
4.4.96	Overvoltage Reset threshold on Q_LDO2	$V_{ORT\ Q\_LDO2, in}$	3.70	–	3.85	V	SEL_LDO2 = Q_LDO2; V_{Q_LDO2} increasing

Electrical Characteristics (cont'd)

$V_{IN} = V_{IN\_STBY}$ = 13.5 V, T_j = -40 °C to +150 °C,
V_{CCP} = 9.0 V; SEL_STBY = Q_STBY; all voltages with respect to ground.

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
4.4.97	Overvoltage Reset threshold on Q_LDO2	$V_{ORT\ Q\_LDO2,\ de}$	3.55	–	3.80	V	SEL_LDO2 = Q_LDO2; V_{Q_LDO2} decreasing
4.4.98	Overvoltage Reset hysteresis	$V_{ORO\_2,\ hyst}$	50	–	200	mV	SEL_LDO2 = Q_LDO2;
4.4.99	Undervoltage Reset threshold on Q_LDO2	$V_{URT\ Q\_LDO2,\ de}$	2.485	–	2.560	V	SEL_LDO2 = GND; V_{Q_LDO2} decreasing; V_{IN_LDO2} = open
4.4.100	Undervoltage Reset headroom on Q_LDO2	$V_{URT\ Q\_LDO2,\ head}$	47	–	–	mV	SEL_LDO2 = GND; $V_{URT\ Q\_LDO2,\ head} = V_{Q\_LDO2} - V_{URT\ Q\_LDO2,\ de}$; V_{Q_LDO2} @ I_{Q_LDO2} = 500 mA
4.4.101	Undervoltage Reset hysteresis Q_LDO2	$V_{URO\_2,\ hyst}$	15	–	60	mV	SEL_LDO2 = GND; $V_{URO\_2,\ hyst} = V_{URT\ Q\_LDO2,\ in} - V_{URT\ Q\_LDO2,\ de}$
4.4.102	Overvoltage Reset threshold on Q_LDO2	$V_{ORT\ Q\_LDO2,\ in}$	2.85	–	3.0	V	SEL_LDO2 = GND; V_{Q_LDO2} increasing
4.4.103	Overvoltage Reset threshold on Q_LDO2	$V_{ORT\ Q\_LDO2,\ de}$	2.73	–	2.95	V	SEL_LDO2 = GND; V_{Q_LDO2} decreasing
4.4.104	Overvoltage Reset hysteresis Q_LDO2	$V_{ORO\_2,\ hyst}$	50	–	120	mV	SEL_LDO2 = GND;
4.4.105	Undervoltage Reset threshold on FB_EXT	$V_{URT\ FB\_EXT,\ de}$	1.425	–	1.480	V	TLE7368G, TLE7368E V_{FB_EXT} decreasing; V_{FB/L_IN} = 5 V or V_{Q_LDO2} = 3.3/2.6 V
4.4.106	Undervoltage Reset headroom on FB_EXT	$V_{FB\_EXT} - V_{URT\ FB\_EXT,\ de}$	40	60	–	mV	TLE7368G, TLE7368E V_{FB/L_IN} = 5 V or V_{Q_LDO2} = 3.3/2.6 V; V_{FB_EXT} @ I_{FB_EXT} = 1 A
4.4.107	Undervoltage Reset hysteresis FB_EXT	$V_{URO\_2,\ hyst}$	15	–	45	mV	TLE7368G, TLE7368E
4.4.108	Overvoltage Reset threshold on FB_EXT	$V_{ORT\ FB\_EXT,\ in}$	1.65	–	1.72	V	TLE7368G, TLE7368E V_{FB_EXT} increasing
4.4.109	Overvoltage Reset threshold on FB_EXT	$V_{ORT\ FB\_EXT,\ de}$	1.55	–	1.67	V	TLE7368G, TLE7368E V_{FB_EXT} decreasing
4.4.110	Overvoltage Reset hysteresis FB_EXT	$V_{ORO\_2,\ hyst}$	50	–	120	mV	TLE7368G, TLE7368E
4.4.111	Undervoltage Reset threshold on FB_EXT	$V_{URT\ FB\_EXT,\ de}$	1.08	–	1.15	V	TLE7368-2E V_{FB_EXT} decreasing; V_{FB/L_IN} = 5 V or V_{Q_LDO2} = 3.3/2.6 V;

Electrical Characteristics (cont'd)

V_{IN} = V_{IN_STBY} = 13.5 V, T_j = -40 °C to +150 °C,
V_{CCP} = 9.0 V; SEL_STBY = Q_STBY; all voltages with respect to ground.

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
4.4.112	Undervoltage Reset headroom on FB_EXT	V_{FB_EXT} - $V_{URT\ FB\_EXT,\ de}$	40	60	–	mV	TLE7368-2E V_{FB/L_IN} = 5 V or V_{Q_LDO2} = 3.3/2.6 V;
4.4.113	Undervoltage Reset hysteresis	$V_{URO\_2,\ hyst}$	15	–	45	mV	TLE7368-2E
4.4.114	Overvoltage Reset threshold on FB_EXT	$V_{ORT\ FB\_EXT,\ in}$	1.30	–	1.39	V	TLE7368-2E V_{FB_EXT} increasing;
4.4.115	Overvoltage Reset threshold on FB_EXT	$V_{ORT\ FB\_EXT,\ de}$	1.23	–	1.38	V	TLE7368-2E V_{FB_EXT} decreasing;
4.4.116	Overvoltage Reset hysteresis	$V_{ORO\_2,\ hyst}$	10	–	70	mV	TLE7368-2E
4.4.117	Undervoltage Reset threshold on FB_EXT	$V_{URT\ FB\_EXT,\ de}$	1.17	–	1.25	V	TLE7368-3E V_{FB_EXT} decreasing; V_{FB/L_IN} = 5 V or V_{Q_LDO2} = 3.3/2.6 V;
4.4.118	Undervoltage Reset headroom on FB_EXT	V_{FB_EXT} - $V_{URT\ FB\_EXT,\ de}$	40	60	–	mV	TLE7368-3E V_{FB/L_IN} = 5 V or V_{Q_LDO2} = 3.3/2.6 V;
4.4.119	Undervoltage Reset hysteresis	$V_{URO\_2,\ hyst}$	15	–	45	mV	TLE7368-3E
4.4.120	Overvoltage Reset threshold on FB_EXT	$V_{ORT\ FB\_EXT,\ in}$	1.35	–	1.43	V	TLE7368-3E V_{FB_EXT} increasing;
4.4.121	RO_2, Reset output low voltage	$V_{RO\_2,\ low}$	–	–	0.4	V	I_{RO_2} = -10 mA; V_{Q_LDO2} > 2.0 V
4.4.122	RO_2, Reset output low voltage	$V_{RO\_2,\ low}$	–	–	0.25	V	I_{RO_2} = -500 µA; V_{Q_LDO2} = 1V
4.4.123	RO_2, Reset output leakage	$I_{RO\_2,\ high}$	-1	–	1	µA	V_{RO_2} = 5.0 V
4.4.124	Reset delay time RO_2	$t_{RD,\ RO\_2}$	–	160	–	T_{cycle}	–
4.4.125	Undervoltage Reset reaction time	$t_{UVRR,\ RO\_2}$	2	–	10	µs	Voltage step on Q_LDO2 from $V_{Q\_LDO2,\ nom}$ to $V_{URT\ Q\_LDO2,\ de,\ min}$ - 20 mV
4.4.126	Undervoltage Reset reaction time	$t_{UVRR,\ RO\_2}$	2	–	10	µs	Voltage step on FB_EXT from $V_{FB\_EXT,\ nom}$ to $V_{URT\ FB\_EXT,\ de,\ min}$ - 20 mV
4.4.127	Overvoltage Reset reaction time	$t_{OVRR,\ RO\_2}$	20	–	80	µs	Buck converter operating; Voltage step on Q_LDO2 from $V_{Q\_LDO2,\ nom}$ to $V_{ORT\ Q\_LDO2,\ in,\ max}$ + 20 mV

Electrical Characteristics (cont'd)

V_{IN} = V_{IN_STBY} = 13.5 V, T_j = -40 °C to +150 °C,
V_{CCP} = 9.0 V; SEL_STBY = Q_STBY; all voltages with respect to ground.

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
4.4.128	Overvoltage Reset reaction time	t_{OVRR, RO_2}	20	–	80	µs	Buck converter operating; Voltage step on FB_EXT from $V_{FB\_EXT, nom}$ to $V_{ORT\ FB\_EXT, in, max}$ + 20 mV

Electrical Characteristics (cont'd)

V_{IN} = V_{IN_STBY} = 13.5 V, T_j = -40 °C to +150 °C,
V_{CCP} = 9.0 V; SEL_STBY = Q_STBY; all voltages with respect to ground.

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	**Typ.**	**Max.**		
Monitoring Block							
4.4.129	MON_STBY, Threshold on Q_STBY	$V_{MON, Q\_STBY, de}$	0.90	–	–		V_{IN_STBY} = 3.0 V; SEL_STBY = Q_STBY; V_{Q_STBY} decreasing;
4.4.129a	MON_STBY headroom	$V_{MON, Q\_STBY, head}$	10	–	–	mV	V_{IN_STBY} = 3.0 V; SEL_STBY = Q_STBY; V_{Q_STBY} decreasing;
4.4.130	MON_STBY hysteresis	$V_{MON\_STBY, hyst}$	10	–	30	mV	SEL_STBY = Q_STBY
4.4.131	MON_STBY, Threshold on Q_STBY	$V_{MON, Q\_STBY, de}$	2.36	–	2.50	V	V_{IN_STBY} = 3.0 V; SEL_STBY = GND; V_{Q_STBY} decreasing;
4.4.132	MON_STBY hysteresis	$V_{MON\_STBY, hyst}$	20	–	50	mV	SEL_STBY = GND
4.4.133	MON_STBY, Monitoring output low voltage	$V_{MON\_STBY, low}$	–	–	0.4	V	I_{MON_STBY1} < 10 mA; V_{IN_STBY} > 3.0 V
4.4.134	MON_STBY time delay	t_{MON_STBY}	–	8	–	t_{RD, RO_1}	see diagram in section **"Monitoring Circuit" on Page 31**
4.4.135	Monitor reaction time	t_{RR, MON_STBY}	3	–	6	µs	–

Electrical Characteristics (cont'd)

V_{IN} = V_{IN_STBY} = 13.5 V, T_j = -40 °C to +150 °C,
V_{CCP} = 9.0 V; SEL_STBY = Q_STBY; all voltages with respect to ground.

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Window Watchdog							
4.4.136	H-input voltage threshold	$V_{WDI,\ high}$	–	–	2.0	V	–
4.4.137	L-input voltage threshold	$V_{WDI,\ low}$	0.8	–	–	V	–
4.4.138	WDI pull-up resistor	R_{WDI}	60	100	140	kΩ	connected to Q_LDO2
4.4.139	Watchdog cycle time	T_{WD}	–	2	–	T_{cycle}	–
4.4.140	Window duration (OW, CW, FW)	$t_{WD,\ W}$	–	512	–	T_{WD}	–
4.4.141	Window duration (IW)	$t_{WD,\ IW}$	–	32	–	T_{WD}	–
4.4.142	Window watchdog initialization time	$t_{WD,\ start}$	–	32	–	T_{WD}	Watchdog will start/initialized if WDI is kept low for this period and RO_2 is released
4.4.143	Watchdog output low voltage	$V_{WDO,low}$	–	–	0.4	V	I_{WDO} = 2 mA
4.4.144	Watchdog output leakage current	$I_{WDO,leak}$	–	–	1	µA	WDO state = High
Thermal Shutdown							
4.4.145	Overtemperature shutdown	$T_{j,\ shtdwn}$	160	175	190	°C	[1) 8)]
4.4.146	Overtemperature shutdown hysteresis	ΔT	15	–	30	K	[1)]

1) Specified by design, not subject to production test.
2) Tested according to measurement circuit 1.
3) V_{CCP} supplied externally with a voltage according to the actual value of V_{CCP} measurement.
4) $V_{dr,\ Q\_LDO1} = V_{FB/L\_IN} - V_{Q\_LDO1}$; $V_{dr,\ Q\_LDO2} = V_{IN\_LDO2} - V_{Q\_LDO2}$; $V_{dr,\ T<1,\ 2>} = V_{FB/L\_IN} - V_{Q\_T<1,\ 2>}$
5) Minimum value given is needed for regulator stability; application might need higher capacitance than the minimum.
6) Measured when V_{Q_LDO2} has dropped 100 mV from its nominal value obtained at V_{IN_LDO2} = 5.4 V.
7) External power transistor type: Fairchild KSH200.
8) Permanent operation of the device above 150 °C degrades lifetime; please refer to quality information.

5 Detailed Internal Circuits Description

In the following the main circuit blocks of the TLE7368, namely the Buck converter, the linear regulators, the trackers, the charge pump, the enable and reset circuits and the watchdog are described in more detail.

5.1 Buck Regulator

The TLE7368's DC to DC converter features all the functions necessary to implement a high efficient, low emission Buck regulator with minimum external components. The step down regulator in the TLE7368 follows a concept similar to the one of its predecessor, TLE6368, which allows operation over a battery voltage range from as low as 4.5 V up to a maximum of 45 V at peak currents of 2.5 A at minimum. **Figure 3** shows the block diagram of the converter with its major components, i.e. the internal DMOS power stages, the high side driver including its supply scheme, the power stage slope control circuit for reduced EME, the current mode control scheme and various protection circuits for safe converter operation.

5.1.1 Buck Regulator Control Scheme

The step down converter's control method is based upon the current mode control scheme. Current mode control provides an inherent line feed forward, cycle by cycle current limiting and ease of loop compensation. No external compensation components are needed to stabilize the loop, i.e. the operation of the Buck converter. The slope compensation circuit in addition to the current sense amplifier and the error amplifier prevents instabilities/sub harmonic oscillations at duty cycles higher than 0.5. The cycle by cycle current limiting feature supports also a soft start feature during power up. Additional implemented current blanking prevents faulty DMOS turn off signals during switching operation.

5.1.2 High Side Driver Supply and 100% Duty Cycle Operation

The supply concept of the Buck converter's power stage driver follows the Bootstrapping principle. A small external capacitor, placed between pins SW and BST, is used to provide the necessary charge at the gate of the power stage. The capacitor is refreshed at each switching cycle while the power stage is turned off resulting in the ability to power the gate at the next turn on of the power stage.

In cases where the input/battery voltage approaches the nominal Buck converter output voltage, the duty cycle of the converter increases. At the point where the power stage is statically turned on (100% duty cycle) a refresh of the Bootstrap capacitor as described above is not possible. In this case the charge pump helps to accomplish the gate over drive in order to keep the power stage turned on with low R_{dson}. With decreasing input voltage, shortly before switching to 100% duty cycle, the device operates in pulse skipping mode. In this mode the device appears to be operating at much lower frequencies with very small duty cycles. In real, the device is doing a few 100% duty cycle periods followed by a period with a duty cycle smaller than 1.

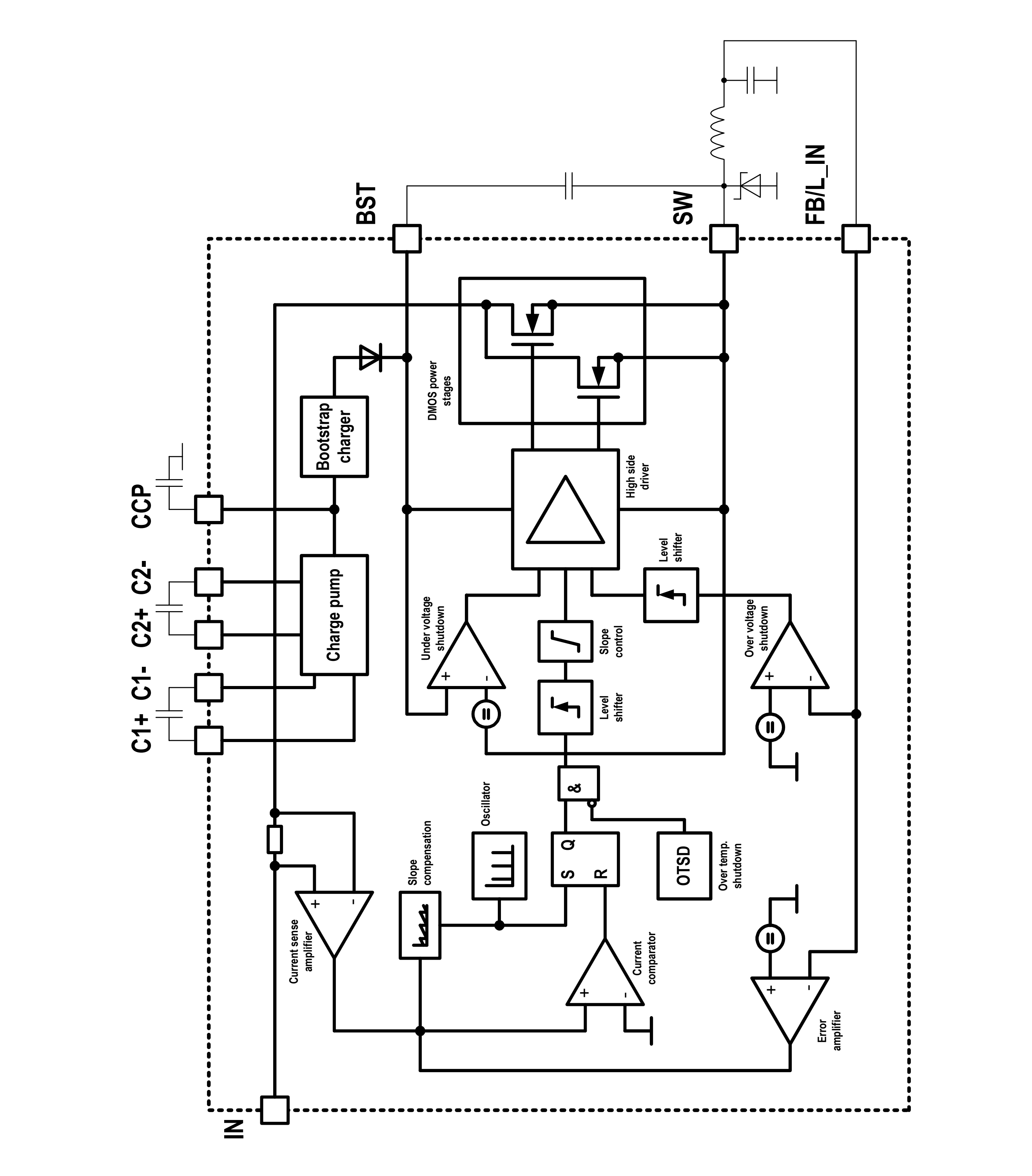


Figure 3 Buck Converter Block Diagram

5.1.3 Electromagnetic Emission Reduction

The Buck DMOS power stage is implemented as multiple cells. This allows to control the slope of the power stage's current at turn on/off by sequentially turning on/off the cells, achieving a smooth turn on/off and therefore avoiding high frequency components in the electromagnetic emissions to the battery line. The current slope control is adjusted internally, the typical current slew rate is 50 ns/A.