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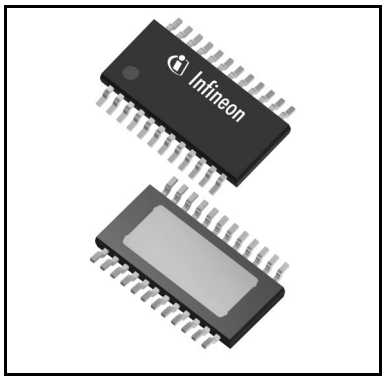
TLE75242-ESD

SPIDER+ 12V

SPI Driver for Enhanced Relay Control

AEC Qualified RoHS

Package	PG-TSDSO-24-21
Marking	TLE75242ESD



1 Overview

Applications

- Low-side and High-side switches for 12 V in automotive or industrial applications such as lighting, heating, motor driving, energy and power distribution
- Especially designed for driving relays, LEDs and motors.

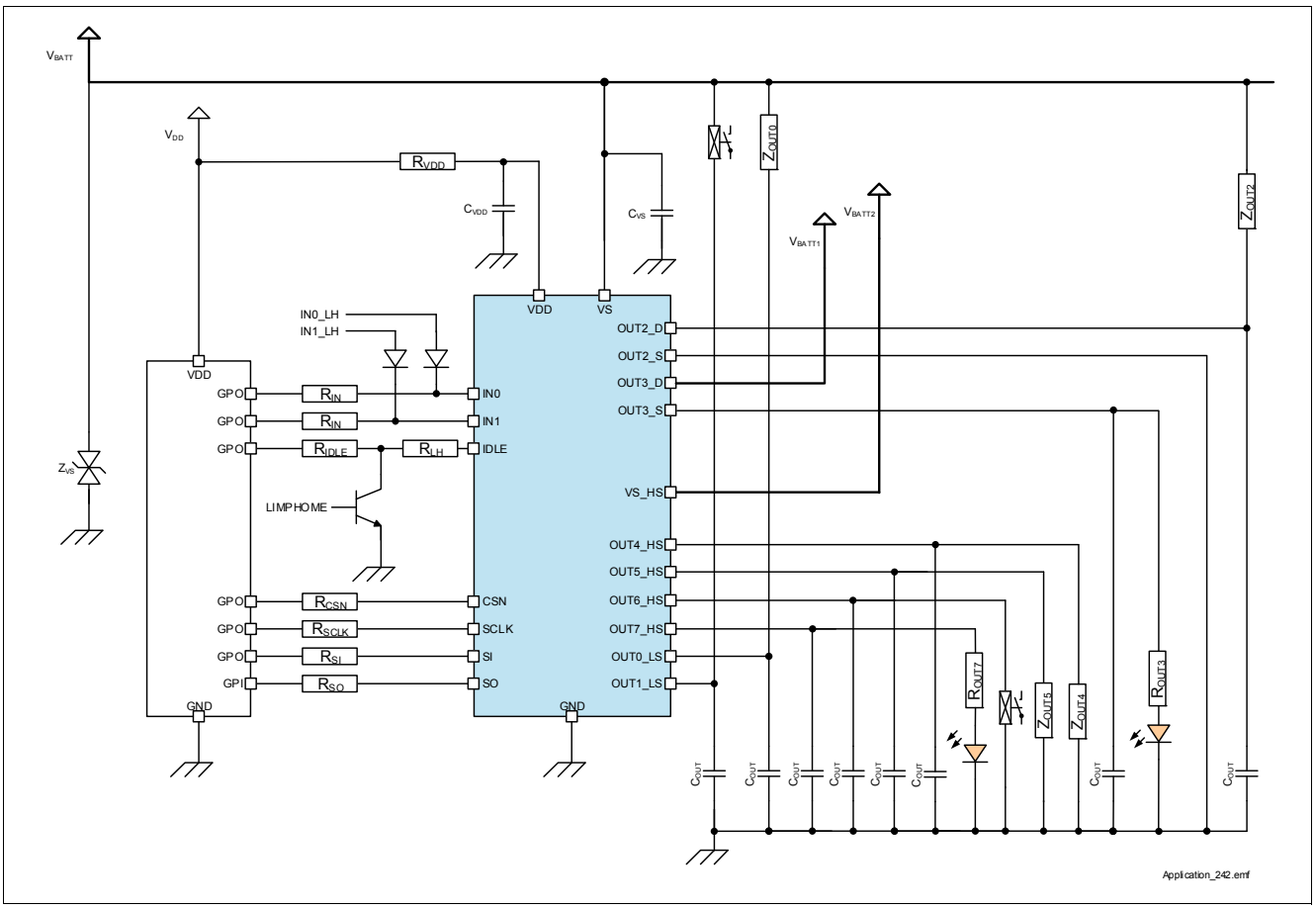


Figure 1 TLE75242-ESD Application Diagram

Overview

Basic Features

- 16-bit serial peripheral interface for control and diagnosis
- Daisy Chain capability SPI also compatible with 8-bit SPI devices
- 2 CMOS compatible parallel input pins with Input Mapping functionality
- Cranking capability down to V_S = 3.0 V (supports LV124)
- Digital supply voltage range compatible with 3.3 V and 5 V microcontrollers
- Independend supply pin (V_{S_HS}) for high-side channels
- Very low quiescent current (with usage of IDLE pin)
- Limp Home mode (with usage of IDLE and IN pins)
- Green Product (RoHS compliant)
- AEC Qualified

Protection Features

- Reverse battery protection on V_S without external components
- Short circuit to ground and battery protection
- Stable behavior at under voltage conditions (“Lower Supply Voltage Range for Extended Operation”)
- Over Current latch OFF
- Thermal shutdown latch OFF
- Overvoltage protection
- Loss of ground protection
- Loss of battery protection
- Electrostatic discharge (ESD) protection

Diagnostic Features

- Latched diagnostic information via SPI register
- Over Load detection at ON state
- Open Load detection at OFF state using Output Status Monitor function
- Output Status Monitor
- Input Status Monitor

Application Specific Features

- Fail-safe activation via Input pins in Limp-Home Mode
- SPI with Daisy Chain capability
- Safe operation at low battery voltage (cranking)
- One supply pin for high-side switches independent from main supply pin V_S

Description

The TLE75242-ESD is an eight channel low-side and high-side power switch in PG-TSDSO-24-21 package providing embedded protective functions. It is specially designed to control relays and LEDs in automotive and industrial applications.

A serial peripheral interface (SPI) is utilized for control and diagnosis of the loads as well as of the device. For direct control and PWM there are two input pins available connected to two outputs by default. Additional or different outputs can be controlled by the same input pins (programmable via SPI).

Overview

Table 1 Product Summary

Parameter	Symbol	Values
Analog supply voltage	V_S	3.0 V … 28 V
Digital supply voltage	V_{DD}	3.0 V … 5.5 V
Minimum overvoltage protection	$V_{S(AZ)}$	42 V (see **Chapter 8.5** for details)
Maximum on-state resistance at T_J = 150 °C	$R_{DS(ON)}$	2.2 Ω
Nominal load current (T_A = 85 °C, all channels)	$I_{L(NOM)}$	330 mA
Maximum Energy dissipation - repetitive	E_{AR}	10 mJ @ $I_{L(EAR)}$ = 220 mA
Minimum Drain to Source clamping voltage	$V_{DS(CL)}$	42 V (when used as low-side switches)
Maximum Source to Ground clamping voltage	$V_{OUT\_S(CL)}V_{OUT(CL)}$	-16 V
Maximum overload switch OFF threshold	$I_{L(OVL0)}$	2.3 A
Maximum total quiescent current at $T_J \leq 85$ °C	I_{SLEEP}	5 µA
Maximum SPI clock frequency	f_{SCLK}	5 MHz

Detailed Description

The TLE75242-ESD is an eight channel low-side and high-side switch providing embedded protective functions. The output stages incorporate two low-side, four high-side and two auto-configurable high-side or low-side switches (typical $R_{DS(ON)}$ at T_J = 25°C is 1 Ω). The auto-configurable switches can be utilized in high-side or low-side configuration just by connecting the load accordingly. Protection and diagnosis functions adjust automatically to the hardware configuration.

The 16-bit serial peripheral interface (SPI) is utilized to control and diagnose the device and the loads. The SPI interface provides daisy chain capability in order to assemble multiple devices (also devices with 8 bit SPI) in one SPI chain by using the same number of microcontroller pins.

This device is designed for low supply voltage operation, therefore being able to keep its state at low battery voltage ($V_S \geq 3.0$ V). The SPI functionality, including the possibility to program the device, is available only when the digital power supply is present (see **Chapter 6** for more details).

The TLE75242-ESD is equipped with two input pins that are connected to two configurable outputs, making them controllable even when the digital supply voltage is not available. With the Input Mapping functionality it is possible to connect the input pins to different outputs, or assign more outputs to the same input pin. In this case more channels can be controlled with one signal applied to one input pin.

In Limp Home mode (Fail-Safe mode) the input pins are directly routed to channels 2 and 3. When IDLE pin is “low”, it is possible to activate the two channels using the input pins independently from the presence of the digital supply voltage.

The device provides diagnosis of the load via Open Load at OFF state (with **DIAG_OSM.OUTn** bits) and short circuit detection. For Open Load at OFF state detection, a internal current source I_{OL} can be activated via SPI.

Each output stage is protected against short circuit. In case of Overload, the affected channel switches OFF when the Overload Detection Current $I_{L(OVLn)}$ is reached and can be reactivated via SPI. In Limp Home mode operation, the channels connected to an input pin set to “high” restart automatically after Output Restart time $t_{RETRY(LH)}$ is elapsed. Temperature sensors are available for each channel to protect the device against Over Temperature.

The power transistors are built by N-channel power MOSFET with one central chargepump for auto-configurable and high-side channels. The inputs are ground referenced TTL compatible. The device is monolithically integrated in Smart Power Technology.

2 Block Diagram and Terms

2.1 Block Diagram

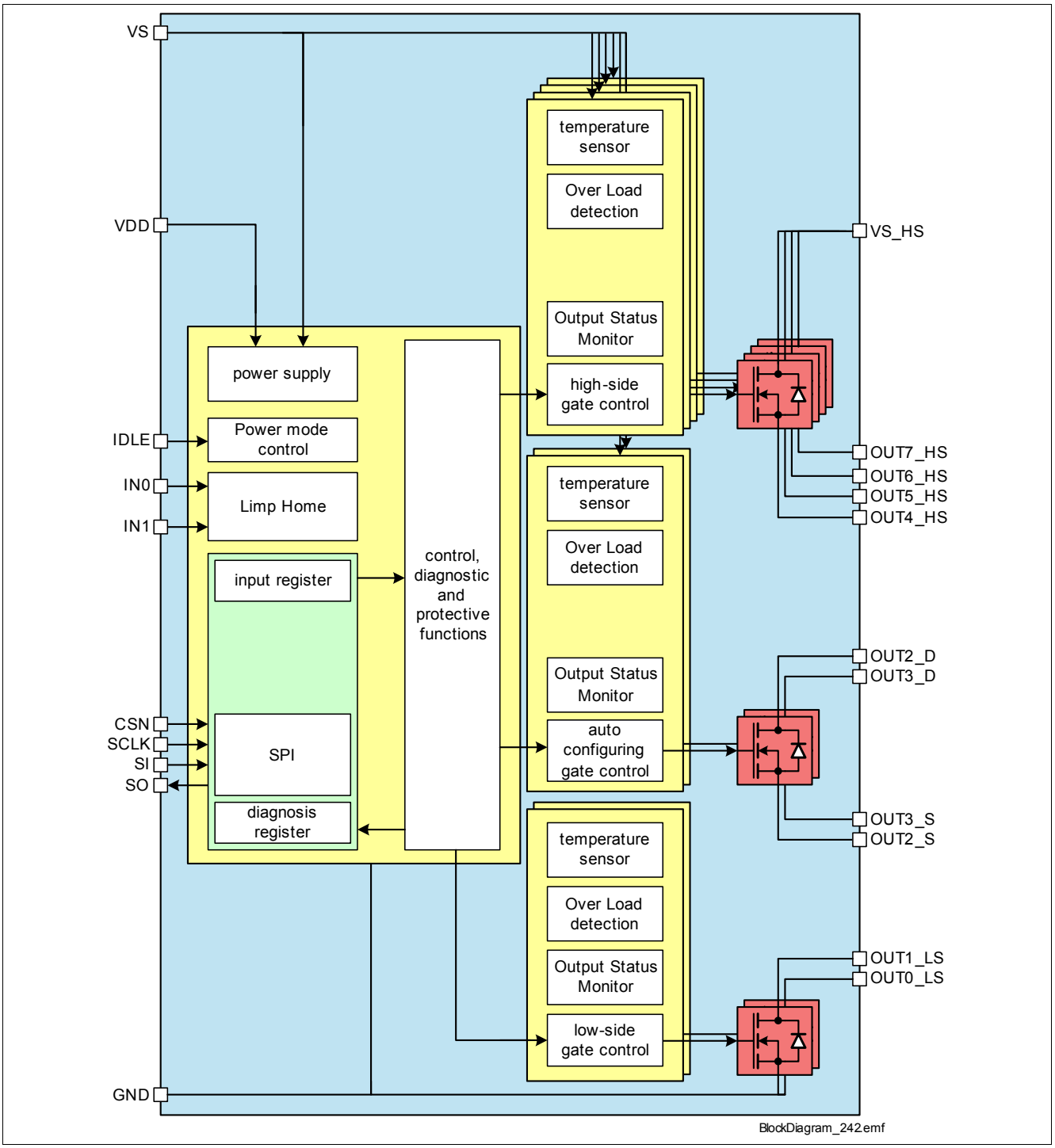


Figure 2 Block Diagram of TLE75242-ESD

2.2 Terms

Figure 3 shows all terms used in this data sheet, with associated convention for positive values.

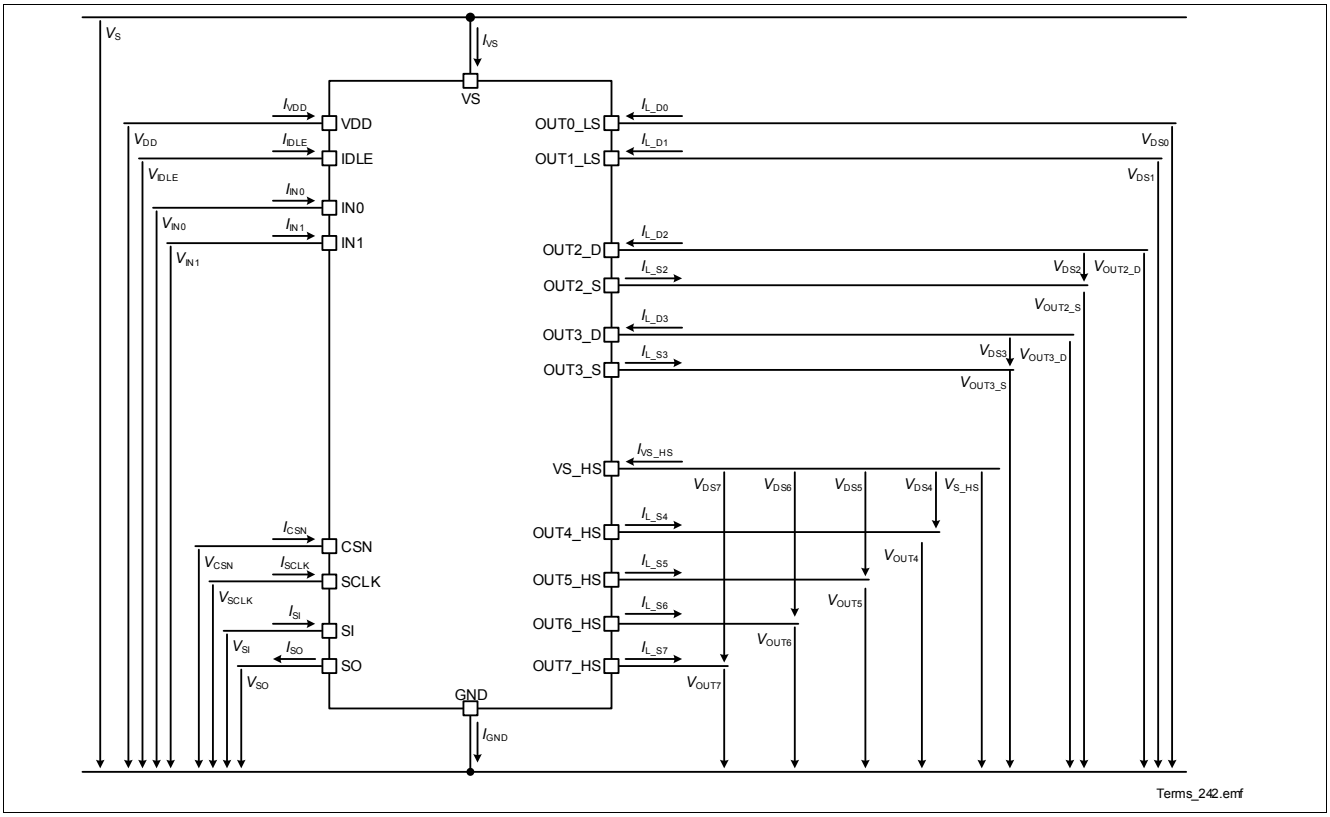


Figure 3 Voltage and Current definition

In all tables of electrical characteristics the channel related symbols without channel numbers are valid for each channel separately (e.g. V_{DS} specification is valid for V_{DS0} ... V_{DS7}).

Furthermore, parameters relative to output current can be indicated without specifying whether the current is going into the Drain pin or going out of the Source pin, unless otherwise specified. For instance, nominal output current can be indicated in the following ways: $I_{L(NOM)}$ $I_{L\_LS(NOM)}$ $I_{L\_HS(NOM)}$ $I_{L\_D(NOM)}$ $I_{L\_S(NOM)}$

All SPI registers bits are marked as follows: `ADDR.PARAMETER` (e.g. `HWCR.RST`) with the exception of the bits in the Diagnosis frames which are marked only with `PARAMETER` (e.g. `UVRVS`).

3 Pin Configuration

3.1 Pin Assignment

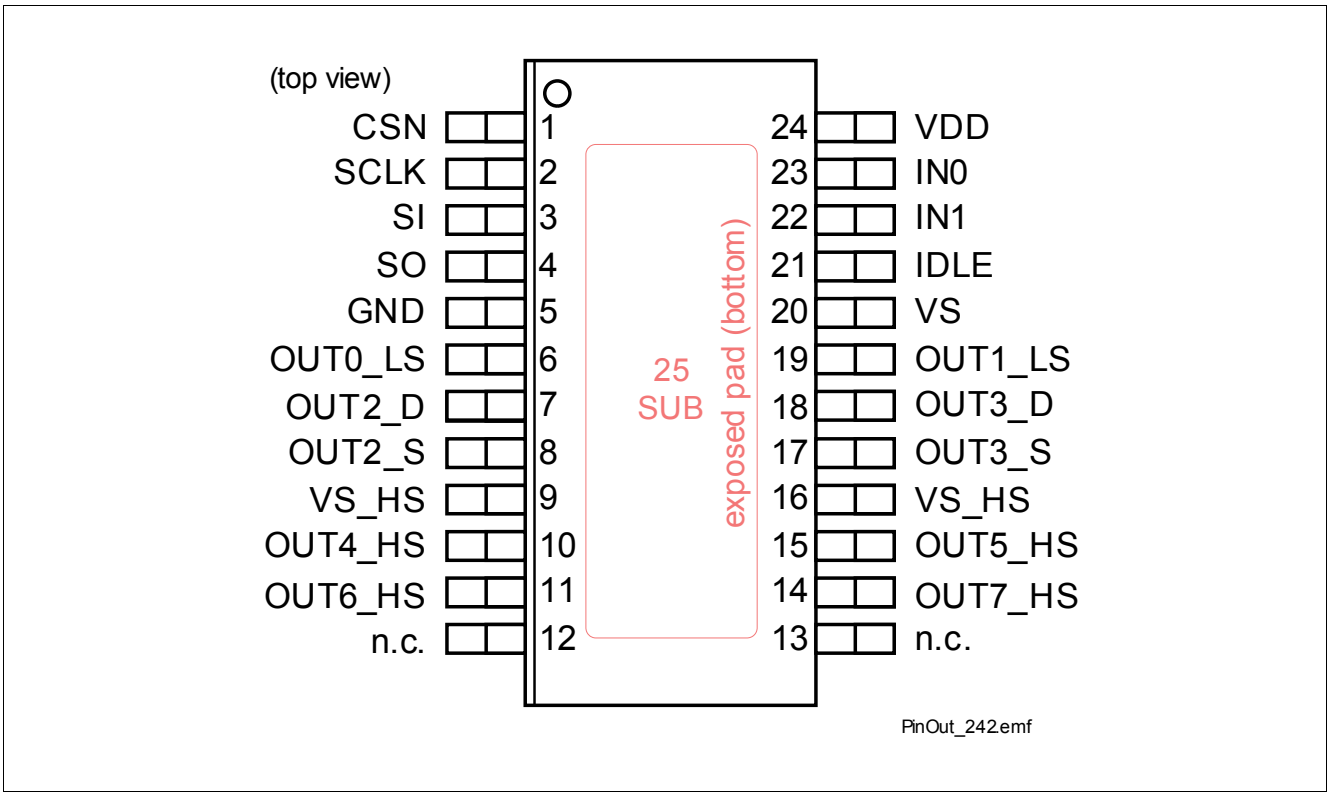


Figure 4 Pin Configuration TLE75242-ESD in PG-TSDSO-24-21

3.2 Pin Definitions and Functions

Pin	Symbol	I/O	Function
Power Supply Pins			
20	VS	–	**Analog supply V_S** Positive supply voltage for power switches gate control (incl. protections)
9, 16	VS_HS	–	**Analog supply V_{S_HS}** Positive supply voltage for power switches drain current
24	VDD	–	**Digital supply V_{DD}** Supply voltage for SPI with support function to V_S
5	GND	–	**Ground** Ground connection (also for the low-side switches)
SPI Pins			
1	CSN	I	**Chip Select** “low” active, integrated pull-up to V_{DD}
2	SCLK	I	**Serial Clock** “high” active, integrated pull-down to ground
3	SI	I	**Serial Input** “high” active, integrated pull-down to ground
4	SO	O	**Serial Output** “Z” (tri-state) when CSN is “high”
Input and Stand-by Pins			
21	IDLE	I	**Idle mode** power mode control, “high” activates Idle mode, integrated pull-down to ground
23	IN0	I	**Input pin 0** connected to channel 2 by default and in Limp Home mode, “high” active, integrated pull-down to ground
22	IN1	I	**Input pin 1** connected to channel 3 by default and in Limp Home mode, “high” active, integrated pull-down to ground
Power Ouput Pins			
6	OUT0_LS	O	Drain of low-side power transistor (channel 0)
7	OUT2_D	O	Drain of auto configurable power transistor (channel 2)
8	OUT2_S	O	Source of auto configurable power transistor (channel 2)
17	OUT3_S	O	Source of auto configurable power transistor (channel 3)
18	OUT3_D	O	Drain of auto configurable power transistor (channel 3)
19	OUT1_LS	O	Drain of low-side power transistor (channel 1)
10	OUT4_HS	O	Source of high-side power transistor (channel 4)
11	OUT6_HS	O	Source of high-side power transistor (channel 6)
14	OUT7_HS	O	Source of high-side power transistor (channel 7)

Pin Configuration

Pin	Symbol	I/O	Function
15	OUT5_HS	O	Source of high-side power transistor (channel 5)
Not Connected pins / Cooling Tab			
12, 13	n.c.	–	Not Connected, internally not bonded
25	GND	–	**Exposed pad** It is recommended to connect it to PCB ground for cooling and EMC - not usable as electrical GND pin. Electrical ground must be provided by pin 5.

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings [1)]

T_J = -40 °C to +150 °C
all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)
Voltage ranges specifed for V_S apply also to V_{S_HS} (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Supply Voltages							
Analog Supply voltage	V_S	-0.3	–	28	V	–	P_4.1.1
Digital Supply voltage	V_{DD}	-0.3	–	5.5	V	–	P_4.1.2
Supply voltage for load dump protection	$V_{S(LD)}$	–	–	42	V	[2)]	P_4.1.3
Supply voltage for short circuit protection (single pulse)	$V_{S(SC)}$	0	–	28	V	–	P_4.1.4
Reverse polarity voltage	$-V_{S(REV)}$	–	–	16	V	[3)] $T_{J(0)}$ = 25 °C t ≤ 2 min See **Chapter 11** for general setup. R_L = 70 Ω on all channels	P_4.1.5
Current through VS pin	I_{VS}	-10	–	10	mA	t ≤ 2 min	P_4.1.7
Current through VDD pin	I_{VDD}	-50	–	10	mA	t ≤ 2 min	P_4.1.8
Power Stages							
Load current	$\|I_L\|$	–	–	$I_{L(OVL0)}$	A	single channel	P_4.1.9
Voltage at power transistor	V_{DS}	-0.3	–	42	V	–	P_4.1.10
Power transistor source voltage	V_{OUT_S}	-16	–	V_{OUT_D} +0.3	V	–	P_4.1.11
Power transistor drain voltage ($V_{OUT\_S} \geq 0$ V)	V_{OUT_D}	V_{OUT_S} - 0.3	–	42	V	–	P_4.1.12
Power transistor drain voltage ($V_{OUT\_S} < 0$ V)	V_{OUT_D}	-0.3	–	42	V	–	P_4.1.59
Maximum energy dissipation single pulse	E_{AS}	–	–	50	mJ	[4)] $T_{J(0)}$ = 25 °C $I_{L(0)} = 2^* I_{L(EAR)}$	P_4.1.13
Maximum energy dissipation single pulse	E_{AS}	–	–	25	mJ	[4)] $T_{J(0)}$ = 150 °C $I_{L(0)}$ = 400 mA	P_4.1.14

Table 2 Absolute Maximum Ratings (cont'd)[1)]

T_J = -40 °C to +150 °C
all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)
Voltage ranges specifed for V_S apply also to V_{S_HS} (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Maximum energy dissipation repetitive pulses - $I_{L(EAR)}$	E_{AR}	–	–	10	mJ	[4)] $T_{J(0)}$ = 85 °C $I_{L(0)} = I_{L(EAR)}$ $2*10^6$ cycles	P_4.1.15
IDLE pin							
Voltage at IDLE pin	V_{IDLE}	-0.3		5.5	V	–	P_4.1.23
Current through IDLE pin	I_{IDLE}	-0.75		0.75	mA	–	P_4.1.25
Current through IDLE pin	I_{IDLE}	-10.0		2.0	mA	$t \leq 2$ min.	P_4.1.26
Input Pins							
Voltage at input pins	V_{IN}	-0.3		5.5	V	–	P_4.1.28
Current through input pins	I_{IN}	-0.75		0.75	mA	–	P_4.1.30
Current through input pins	I_{IN}	-10.0		2.0	mA	$t \leq 2$ min.	P_4.1.31
SPI Pins							
Voltage at chip select pin	V_{CSN}	-0.3		5.5	V	–	P_4.1.33
Current through chip select pin	I_{CSN}	-0.75		0.75	mA	–	P_4.1.34
Current through chip select pin	I_{CSN}	-10.0		2.0	mA	$t \leq 2$ min.	P_4.1.35
Voltage at serial clock pin	V_{SCLK}	-0.3		5.5	V		P_4.1.37
Current through serial clock pin	I_{SCLK}	-0.75		0.75	mA	–	P_4.1.38
Current through serial clock pin	I_{SCLK}	-10.0		2.0	mA	$t \leq 2$ min.	P_4.1.39
Voltage at serial input pin	V_{SI}	-0.3		5.5	V		P_4.1.41
Current through serial input pin	I_{SI}	-0.75		0.75	mA	–	P_4.1.42
Current through serial input pin	I_{SI}	-10.0		2.0	mA	$t \leq 2$ min.	P_4.1.43
Voltage at serial output pin SO	V_{SO}	-0.3		V_{DD}+0.3	V		P_4.1.58
Current through serial output pin SO	I_{SO}	-0.75		0.75	mA		P_4.1.45
Current through serial output pin SO	I_{SO}	-2.0		10.0	mA	$t \leq 2$ min.	P_4.1.46
Temperatures							
Junction Temperature	T_J	-40	–	150	°C	–	P_4.1.48
Storage Temperature	T_{stg}	-55	–	150	°C	–	P_4.1.49
ESD Susceptibility							
ESD Susceptibility HBM OUT pins vs. V_S or GND	V_{ESD}	-4	–	4	kV	[5)] HBM	P_4.1.50
ESD Susceptibility HBM other pins	V_{ESD}	-2	–	2	kV	[5)] HBM	P_4.1.51

Table 2 Absolute Maximum Ratings (cont'd)[1)]

T_J = -40 °C to +150 °C
all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)
Voltage ranges specifed for V_S apply also to V_{S_HS} (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
ESD Susceptibility CDM Pin 1, 12, 13, 24 (corner pins)	V_{ESD}	-750	–	750	V	6) CDM	P_4.1.52
ESD Susceptibility CDM	V_{ESD}	-500	–	500	V	6) CDM	P_4.1.54

1) Not subject to production test, specified by design.
2) For a duration of t_{on} = 400 ms; t_{on}/t_{off} = 10%; limited to 100 pulses
3) Device is mounted on a FR4 2s2p board according to Jedec JESD51-2,-5,-7 at natural convection; the Product (Chip+Package) was simulated on a 76.2 *114.3 *1.5 mm board with 2 inner copper layers (2 * 70 µm Cu, 2 * 35 µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.
4) Pulse shape represents inductive switch off: $I_L(t) = I_L(0)$ x (1 - t / t_{pulse}); 0 < t < t_{pulse}
5) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS001 (1.5k Ω, 100 pF)
6) ESD susceptibility, Charged Device Model "CDM" ESDA STM5.3.1 or ANSI/ESD S.5.3.1

Notes

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.*

4.2 Functional Range

Table 3 Functional range

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Supply Voltage Range for Normal Operation	$V_{S(NOR)}$	7	–	18	V	–	P_4.2.1
Upper Supply Voltage Range for Extended Operation	$V_{S(EXT,UP)}$	18	–	28	V	Parameter deviation possible	P_4.2.2
Lower Supply Voltage Range for Extended Operation	$V_{S(EXT,LOW)}$	3	–	7	V	Parameter deviation possible	P_4.2.3
Junction Temperature	T_J	-40	–	150	°C	–	P_4.2.4
Logic supply voltage	V_{DD}	3	–	5.5	V	–	P_4.2.5

Note: Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the Electrical Characteristics table.

4.3 Thermal Resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to **www.jedec.org**.*

Table 4 Thermal Resistance

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction to Soldering Point	R_{thJSP}	–	3	5	K/W	1) measured to exposed pad (pin 25)	P_4.3.4
Junction to Ambient	R_{thJA}	–	28	–	K/W	1)2)	P_4.3.5

1) not subject to production test, specified by design

2) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; the Product (Chip+Package) was simulated on a 76.2 * 114.3 * 1.5 mm board with 2 inner copper layers (2 * 70 µm Cu, 2 * 35 µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

4.3.1 PCB set up

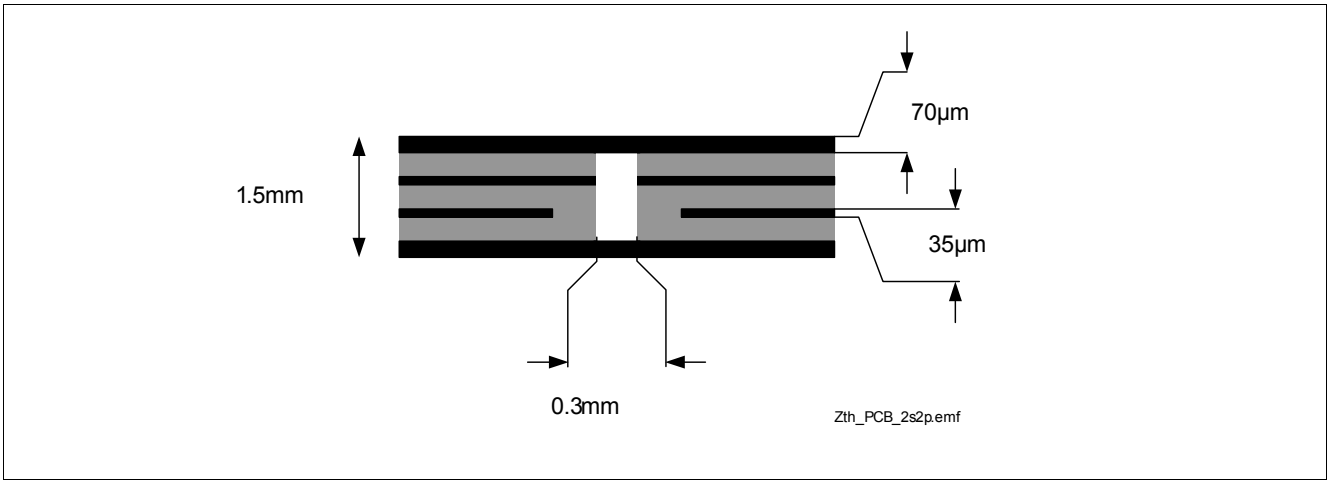


Figure 5 2s2p PCB Cross Section

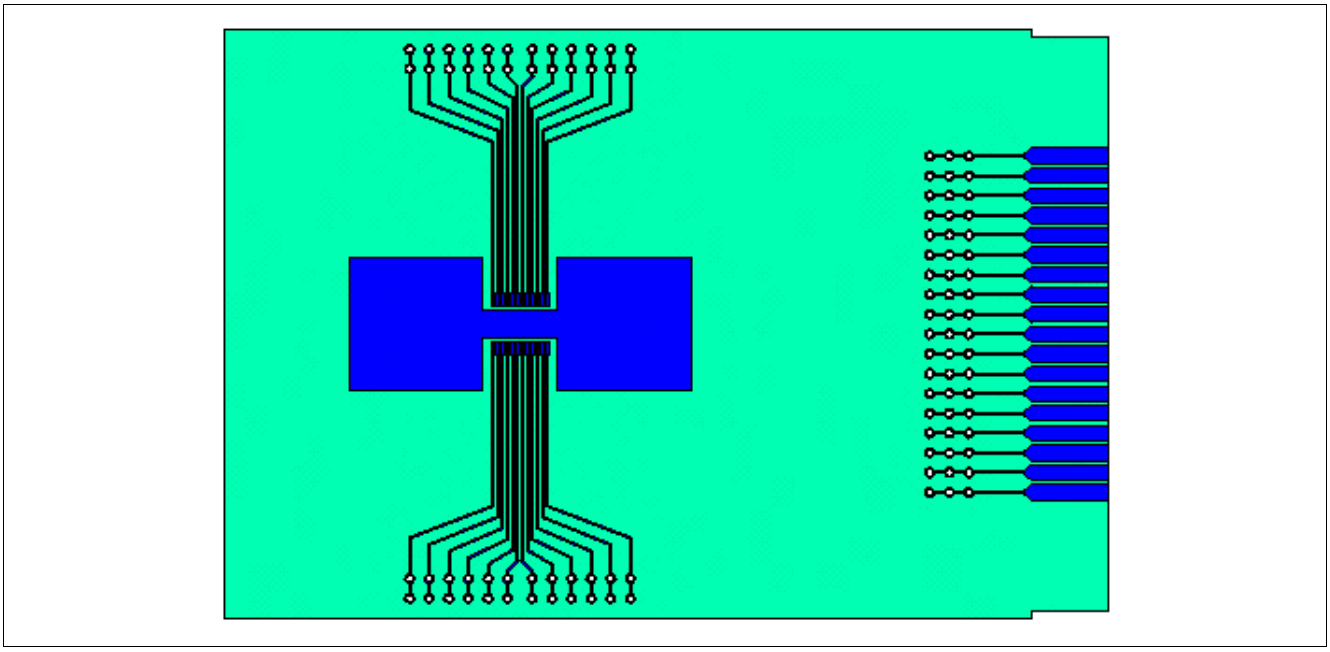


Figure 6 PC Board for Thermal Simulation with 600 mm² Cooling Area

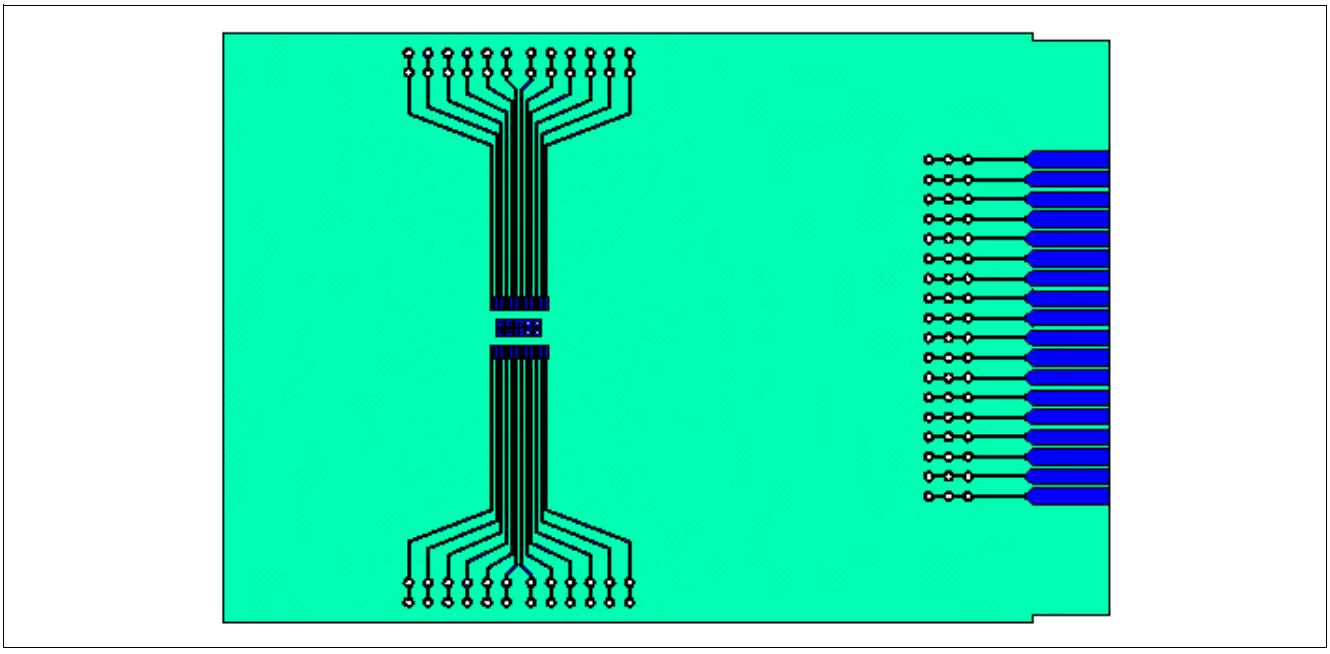


Figure 7 PC Board for Thermal Simulation with 2s2p Cooling Area

4.3.2 Thermal Impedance

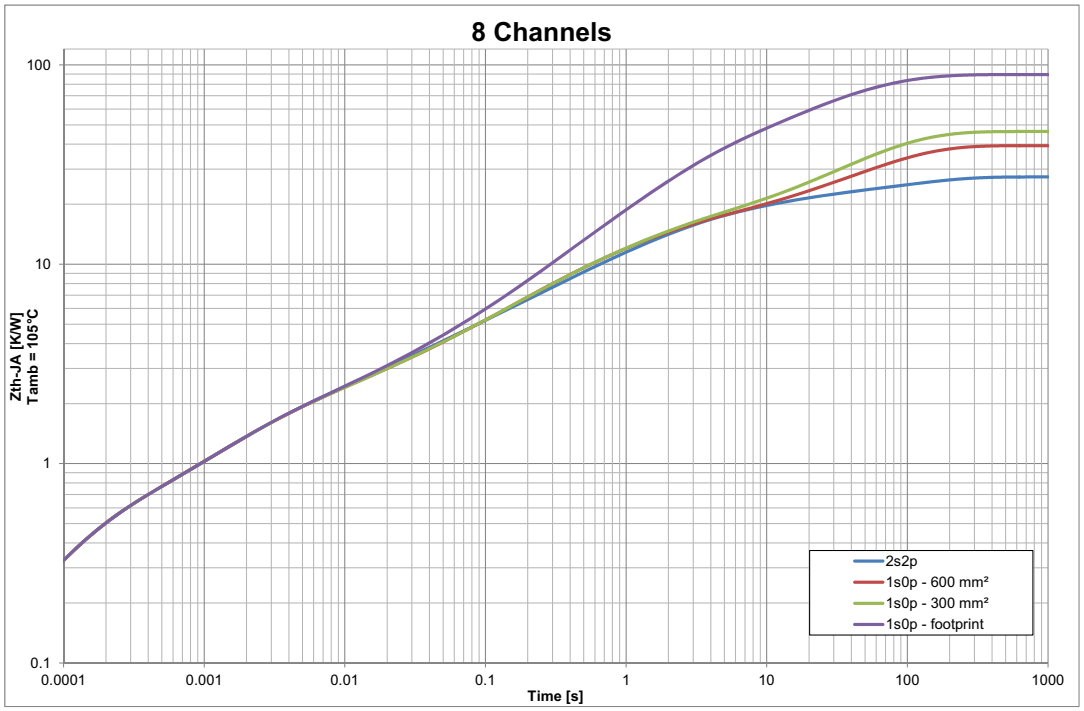


Figure 8 Typical Thermal Impedance. PCB setup according Chapter 4.3.1

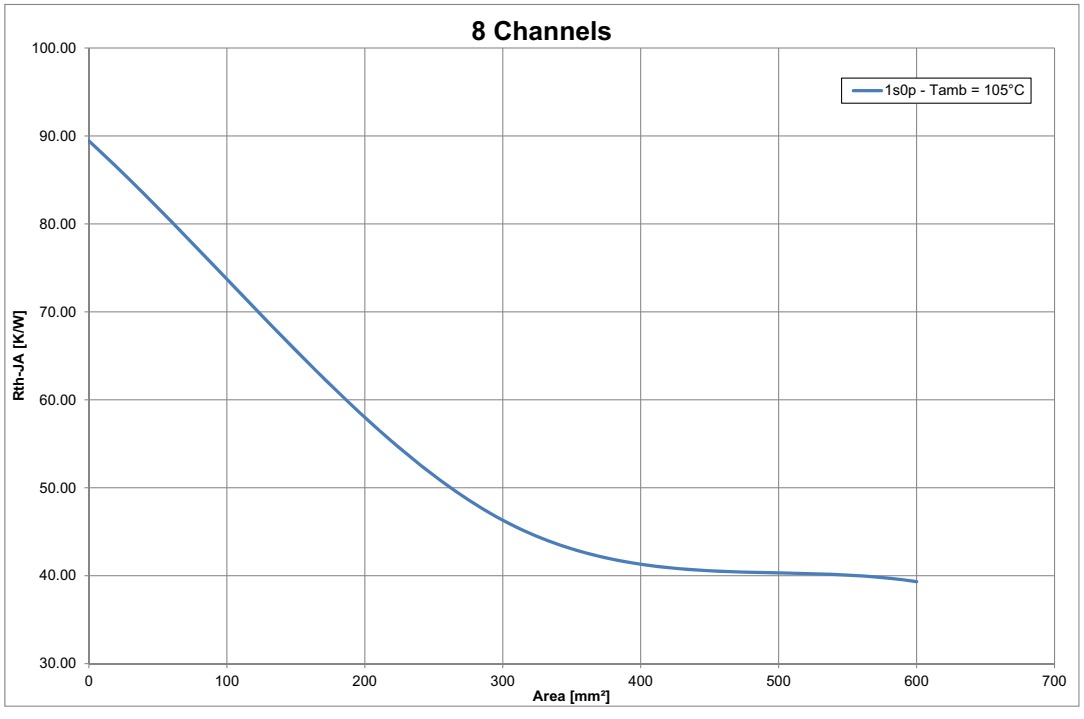


Figure 9 Typical Thermal Resistance. PCB setup 1s0p

5 Control Pins

The device has three pins (IN0, IN1 and IDLE) to control directly the device without using SPI.

5.1 Input pins

TLE75242-ESD has two input pins available. Each input pin is connected by default to one channel (IN0 to channel 2, IN1 to channel 3). Input Mapping Registers **MAPIN0** and **MAPIN1** can be programmed to connect additional or different channels to each input pin, as shown in **Figure 10**. The signals driving the channels are an OR combination between **OUT** register status, IN0 and IN1 (according to Input Mapping registers status).

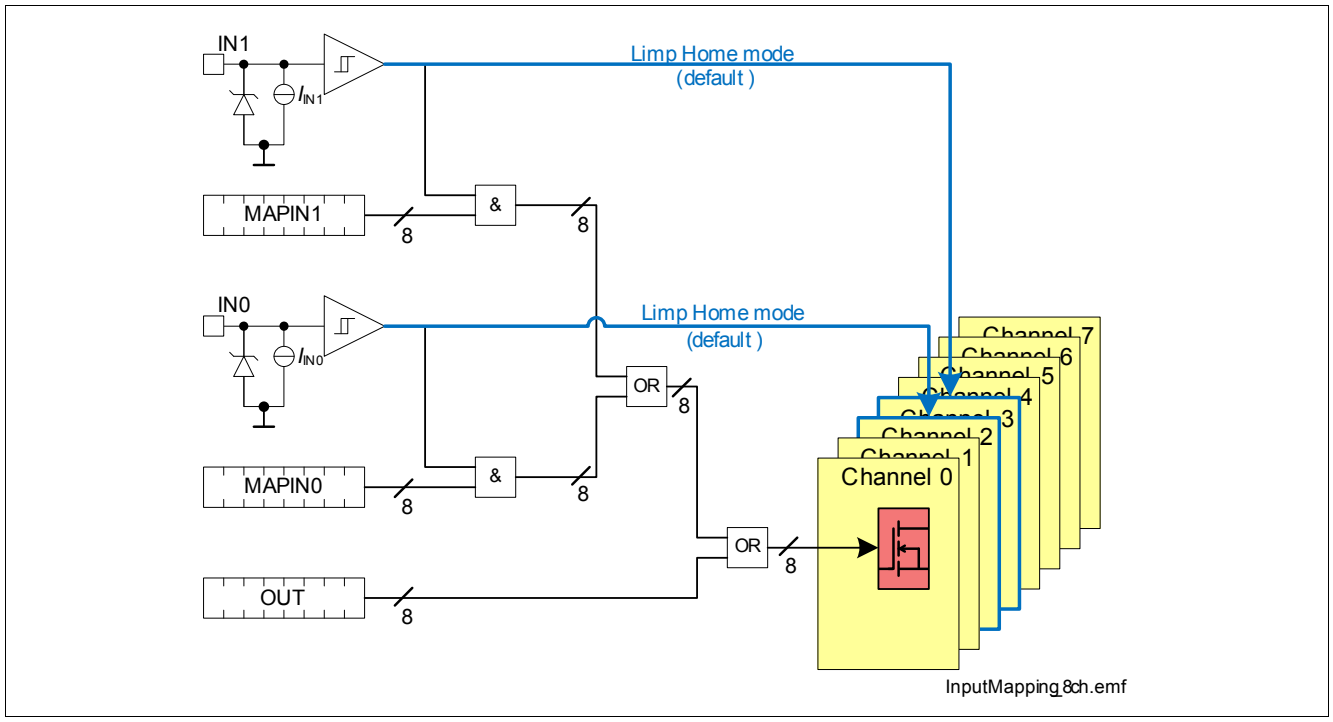


Figure 10 Input Mapping

The logic level of the input pins can be monitored via the Input Status Monitor Register (**INST**). The Input Status Monitor is operative also when TLE75242-ESD is in Limp Home mode. If one of the Input pins is set to “high” and the IDLE pin is set to “low”, the device switches into Limp Home mode and activates the channel mapped by default to the input pins. See **Chapter 6.1.5** for further details.

5.2 IDLE pin

The IDLE pin is used to bring the device into Sleep mode operation when is set to “low” and all input pins are set to “low”.When IDLE pin is set to “low” while one of the input pins is set to “high” the device enters Limp Home mode.

To ensure a proper mode transition, IDLE pin must be set for at least $t_{IDLE2SLEEP}$ (P_6.3.54, transition from “high” to “low”) or $t_{SLEEP2IDLE}$ (P_6.3.53, transition from “low” to “high”).

Setting the IDLE pin to “low” has the following consequences:

- All registers in the SPI are reset to default values
- V_{DD} and V_S Undervoltage detection circuits are disabled to decrease current consumption (if both inputs are set to “low”)

Control Pins

- No SPI communication is allowed (SO pin remains in high impedance state also when CSN pin is set to “low”) if both input pins are set to “low”

5.3 Electrical Characteristics Control Pins

Table 5 Electrical Characteristics: Control Pins

V_{DD} = 3 V to 5.5 V, V_S = 7 V to 18 V, T_J = -40 °C to +150 °C (unless otherwise specified)
Typical values: V_{DD} = 5 V, V_S = 13.5 V, T_J = 25 °C

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
IDLE pin							
L-input level	$V_{IDLE(L)}$	0		0.8	V	–	P_5.3.1
H-input level	$V_{IDLE(H)}$	2.0		5.5	V	–	P_5.3.2
L-input current	$I_{IDLE(L)}$	5	12	20	µA	V_{IDLE} = 0.8 V	P_5.3.3
H-input current	$I_{IDLE(H)}$	14	28	45	µA	V_{IDLE} = 2.0 V	P_5.3.4
Input Pins							
L-input level	$V_{IN(L)}$	0		0.8	V	–	P_5.3.5
H-input level	$V_{IN(H)}$	2.0		5.5	V	–	P_5.3.6
L-input current	$I_{IN(L)}$	5	12	20	µA	V_{IN} = 0.8 V	P_5.3.7
H-input current	$I_{IN(H)}$	14	28	45	µA	V_{IN} = 2.0 V	P_5.3.8

6 Power Supply

The TLE75242-ESD is supplied by three supply voltages:

- V_S (analog supply voltage used also for the logic)
- V_{S_HS} (analog supply voltage used as drain for channels 4, 5, 6 and 7)
- V_{DD} (digital supply voltage)

The V_S supply line is connected to a battery feed and used, in combination with V_{DD} supply, for the driving circuitry of the power stages. In situations where V_S voltage drops below V_{DD} voltage (for instance during cranking events down to 3.0 V), an increased current consumption may be observed at VDD pin.

V_S and V_{DD} supply voltages have an undervoltage detection circuit, which prevents the activation of the associated function in case the measured voltage is below the undervoltage threshold. More in detail:

- An undervoltage on both V_S and V_{DD} supply voltages prevents the activation of the power stages and any SPI communication (the SPI registers are reset)
- An undervoltage on V_{DD} supply prevents any SPI communication. SPI read/write registers are reset to default values.
- An undervoltage on V_S supply forces the TLE75242-ESD to drain all needed current for the logic from V_{DD} supply. All channels are disabled, and are enabled again as soon as $V_S \geq V_{S(OP)}$.

Figure 11 shows a basic concept drawing of the interaction between supply pins VS and VDD, the output stage drivers and SO supply line.

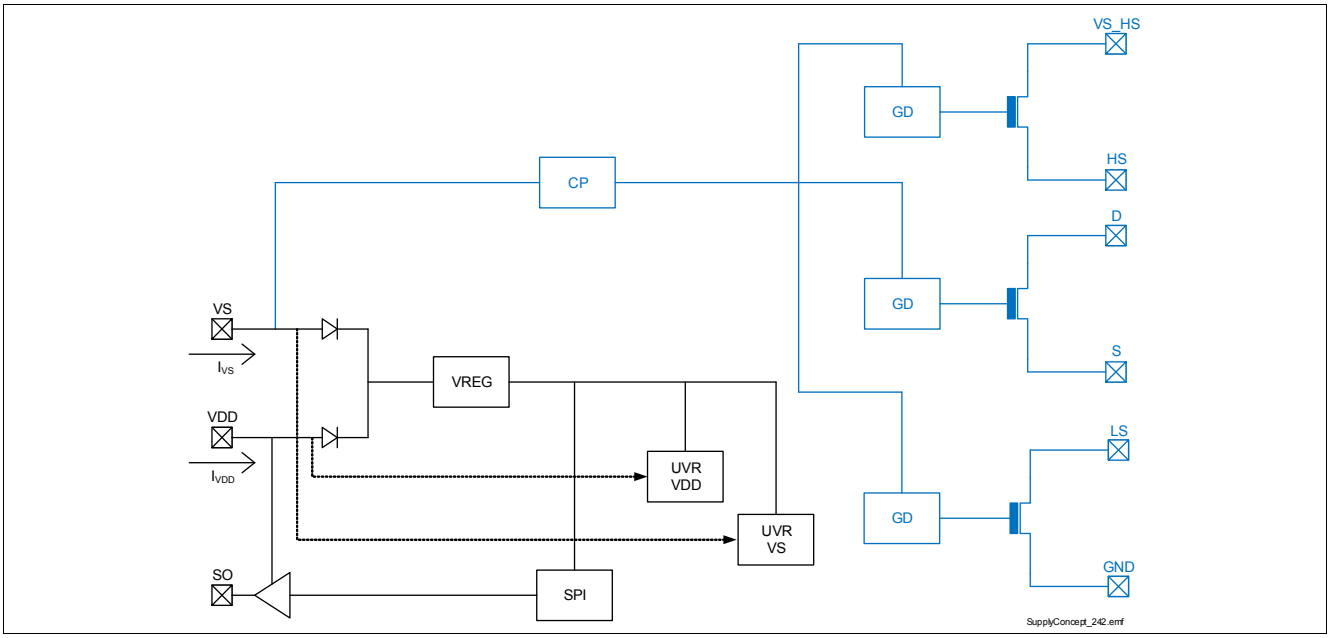


Figure 11 TLE75242-ESD Internal Power Supply concept

When 3.0 V ≤ V_S ≤ V_{DD} - V_{SDIFF} TLE75242-ESD operates in “Cranking Operative Range” (COR). In this condition the current consumption from VDD pin increases while it decreases from VS pin where the total current consumption remains within the specified limits. **Figure 12** shows the voltage levels at VS pin where the device goes in and out of COR. During the transition to and from COR operative region, I_{VS} and I_{VDD} change between values defined for normal operation and for COR operation. The sum of both current remains within limits specified in “Overall current consumption” section (see **Table 8**).

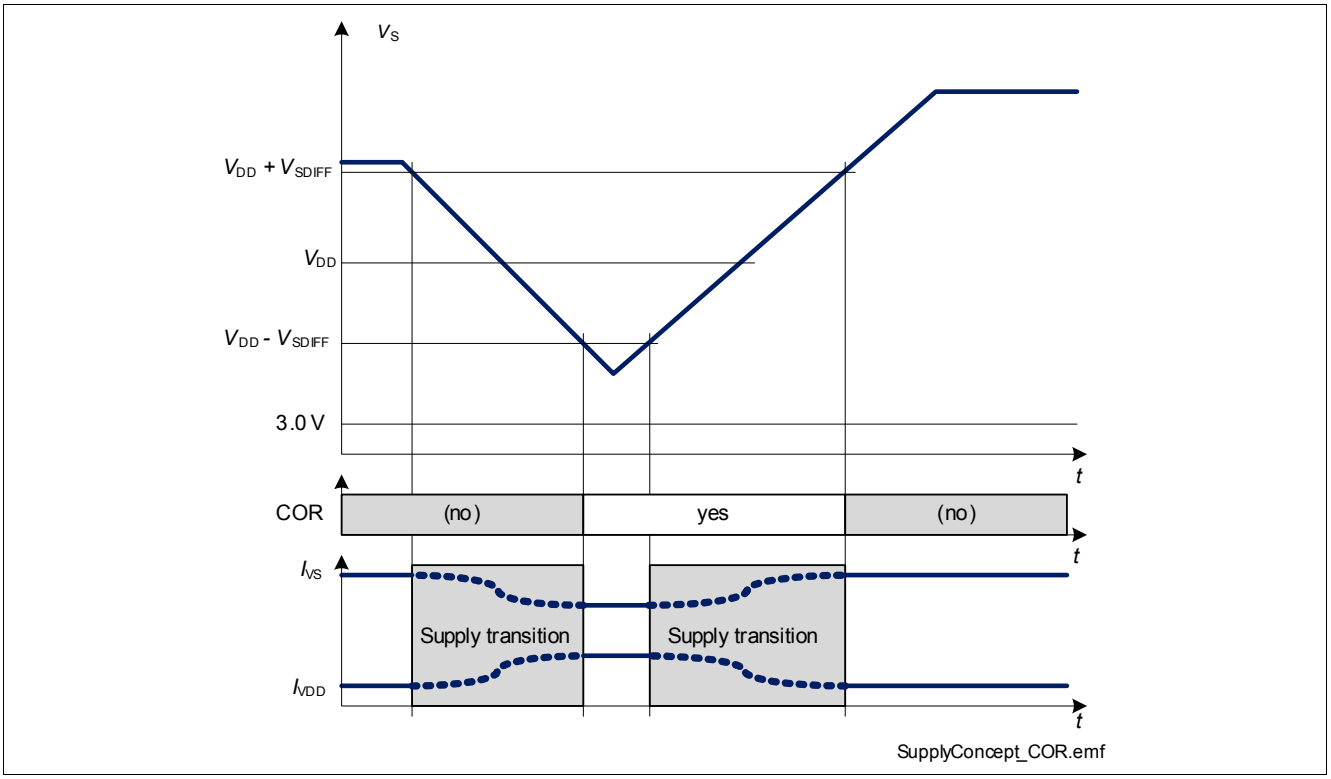


Figure 12 “Cranking Operative Range”

Furthermore, when $V_{S(UV)} \leq V_S \leq V_{S(OP)}$ it may be not possible to switch ON a channel that was previously OFF. All channels that are already ON keep their state unless they are switched OFF via SPI or via INn pins. An overview of channel behavior according to different V_S and V_{DD} supply voltages is shown in **Table 6** (the table is valid after a successful power-up, see **Chapter 6.1.1** for more details).

Table 6 Device capability as function of V_S and V_{DD}

	$V_{DD} \le V_{DD(UV)}$ ($V_{DD(UV)}$ = P_6.3.25)	$V_{DD} = V_{DD(LOP)}$ ($V_{DD(LOP)}$ = P_6.3.24)	$V_{DD} > V_{DD(LOP)}$
$V_S \le 3.0$ V 3.0 V = $V_{S(UV),max}$ (P_6.3.1)	channels cannot be controlled	channels cannot be controlled	channels cannot be controlled
	SPI registers reset	SPI registers available	SPI registers available
	SPI communication not available (f_{SCLK} = 0 MHz)	SPI communication possible (f_{SCLK} = 1 MHz) (P_10.4.34)	SPI communication possible (f_{SCLK} = 5 MHz) (P_10.4.22)
	Limp Home mode not available	Limp Home mode available (channels are OFF)	Limp Home mode available (channels are OFF)
3.0 V < $V_S \le V_{S(OP)}$ ($V_{S(OP)}$ = P_6.3.2)	channels cannot be controlled by SPI	channels can be switched ON and OFF (SPI control)[1] ($R_{DS(ON)}$ deviations possible)	channels can be switched ON and OFF (SPI control)[1] ($R_{DS(ON)}$ deviations possible)
	SPI registers reset	SPI registers available	SPI registers available
	SPI communication not available (f_{SCLK} = 0 MHz)	SPI communication possible (f_{SCLK} = 1 MHz) (P_10.4.34)	SPI communication possible (f_{SCLK} = 5 MHz) (P_10.4.22)
	Limp Home mode available[1] ($R_{DS(ON)}$ deviations possible)	Limp Home mode available[1] ($R_{DS(ON)}$ deviations possible)	Limp Home mode available[1] ($R_{DS(ON)}$ deviations possible)
$V_S \ge V_{S(OP)}$	channels cannot be controlled by SPI	channels can be switched ON and OFF (small $R_{DS(ON)}$ dev. possible when $V_S = V_{S(EXT,LOW)}$)	channels can be switched ON and OFF (small $R_{DS(ON)}$ dev. possible when $V_S = V_{S(EXT,LOW)}$)
	SPI registers reset	SPI registers available	SPI registers available
	SPI communication not available (f_{SCLK} = 0 MHz)	SPI communication possible (f_{SCLK} = 5 MHz) (P_10.4.22)	SPI communication possible (f_{SCLK} = 5 MHz) (P_10.4.22)
	Limp Home mode available (small $R_{DS(ON)}$ dev. possible when $V_S = V_{S(EXT,LOW)}$)	Limp Home mode available (small $R_{DS(ON)}$ dev. possible when $V_S = V_{S(EXT,LOW)}$)	Limp Home mode available (small $R_{DS(ON)}$ dev. possible when $V_S = V_{S(EXT,LOW)}$)

1) undervoltage condition on V_S must be considered - see **Chapter 6.2.1** for more details

6.1 Operation Modes

TLE75242-ESD has the following operation modes:

- Sleep mode
- Idle mode
- Active mode
- Limp Home mode

The transition between operation modes is determined according to following levels and states:

- logic level at IDLE pin
- logic level at INn pins
- **OUT.OUTn** bits state
- **HWCR.ACT** bit state

The state diagram including the possible transitions is shown in **Figure 13**. The behaviour of TLE75242-ESD as well as some parameters may change in dependence from the operation mode of the device. Furthermore, due to the undervoltage detection circuitry which monitors V_S and V_{DD} supply voltages, some changes within the same operation mode can be seen accordingly.

The operation mode of the TLE75242-ESD can be observed by:

- status of output channels
- status of SPI registers
- current consumption at VDD pin (I_{VDD})
- current consumption at VS pin (I_{VS})

The default operation mode to switch ON the loads is Active mode. If the device is not in Active mode and a request to switch ON one or more outputs comes (via SPI or via Input pins), it will switch into Active or Limp Home mode, according to IDLE pin status. Due to the time needed for such transitions, output turn-on time t_{ON} will be extended due to the mode transition latency.

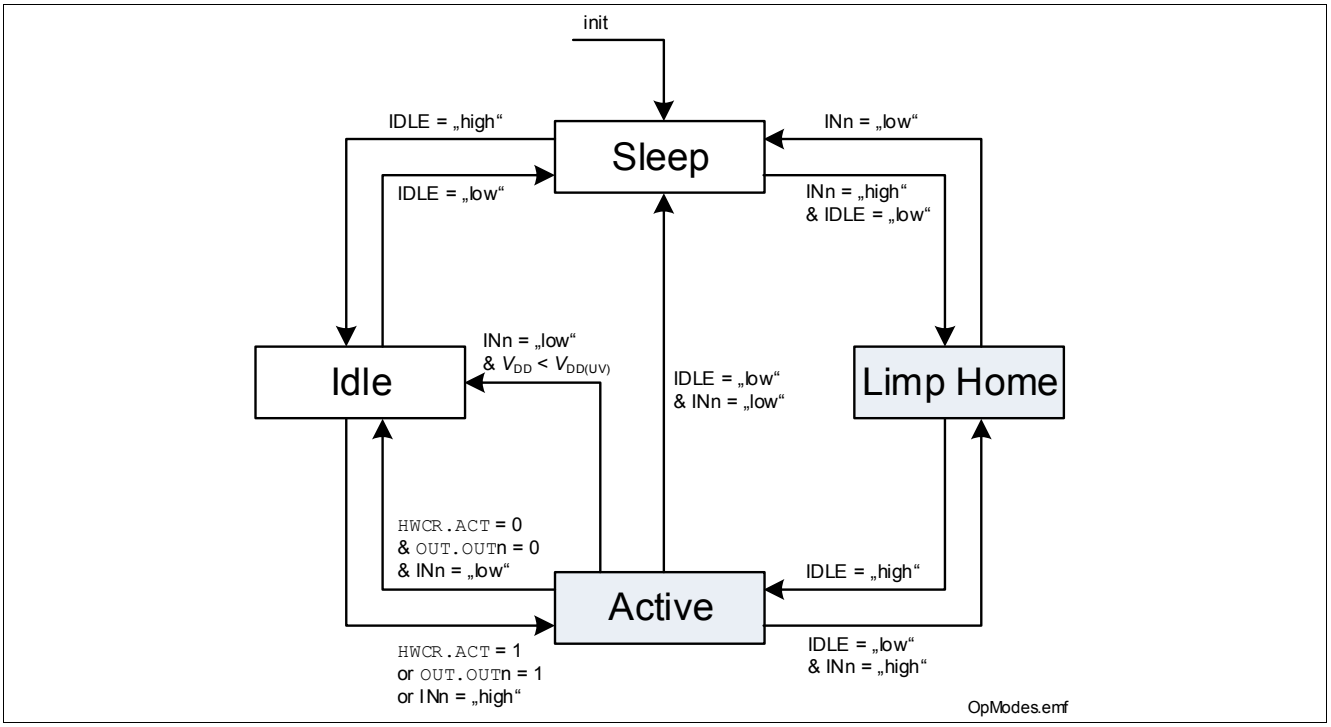


Figure 13 Operation Mode state diagram

Table 7 shows the correlation between device operation modes, V_S and V_{DD} supply voltages, and state of the most important functions (channels operativity, SPI communication and SPI registers).

Table 7 Device function in relation to operation modes, V_S and V_{DD} voltages

Operation Mode	Function	Undervoltage condition on V_S [1] $V_{DD} \le V_{DD(UV)}$	Undervoltage condition on V_S $V_{DD} > V_{DD(UV)}$	V_S not in undervoltage $V_{DD} \le V_{DD(UV)}$	V_S not in undervoltage $V_{DD} > V_{DD(UV)}$
Sleep	Channels	not available	not available	not available	not available
	SPI comm.	not available	not available	not available	not available
	SPI registers	reset	reset	reset	reset
Idle	Channels	not available	not available	not available	not available
	SPI comm.	not available	✓	not available	✓
	SPI registers	reset	✓	reset	✓
Active	Channels	not available	not available	✓ (IN pins only)	✓
	SPI comm.	not available	✓	not available	✓
	SPI registers	reset	✓	reset	✓
Limp Home	Channels	not available	not available	✓ (IN pins only)	✓ (IN pins only)
	SPI comm.	not available	✓ (read-only)	not available	✓ (read-only)
	SPI registers	reset	✓ (read-only)[2]	reset	✓ (read-only)[2]

1) see **Chapter 6.2.1** for more details

2) see **Chapter 6.1.5** for a detailed overview

6.1.1 Power-up

The Power-up condition is satisfied when one of the supply voltages (V_S or V_{DD}) is applied to the device and the INn or IDLE pins are set to “high”. If V_S is above the threshold $V_{S(OP)}$ or if V_{DD} is above the threshold $V_{DD(LOP)}$ the internal power-on signal is set.

6.1.2 Sleep mode

When TLE75242-ESD is in Sleep mode, all outputs are OFF and the SPI registers are reset, independently from the supply voltages. The current consumption is minimum. See parameters $I_{VDD(SLEEP)}$ and $I_{VS(SLEEP)}$, or parameter I_{SLEEP} for the whole device.

6.1.3 Idle mode

In Idle mode, the current consumption of the device can reach the limits given by parameters $I_{VDD(IDLE)}$ and $I_{VS(IDLE)}$, or by parameter I_{IDLE} for the whole device. The internal voltage regulator is working. Diagnosis functions are not available. The output channels are switched OFF, independently from the supply voltages. When V_{DD} is available, the SPI registers are working and SPI communication is possible. In Idle mode the **ERRn** bits are not cleared for functional safety reasons.

6.1.4 Active mode

Active mode is the normal operation mode of TLE75242-ESD when no Limp Home condition is set and it is necessary to drive some or all loads. Voltage levels of V_{DD} and V_S influence the behavior as described at the beginning of **Chapter 6**. Device current consumption is specified with $I_{VDD(ACTIVE)}$ and $I_{VS(ACTIVE)}$ (I_{ACTIVE} for the whole device). The device enters Active mode when IDLE pin is set to “high” and one of the input pins is set to “high” or one **OUT.OUTn** bit is set to “1”. If **HWCR.ACT** is set to “0”, the device returns to Idle mode as soon as all inputs pins are set to “low” and **OUT.OUTn** bits are set to “0”. If **HWCR.ACT** is set to “1”, the device remains in Active mode independently of the status of input pins and **OUT.OUTn** bits. An undervoltage condition on V_{DD} supply brings the device into Idle mode, if all input pins are set to “low”. Even if the registers **MAPIN0** and **MAPIN1** are both set to “00_H” but one of the input pins INn is set to “high”, the device goes into Active mode.

6.1.5 Limp Home mode

TLE75242-ESD enters Limp Home mode when IDLE pin is “low” and one of the input pins is set to “high”, switching ON the channel connected to it. SPI communication is possible but only in read-only mode (SPI registers can be read but cannot be written). More in detail:

- **UVRVS** and **LOPVDD** are set to “1”
- **MODE** bits are set to “01_B” (Limp Home mode)
- **TER** bit is set to “1” on the first SPI command after entering Limp Home mode. Afterwards it works normally
- **OLOFF** bits is set to “0”
- **ERRn** bits work normally
- **DIAG_OSM.OUTn** bits can be read and work normally
- All other registers are set to their default value and cannot be programmed as long as the device is in Limp Home mode

See **Table 6** for a detailed overview of supply voltage conditions required to switch ON channels 2 and 3 during Limp Home. All other channels are OFF.

A transmission of SPI commands during transition from Active to Limp Home mode or Limp Home to Active mode may result in undefined SPI responses.

6.1.6 Definition of Power Supply modes transition times

The channel turn-ON time is as defined by parameter t_{ON} when TLE75242-ESD is in Active mode or in Limp Home mode. In all other cases, it is necessary to add the transition time required to reach one of the two aforementioned Power Supply modes (as shown in **Figure 14**).

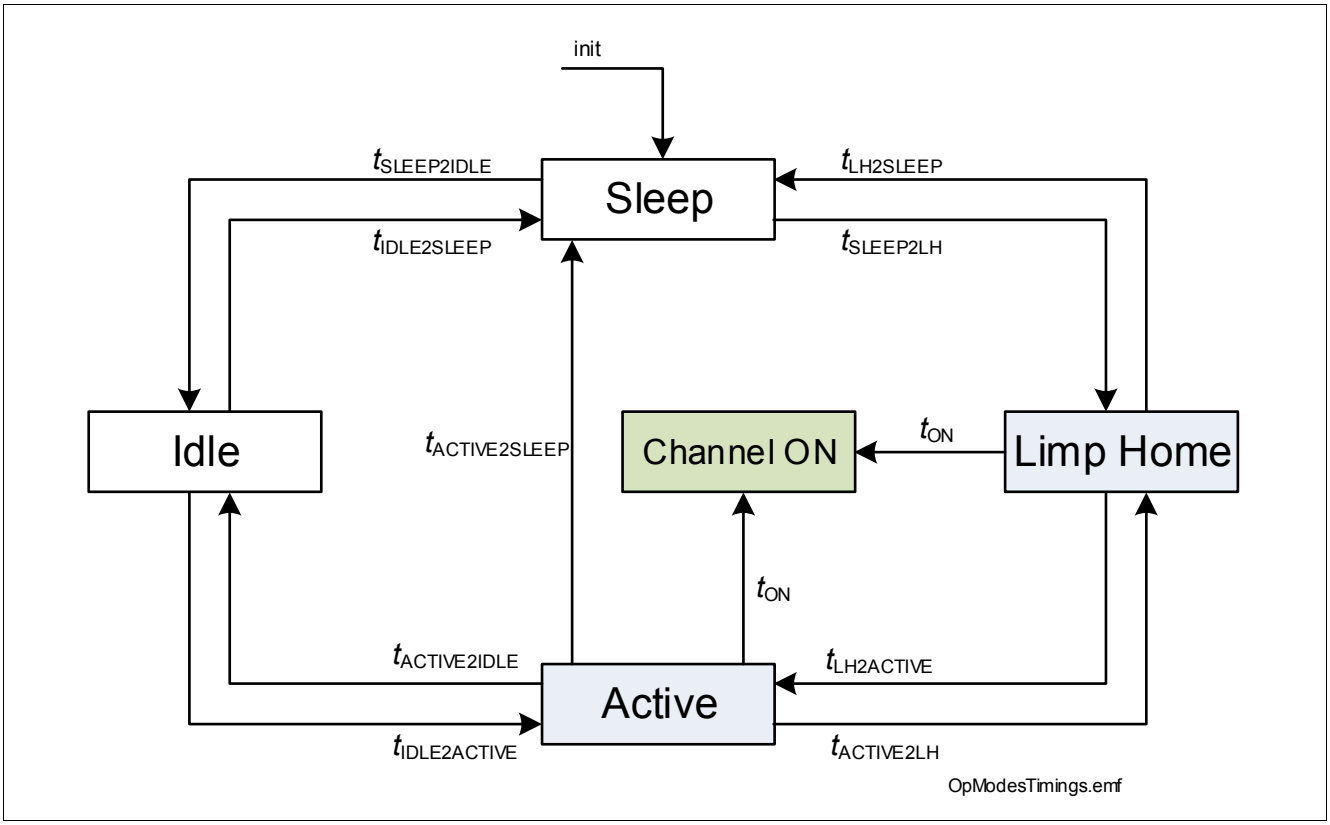


Figure 14 Transition Time diagram

6.2 Reset condition

One of the following 3 conditions resets the SPI registers to the default value:

- V_{DD} is not present or below the undervoltage threshold $V_{DD(UV)}$
- IDLE pin is set to “low”
- a reset command (**HWCR.RST** set to “1”) is executed
  - **ERRn** bits are not cleared by a reset command (for functional safety)
  - **UVRVS** and **LOPVDD** bits are cleared by a reset command

In particular, all channels are switched OFF (if there are no input pin set to “high”) and the Input Mapping configuration is reset.

6.2.1 Undervoltage on V_S

Between $V_{S(UV)}$ and $V_{S(OP)}$ the undervoltage mechanism is triggered. If the device is operative and the supply voltage drops below the undervoltage threshold $V_{S(UV)}$, the logic set the bit **UVRVS** to “1”. As soon as the supply voltage VS is above the minimum voltage operative threshold $V_{S(OP)}$, the bit **UVRVS** is set to “0” after the first Standard Diagnosis readout. Undervoltage condition on VS influences the status of the channels, as described in **Table 6**. **Figure 15** sketches the undervoltage behavior (the “V_S - V_{DS}” line refers to a channel which is programmed to be ON).

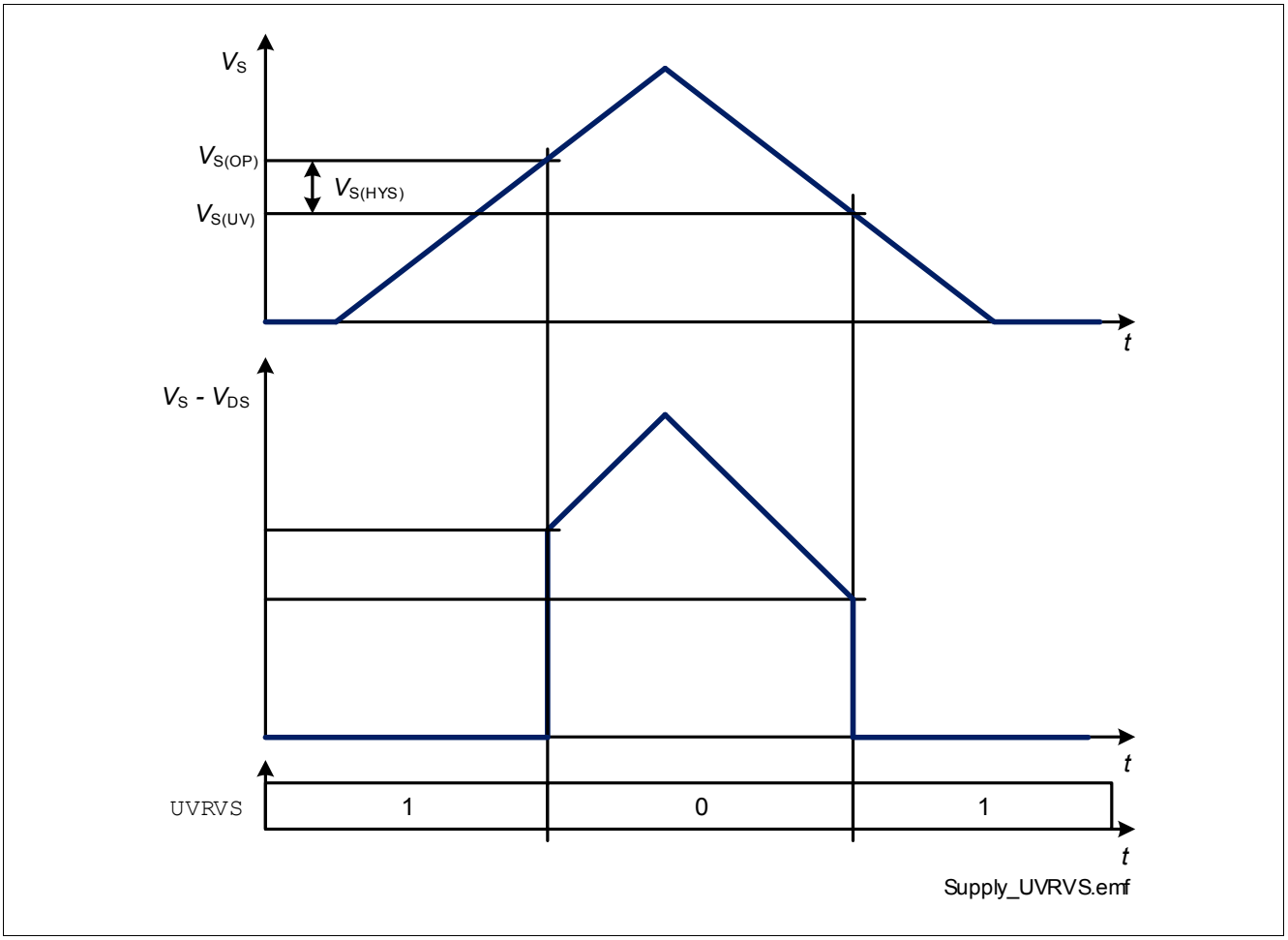


Figure 15 V_S Undervoltage Behavior

6.2.2 Low Operating Power on V_{DD}

When V_{DD} supply voltage is in the range indicated by $V_{DD(LOP)}$, the bit **LOPVDD** is set to “1”. As soon as V_{DD} > $V_{DD(LOP)}$ the bit **LOPVDD** is set to “0” after the first Standard Diagnosis readout.

If V_{DD} supply voltage is not present, a voltage applied to pins CSN or SO can supply the internal logic (not recommended in normal operation due to internal design limitations).