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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

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Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



TLE7824G

Integrated double low-side switch, high-side/LED driver, hall supply, wake-up inputs and LIN communication with embedded MCU (24kB Flash)

Automotive Power



Never stop thinking

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TLE7824G



1 Overview

Relay Driver - System Basis Chip

- Low-Dropout Voltage Regulator (LDO)
- LIN Transceiver
- Standard 16-bit SPI-Interface
- 2 × Low-Side Switches, e.g. as Relay Driver
- 2 × Supply e.g. for Hall Sensor Supply / LED Driver
- 5 × High-Voltage Wake-Up Inputs
- Programmable. Window Watchdog & Power Saving Modes
- Power-On and Undervoltage Reset Generator
- Overtemperature Protection
- Short Circuit Protection



PG-DSO-28-38

8-bit Microcontroller

- Compatible to 8051 μ C Core
- Two clocks per machine cycle
- 12kByte Boot ROM for test and Flash routines
- LIN Bootloader (Boot ROM)
- 256 Byte RAM / 1.5 kByte XRAM
- 24kByte Flash Memory for Program Code & Data
- On-Chip Oscillator
- Power Saving Modes (slow-down & idle mode)
- Programmable Watchdog Timer
- 10-bit A/D Converter, e.g. for Temperature & V_{bat} -Measurement
- Three 16-bit Timers & Capture/Compare Unit
- General Purpose I/Os, e.g. with PWM Functionality
- On-Chip Debug Support (JTAG)
- UART and Synchronous Serial Channel (SSC respective SPI)
- Multiply-Divide-Unit (MDU)

General Characteristics

- Package PG-DSO-28-38
- Temperature Range T_j : -40 °C up to 150 °C
- Green Package (RoHS compliant)
- AEC Qualified

Type	Package	Marking
TLE7824G	PG-DSO-28-38	TLE7824G

Description

This single-packaged solution incorporates an 8-bit state-of-the-art microcontroller compatible to the standard 8051 core with On-Chip Debug Support (OCDS), and a System-Basis-Chip (SBC). The SBC is equipped with LIN transceiver, low-dropout voltage regulator (LDO) as well as two low-side switches (relay driver) and a high-side driver e.g. for driving LEDs. An additional supply, e.g. to supply hall sensors (TLE 4966) is also available.

For Micro Controller Unit (MCU) supervision and additional protection of the circuit a programmable window watchdog circuit with a reset feature, supply voltage supervision and integrated temperature sensor is implemented on the SBC.

Microcontroller and LIN module offer low power modes in order to support terminal 30 connected automotive applications. A wake-up from the low power mode is possible via a LIN bus message or wake-up inputs.

This integrated circuit is realized as Multi-Chip-Module (MCM) in a PG-DSO-28-38 package, and is designed to withstand the severe conditions of automotive and industrial applications.

Note: A detailed description of the 8-bit microcontroller XC885 can be found in a dedicated User's Manual and Data Sheet.

2 Block Diagram

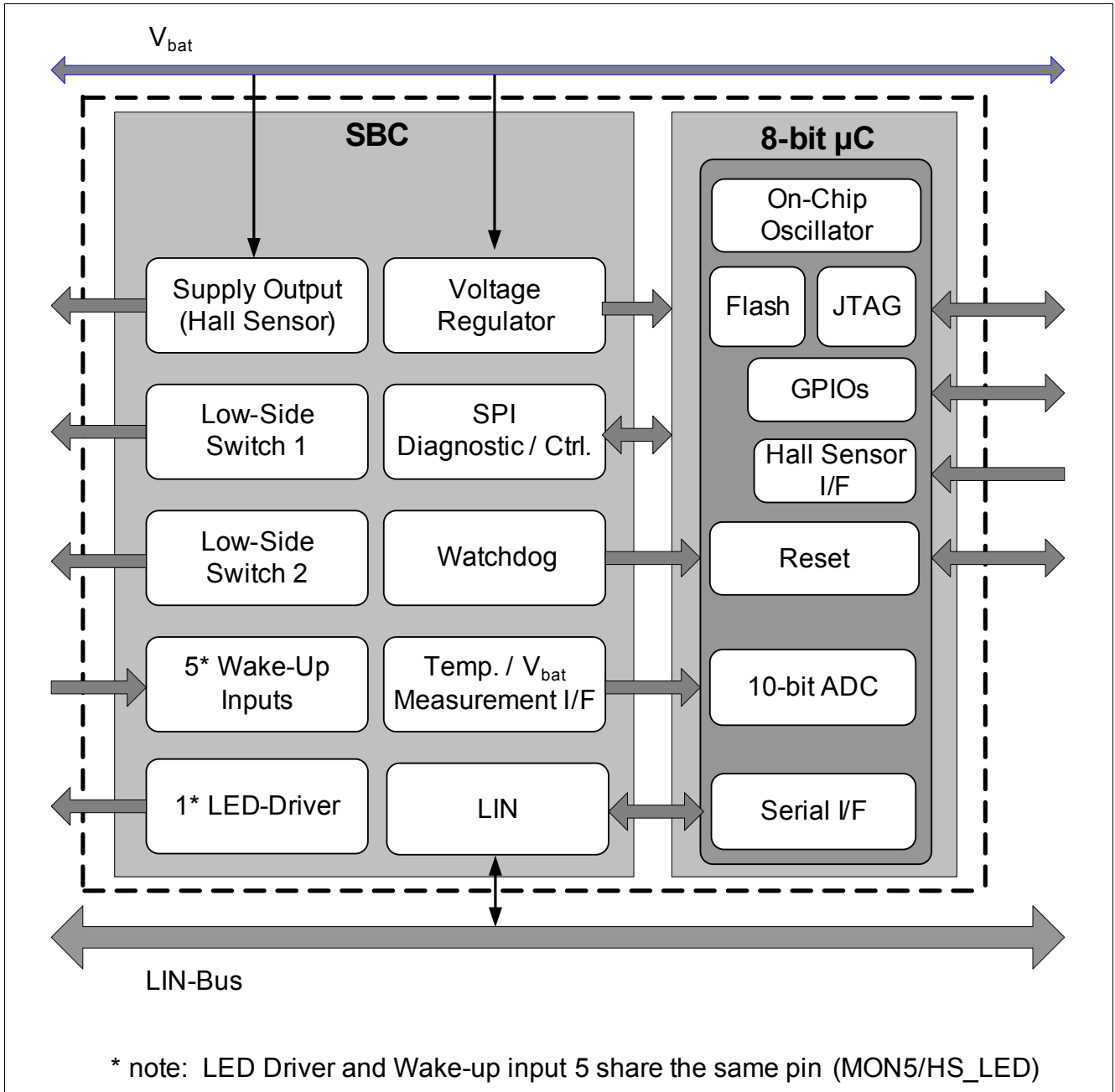


Figure 1 Functional Block Diagram (Module Overview)

3 Pin Definitions and Functions

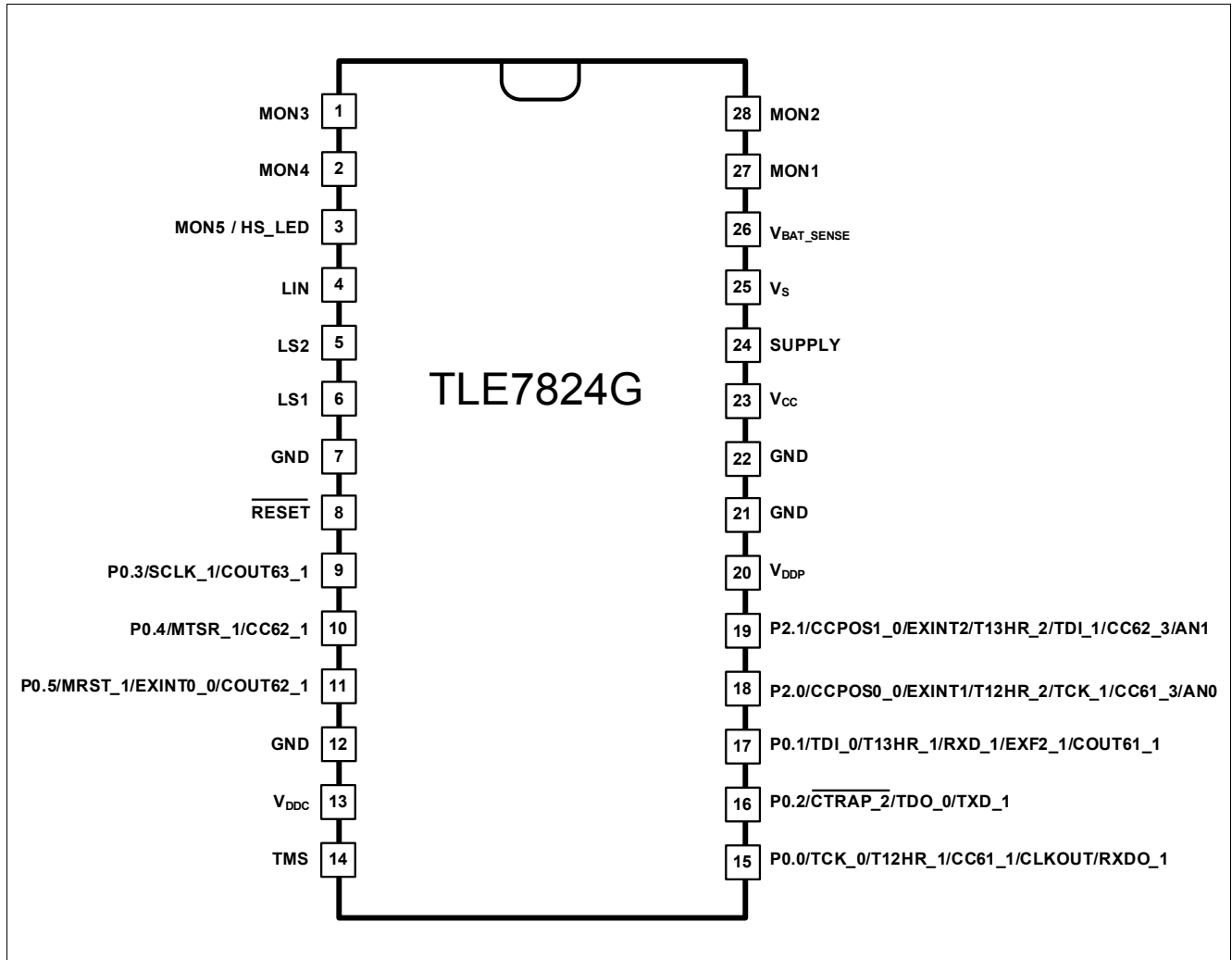


Figure 2 Pin Configuration

Pin No.	Symbol	Function
27 28 1 2 3	MON1, MON2, MON3, MON4, MON5/HS_LED	Monitoring / Wake-Up Inputs; bi-level sensitive inputs used to monitor signals for example coming from an external switch panel MON5 is combined with an LED Driver output
25	V _S	Power Supply Input; recommendation to block to GND directly at the IC with ceramic capacitor (ferrite bead for better EMC behavior)
26	V _{BAT_SENSE}	Battery Voltage Sense Input; for connection to terminal 30 with external serial resistor
23	V _{CC}	Voltage Regulator Output; for internal supply (5 V); to stabilize block to GND with an external capacitor; for external loads up to the specified value (see Table 13 "Operating Range" on Page 35)
8	RESET	Reset; output of SBC; "low active"; input for μController

Pin Definitions and Functions

Pin No.	Symbol	Function
4	LIN	LIN Bus ; Bus Line for the LIN interface, according to ISO 9141 and LIN specification 1.3 and 2.0
24	SUPPLY	Supply Output ; e.g. for Hall Sensor; controlled via SPI
5	LS2	Low Side Switch 2 Output ; controlled via SPI
6	LS1	Low Side Switch 1 Output ; controlled via SPI
9	P0.3	General Purpose I/O with PWM Functionality (alternate function: SCK, see XC885 data sheet)
10	P0.4	General Purpose I/O with Capture and PWM Functionality (alternate function: MTSR, see XC885 data sheet)
11	P0.5	General Purpose I/O with PWM Functionality (alternate function: MRST and EXINT0, see XC885 data sheet)
13	V_{DDC}	Voltage Regulator Output for μController Core (2.5 V) ; for connection of block capacitor to GND; not to be used for external loads
14	TMS	Test Mode Select (JTAG)
15	P0.0 [TCK_0]	General Purpose I/O ; see XC885 data sheet (alternate function: JTAG Clock Input)
16	P0.2 [TDO_0]	General Purpose I/O ; see XC885 data sheet (alternate function: JTAG Serial Data Output; RxD1)
17	P0.1 [TDI_0]	General Purpose I/O ; see XC885 data sheet (alternate function: JTAG Serial Data Input; TxD1)
18	P2.0	General Purpose Input (digital/analog) with Capture Functionality ; e.g. for Hall Sensor (alternate function: EXINT1)
19	P2.1	General Purpose Input (digital/analog) with Capture Functionality ; e.g. for Hall Sensor (alternate function: EXINT2)
20	V_{DDP}	Voltage Supply Input for μController I/Os (5 V) ; to be connected with V_{CC} pin
–	RxD	LIN Transceiver Data Output ; according to the ISO 9141 and LIN specification 1.3 and 2.0; LOW in dominant state; connected to μC General Purpose Input P1.0
–	TxD	LIN Transceiver Data Input ; according to ISO 9141 and LIN specification 1.3 and 2.0; TxD has an internal pull-up; connected to μC General Purpose Input P1.1
–	DI	SPI Data Input ; receives serial data from the control device; serial data transmitted to DI is a 16-bit control word with the Least Significant Bit (LSB) transferred first; the input has a pull-down and requires CMOS logic level inputs; DI will accept data on the falling edge of CLK-signal; connected to μC General Purpose Input P1.3
–	DO	SPI Data Output ; this tri-state output transfers diagnosis data to the control device; the output will remain in the high-impedance state unless the device is selected by a low on Chip-Select-Not (CSN); connected to μC General Purpose Input P1.4 (EXTINT0_1)
–	CLK	SPI Clock Input ; clock input for shift register; CLK has an internal pull-down and requires CMOS logic level inputs; connected to μC General Purpose Input P1.2
–	CSN	SPI Chip Select Not Input ; CSN is an active low input; serial communication is enabled by pulling the CSN terminal low; CSN input should only be transitioned when CLK is low; CSN has an internal pull-up and requires CMOS logic level inputs; connected to μC General Purpose Input P1.5
–	V_{AREF}	Voltage Reference for ADC

Pin Definitions and Functions

Pin No.	Symbol	Function
–	V_A	ADC Measurement Output (analog); for chip temperature and battery voltage measurement
–	$\overline{\text{ERR}}$	Error Pin; bi-directional signal; ERR has an internal pull-up; low-active; connected to μC General Purpose Input P3.6 (RSTOUT)
7	GND	Ground; including GND for LSx and LIN
12		Ground; corresponding GND to V_{DDC}
21		Ground; V_{AGND} (ADC) & corresponding GND to V_{DDP}
22		Ground; V_{AGND} (ADC); also GND for LDO and Measurement Interface

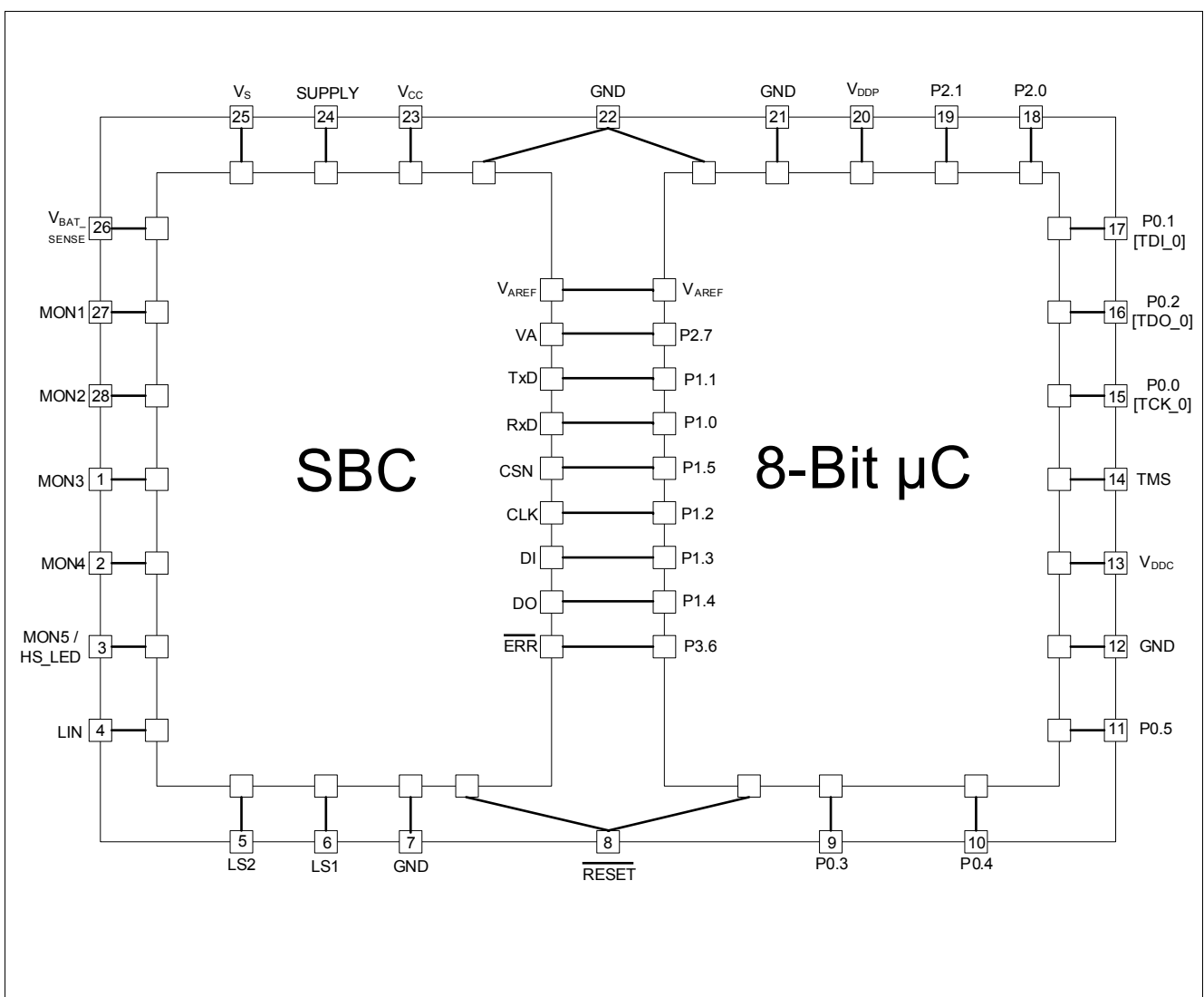


Figure 3 Pinout and Module Interconnects

4 Operating Modes

The TLE7824G incorporates several SBC operating modes, that are listed in [Table 1](#).

Table 1 SBC Operating Modes

Functional Block	SBC Standby Mode	SBC Active Mode	SBC Stop Mode	SBC Sleep Mode
V_{CC} , 5 V, LDO	ON	ON	ON	OFF
Window Watchdog	ON	ON	OFF / ON ¹⁾²⁾	OFF / ON ²⁾
Monitoring / wake-up pins	ON / OFF ³⁾	SPI-controlled	ON / OFF ³⁾	ON / OFF ³⁾
LS1,LS2 -switch	OFF	SPI-controlled	OFF	OFF
Supply Output	ON / OFF ³⁾	SPI-controlled	ON / OFF ³⁾	OFF
HS-LED	OFF	SPI-controlled	OFF	OFF
16-bit SPI	ON	ON	ON	OFF
LIN wake-up via bus message	ON	OFF	ON	ON
LIN Transmit	OFF	ON	OFF	OFF
LIN Receive	OFF	ON	OFF	OFF
RxD	Active low wake-up interrupt	L / H	Active low wake-up interrupt	Active low wake-up interrupt
Measurement I/F	OFF	SPI-controlled	OFF	OFF
V_{AREF}	OFF	ON (2.5V)	OFF	OFF
Voltage Monitoring at V_S and V_{BAT}	OFF	ON	OFF	OFF

1) WD "off" when voltage-regulator output current below "watchdog disable current threshold"

2) WD default "off" in SBC Stop / Sleep Mode; WD can be active in order to generate period wake-ups of SBC

3) "ON / OFF" state is inherited from previous operating mode ("OFF" after POR and RESET)

The System-Basis-Chip (SBC) offers several operation modes that are controlled via three mode select bits MS0, MS1 and MS2 within the SPI: SBC Active, Sleep and Stop mode, as well as LIN Receive-Only mode.

An overview of the operating modes and the operating mode transitions is indicated in [Figure 4](#) below.

Note: It is possible to directly change from Stand-By to Stop or Sleep mode, however this might result in a higher current consumption (~200µA). The higher current consumption will occur in case of a power up and in case of a LIN wake-up from Stop and Sleep mode. To avoid this conditions its recommended to prior set Active mode before changing to Stop or Sleep mode.

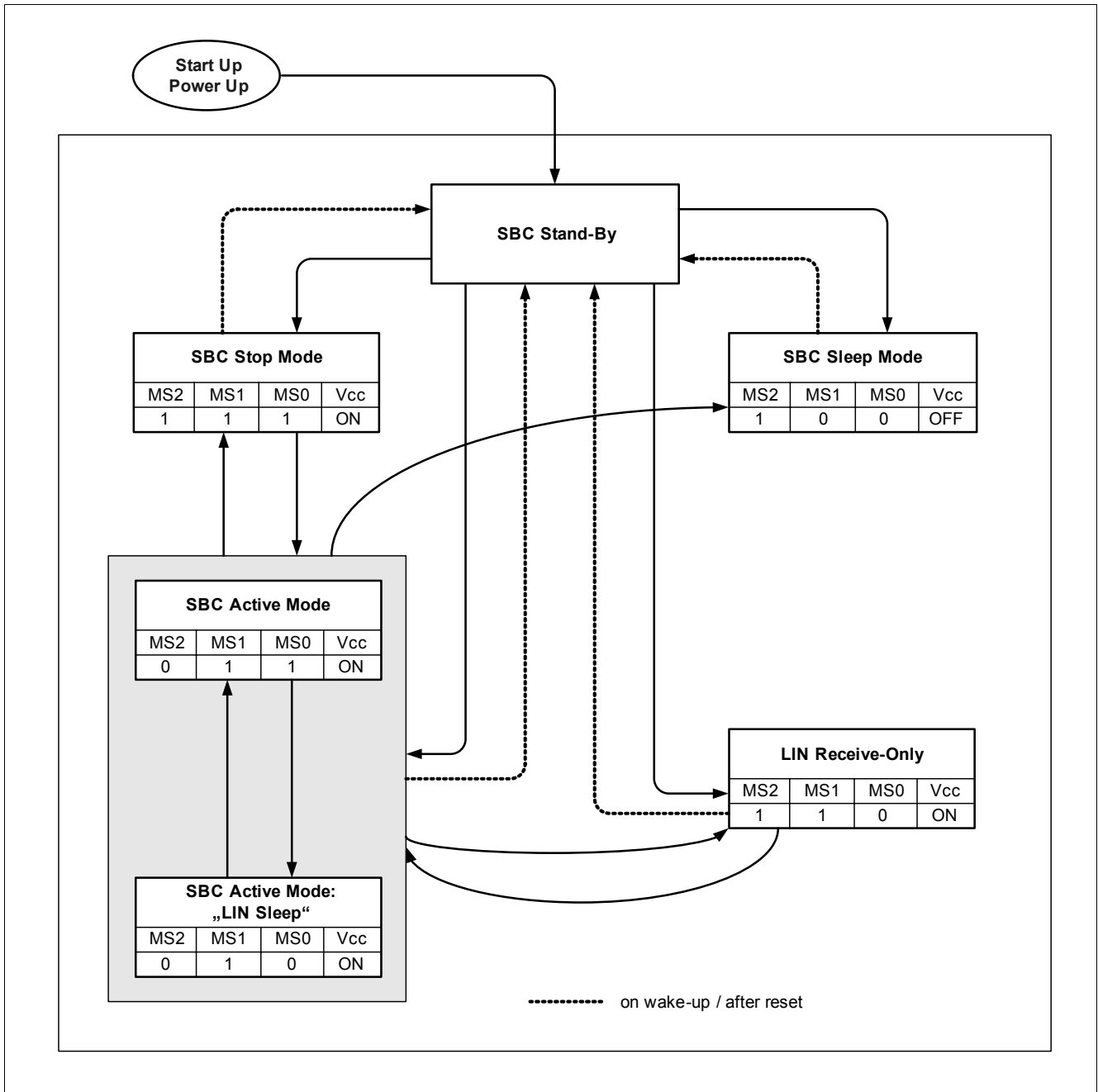


Figure 4 State Diagram "SBC Operation Modes"

4.1 SBC Standby Mode

After powering-up the SBC or wake-up from power-saving, it automatically starts-up in **SBC Standby Mode**, waiting for the microcontroller to finish its startup and initialization sequences. However, this mode cannot be selected via SPI command. From this transition mode the SBC can be switched via SPI command into the desired operating mode. All modes are selected via SPI bits or certain operation conditions, e.g. external wake-up events.

4.2 SBC Active Mode

The **SBC Active Mode** is used to transmit and receive LIN messages and provides the sub-mode "LIN Sleep".

4.3 SBC Active Mode “LIN Sleep”

In **SBC Active Mode “LIN Sleep”** the SBC’s current consumption is reduced by disabling the LIN transceiver. This also means that the internal pull-up resistor of the LIN transceiver is turned off in SBC Active Mode “LIN Sleep”. During this mode the LIN transceiver remains its wake-up capability in order to react on a remote frame or wake-up pulse (specified in LIN Specification V2.0) from the master node or other slave nodes. In case of a wake-up event via LIN message the (internal) RxD is pulled “low” and the “bus wake-up bit” within the SPI status word is set. However, the LIN transceiver needs to be activated by switching to “SBC Active Mode”.

4.4 LIN Receive-Only Mode (“LIN RxD-Only”)

The **LIN Receive-Only Mode (“LIN RxD-Only”)** is designed for a special test procedure to check the bus connections. **Figure 5** shows a network consisting of 5 nodes. Node 1 is the LIN master node, the others are LIN slave nodes. If the connection between node 1 and node 3 shall be tested, the nodes 2, 4 and 5 are switched into LIN Receive-Only Mode. Node 1 and node 3 are in Active Mode. If node 1 sends a message (“remote frame”), node 3 is the only node which is physically able to reply to the remote frame. The other nodes have their outputs drivers disabled.

The main difference between the **SBC Active Mode** and the **LIN Receive-Only Mode** is that the LIN transmit stage is automatically turned-off in LIN Receive-Only-Mode. However, the LIN receiver is still active in both modes.

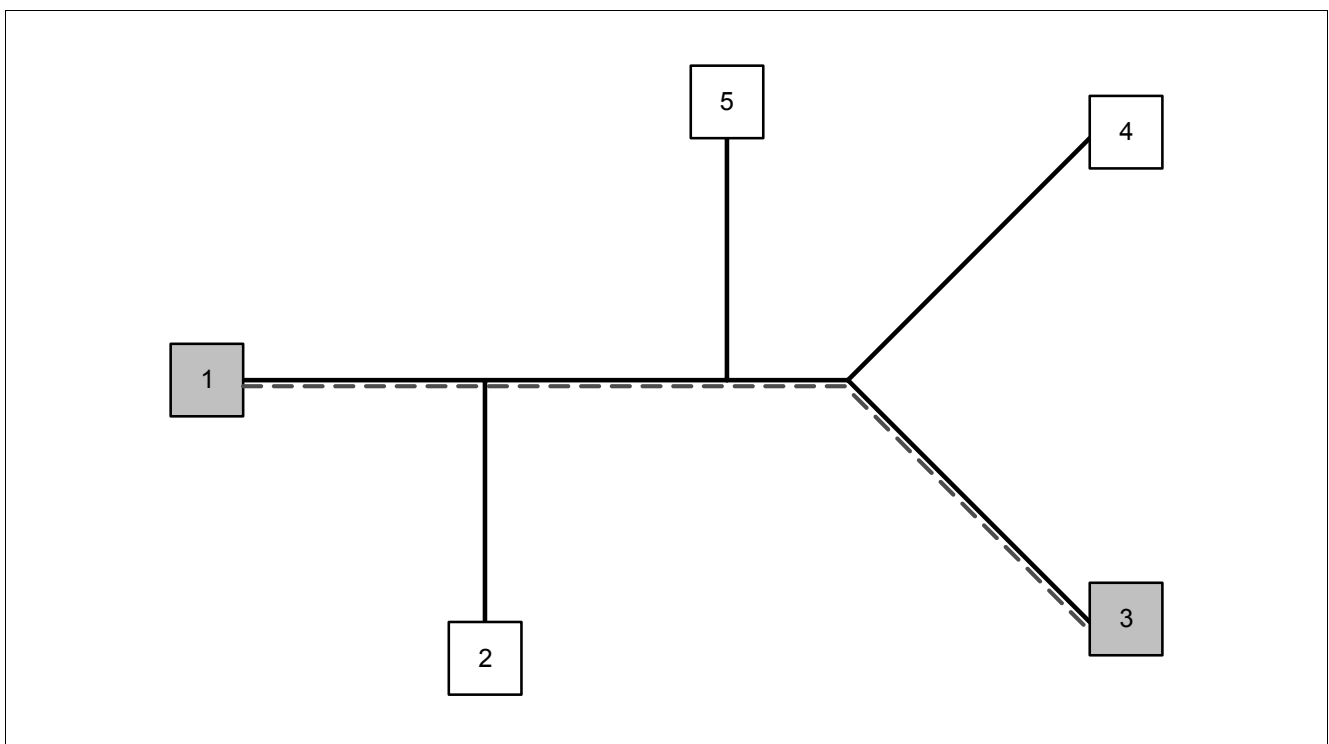


Figure 5 Network Diagram “LIN Receive-Only Mode”

4.5 Power Saving Modes

4.5.1 SBC Sleep Mode

During **SBC Sleep Mode** (see **Figure 6**), the lowest power consumption is achieved, by having its main voltage regulator switched-off. As the microcontroller cannot be supplied, the integrated window watchdog can be disabled in Sleep Mode via a dedicated SPI control bit. However, it can be turned-on for periodically waking-up the system, e.g. ECU, by generating a reset and automatically switching to SBC Standby Mode.

This mode is entered via SPI command, and turns-off the integrated LIN bus transceiver, main voltage regulator as well as all switches. Upon a voltage level change at the monitoring / wake-up pins or by LIN message the SBC Sleep Mode will be terminated and the SBC Standby Mode will automatically be entered (turning-on the LDO).

Note: Upon a wake-up via LIN message the (internal) RxD signal stays “low” until mode switch.

Note: If the Window Watchdog was not enabled in Sleep Mode the Window Watchdog starts after wake-up with a “long open window” in SBC Standby Mode.

*Note: In Sleep Mode with activated watchdog (see **Table 2 “SPI Input Data Bits” on Page 21**) the oscillator remains turned on.*

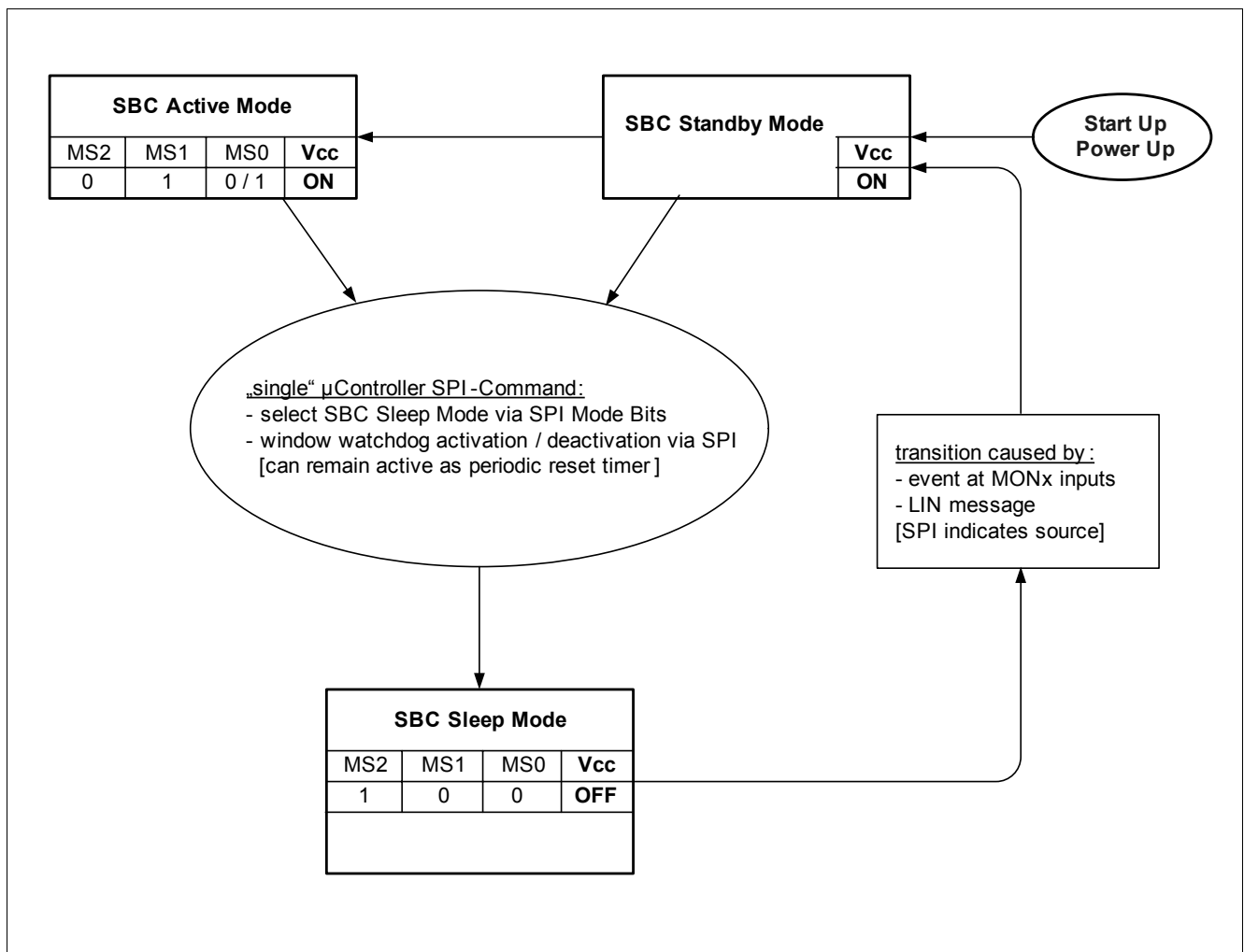


Figure 6 State Diagram “SBC Sleep Mode”

4.5.2 SBC Stop Mode

The **SBC Stop Mode** has the advantage of reducing the current consumption to a minimum, while supplying the microcontroller with its quiescent current during its power saving mode (“Stop”). This mode is entered via SPI command, and turns-off the integrated bus transceivers and respective termination, but the voltage regulator for the microcontroller supply remains active. A microcontroller in a power saving mode has the advantage over a turned-off microcontroller to have a reduced reaction time upon a wake-up event.

A voltage level change at the monitoring/wake-up pins will, in contrast to the behavior in Sleep Mode, generate a signal that indicates the wake-up event at the microcontroller in Power-Down Mode. This is realized via an interconnect from the SPI of the SBC [DO] to the microcontroller [P1.4]. In case the wake-up event was a LIN message, the respective RxD pin of the SBC **and** the SPI Data Out [DO] will be pulled “low”. RxD is pulled “low” until mode switch, while DO stays “low” for **two** internal SBC cycles. (The microcontroller itself has to take care of switching SBC modes after a wake-up event notification (see [Figure 7](#)).)

Note: The window watchdog is automatically disabled once the LDO output current goes below a specified “watchdog current threshold”, unless the SPI setting “WD On/Off” prevents this (see [Figure 10, Watchdog disable current threshold, Table 14](#) and “[Window Watchdog Reset Period Settings](#)” on [Page 23](#)).

Note: If the Window Watchdog was not enabled in Stop Mode the Window Watchdog starts after wake-up with a “long open window” in SBC Standby Mode.

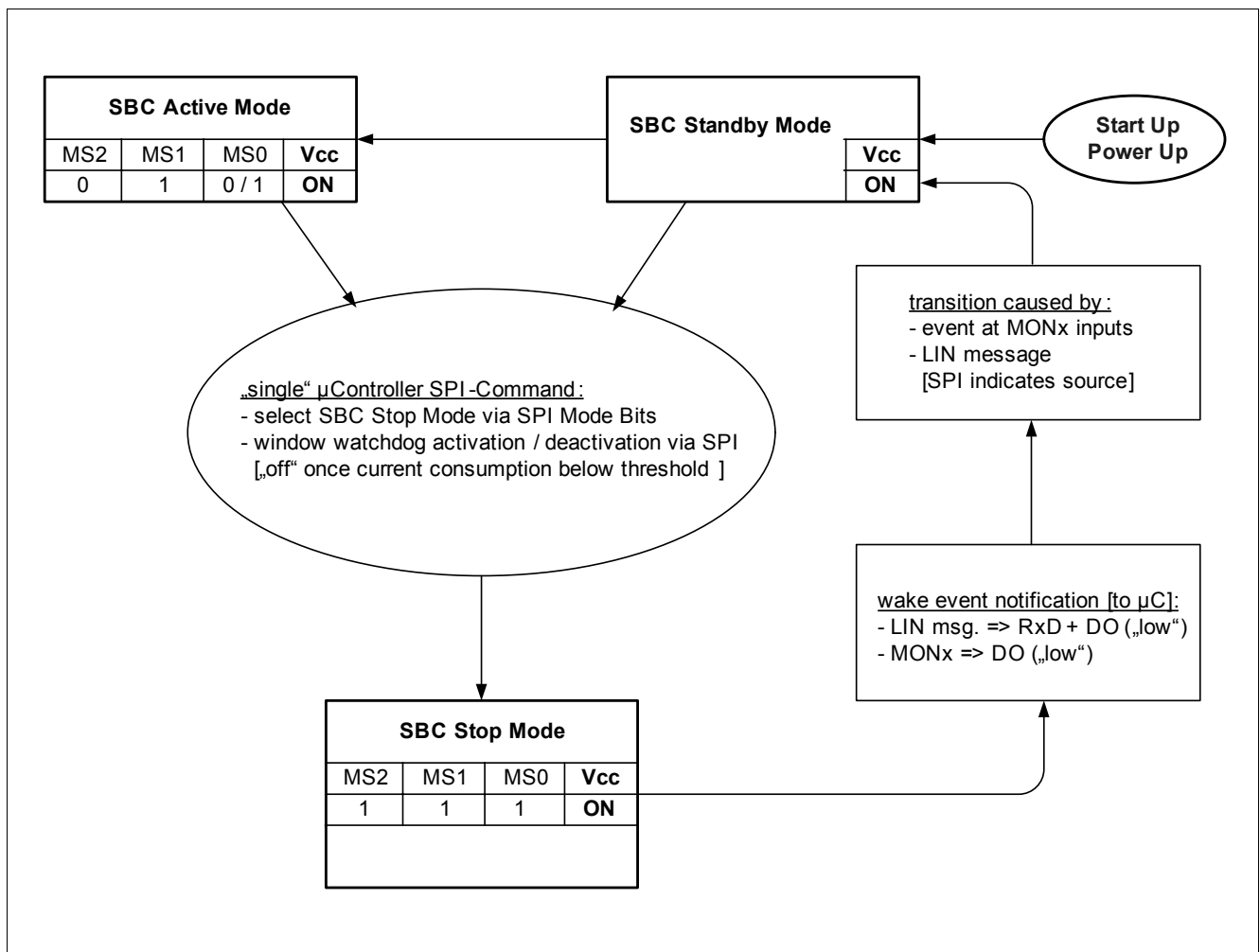


Figure 7 State Diagram “SBC Stop Mode”

4.5.3 SBC Stop Mode with Cyclic Wake

The SBC Stop Mode has the advantage of reducing the current consumption to a minimum, while supplying the microcontroller with its quiescent current during its power saving mode (“Stop”). This mode is entered via SPI command, and turns-off the integrated LIN bus transceiver, but the voltage regulator remains active.

The SBC periodically generates a wake-up “low” pulse at DO (“interconnect signal”) that is connected to an interrupt input [P1.4] of the microcontroller. This period can be defined via the “cyclic wake period” bit field within the SPI register. This pulse at DO has a length of **two** internal SBC cycles.

In case of a detected wake-up event via LIN message or any of the MONx pins, DO stays “low” until the first valid SPI command.

Note: The window watchdog is automatically disabled once the LDO output current goes below a specified “watchdog current threshold”, unless the SPI setting “WD On/Off” prevents this (see Figure 10).

Note: A wake-up event via LIN message or via MONx inputs can happen independently of the cyclic wake phase.

Note: The Window Watchdog starts with a “long open window” after a mode switch, e.g. to SBC Active Mode.

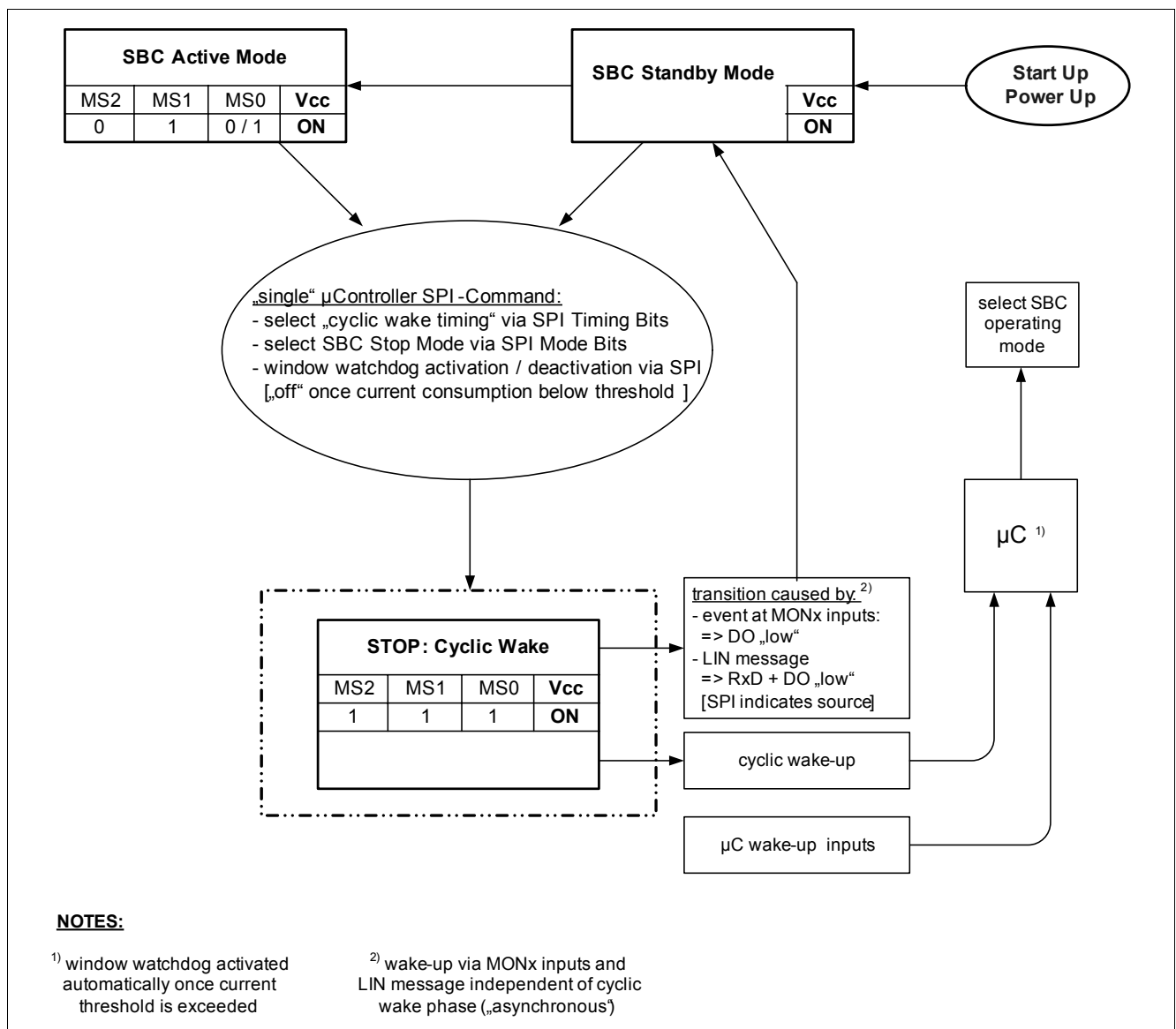


Figure 8 State Diagram “SBC Stop Mode with Cyclic Wake”

5 LIN Transceiver

The TLE7824G offers a LIN transceiver, which is compatible to ISO9141 and certified according to LIN Specification 1.3 and 2.0 "Physical Layer". The transceiver has a pull-up resistor of 30 k Ω implemented and is protected against short to battery and short to GND.

The LIN transceiver has an implemented wake-up capability during operation in power saving modes. In Stop Mode a wake-up event is indicated via (internal) RxD and DO signals, that are pulled "low". Out of Sleep Mode a wake-up event causes an automatic transition into Standby Mode and the (internal) RxD and DO signals are pulled "low". If the TxD input is pulled low for longer than the TxD dominant timeout the TxD input is ignored and the LIN bus goes back to recessive state. This fail-safe feature in case of a permanent low TxD signal recovers if the TxD pin is high for TxD dominant timeout recovery time.

For LIN automotive applications in the United States a dedicated mode by the name "Low Slope Mode" can be used. This mode reduces the maximum data transmission rate of 20 kBaud to 10.4 kBaud by switching to a different slew rate. By using this mode the EM noise emission can be reduced.

6 ADC Measurement Interface

The SBC measurement interface comprises a battery measurement unit (high voltage input V_{bat_sense}) and an on-chip temperature sensor. A multiplexer is used to select the desired input channel that is connected to the ADC of the μC . This multiplexer is controlled via the SPI interface. Also, the reference voltage V_{AREF} is provided by the SBC. The V_{bat_sense} input must be protected against voltage transients, like ISO pulses by a resistor in series to terminal 30.

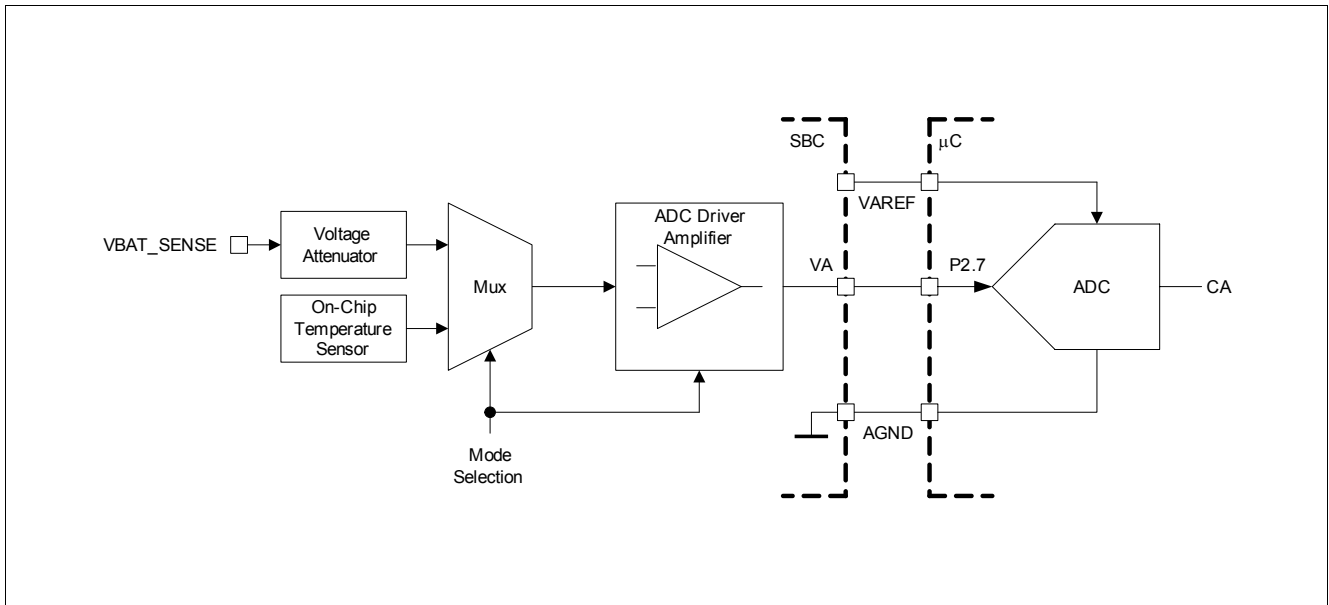


Figure 9 Simplified Block Diagram of ADC Measurement Interface

6.1 Voltage Measurement

The input voltage is filtered and scaled down to the input voltage range of the ADC converter. The voltage measurement output code of the ADC can be calculated using the following equation, where V_{SENS} is the voltage at the pin V_{BAT_SENSE} and N the resolution of the ADC:

$$C_{VSENS} = \text{round}\left[\frac{V_{SENS}}{V_{AREF}} \frac{1}{8} (2^N - 1)\right], 0V \leq V_{SENS} \leq V_{bat-fs} \quad (1)$$

The input voltage corresponding to the ADC output code C_{VSENS} can be calculated with the following equation:

$$V_{SENS} = \frac{8 \times V_{AREF}}{2^N - 1} \times C_{VSENS} \quad (2)$$

6.1.1 Voltage Measurement Calibration Concept

Best measurement accuracy can be obtained by applying the calibration function:

$$C_{VSENSCAL} = \text{round}[c_1(C_{VSENS} - c_0)] \quad (3)$$

C_{VSENS} represents the ADC output code for the analog input voltage at the pin V_{BAT_SENSE} . The correction coefficients c_1 and c_0 correct for slope variations and offset errors of the measurement transfer function.

During the production test these calibration figures are calculated and stored in the flash memory of the microcontroller.

Further details on the implementation of the calibration function and location of the calibration figures in Flash memory can be found in a dedicated application note. The voltage measurement target parameters can be found in [“ADC Battery Voltage Measurement Interface, VBAT_SENSE” on Page 44](#).

6.2 Temperature Measurement

In the temperature measurement mode the typical internal analog output voltage of the on-chip temperature sensor can be described with the first order approximation:

$$V_A \approx m_0 - m_1 \times T_j \quad (4)$$

Where:

- T_j is the junction temperature in Kelvin
- m_0 and m_1 are typical linear fitting parameters
(see [Table “ADC Temperature Measurement Interface” on Page 44](#))

The output code of the ADC is given by the following equation, where V_{AREF} and N denote the ADC reference voltage and the resolution of the ADC:

$$C_A = \text{round} \left[V_A(T_j) \times \frac{(2^N - 1)}{V_{AREF}} \right], V_A \leq V_{AREF} \quad (5)$$

The junction temperature T_j corresponding to the output code C_A is given by:

$$T_j = \frac{1}{m_1} \left[m_0 - \frac{C_A(T_j) \times V_{AREF}}{2^N - 1} \right] \quad [\text{unit: K}] \quad (6)$$

273.15 °C need to be subtracted to convert T_j [K] into Centigrade Scale [°C].

The temperature measurement target parameters can be found in [“ADC Temperature Measurement Interface” on Page 44](#).

6.2.1 Temperature Measurement Calibration Concept

Best measurement accuracy can be obtained by applying the calibration function:

$$T_{CAL} = 586 + f_0 \cdot 2^{-1} - [2^{-2} + f_1 \cdot 2^{-10}] C_A(T_j) \quad (7)$$

The calibration coefficients $f_{0/1}$ are computed during the production test and stored in the flash memory of the microcontroller.

The selection between battery voltage and temperature measurement is done via SPI bit (see [“SPI \(Serial Peripheral Interface\)” on Page 20](#)).

Further details on the implementation of the calibration function and location of the calibration figures can be found in a dedicated application note.

7 Low Dropout Voltage Regulator

The Low Drop-Out Voltage Regulator (LDO) has mainly been integrated in the TLE7824G in order to supply the integrated microcontroller and several modules of the SBC.

*Note: The LDO is **not** intended to be used as supply for external loads. However, it might be used as supply for small external loads (see [Table 13 "Operating Range" on Page 35](#)).*

In the event of a short circuit condition at the V_{CC} pin, a shutdown/reset of the TLE7824G may occur due to overcurrent condition. This maximum output current for external loads is specified in the electrical characteristics.

The voltage regulator output is protected against overload and overtemperature.

An external reverse current protection is required at the pin V_S to prevent the output capacitor at V_{CC} from being discharged by negative transients or low V_S voltage.

8 SPI (Serial Peripheral Interface)

Control and status information between SBC and μ C is exchanged via a digital interface, that is called “serial peripheral interface” (SPI) on the SBC side, and “synchronous serial channel” (SSC) on the μ C side. The 16-bit wide Programming or Input Word of the SBC (see [Table 2](#) to [Table 8](#)) is read in via the data input DI (with “LSB first”), which is synchronized with the clock input CLK supplied by the μ C. The Diagnosis or Output Word appears synchronously at the data output DO (see [Table 9](#)).

The transmission cycle begins when the chip is selected by the Chip Select Not input CSN (“low” active). After the CSN input returns from L to H, the word that has been read in becomes the new control word. The DO output switches to tri-state status at this point, thereby releasing the DO bus for other usage.

The state of DI is shifted into the input register with every falling edge on CLK. The state of DO is shifted out of the output register after every rising edge on CLK. The number of received input clocks is supervised by a modulo-16 operation and the Input/Control Word is discarded in case of a mismatch.

This error is flagged by a “high” at the data output pin DO (interconnect to μ C: P1.4) of the following SPI output word before the first rising edge of the clock is received. Additionally the logic level of DO will be “OR-ed” with the logic level of DI (P1.3).

Note: After wake-up from low-power modes the device needs to be set to Active Mode first before switches like LS1, LS2, Supply Output and LED Driver can be turned on with the second SPI command.

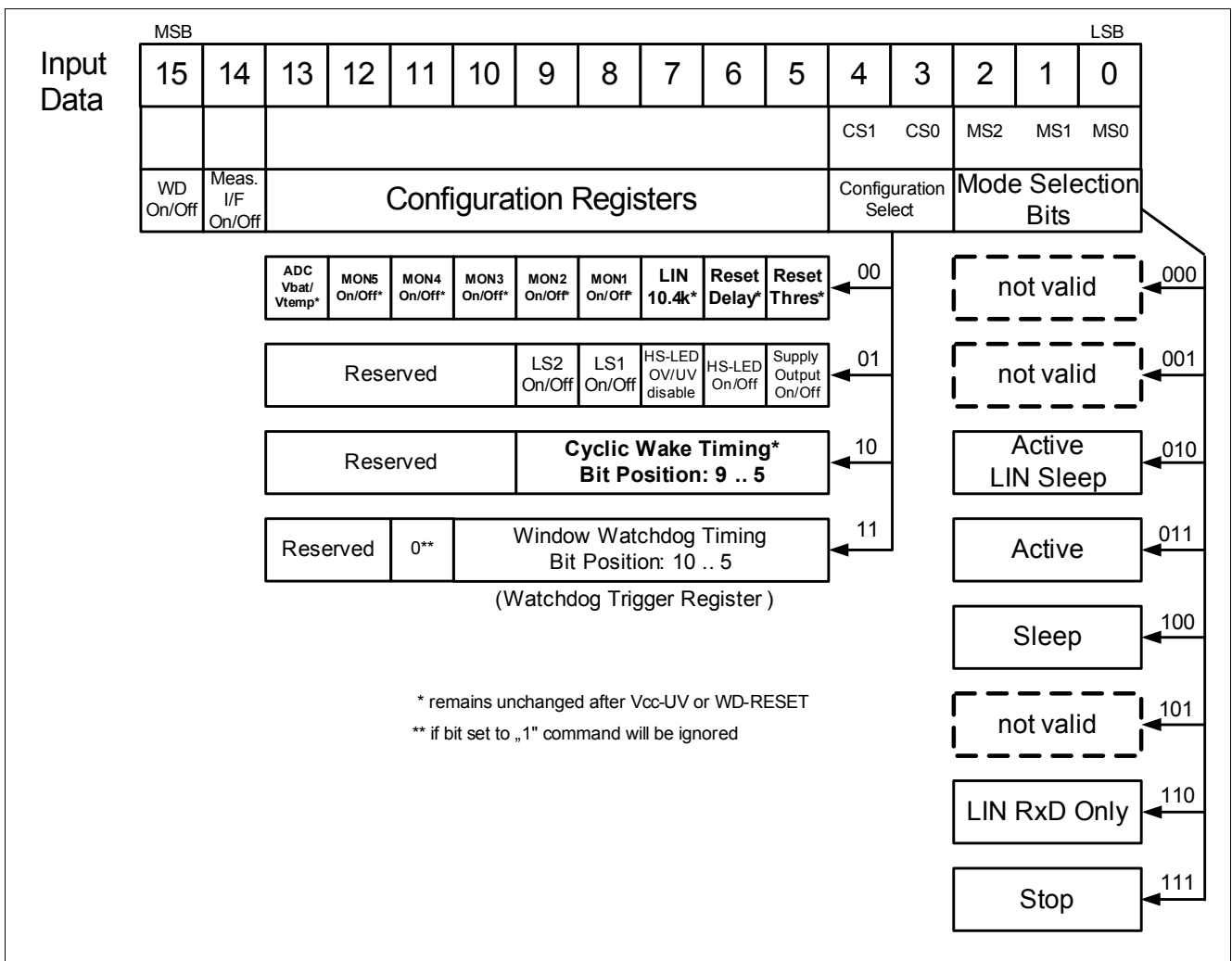


Figure 10 16-Bit SPI Input Data / Control Word

Table 2 SPI Input Data Bits

BIT	Input Data
0	Mode Selection Bit 0 (MS0)
1	Mode Selection Bit 1 (MS1)
2	Mode Selection Bit 2 (MS2)
3	Configuration Selection Bit 0 (CS0)
4	Configuration Selection Bit 1 (CS1)
5 ... 13	Configuration Register (meaning based on "Configuration Selection Bits")
14	Measurement Interface "on" / "off" (setting only valid in active mode, in power saving modes the Measurement interface is turned off)
15	Window Watchdog Stop/Sleep mode configuration "on" / "off" (the configuration is only valid for Stop/Sleep mode, in Active mode the Window Watchdog is always on); if "on" is set before Stop Mode is entered, watchdog remains active regardless of "watchdog disable current threshold"

Table 3 Mode Selection Bits

MS2	MS1	MS0	Mode Selection: SBC Mode
0	0	0	"reserved" / not used
0	0	1	"reserved" / not used
0	1	0	SBC Active Mode: "LIN Sleep"
0	1	1	SBC Active Mode (LIN "on")
1	0	0	SBC Sleep (LIN & VReg "off")
1	0	1	"reserved" / not used
1	1	0	LIN Transceiver: LIN Receive-Only
1	1	1	SBC Stop Mode (LIN "off")

Table 4 Configuration Selection Bits

CS1	CS0	Configuration Selection
0	0	General Configuration
0	1	Integrated Switch Configuration
1	0	Cyclic Wake Configuration
1	1	Window Watchdog Configuration

Table 5 General & Integrated Switch Configuration

Pos.	General Configuration ¹⁾	Integrated Switch Configuration ²⁾
5	Reset Threshold: "default" or "SPI option" (see Table 14: Reset Generator; Pin RESET)	Supply Output "on" / "off"
6	Reset Delay: "default" or "SPI option" (see Table 14: Reset Generator; Pin RESET)	HS-LED "on" / "off"
7	LIN "Low Slope Mode" (10.4 kBaud)	HS-LED OV/UV disable "0": HS-LED will be turned off in case of V_{bat} OV/UV "1": HS-LED will <u>not</u> be turned off in case of V_{bat} OV/UV
8	MON1 Input Activation	LS1 "on" / "off"
9	MON2 Input Activation	LS2 "on" / "off"
10	MON3 Input Activation	"reserved" / not used
11	MON4 Input Activation	"reserved" / not used
12	MON5 Input Activation	"reserved" / not used
13	ADC Measurement: V_{bat} / V_{temp} ("0" = V_{bat} ; "1" = V_{temp})	"reserved" / not used

1) "1" = ON / enable, "0" = OFF / disable

2) "1" = ON, "0" = OFF

Table 6 Cyclic Wake & Window Watchdog Period Settings¹⁾²⁾

Pos.	Cyclic Sense / Wake Config.	Window Watchdog Config.
5	Cyclic Period Bit 0 (T0)	Watchdog Period Bit 0 (T0)
6	Cyclic Period Bit 1 (T1)	Watchdog Period Bit 1 (T1)
7	Cyclic Period Bit 2 (T2)	Watchdog Period Bit 2 (T2)
8	Cyclic Period Bit 3 (T3)	Watchdog Period Bit 3 (T3)
9	Cyclic Period Bit 4 (T4)	Watchdog Period Bit 4 (T4)
10	"reserved" / not used	Watchdog Period Bit 5 (T5)
11	"reserved" / not used	"0" (mandatory)
12	"reserved" / not used	"reserved" / not used
13	"reserved" / not used	"reserved" / not used

1) "1" = ON, "0" = OFF

2) Cyclic wake and window watchdog period settings see [Table 7 "Cyclic Wake Period Settings \(Stop Mode only\)" on Page 23](#)

Table 7 Cyclic Wake Period Settings (Stop Mode only)

T4	T3	T2	T1	T0	Cyclic Wake Period
0	0	0	0	0	Cyclic Wake "off"
0	0	0	0	1	16 ms
0	0	0	1	0	32 ms
0	0	0	1	1	48 ms
0	0	1	0	0	64 ms
0	0	1	0	1	80 ms
0	0	1	1	0	96 ms
... ms
1	1	1	1	1	496 ms

Table 8 Window Watchdog Reset Period Settings

T5	T4	T3	T2	T1	T0	Window Watchdog Reset Period
0	0	0	0	0	0	"not a valid selection"
0	0	0	0	0	1	16 ms
0	0	0	0	1	0	32 ms
0	0	0	0	1	1	48 ms
0	0	0	1	0	0	64 ms
0	0	0	1	0	1	80 ms
0	0	0	1	1	0	96 ms
... ms
1	1	1	1	1	1	1008 ms

Table 9 SPI Output Data

Pos.	Output Data ¹⁾	Output Data after Wake-up ²⁾
0	V_{CC} Temperature Prewarning	V_{CC} Temperature Prewarning
1	HS-LED fail (OC / OT)	HS-LED fail (OC / OT)
2	V_{INT} -Fail ("active low")	V_{INT} -Fail ("active low")
3	LS1/2 (OC / OT)	LS1/2 (OC / OT)
4	Window Watchdog Reset	Window Watchdog Reset
5	MON1 Logic Input Level	Wake-Up via MON1
6	MON2 Logic Input Level	Wake-Up via MON2
7	MON3 Logic Input Level	Wake-Up via MON3
8	MON4 Logic Input Level	Wake-Up via MON4
9	MON5 Logic Input Level	Wake-Up via MON5
10	"reserved" / not used	"reserved" / not used
11	LIN Failure	Bus Wake-Up via LIN Msg.
12	V_{bat} Range 1 (UV) ³⁾ [only "SBC Active Mode"]	End of Cyclic Wake Period
13	V_{bat} Range 2 (OV) [only "SBC Active Mode"]	"low" ⁴⁾

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Table 9 SPI Output Data (cont'd)

Pos.	Output Data ¹⁾	Output Data after Wake-up ²⁾
14	Supply Output (OC / OT)	Supply Output (OC / OT)
15	V_S UV ⁵⁾ [only "SBC Active Mode"]	"low"

- 1) "1" = ON / enable, "0" = OFF / disable, OC = overcurrent, UV = undervoltage, OT = overtemperature (temp. shut-down)
- 2) "1" = ON, "0" = OFF, OC = overcurrent, UV = undervoltage, OT = overtemperature (temp. shut-down)
- 3) Becomes valid after start-up time for voltage monitoring
- 4) Voltage monitoring not active in SBC Standby Mode
- 5) This bit needs to be read twice to indicate an undervoltage condition (only for V_S ramping down - bit15 set to "1")

Table 10 Diagnostic, Protection and Safety Functions

Module	Function	Effect	Concept
Window Watchdog	WD ¹⁾ Failure	Reset; see Table 11 "Reset Behavior SBC" on Page 26	SPI status latched until next read-out
LDO (VReg)	OC ²⁾ at V_{CC}	current limitation	–
	voltage regulator UV condition (V_S related)	Reset, see Table 11 "Reset Behavior SBC" on Page 26	Condition occurs at V_S below operating range
	V_{CC} -UV	Reset, see Table 11 "Reset Behavior SBC" on Page 26	–
	WD current threshold (Stop Mode)	WD only disabled if V_{CC} -current < threshold and WD not enabled via SPI	WD enabled if V_{CC} -current > threshold
	OT ³⁾	V_{CC} -shutdown, Reset as soon as V_{CC} falls below reset threshold, see Table 11 "Reset Behavior SBC" on Page 26	automatically enabled with thermal hysteresis
	OT prewarning	SPI status output	SPI status latched until next read-out
internal supply [SBC] (V_S related)	V_{INT} -UV	(internal) Reset; register settings cleared; SPI status output; see Table 11 "Reset Behavior SBC" on Page 26	–
LS-Switches	OC, OT	LSx-shutdown; SPI status output; signalization via ERR pin	re-activation via SPI command; SPI status latched until next read-out
	microcontroller error signalization (ERR)	LSx-shutdown; see "Error Interconnect (ERR)" on Page 33	re-activation via SPI command
Supply Output	OC, OT	Supply-shutdown; SPI status output	re-activation via SPI command; SPI status latched until next read-out

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Table 10 Diagnostic, Protection and Safety Functions (cont'd)

Module	Function	Effect	Concept
HS-LED	OC, OT	HS-LED-shutdown; SPI status output	re-activation via SPI command; SPI status latched until next read-out
	V_{BAT-UV}	HS-LED-shutdown (optional), SPI status output	re-activation via SPI command; SPI status latched until next read-out
	V_{BAT-OV}	HS-LED-shutdown (optional), SPI status output	re-activation via SPI command; SPI status latched until next read-out
V_{BAT} -Monitor (at V_{BAT_SENSE} pin)	V_{BAT-UV}	HS-LED-shutdown (optional), SPI status output	SPI status latched until next read-out
	V_{BAT-OV}	HS-LED-shutdown (optional), SPI status output	SPI status latched until next read-out
V_S -Monitor	V_S-UV	SPI status output	SPI status latched until next read-out
LIN	LIN-Failure (OT, UV, TxD time-out)	SPI status output	–
	Wake-up	signalization via interconnect to μC (RxD and DO “low”) and SPI status output	–
MONx-Inputs	Wake-up	signalization via interconnect to μC (DO “low”) and SPI status output	–
SPI	Failure Indicator	signalled at interconnect (DO “high” OR-ed with DI) once CSN is active	–

- 1) WD (Window) Watchdog
- 2) OC overcurrent detection
- 3) OT overtemperature detection