Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

TLE8102SG

Smart Dual Channel Powertrain Switch coreFLEX

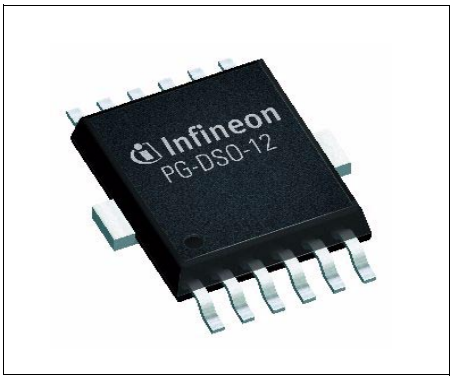
Automotive Power

Never stop thinking

Table of Contents

AEC Qualified RoHS

1 Overview



PG-DSO-12-11

Features

- Overload Protection
- DMOS Overtemperature protection
- Open load detection
- Current limitation
- Low quiescent current mode
- 3.3 V µC compatible input
- Electrostatic discharge (ESD) protection
- Green Product (RoHS compliant)
- AEC Qualified

Description

- Proportional load current sense with improved Precision:
  +/- 6% at I_D=3A and +/-3% Current Sense Temperature Deviation refering to T_J=25°C
- Two Low-Side Channels with $R_{ON(max.\ @\ 150°C)}$ = 360mOhm.
- IC Overtemperature warning
- 8-Bit SPI (for diagnosis and control)
- Short to GND detection
- Programmable overload behaviour

Dual Current Sense Low-Side Switch in Smart Power Technology (SPT) with two open drain DMOS output stages. The TLE8102SG is protected by embedded protection functions and designed for automotive applications. The output stages can be controlled directly by parallel inputs for PWM applications (e.g. Oxygen Probe Heater) or by SPI. All output stages can provide a load current proportional sense signal. Diagnosis can be read from an 8-bit SPI or by the external fault pin.

Type	Package	Marking
TLE8102SG	PG-DSO-12-11	TLE8102SG

Parameter Summary

Parameter	Symbol	Value	Unit
Supply voltage	V_{DD}	4.5 … 5.5	V
Drain source voltage	$V_{DS(CL)}$	48 … 60	V
On resistance	$R_{ON(max.\ @\ 150°C)}$	0.36	Ω

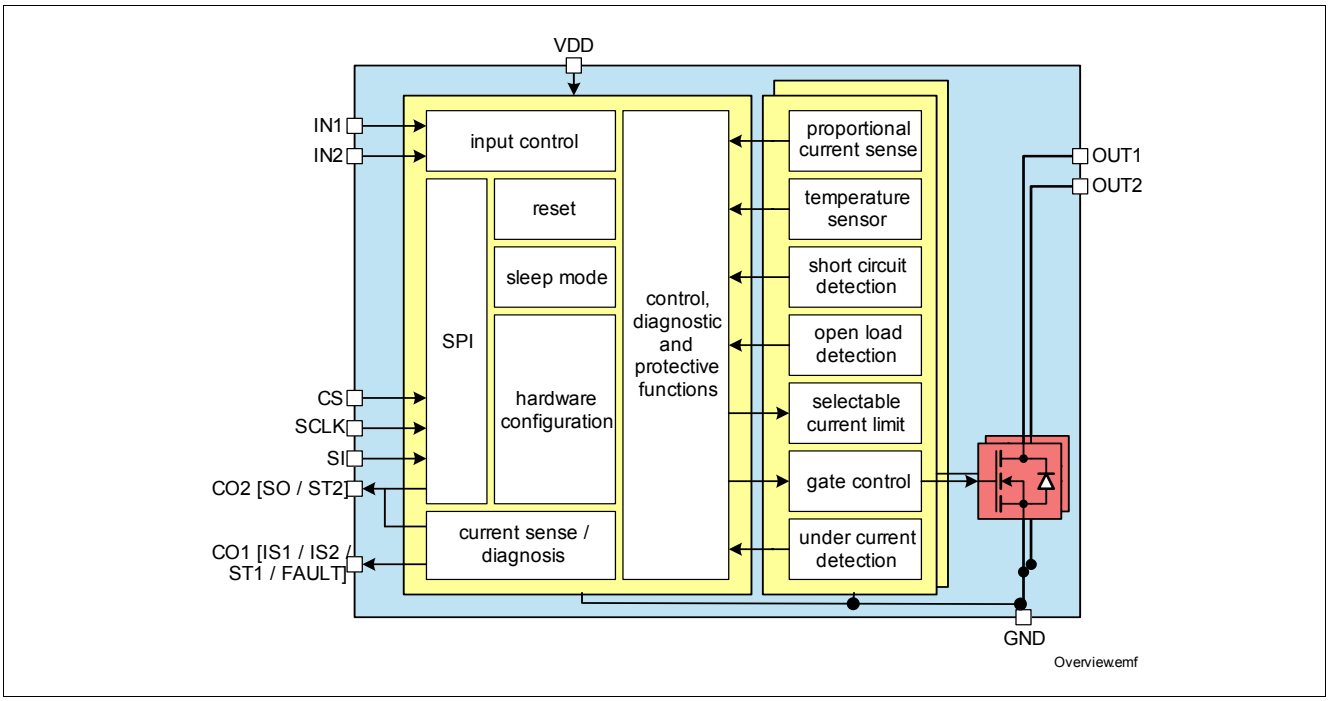


Figure 1 Block Diagram

2 Overview

2.1 Terms

Figure 2 shows all terms used in this Target Data Sheet.

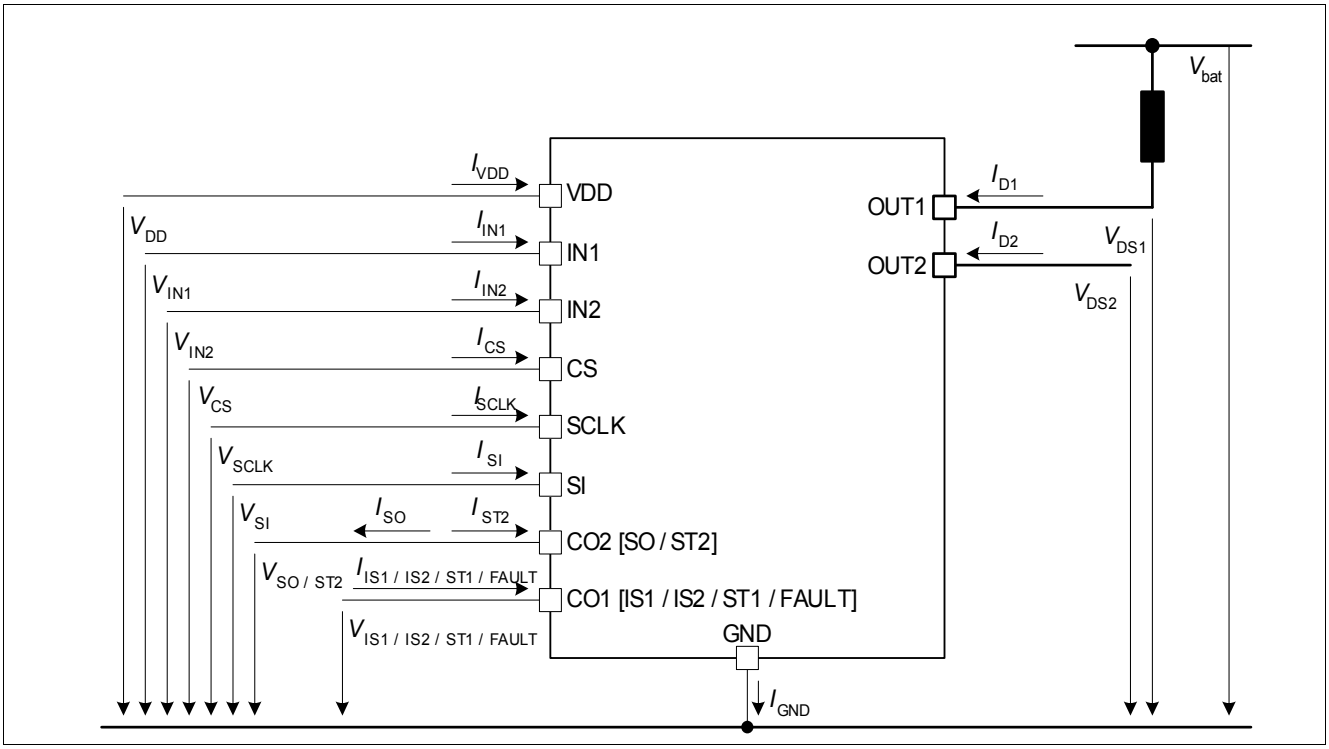


Figure 2 Terms

In all tables of electrical characteristics is valid: Channel related symbols without channel number are valid for each channel separately (e.g. V_{DS} specification is valid for V_{DS1} and V_{DS2}).

3 Pin Configuration

3.1 Pin Assignment

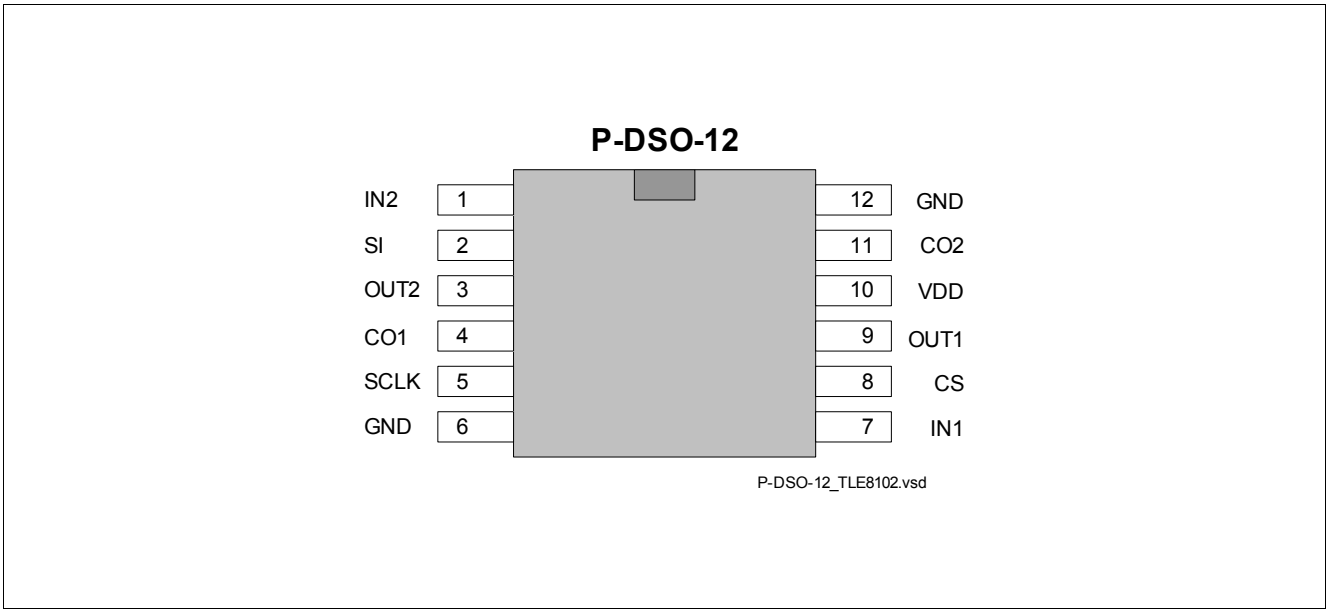


Figure 3 Pin Configuration (top view)

Both GND pins and the heat sink must be connected to GND externally.

3.2 Pin Definitions and Functions

Pin	Symbol	Function
1	IN2	**Input Channel 2**
2	SI	**SPI Signal In**
3	OUT2	**Power Output Channel 2**
4	CO1	**Current Sense 1/2/Fault/Status Ch1**
5	SCLK	**SPI Clock**
6	GND	**Ground**
7	IN1	**Input Channel 1**
8	CS	**SPI Chip Select**
9	OUT1	**Power Output Channel 1**
10	V_{DD}	**Supply Voltage**
11	CO2	**SPI Signal Out/Status Ch2**
12	GND	**Ground**

4 Maximum Ratings and Operating Conditions

4.1 Absolute Maximum Ratings

Absolute Maximum Ratings [1)]

T_j = -40 ·C to +150 ·C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
4.1.1	Supply Voltage	V_{DD}	-0.3	7	V	–
4.1.2	Continuous Drain Source Voltage (OUT1 to OUT2)	V_{DS}	-0.3	48	V	–
4.1.3	Input Voltage, All Inputs and Data outputs, Sense Lines	V_{IN}	-0.3	7	V	–
4.1.4	Output Current per Channel[2)]	I_D	-3	$I_{D(lim1,2)\ min.}$	A	Output ON
4.1.5	Maximum Voltage for short circuit Protection (single event)[3)]	$V_{SC,\ single}$	–	48	V	Current Limit 2, slew rate 1 (default setting)
			–	32	V	Current Limit 2, slew rate 2
			–	18	V	Current Limit 1, slew rate 1 or 2
4.1.6	**E**lectro**s**tatic **D**ischarge Voltage (human body model) according to EIA/JESD22-A114-E	V_{ESD}	-4000 -2000	4000 2000	V V	Output Pins All other Pins
4.1.7	DIN Humidity Category, DIN 40 040		E			–
4.1.8	IEC Climatic Category, DIN IEC 68-1		40/150/ 56			–

1) Not subject to production test, specified by design.

2) Output current rating as long as maximum junction temperature is not exceeded. The maximum output current in the application has to be calculated using R_{thJA} depending onmounting conditions.

3) Device mounted on PCB (50 mm × 50 mm × 1.5 mm epoxy, FR4) with 6 cm^2 copper heatsink area (one layer, 70 µm thick); PCB in test chamber with blown air.

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

4.2 Operating Conditions

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
4.2.1	Output Clamping Energy (single event), linearly decreasing current[1)]	E_{AS}	–	–	75	mJ	$I_{D(0)}$ = 2 A, $T_{J(0)}$ = 150 °C, max. 100 cycles over lifetime
Thermal Resistance							
4.2.2	Junction to case	R_{thJSP}	–	1.3	2	K/W	Pv = 2W
4.2.3	Junction to ambient (see **Figure 4**)	R_{thJA}	–	25	–	K/W	Pv = 2W
Temperature Range							
4.2.4	Operating Temperature Range	T_j	-40	–	150	°C	–
4.2.5	Storage Temperature Range	T_{stg}	-55	–	150	°C	–

1) Pulse shape represents inductive switch off: $I_{D(t)} = I_{D(0)} \times (1 - t / t_{pulse})$; $0 < t < t_{pulse}$

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given by the related electrical characteristics table.

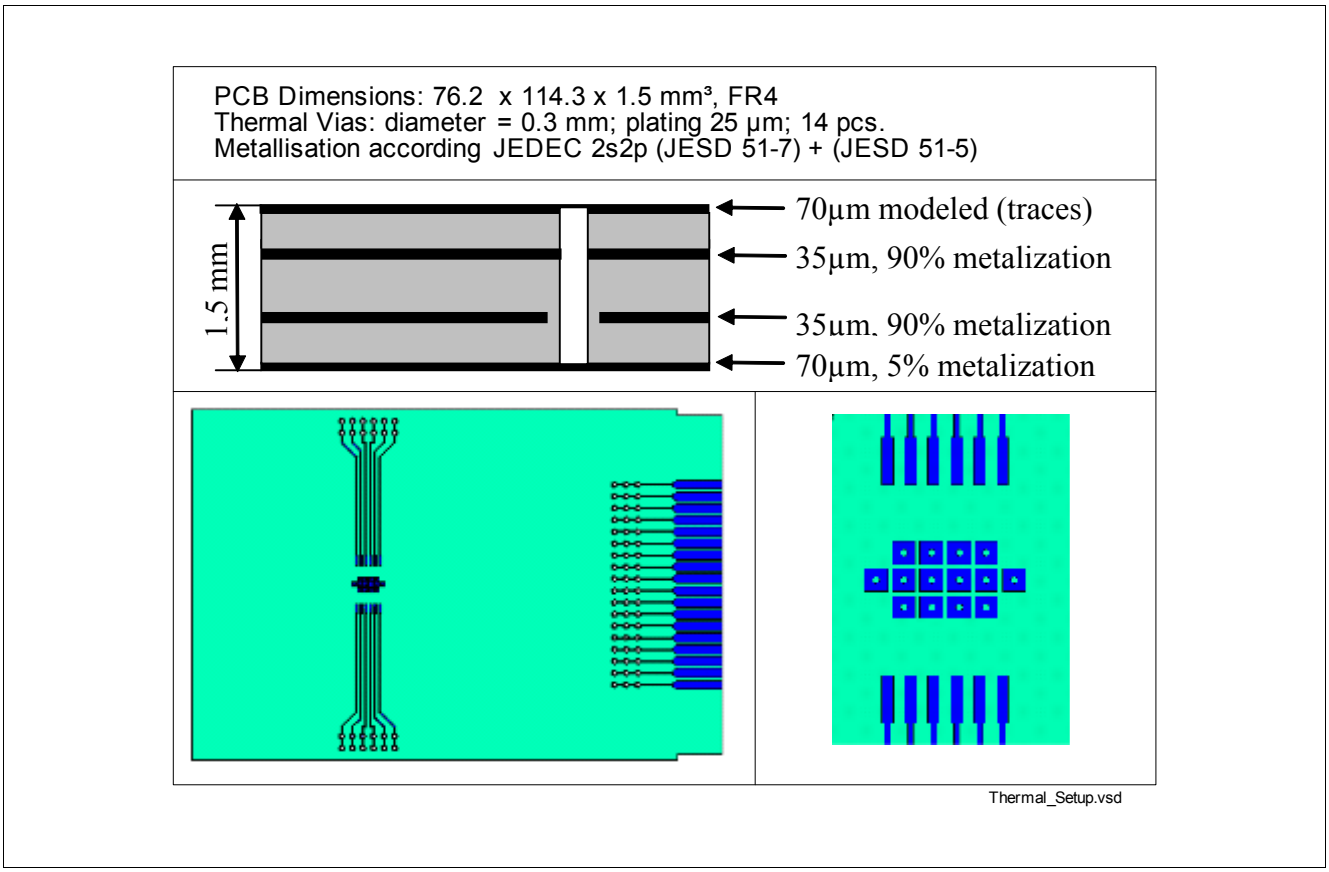


Figure 4 Thermal Simulation - PCB set-up

5 Electrical and Functional Description of Blocks

5.1 Power Supply

The TLE8102SG is supplied by power supply line V_{DD}, used for the digital as well as the analog functions of the device including the gate control of the power stages. A capacitor between pins V_{DD} to GND is recommended.

The TLE8102SG can be programmed via SPI to enter sleep mode. In sleep mode, all outputs are turned off and all diagnosis and biasing circuits are disabled. These actions reduce the quiescent current consumption from the power supply. However, the SPI configuration registers (except for the channel on/off register) are not reset when the TLE8102SG enters sleep mode. To exit sleep mode, a wake up command must be sent via SPI.

Electrical Characteristics: Power Supply

V_{DD} = 4.5 V to 5.5 V, T_j = -40 ·C to +150 ·C, (unless otherwise specified)
all voltages with respect to ground, positive current flowing into pin

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.1.1	Supply Voltage	V_{DD}	4.5	–	5.5	V	–
5.1.2	Supply Current	I_{VDD}	–	–	5	mA	–
5.1.3	Supply Current in Sleep Mode	$I_{VDD(sleep)}$	–	–	10	µA	–
5.1.4	Wake up Time (after sleep mode)[1)]	t_{wake}	–	–	100	µs	–

1) Not subject to production test, specified by design.

5.2 Parallel Inputs

There are two input pins available on the TLE8102SG to control the output stages.

Each input signal controls the output stages of its assigned channel. For example, IN1 controls OUT1 and IN2 controls OUT2. Please refer to **Figure 5** for details. The input pins are active high and each have an integrated pull-down current source. A comparator with hysteresis determines the state of the signal on IN$_n$. The zener diode protects the input circuit against ESD pulses.

The *BOL* bit can be set via SPI. This bit determines if the output is exclusively controlled by the *INn* signals, exclusively controlled by the corresponding data bits *CHn$_{IN}$* or by a Boolean OR or AND operation of the two inputs. The default setting of the *BOL* bits programs the outputs to be controlled exclusively by the *INn* signals.

The *SLEn* bit can be set via SPI. This bit sets the slew rate of its assigned channel by selecting either slew rate 1 or slew rate 2. The slew rate also changes the over load switch off delay time (only for current limit 2).

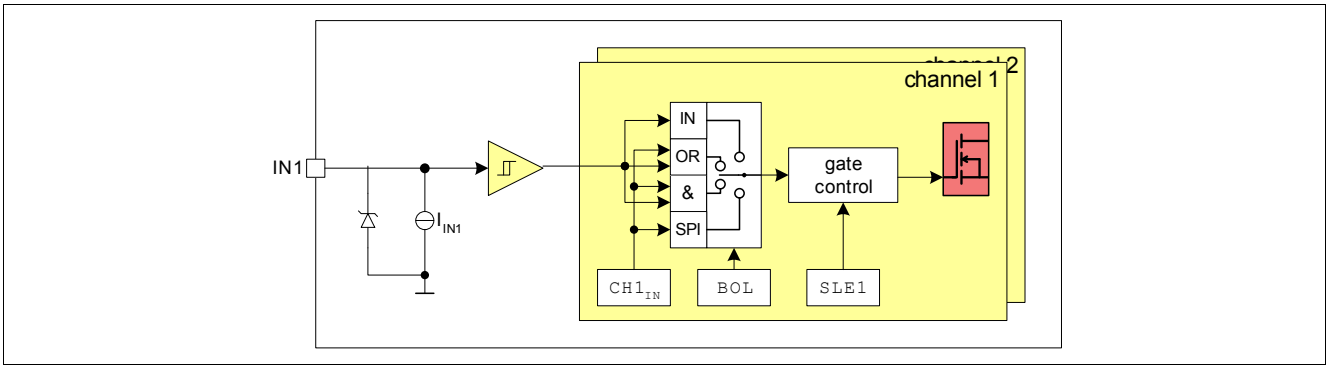


Figure 5 Input Control and Boolean Operator

Electrical Characteristics: Parallel Inputs

V_{DD} = 4.5 V to 5.5 V, T_j = -40 ·C to +150 ·C, (unless otherwise specified)
all voltages with respect to ground, positive current flowing into pin

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.2.1	Input Low Voltage	V_{INL}	–	–	1.0	V	–
5.2.2	Input High Voltage	V_{INH}	2.0	–	–	V	–
5.2.3	Input Voltage Hysteresis[1)]	V_{INHys}	100	200	400	mV	–
5.2.4	Input Pull-down Current (IN1 to IN2)	$I_{IN(1 \ldots 2)}$	20	50	100	µA	–

1) Not subject to production test, specified by design.

5.3 Power Outputs

5.3.1 Timing Diagrams

The power transistors are switched on and off with a dedicated slope either via the parallel inputs or by the CHn_{IN} bits of the serial peripheral interface SPI. The switching times t_{ON} and t_{OFF} are designed equally. The switching time of each channel can be selected via SPI by programming the $SLEn$ bit of the desired output. See **Figure 6** for details

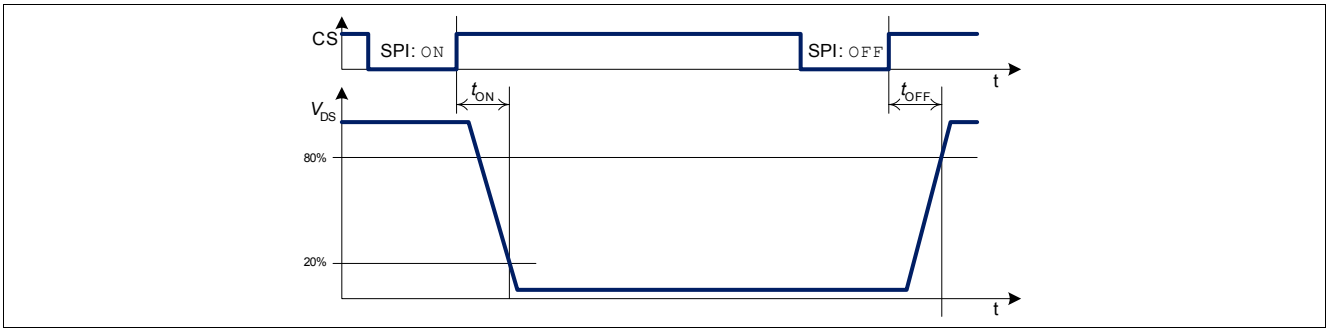


Figure 6 Switching a Resistive Load

5.3.2 Inductive Output Clamp

When switching off inductive loads, the potential at pin OUT rises to $V_{DS(CL)}$, as the inductance continues to drive current. The inductive output clamp is necessary to prevent destruction of the device. See **Figure 7** for details. The maximum allowed load inductance and current, however, are limited.

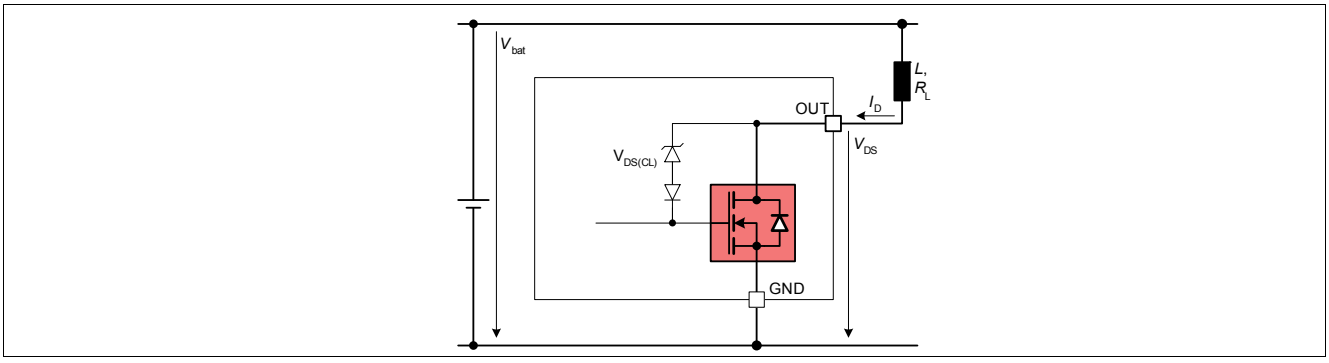


Figure 7 Inductive Output Clamp

Maximum Load Inductance

During demagnetization of inductive loads, energy has to be dissipated in the TLE8102SG. This energy can be calculated with following equation:

$$E = V_{DS(CL)} \cdot \left[\frac{V_{bat} - V_{DS(CL)}}{R_L} \cdot \ln\left(1 - \frac{R_L \cdot I_D}{V_{bat} - V_{DS(CL)}}\right) + I_D \right] \cdot \frac{L}{R_L}$$

The equation simplifies under the assumption of R_L = 0:

$$E = \frac{1}{2} L I_D^2 \cdot \left(1 - \frac{V_{bat}}{V_{bat} - V_{DS(CL)}}\right)$$

The energy, which is converted into heat, is limited by the thermal design of the component.

5.3.3 Protection Functions

The TLE8102SG provides embedded protective functions. Integrated protection functions are designed to prevent IC destruction under fault conditions described in this data sheet. Fault conditions are considered “outside” the normal operating range. Protection functions are not designed for continuous repetitive operation.

Over load and over temperature protections are implemented in the TLE8102SG. **Figure 8** gives an overview pf the protective functions.

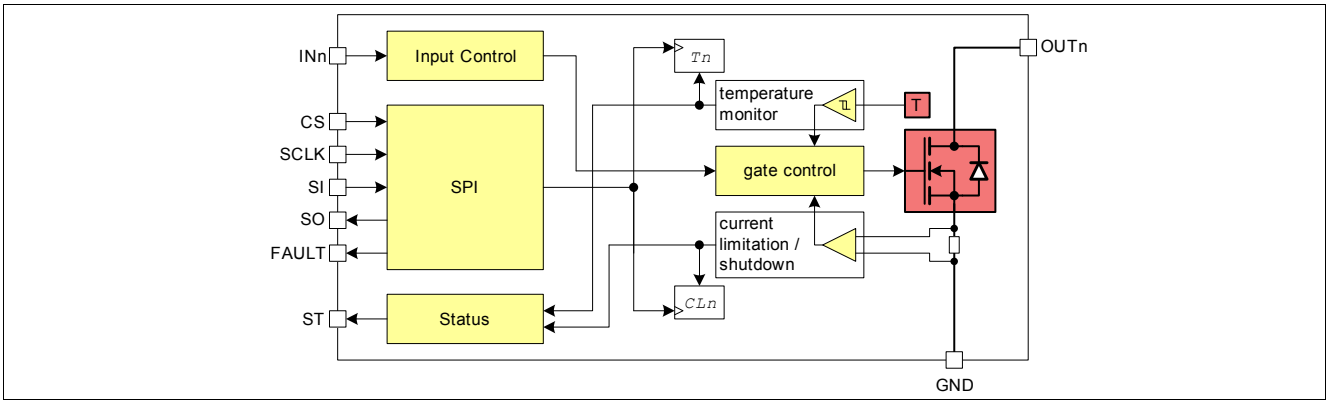


Figure 8 Protection Functions

5.3.3.1 Over Load Protection

The TLE8102SG is protected in case of over load or short circuit of the load. If the device is programmed for current limitation (current limit 1), the current is limited to $I_{DS(lim1)}$. After time $t_{d(fault)}$, the corresponding over load flag CLn is set. If using the status outputs for diagnosis, the over load flag is cleared immediately after the over load condition is no longer present. If using the SPI interface and fault pin for diagnosis, the over load flag of the affected channel is cleared by the rising edge of the $\overline{CS}$ signal after a successful SPI transmission.

If the TLE8102SG is programmed for current shutdown (current limit 2), the current threshold is $I_{DS(lim2)}$. However, unlike in current limit 1, after time $t_{d(fault)}$, the affected channel is turned off and the according over load flag CLn is set. To turn on the channel again, this overload latch has to be reset by turning off the affected channel with either the parallel input or SPI. In addition, the switch off delay time can be programmed by changing the slew rate setting. If using the SPI interface and fault pin for diagnosis in case of current limit 2, the over load flag of the affected channel is cleared by the rising edge of the CS signal after a successful SPI transmission when the IN pin is low. A valid SPI cycle would not lead to a reset of the OVL flag of the affected channel during the IN-Pin is high.

In both cases, the channel may shut down due to over temperature.

For timing information, please refer to **Figure 9** and **Figure 10** for details.

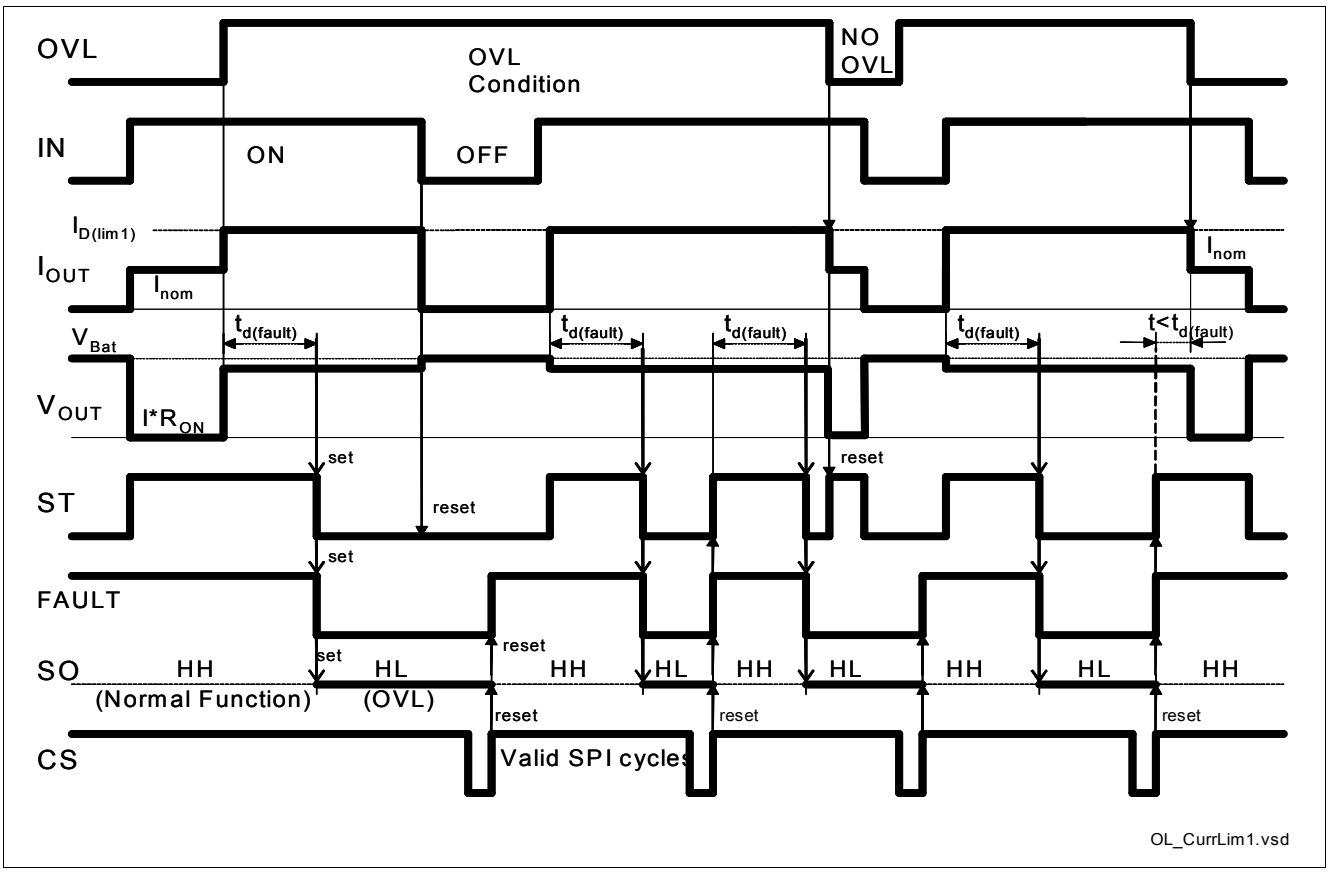


Figure 9 Over Load Behavior - Current Limitation (current limit 1)

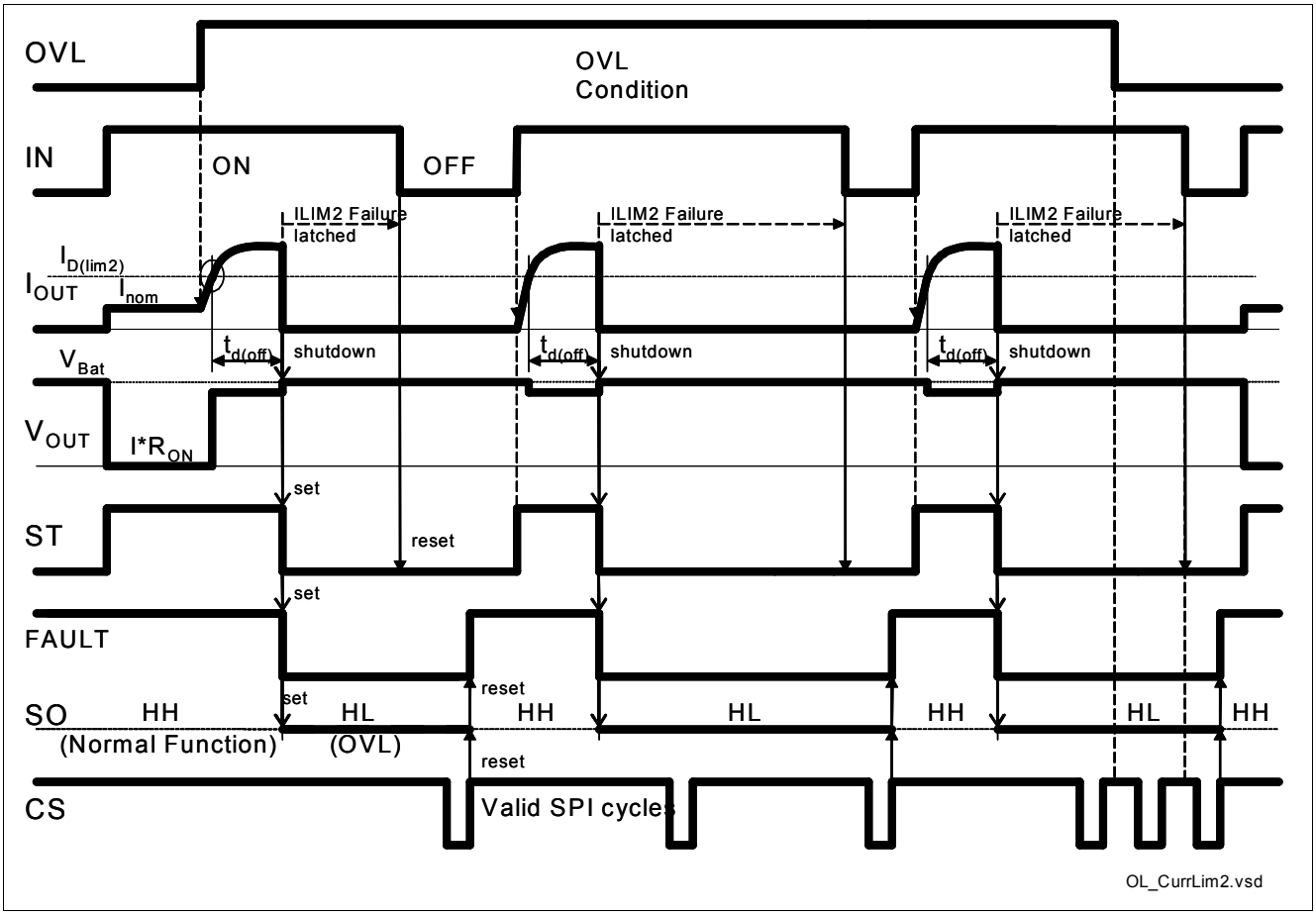


Figure 10 Over Load Behavior - Latched Shutdown (current limit 2)

5.3.3.2 Over Temperature Protection

A dedicated temperature sensor for each channel detects if the temperature of its channel exceeds the over temperature shutdown threshold. If the channel temperature exceeds the over temperature shutdown threshold, the overheated channel is switched off immediately to prevent destruction. At the same time (no delay), the over temperature flag Tn is set. If the status outputs are used for diagnosis, the over temperature flag is cleared immediately after the over temperature condition is no longer present. If using the SPI interface and fault pin for diagnosis, the over temperature flag of the affected channel is cleared by the rising edge of the $\overline{CS}$ signal after a successful SPI transmission.

The restart response of the channel can be programmed via SPI. If automatic autorestart is selected, after cooling down, the channel is switched on again with thermal hysteresis ΔT_j. If latching shutdown is selected, the channel remains switched off even after cooling down. The channel can be restarted only if first turned off with either the parallel input or SPI. In addition, the channel must first be turned off before the the over temperature flag of the affected channel can be cleared by the rising edge of the $\overline{CS}$ signal after a successful SPI transmission.

For timing information, please refer to **Figure 11** and **Figure 12** for details.

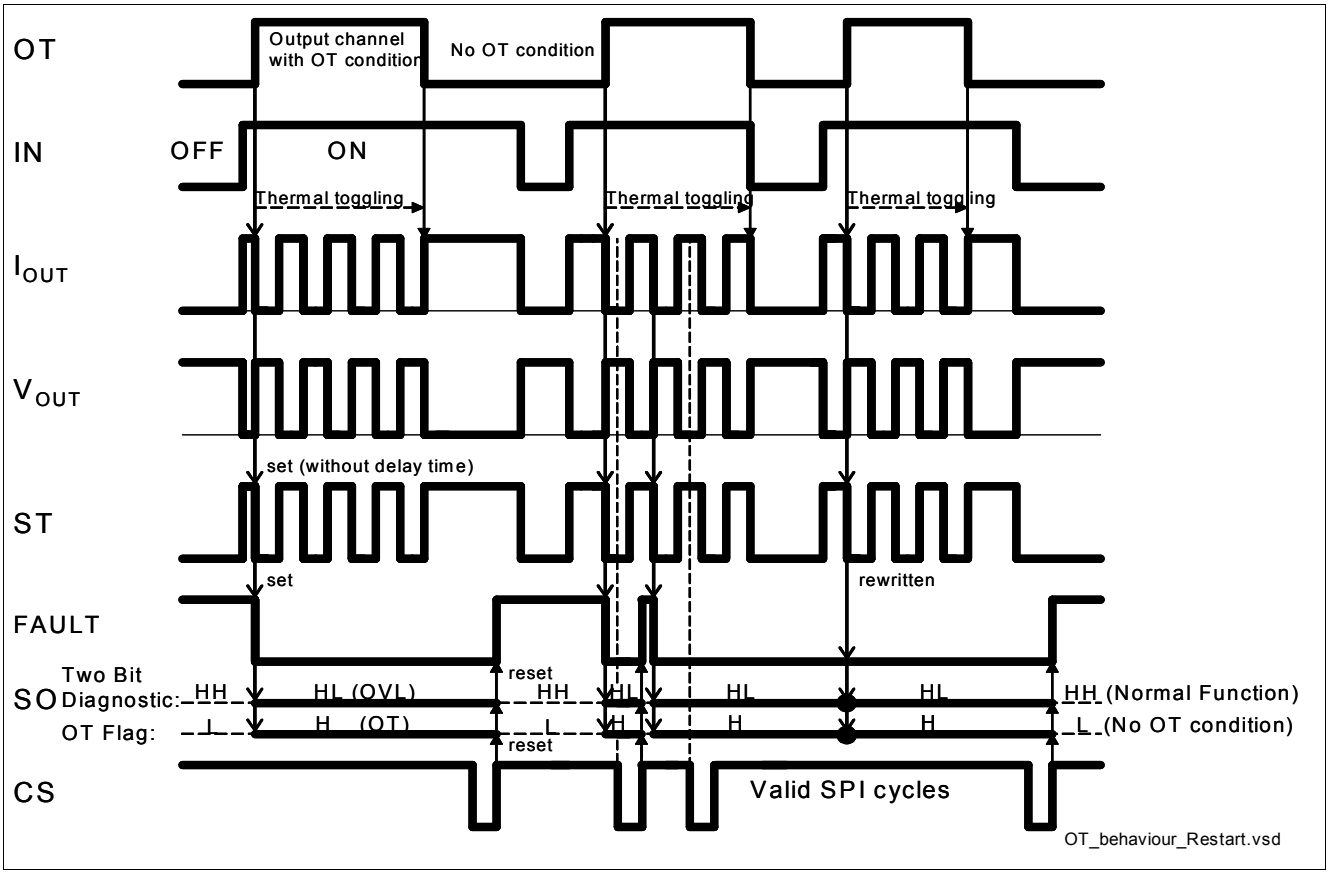


Figure 11 Over Temperature Behavior - Automatic Autorestart

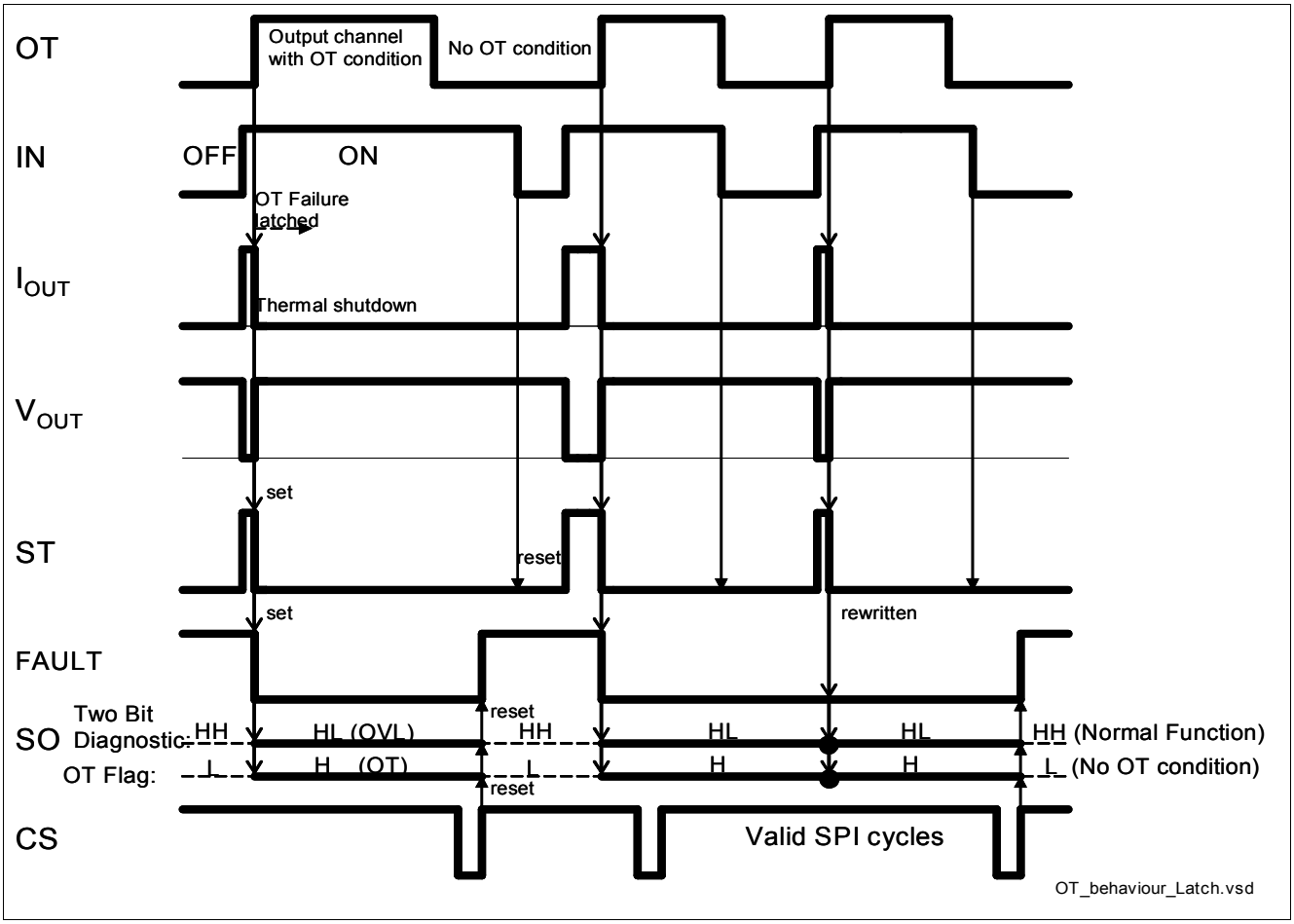


Figure 12 Over Temperature Behavior - Latched Shutdown

5.3.4 Reverse Current

In the case of reverse polarity when outputs are turned on, the power stages of the TLE8102SG are able to conduct reverse current I_{rev}, defined as current that flows from ground to the output pin. Please note that neither the over load, over temperature, nor current sense diagnostics are functional in reverse current operation. Additionally, it is possible for the supply current I_{VDD} to be greater than 5 mA.

5.3.5 Reverse Polarity Protection

In the case of reverse polarity when outputs are turned off, the intrinsic body diode of the power transistor causes power dissipation. The reverse current through the intrinsic body diode has to be limited by the connected load. The V_{DD} supply pin must be protected against reverse polarity externally. Please note that neither the over load, over temperature, nor current sense diagnostics are functional in reverse current operation.

Electrical Characteristics: Power Outputs

V_{DD} = 4.5 V to 5.5 V, T_j = -40 ·C to +150 ·C, (unless otherwise specified)
all voltages with respect to ground, positive current flowing into pin

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.3.1	ON Resistance	$R_{DS(ON)}$	–	0.18	–	Ω	T_J = 25 °C,[1] V_{DD} = 5 V, I_D = 2 A
			–	0.27	–	Ω	T_J = 125 °C,[1] V_{DD} = 5 V, I_D = 2 A
			–	0.3	0.36	Ω	T_J = 150 °C, V_{DD} = 5 V, I_D = 2 A
5.3.2	Output Clamping Voltage	$V_{DS(CL)}$	48	–	60	V	output OFF
5.3.3	Current Limit 1: Current limitation	$I_{D(lim1)}$	5	6.5	8	A	–
5.3.4	Current Limit 2: Overload switch off	$I_{D(lim2)}$	9	10.5	12	A	$V_{DD} \geq$ 5 V
			9	–	12	A	V_{DD} < 5 V, $T_J \leq$ 125 °C
			8	–	12	A	V_{DD} < 5 V, T_J > 125 °C[1]
5.3.5	Reverse Current per channel[1)2)]	I_{rev}	–	–	2	A	–
5.3.6	Output Leakage Current	$I_{D(lkg)}$	–	–	5	µA	Sleep mode active
5.3.7	Turn-On Time 1 Turn-On Time 2	t_{ON}	– –	5 20	10 50	µs	I_D = 2 A, resistive load
5.3.8	Turn-Off Time 1 Turn-Off Time 2	t_{OFF}	– –	5 20	10 50	µs	I_D = 2 A, resistive load
5.3.9	Turn On slew rate Slew rate 1 Slew rate 2	s_{ON}	 1 –	 5 1	 20 5	V/µs	V_{bat} = 14 V, I_D = 2 A, resistive load, U_{DS} = 80% to 30%
5.3.10	Turn Off slew rate Slew rate 1 Slew rate 2	s_{OFF}	 1 –	 5 1	 20 5	V/µs	V_{bat} = 14 V, I_D = 2 A, resistive load, U_{DS} = 30% to 80%
5.3.11	IC Overtemperature Warning[1] Hysteresis[1]	T_w $T_{(w)\ hys}$	155 –	– 10	185 –	°C K	– –
5.3.12	Channel Overtemp. Shutdown[1] Hysteresis[1]	$T_{th(sd)}$ $T_{(sd)hys}$	170 –	– 10	200 –	°C K	– –

1) Not subject to production test, specified by design.

2) Device functions normally, but supply current I_{VDD} can be greater than 5 mA.

5.4 Diagnostic Functions

The TLE8102SG provides diagnosis information about the device and about the load. The following diagnosis functions are implemented:

- The protective functions (flags *CLn* and *Tn*) of channel n are registered in the diagnosis flag *Pn*.
- The open load diagnosis of channel n is registered in the diagnosis flag *OLn*.
- The under current diagnosis of channel n is registered in the diagnosis flag *UCn*.
- The short to ground monitor information of channel n is registered in the diagnosis flag *SGn*

The diagnosis information of the TLE8102SG can either be accessed by status (ST) pins or the SPI interface and/or fault pin. With the exception of over temperature, a fault is only recognized if it lasts longer than the fault delay time $t_{d(fault)}$. If using the status pins for diagnosis, the status pins change state in normal operation to match the input signal of the corresponding channel. If a fault condition appears and the fault delay time elapses, the status pin for the channel shows the inverted input signal. This diagnosis flag is not latched. Therefore, if the fault condition is removed, the status pins will indicate normal operation.

Unlike the status pins, when using the SPI interface and/or fault pin, diagnosis flags are latched in the diagnosis register of the SPI interface. In this case, diagnosis flags are cleared by the rising edge of the $\overline{CS}$ signal after a successful SPI transmission.

Please see **Table 1** and **Figure 13** for details.

Table 1 Diagnostic Information

Operating Condition	Control Input	Power Output	Filter Time	Status Output	Fault Output	Channel Diagnosis Bits MSB, LSB	Channel Overtemp. Flag
Sleep Mode	x	off	–	L	H	– –	–
Normal Operation	L H	off on	–	L H	H H	H, H H, H	L L
Short to ground	L H	off on	$t_{d(fault)}$ $t_{d(fault)}$	H L	L L	L, L L, H	L L
Open load, Under current.[1)]	L H	off on	$t_{d(fault)}$ $t_{d(fault)}$	H L	L L	L, H L, H	L L
Over load (current limit 1, current limitation)[1)]	H	on	$t_{d(fault)}$	L	L	H, L	L
Over load (current limit 2, latching shutdown)[2)]	H	off	$t_{d(off)}$	L	L	H, L	L
Overtemp. (autorestart)	H	off[3)]	–	L	L	H, L	H
Overtemp. (latching shutdown)	H	off[4)]	–	L	L	H, L	H

1) Short to ground/open load/ under current /overload/short-to-supply - events shorter than min. time $t_{d(fault)}$ will not be latched and not reported at the diagnosis pins.
2) Overload/short-to-supply - events shorter than min. time $t_{d(off)}$ will not be latched and not reported at the diagnosis pins.
3) Off as long as overtemperature occurs, restart after cooling down.
4) Shutdown latch reset by falling input edge.

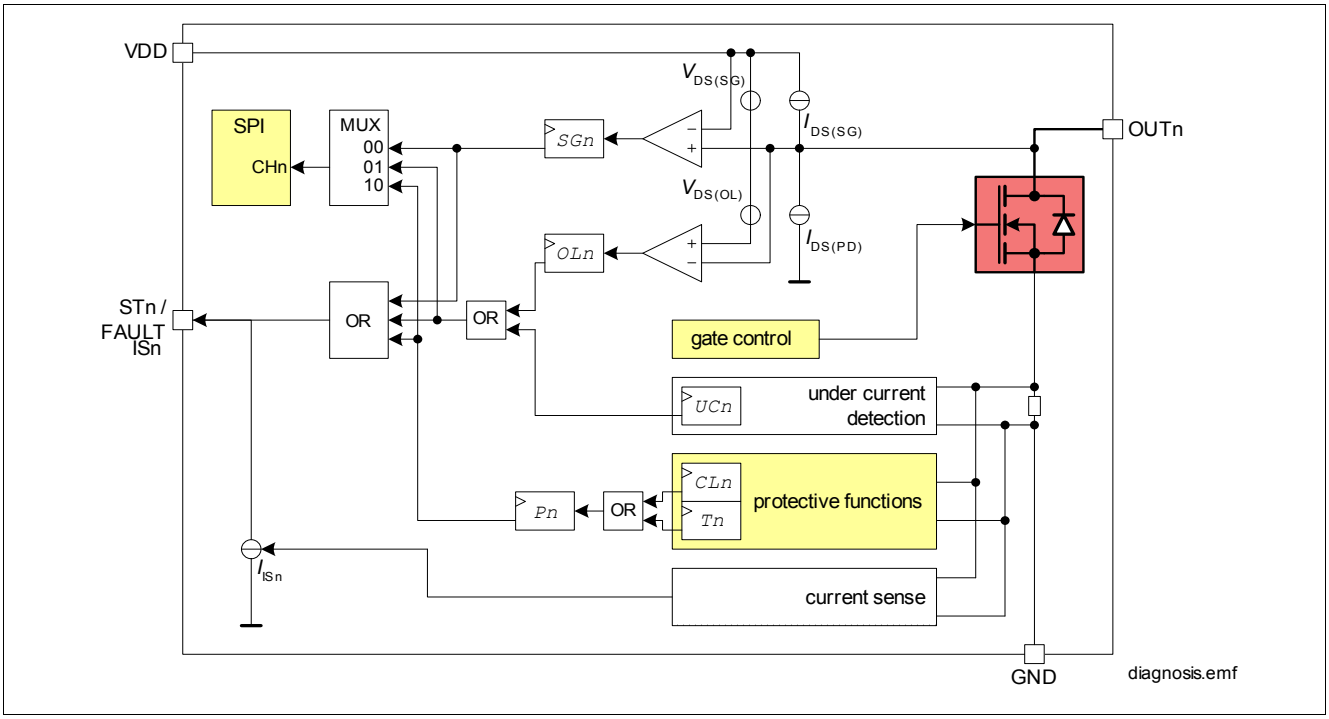


Figure 13 Block Diagram of Diagnostic Functions

Electrical Characteristics: Diagnostic Functions

V_{DD} = 4.5 V to 5.5 V, T_j = -40 ·C to +150 ·C, (unless otherwise specified)
all voltages with respect to ground, positive current flowing into pin

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.4.1	Open Load Detection Voltage (Channel OFF)	$V_{DS(OL)}$	0.5 × V_{DD}	0.6 × V_{DD}	0.7 × V_{DD}	V	–
5.4.2	Output Pull-down Current (Channel OFF)	$I_{PD(OL)}$	25	50	100	µA	–
5.4.3	Fault Filtering Time	$t_{d(fault)}$	50	100	200	µs	–
5.4.4	Overload switch off delay time (only current limit 2)	$T_{d(off)}$	10 10	– –	50 150	µs	Slew rate 1 Slew rate 2
5.4.5	Short to Ground Detection Voltage	$V_{DS(SHG)}$	0.3 × V_{DD}	0.4 × V_{DD}	0.5 × V_{DD}	V	–
5.4.6	Output Pull-up Current (Channel OFF)	$I_{PU(SHG)}$	-50	-100	-150	µA	–
5.4.7	Under Current Detection Threshold (Channel ON)	$I_{D(OL)}$	100	170	300	mA	–

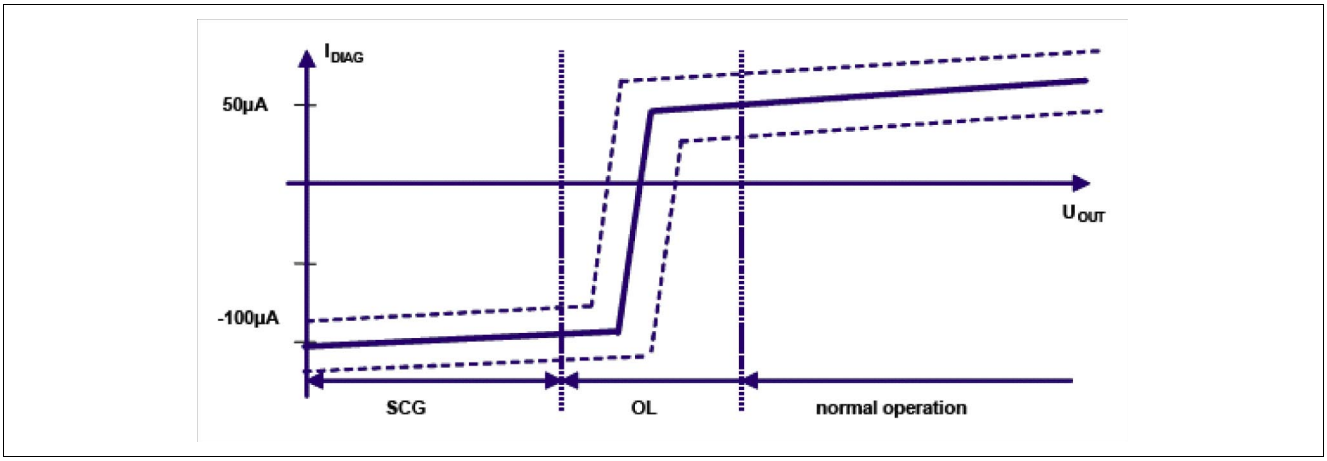


Figure 14 Open load (off) and Short to GND Diagnostics

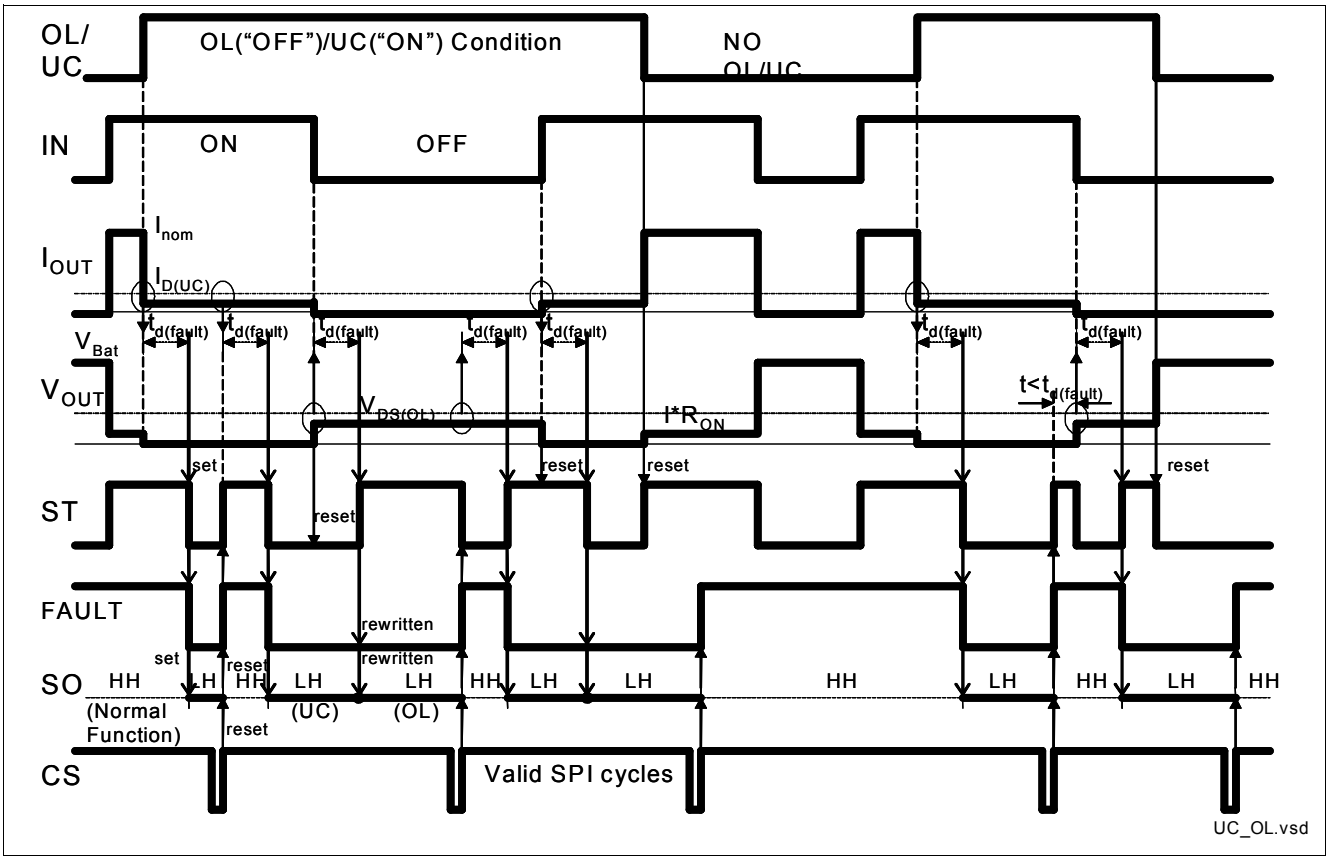


Figure 15 Diagnostic at "Open Load/Under Current" Condition

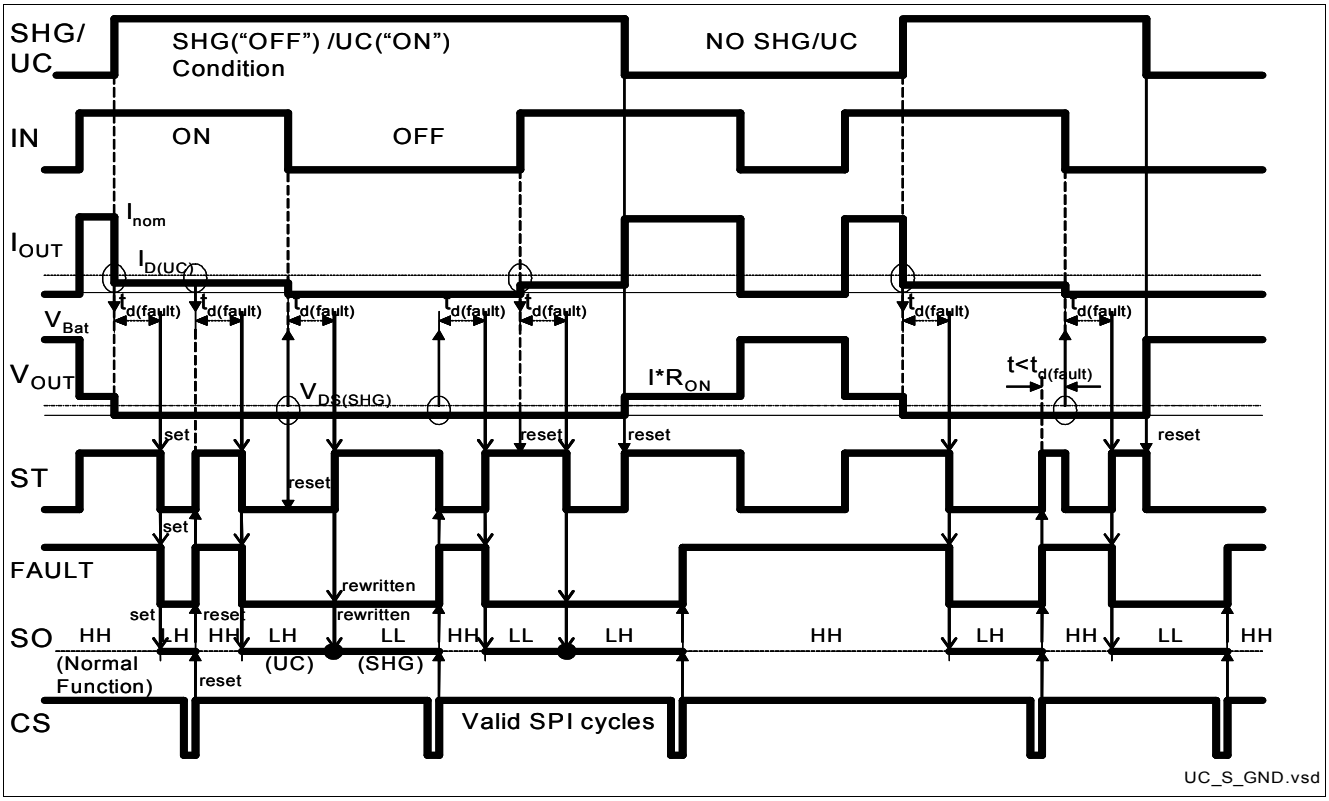


Figure 16 Diagnostic at "Short to GND/Under Current" Condition

5.5 Current Sense

The TLE8102SG includes an integrated current sense feature. If the device is programmed (via SPI) to use this feature, the current source I_{IS} of the current sense pin becomes active and generates a pull-down current proportional to the load current of the selected channel. An external pull-up resistor must be connected to the current sense pin to generate a voltage signal proportional to the load current of the selected channel. To achieve the specified accuracy for current sensing, the voltage V_{IS} at the current sense pin must always be greater than or equal to 2 V. The current source I_{IS} can also be programmed to generate a current proportional to the sum of the load current of both channels.

Electrical Characteristics: Current Sense

V_{DD} = 4.5 V to 5.5 V, T_j = -40 ·C to +150 ·C, (unless otherwise specified)
all voltages with respect to ground, positive current flowing into pin

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.5.1	Current Sense Precision (single channel)[1)] I_{FB}/I_{OUT}	P_{IS}	 0.50 0.80 0.90 0.93 0.94 0.95	 1.00	 1.50 1.20 1.10 1.07 1.06 1.05	mA/A	V_{DD} = 5 V, $U_{CO1} \geq$ 2 V I_D = 100 mA, I_D = 200 mA, I_D = 500 mA, I_D = 1 A, I_D = 3 A, I_D = 5 A,
5.5.2	Current Sense Temperature Deviation[1) 2) 3)] at	I_{Stemp}	 - 25 -10 -4 -3 -3 -3	 $P_{IS(25°C, ID)}$	 +25 +10 +4 +3 +3 +3	%	V_{DD} = 5 V, $U_{CO1} \geq$ 2 V I_D = 100 mA, I_D = 200 mA, I_D = 500 mA, I_D = 1 A, I_D = 3 A, I_D = 5 A,
5.5.3	Current Sense Settle time[2)]	t_{IS}	–	–	4	µs	$U_{CO1} \geq$ 2 V, R_{sense} = 2.5 kΩ (I_{Dmax} = 1 A)
5.5.4	Current Sense Settle time[2)]	t_{IS}	–	–	2	µs	$U_{CO1} \geq$ 2 V, R_{sense} = 500 Ω (I_{Dmax} = 5 A)
5.5.5	Output Tri-state Leakage Current	I_{SOlkg}	-10	0	10	µA	$\overline{CS}$ = H, $0 \leq V_{SO} \leq V_{DD}$
5.5.6	FAULT Output Low Voltage	V_{FAULTL}	–	–	0.4	V	I_{FAULT} = 1.6 mA
5.5.7	Status Output Low Voltage	V_{ST}	–	–	0.4	V	I_{ST} = 1.6 mA

1) If the summed current is sensed the tolerances of the single channels are added.

2) Not subject to production test, specified by design.

3) Temperature Variation of one single device.

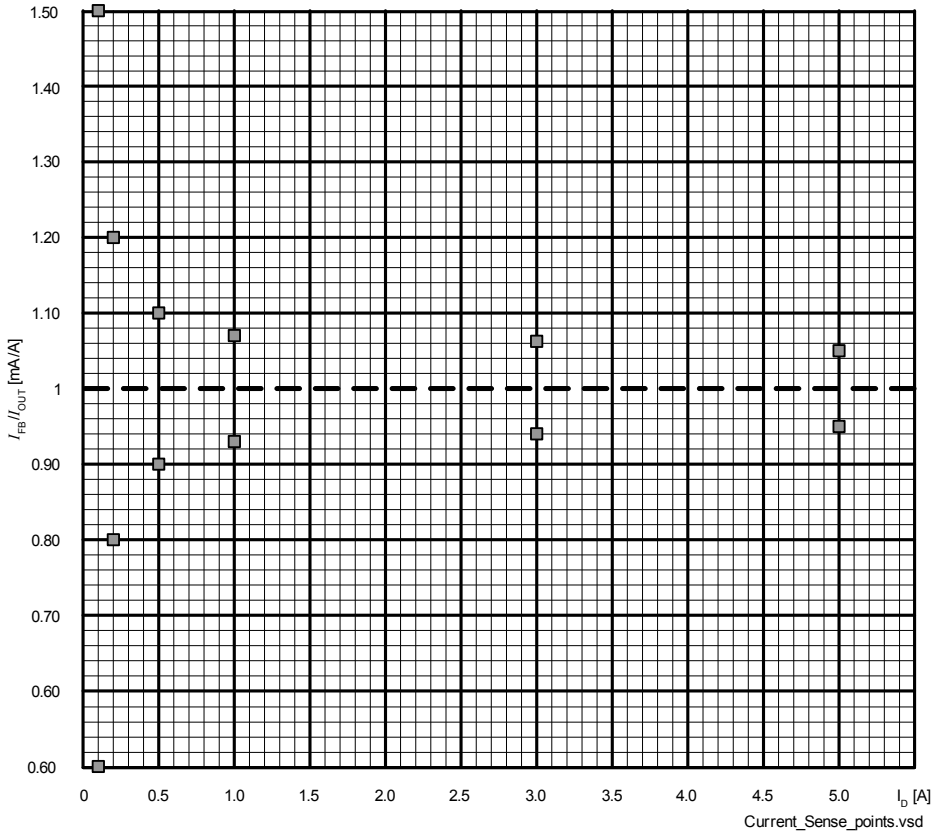


Figure 17 Current Sense Precision

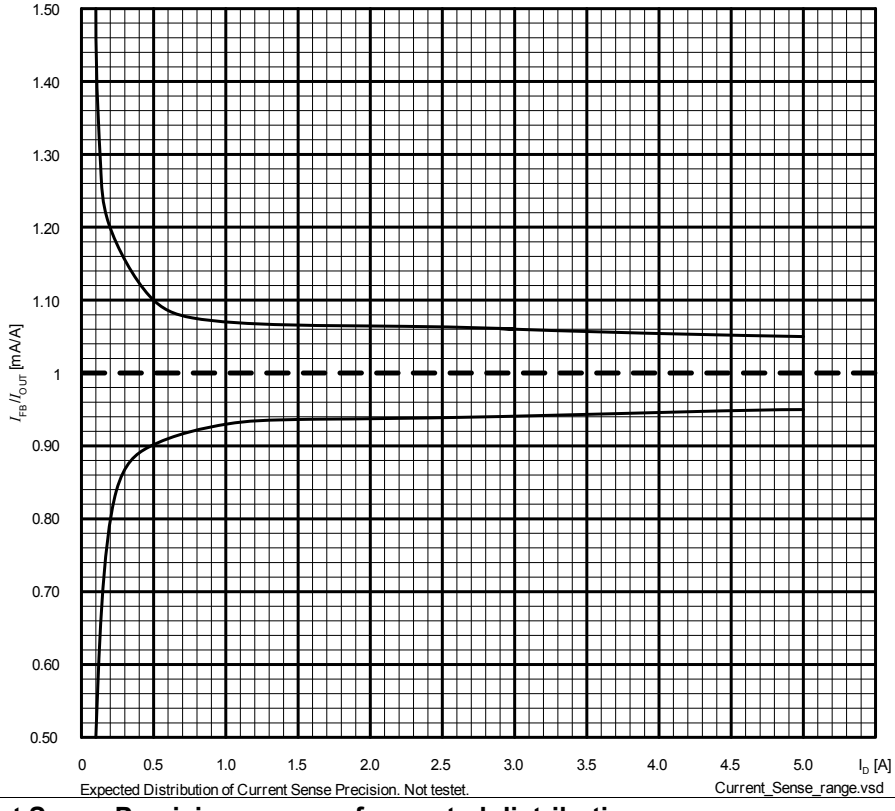


Figure 18 Current Sense Precision - range of expected distribution.

5.6 SPI Interface

The diagnosis and control interface is based on a serial peripheral interface (SPI).

The SPI is a full duplex synchronous serial slave interface, which uses four lines: SO, SI, SCLK and $\overline{CS}$. Data is transferred by the lines SI and SO at the data rate given by SCLK. The falling edge of $\overline{CS}$ indicates the beginning of a data access. Data is sampled in on line SI at the falling edge of SCLK and shifted out on line SO at the rising edge of SCLK. Each access must be terminated by a rising edge of $\overline{CS}$. The interface provides daisy chain capability.

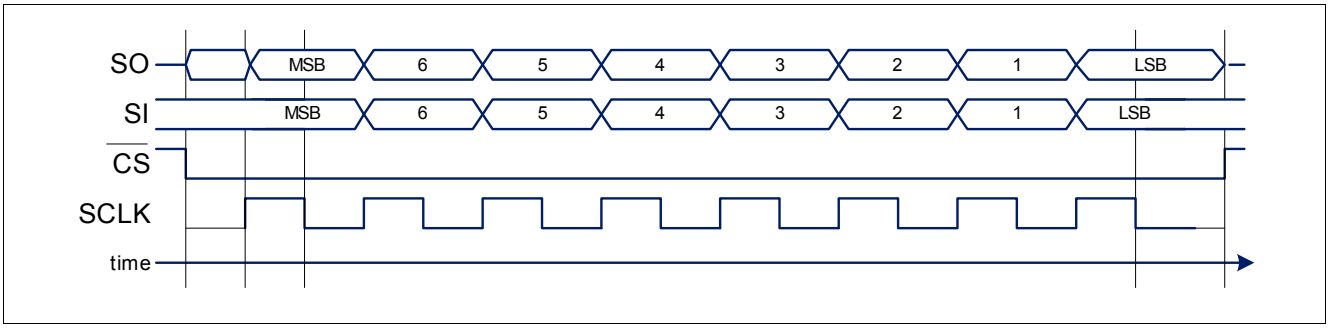


Figure 19 Serial Peripheral Interface

The SPI protocol is described in **Section 6**. All registers are reset to default values after power-on reset or if the chip is programmed via SPI to enter sleep mode.

5.6.1 SPI Signal Description

$\overline{CS}$ - Chip Select: The system micro controller selects the TLE8102SG by means of the $\overline{CS}$ pin. Whenever the pin is in low state, data transfer can take place. When $\overline{CS}$ is in high state, any signals at the SCLK and SI pins are ignored and SO is forced into a high impedance state.

$\overline{CS}$ High to Low transition:

- The diagnosis information is transferred into the shift register.

$\overline{CS}$ Low to High transition:

- Command decoding is only done after the falling edge of $\overline{CS}$ if the command is valid.
- Data from shift register is transferred into the input matrix register.
- The diagnosis flags are cleared.

SCLK - Serial Clock: This input pin clocks the internal shift register. The serial input (SI) transfers data into the shift register on the falling edge of SCLK while the serial output (SO) shifts diagnostic information out on the rising edge of the serial clock. It is essential that the SCLK pin is in low state whenever chip select $\overline{CS}$ makes any transition.

SI - Serial Input: Serial input data bits are shifted in at this pin, the most significant bit first. SI information is read on the falling edge of SCLK. The 8 bit input data consist of two parts (control and data). Please refer to **Section 6** for further information.

SO - Serial Output: Data is shifted out serially at this pin, the most significant bit first. SO is in high impedance state until the $\overline{CS}$ pin goes to low state. New data will appear at the SO pin following the rising edge of SCLK. Please refer to **Section 6** for further information.

5.6.2 Daisy Chain Capability

The SPI of TLE8102SG is daisy chain capable. In this configuration several devices are activated by the same signal $\overline{CS}$. The SI line of one device is connected with the SO line of another device (see **Figure 20**), which builds a chain. The ends of the chain are connected with the output and input of the master device, SO and SI respectively. The master device provides the master clock SCLK, which is connected to the SCLK line of each device in the chain.

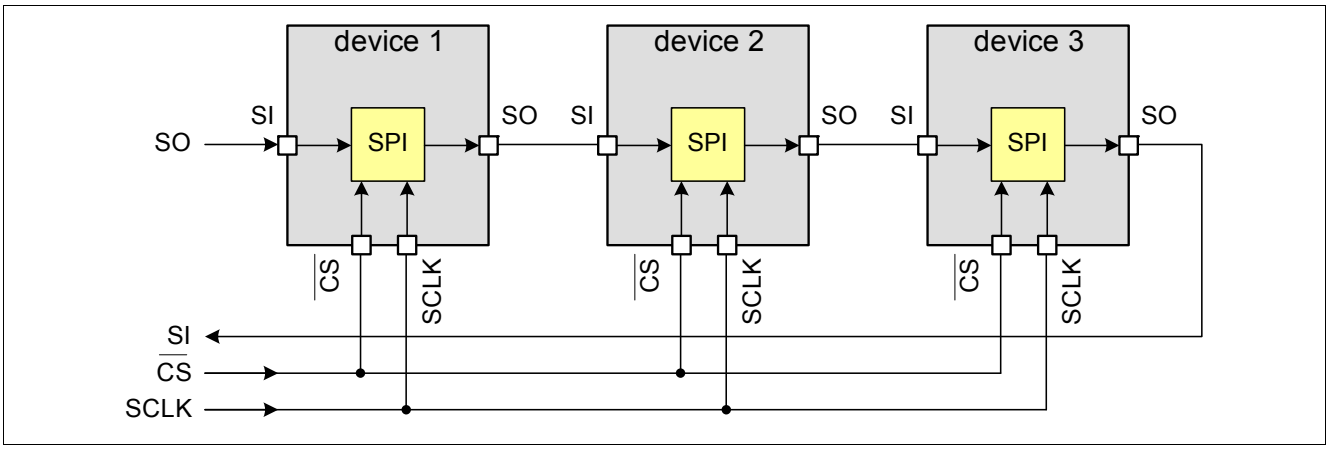


Figure 20 Daisy Chain Configuration

In the SPI block of each device, there is one shift register where one bit from SI line is shifted in each SCLK. The bit shifted out can be seen at SO. After 8 SCLK cycles, the data transfer for one device has been finished. In single chip configuration, the $\overline{CS}$ line must go high to make the device accept the transferred data. In daisy chain configuration the data shifted out at device 1 has been shifted in to device 2. When using three TLE8102SG devices in daisy chain, three times 8 bits have to be shifted through the devices. After that, the $\overline{CS}$ line must go high (see **Figure 21**).

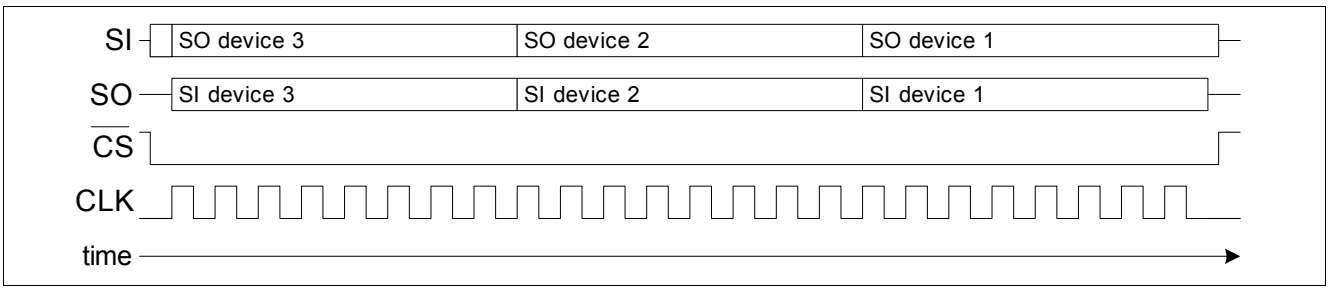


Figure 21 Data Transfer in Daisy Chain Configuration

Electrical Characteristics: SPI Interface

V_{DD} = 4.5 V to 5.5 V, T_j = -40 ·C to +150 ·C, (unless otherwise specified)
all voltages with respect to ground, positive current flowing into pin

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.6.1	Input Pull-down Current (SI, SCLK)	$I_{IN(SI,SCLK)}$	10	20	50	µA	–
5.6.2	Input Pull-up Current ($\overline{CS}$)	$I_{IN(CS)}$	10	20	50	µA	–

Electrical Characteristics: SPI Interface (cont'd)

V_{DD} = 4.5 V to 5.5 V, T_j = -40 ·C to +150 ·C, (unless otherwise specified)
all voltages with respect to ground, positive current flowing into pin

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.6.3	SO High State Output Voltage	V_{SOH}	V_{DD} - 0.4	–	–	V	I_{SOH} = 2 mA
5.6.4	SO Low State Output Voltage	V_{SOL}	–	–	0.4	V	I_{SOL} = 2.5 mA
5.6.5	Serial Clock Frequency (depending on SO load)	f_{SCK}	DC	–	5	MHz	–
5.6.6	Serial Clock Period ($1/f_{sclk}$)	$t_{p(SCK)}$	200	–	–	ns	–
5.6.7	Serial Clock High Time	t_{SCKH}	80	–	–	ns	–
5.6.8	Serial Clock Low Time	t_{SCKL}	80	–	–	ns	–
5.6.9	Enable Lead Time (falling edge of $\overline{CS}$ to rising edge of SCLK)	t_{lead}	200	–	–	ns	–
5.6.10	Enable Lag Time (falling edge of SCLK to rising edge of $\overline{CS}$)	t_{lag}	200	–	–	ns	–
5.6.11	Data Setup Time (required time SI to falling of SCLK)	t_{SU}	20	–	–	ns	–
5.6.12	Data Hold Time (falling edge of SCLK to SI)	t_H	20	–	–	ns	–
5.6.13	Disable Time[1)]	t_{DIS}	–	–	150	ns	–
5.6.14	Transfer Delay Time[2)] ($\overline{CS}$ high time between two accesses)	t_{dt}	300	–	–	ns	–
5.6.15	Data Valid Time	t_{valid}	– –	– –	120 150	ns	C_L = 50 pF[1)] C_L = 100 pF[1)]

1) Not subject to production test, specified by design.

2) This time is necessary between two write accesses. To get the correct diagnostic information, the transfer delay time has to be extended to the maximum fault delay time $t_{d(fault)max}$ = 200 µs.