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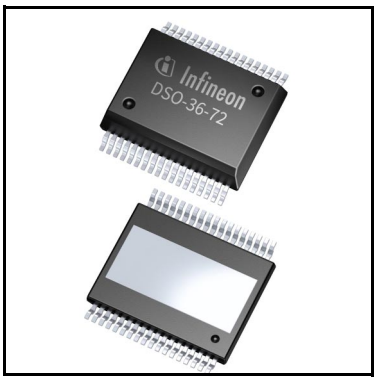
TLE8110ED

Smart Multichannel Low Side Switch with Parallel Control and SPI Interface



1 Overview

Features

- Overvoltage, Overtemperature, ESD-Protection
- Direct Parallel PWM Control of all Channels
- safeCOMMUNICATION (SPI and Parallel)
- Efficient Communication Mode: compactCONTROL
- Compatible with 3.3V- and 5V- Micro Controllers I/O ports
- clampSAFE for highly efficient parallel use of the channels
- Green Product
- AEC Qualified

Potential applications

- Power Switch Automotive and Industrial Systems switching Solenoids, Relays and Resistive Loads

Product validation

Qualified for Automotive Applications. Product Validation according to AEC-Q100/101.

Description

10-channel Low-Side Switch in Smart Power Technology [SPT] with **S**erial **P**eripheral **I**nterface [SPI] and 10 open drain DMOS output stages. The TLE8110ED is protected by embedded protection functions and designed for automotive and industrial applications. The output stages are controlled via Parallel Input Pins for PWM use or SPI Interface. The TLE8110ED is particularly suitable for Engine Management and Powertrain Systems.

Type	Package	Marking
TLE8110ED	PG-DSO-36-72	TLE8110ED

Overview

Table 1 Product Summary

Parameter	Symbol	Value	Unit
Analogue Suppy Voltage	V_{DD}	4.50 ... 5.50	V
Digital Supply Voltage	V_{CC}	3.00 ... 5.50	V
Clamping Voltage (CH 1-10)	$V_{DS(CL)typ}$	55	V
On Resistance maximum at T_j = 25°C and I_{Dnom}	R_{ON1-4}	0.30	Ω
	R_{ON5-6}	0.25	Ω
	R_{ON7-10}	0.60	Ω
On Resistance maximum at T_j = 150°C and I_{Dnom}	R_{ON1-4}	0.60	Ω
	R_{ON5-6}	0.50	Ω
	R_{ON7-10}	1.20	Ω
Nominal Output current (CH 1-4)	I_{Dnom}	1.50	A
Nominal Output current (CH 5-6)	I_{Dnom}	1.70	A
Nominal Output current (CH 7-10)	I_{Dnom}	0.75	A
Output Current Shut-down Threshold (CH 1-4) min.	$I_{DSD(low)}$	2.60	A
Output Current Shut-down Threshold (CH 5-6) min.	$I_{DSD(low)}$	3.70	A
Output Current Shut-down Threshold (CH 7-10) min.	$I_{DSD(low)}$	1.70	A

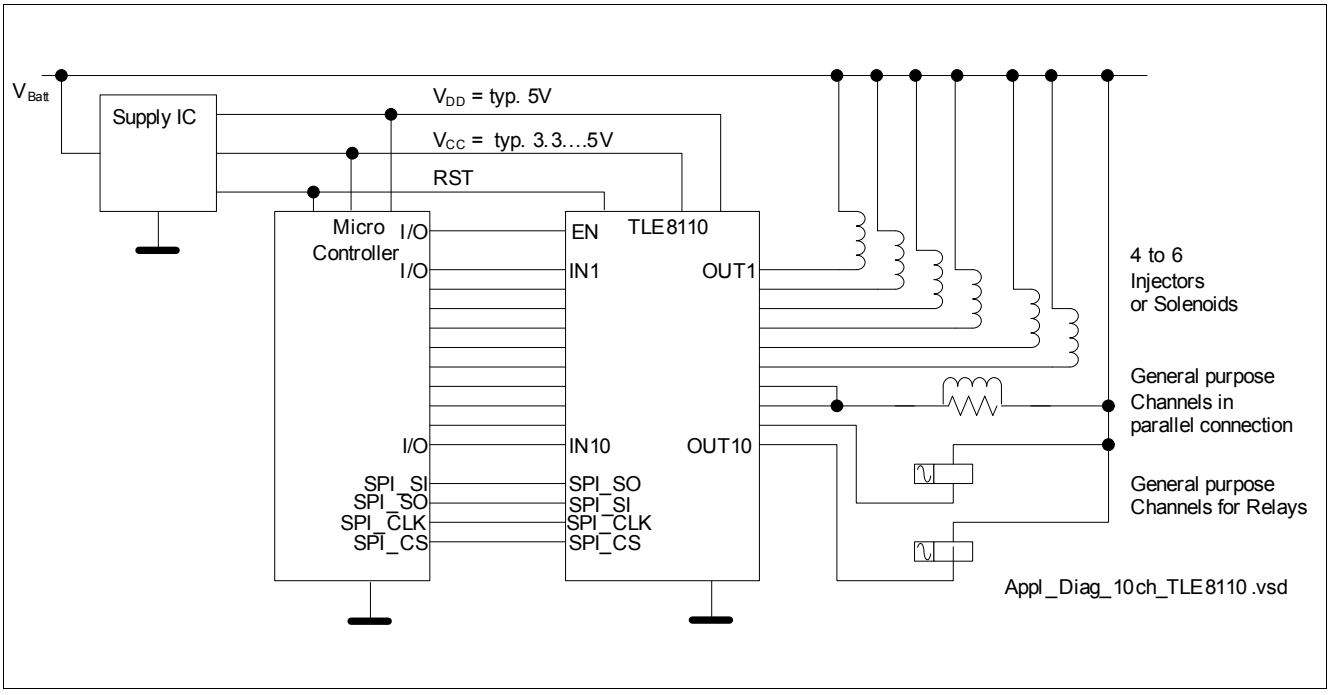


Figure 1 Block Diagram TLE8110ED

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2 Block Diagram

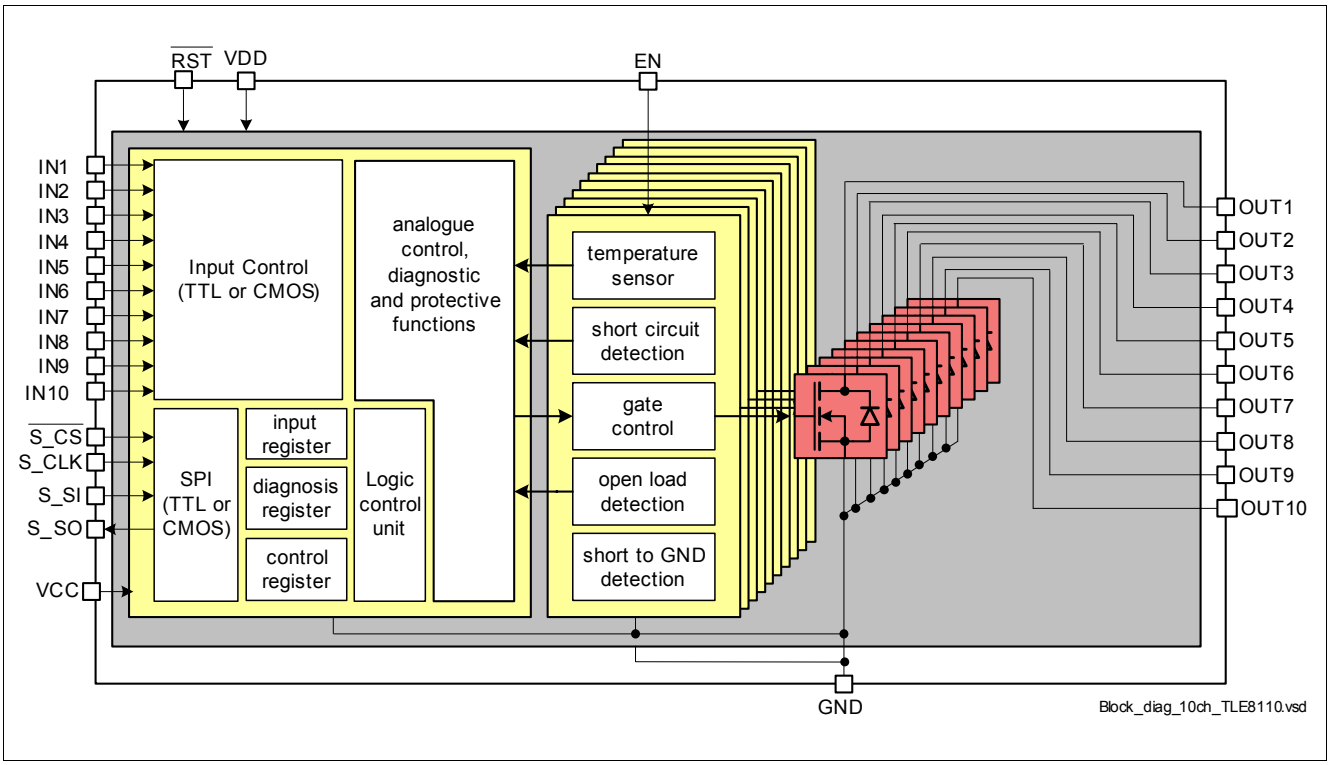

Figure 2 Block Diagram

2.1 Description

Communication

The TLE8110ED is a 10-channel low-side switch in PG-DSO-36-72 package providing embedded protection functions. The 16-bit serial peripheral interface (SPI) can be utilized for control and diagnosis of the device and the loads. The SPI interface provides daisy-chain capability in order to assemble multiple devices in one SPI chain by using the same number of micro-controller pins [1)].

The analogue and the digital part of the device is supplied by 5V. Logic Input and Output Signals are then compatible to 5V logic level [TTL - level]. Optionally, the logic part can be supplied with lower voltages to achieve signal compatibility with e.g. 3.3V logic level [CMOS - level].

The TLE8110ED is equipped with 10 parallel input pins that are routed to each output channel. This allows control of the channels for loads driven by Pulse Width Modulation (PWM). The output channels can also be controlled by SPI.

Reset

The device is equipped with one Reset Pin and one Enable. Reset [RST] serves the whole device, Enable [EN] serves only the Output Control Unit and the Power Stages.

1) Daisy Chain

Diagnosis

The device provides diagnosis of the load, including open load, short to GND as well as short circuit to VBatt detection and over-load/ over-temperature indication. The SPI diagnosis flags indicates if latched fault conditions may have occurred.

Protection

Each output stage is protected against short circuit. In case of over load, the affected channel is switched off. The switching off reaction time is dependent on two switching thresholds. Restart of the channel is done by clearing the Diagnosis Register [1]. This feature protects the device against uncontrolled repetitive short circuits.

There is a temperature sensor available for each channel to protect the device in case of over temperature. In case of over temperature the affected channel is switched off and the Over-Temperature Flag is set. Restart of the channel is done by deleting the Flag. This feature protects the device against uncontrolled temperature toggling.

Parallel Connection of Channels

The device is featured with a central clamping structure, so-called CLAMPsafe. This feature ensures a balanced clamping between the channels and allows in case of parallel connection of channels a high efficient usage of the channel capabilities. This parallel mode is additionally featured by best possible parameter- and thermal matching of the channels and by controlling the channels accordingly.

1) Restart after Clear

3 Pin Configuration

3.1 Pin Assignment

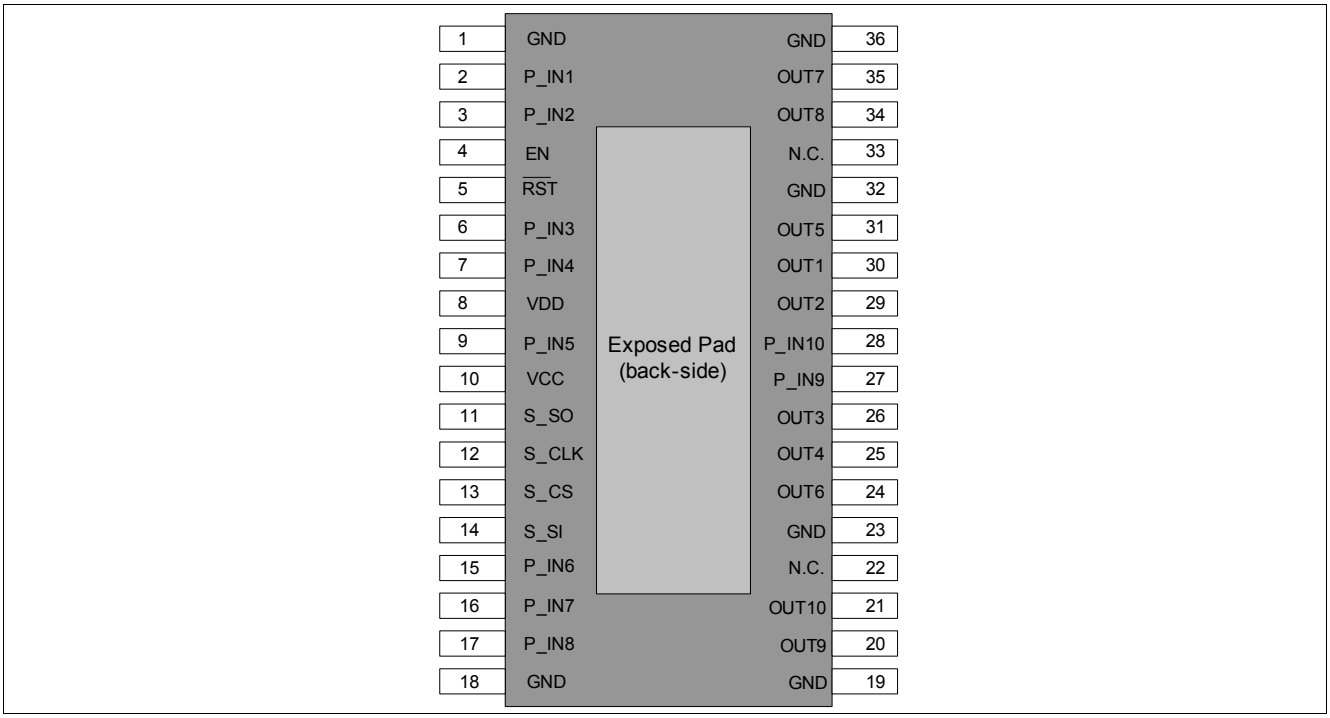

Figure 3 Pin Configuration

3.2 Pin Definitions and Functions

Pin	Symbol	Function
1	GND	Ground
2	P_IN1	Parallel Input Pin 1. Default assignment to Output Channel 1
3	P_IN2	Parallel Input Pin 2. Default assignment to Output Channel 2
4	EN	Enable Input Pin. If not needed, connect with Pull-up resistor to VCC
5	RST	Reset Input Pin (active low). If not needed, connect with Pull-up resistor to VCC
6	P_IN3	Parallel Input Pin 3. Default assignment to Output Channel 3
7	P_IN4	Parallel Input Pin 4. Default assignment to Output Channel 4
8	VDD	Analogue Supply Voltage
9	P_IN5	Parallel Input Pin 5. Default assignment to Output Channel 5
10	VCC	Digital Supply Voltage
11	S_SO	Serial Peripheral Interface [SPI], Serial Output
12	S_CLK	Serial Peripheral Interface [SPI], Clock Input
13	S_CS	Serial Peripheral Interface [SPI], Chip Select (active low)
14	S_SI	Serial Peripheral Interface [SPI], Serial Input
15	P_IN6	Parallel Input Pin 6. Default assignment to Output Channel 6

Pin	Symbol	Function
16	P_IN7	Parallel Input Pin 7. Default assignment to Output Channel 7
17	P_IN8	Parallel Input Pin 8. Default assignment to Output Channel 8
18	GND	Ground
19	GND	Ground
20	OUT9	Drain of Power Transistor Channel 9
21	OUT10	Drain of Power Transistor Channel 10
22	N.C.	internally not connected, connect to Ground
23	GND	Ground
24	OUT6	Drain of Power Transistor Channel 6
25	OUT4	Drain of Power Transistor Channel 4
26	OUT3	Drain of Power Transistor Channel 3
27	P_IN9	Parallel Input Pin 9. Default assignment to Output Channel 9
28	P_IN10	Parallel Input Pin 10. Default assignment to Output Channel 10
29	OUT2	Drain of Power Transistor Channel 2
30	OUT1	Drain of Power Transistor Channel 1
31	OUT5	Drain of Power Transistor Channel 5
32	GND	Ground
33	N.C.	internally not connected, connect to Ground
34	OUT8	Drain of Power Transistor Channel 8
35	OUT7	Drain of Power Transistor Channel 7
36	GND	Ground
Exposed Pad		internally not connected, connect to Ground

Note: The exposed pad of TLE8110ED is not connected to ground pins internally. It is highly recommended to connect the exposed pad to GND pins on the PCB.

3.3 Terms

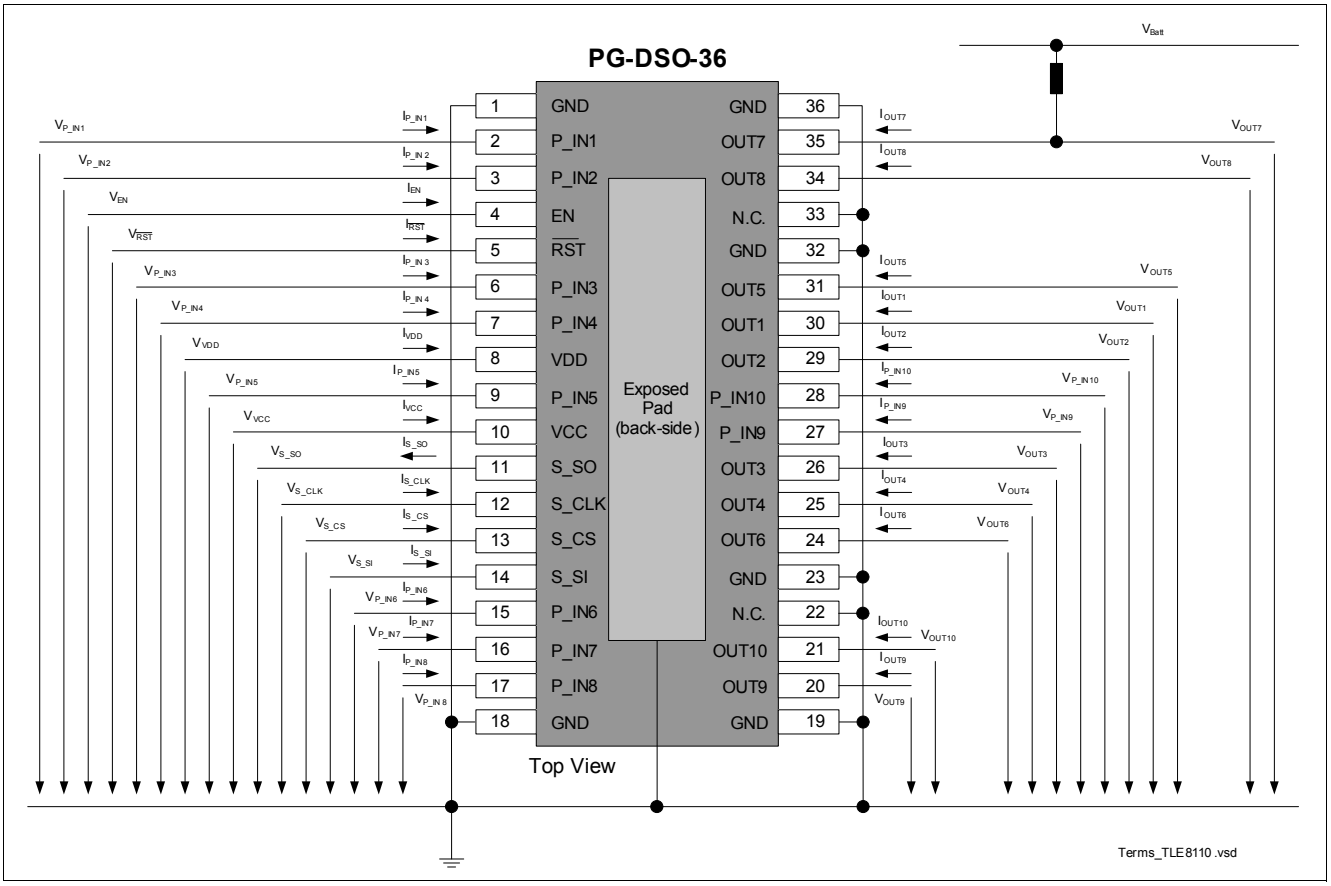

Figure 4 Terms

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings [1)]

T_j = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Supply Voltages							
Digital Supply voltage	V_{CC}	-0.3	–	5.5	V	permanent	P_4.1.1
Digital Supply voltage	V_{CC}	-0.3	–	6.2	V	t < 10s	P_4.1.2
Analogue Supply voltage	V_{DD}	-0.3	–	5.5	V	permanent	P_4.1.3
Analogue Supply voltage	V_{DD}	-0.3	–	6.2	V	t < 10s	P_4.1.4
Power Stages							
Load Current (CH 1 to 10)	I_{Dn}	–	–	$I_{DSD(low)}$	A	–	P_4.1.5
Reverse Current Output (CH 1- 10)	I_{Dn}	$-I_{DSD(low)}$	–	-	A	–	P_4.1.6
Total Ground Current	I_{GND}	-20	–	20	A	–	P_4.1.7
Continuous Drain Source Voltage (Channel 1 to 10)	V_{DSn}	-0.3	–	45	V	–	P_4.1.8
maximum Voltage for short circuit protection on Output	V_{DSn}	–	–	24	V	one event on one single channel	P_4.1.9
Clamping Energy - Single Pulse [2) 3)]							
Single Clamping Energy Channel Group 1-4	E_{AS}	–	–	29	mJ	I_D = 2.6A, 1 single pulse	P_4.1.10
Single Clamping Energy Channel Group 5-6	E_{AS}	–	–	31	mJ	I_D = 3.7A, 1 single pulse	P_4.1.11
Single Clamping Energy Channel Group 7-10	E_{AS}	–	–	11	mJ	I_D = 1.7A, 1 single pulse	P_4.1.12
Logic Pins (SPI, INn, EN, RST)							
Input Voltage at all Logic Pin	V_x	-0.3	–	5.5	V	permanent	P_4.1.13
Input Voltage at all Logic Pin	V_x	-0.3	–	6.2	V	t < 10s	P_4.1.14
Input Voltage at Pin 27, 28 (IN9, 10)	V_x	-0.3	–	45	V	permanent	P_4.1.15
Temperatures							
Junction Temperature	T_j	-40	–	150	°C	–	P_4.1.16
Junction Temperature	T_j	-40	–	175	°C	max. 100hrs cumulative	P_4.1.17
Storage Temperature	T_{stg}	-55	–	150	°C	–	P_4.1.18
ESD Robustness							

Table 2 Absolute Maximum Ratings [1)] (cont'd)

T_j = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Electro Static Discharge Voltage "Human Body Model - HBM"	V_{ESD}	-4	–	4	kV	All Pins HBM, [4)] 1.5KOhm, 100pF	P_4.1.19
Electro Static Discharge Voltage "Charged Device Model - CDM"	V_{ESD}	-500	–	500	V	All Pins CDM [5)]	P_4.1.20
Electro Static Discharge Voltage "Charged Device Model - CDM"	V_{ESD}	-750	–	750	V	Pin 1, 18, 19, 36 (corner pins) CDM [5)]	P_4.1.21

1) Not subject to production test, specified by design.
2) One single channel per time.
3) Triangular Pulse Shape (inductance discharge): $I_D(t) = I_D(0)\cdot(1 - t / t_{pulse})$; $0 < t < t_{pulse}$.
4) ESD susceptibility, HBM according to EIA/JESD 22-A114-B.
5) ESD susceptibility, Charged Device Model "CDM" EIA/JESD22-C101-C.

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.*

4.2 Functional Range

Table 3 Functional Range

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Supply Voltages							
Analogue Supply Voltage	V_{DD}	4.5	–	5.5	V	–	P_4.2.1
Digital Supply Voltage	V_{CC}	3	–	V_{DD}	V	–	P_4.2.2
Digital Supply Voltage	V_{CC}	V_{DD}	–	5.5	V	leakage Currents (ICC) might increase if $V_{CC} > V_{DD}$	P_4.2.3
Power Stages							
Ground Current	I_{GND_typ}		9		A	resistive loads [1)]	P_4.2.4
Temperatures							
Junction Temperature	T_j	-40	–	150	°C	–	P_4.2.5
Junction Temperature	T_j	-40	–	175	°C	for 100hrs [1)]	P_4.2.6

1) Not subject to production test, specified by design

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

4.3 Thermal Resistance

Table 4 Thermal Resistance

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction to Soldering Point	R_{thJC}		1	1.50	K/W	P_{vtot} = 3W 1) 2)	P_4.3.1

1) Not subject to production test, specified by design.
2) Homogenous power distribution over all channels (All Power stages equally heated), dependent on cooling set-up.

5 Power Supply

5.1 Description Power Supply

The TLE8110ED is supplied by analogue power supply line V_{DD} which is used for the analogue functions of the device, such as the gate control of the power stages. The digital power supply line V_{CC} is used to supply the digital part and offers the possibility to adapt the logic level of the serial output pins to lower logic levels.

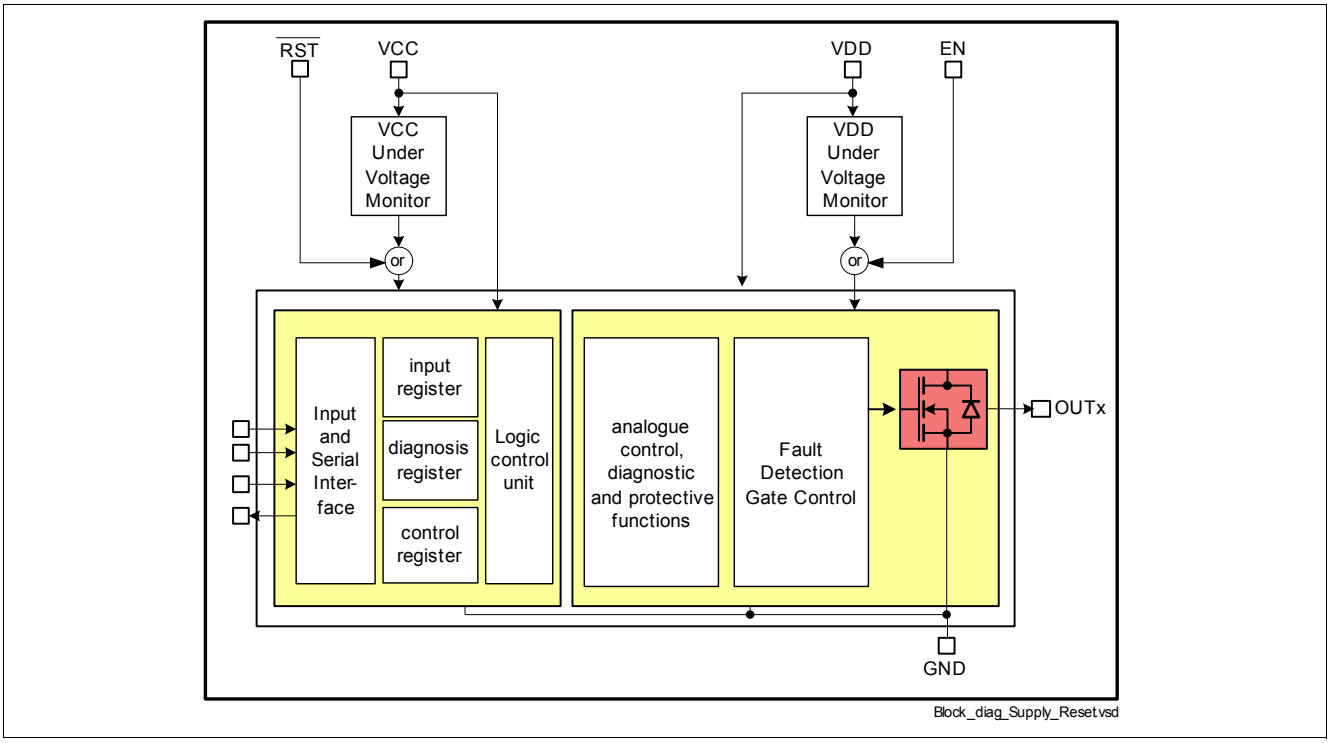

Figure 5 Block Diagram Supply and Reset

Description Supply

The Supply Voltage Pins are monitored during the power-on phase and under normal operating conditions for under voltage.

If during Power-on the increasing supply voltage exceeds the Supply Power-on Switching Threshold, the internal Reset is released after an internal delay has expired.

In case of under voltage, a device internal reset is performed. The Switching Threshold for this case is the Power-on Switching threshold minus the Switching Hysteresis.

In case of under voltage on the analogue supply line V_{DD} the outputs are turned off but the content of the registers and the functionality of the logic part is kept alive. In case of under voltage on the digital supply V_{CC} line, a complete reset including the registers is performed.

After returning back to normal supply voltage and an internal delay, the related functional blocks are turned on again. For more details, refer to the chapter “Reset”.

The device internal under-voltage set will set the related bits in SDS (Short Diagnosis and Device Status) to allow the micro controller to detect this reset. For more information, refer to the chapter “Control of the Device”.

5.2 Electrical Characteristics Power Supply

Table 5 Electrical Characteristics: Power Supply

3.0V < V_{CC} < 5.5V; 4.5V < V_{DD} < 5.5V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Digital Supply and Power-on Reset							
Digital Supply Voltage	V_{CC}	3	–	5.5	V	–	P_5.2.1
Digital Supply Current during Reset (V_{CC} < V_{CCpo})	I_{CCstb}	–	15	20	µA	f_{SCLK} = 0Hz, S_CS = V_{CC}, T_j = 85°C, V_{CC} = 2.0 V, V_{DD} > V_{CC}, 1)	P_5.2.2 a)
		–	20	40	µA	f_{SCLK} = 0Hz, S_CS = V_{CC}, Tj = 150°C, V_{CC} = 2.0V, V_{DD} > V_{CC}	b)
Digital Supply Current during Reset ($\overline{VRST}$ > VRSTI)	I_{CCstb}	–	2	5	µA	f_{SCLK} = 0Hz, S_CS = V_{CC}, T_j = 85°C, V_{DD} > V_{CC}, 1)	P_5.2.3 a)
		–	5	15	µA	f_{SCLK} = 0Hz, S_CS = V_{CC}, T_j = 150°C, V_{DD} > V_{CC}	b)
Digital Supply Operating Current V_{CC} = 3.3V	I_{CC}	–	0.15	2	mA	f_{SCLK} = 0Hz, T_j = 150°C, all Channels ON, 1)	P_5.2.4 a)
		–	0.5	5	mA	f_{SCLK}= 5MHz, T_j = 150°C, all Channels ON, 1) 2)	b)
Digital Supply Operating Current V_{CC} = 5.5V	I_{CC}	–	0.25	2	mA	f_{SCLK} = 0Hz, T_j = 150°C, all Channels ON	P_5.2.5 a)
		–	0.8	10	mA	f_{SCLK} = 5MHz, T_j = 150°C, all Channels ON, 1) 2)	b)
Digital Supply Power-on Switching Threshold	V_{CCpo}	1.9	2.8	3	V	V_{CC} increasing	P_5.2.6

Table 5 Electrical Characteristics: Power Supply

3.0V < V_{CC} < 5.5V; 4.5V < V_{DD} < 5.5V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Digital Supply Switching Hysteresis	V_{CChy}	100	300	500	mV	1)	P_5.2.7
Analogue Supply and Power-on Reset							
Analogue Supply Voltage	V_{DD}	4.5	–	5.5	V	–	P_5.2.8
Analogue Supply Current during Reset (V_{DD} < V_{DDpo})	I_{DDstb}	–	10	20	µA	f_{SCLK} = 0Hz, T_j = 85°C, V_{DD} = 2V, 1)	P_5.2.9 a)
		–	15	40	µA	f_{SCLK} = 0Hz, T_j = 150°C, V_{DD} = 2V	b)
Analogue Supply Current during Reset (V_{EN} < V_{ENI})	I_{DDstb}	–	1	5	µA	f_{SCLK} = 0Hz, T_j = 85°C, 1)	P_5.2.10 a)
		–	2	15	µA	f_{SCLK} = 0Hz, T_j = 150°C	b)
Analogue Supply Operating Current	I_{DD}	–	8	25	mA	f_{SCLK} = 0...5MHz, T_j = 150°C, all Channels ON, 1)	P_5.2.11
Analogue Supply Power-on Switching Threshold	V_{DDpo}	3	4.2	4.5	V	V_{DD} increasing	P_5.2.12
Analogue Supply Switching Hysteresis	V_{DDhy}	100	200	400	mV	1)	P_5.2.13
Analogue Supply Power-on Delay Time	t_{VDDpo}	-	100	200	µs	V_{DD} increasing, 1)	P_5.2.14

1) Parameter not subject to production test. Specified by design.

2) C = 50pF connected to S_SO.

6 Reset and Enable Inputs

6.1 Description Reset and Enable Inputs

The TLE8110ED contains one Reset- and one Enable Input Pin as can be seen in **Figure 5**.

Description:

Reset Pin [$\overline{RST}$] is the main reset and acts as the internal under voltage reset monitoring of the digital supply voltage V_{CC}: As soon as $\overline{RST}$ is pulled low, the whole device including the control registers is reset.

The Enable Pin [EN] resets only the Output channels and the control circuits. The content of the all registers is kept. This functions offers the possibility of a “soft” reset turning off only the Output lines but keeping alive the SPI communication and the contents of the control registers. This allows the read out of the diagnosis and setting up the device during or directly after Reset.

6.2 Electrical Characteristics Reset Inputs

Table 6 Electrical Characteristics: $\overline{Reset}$ Inputs

3.0V < V_{CC} < 5.5V; 4.5V < V_{DD} < 5.5V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Reset Input Pin [$\overline{RST}$]							
Low Level of $\overline{RST}$	V_{RSTl}	-0.3	–	V_{CC}*0.2	V	–	P_6.2.1
High Level of $\overline{RST}$	V_{RSTh}	V_{CC}*0.4	–	V_{CC}	V	–	P_6.2.2
$\overline{RST}$ Switching Hysteresis	V_{RSThy}	20	100	300	mV	1)	P_6.2.3
Reset Pin pull-down Current	$I_{RSTresh}$	20	40	85	µA	$V_{\overline{RST}}$ = 5V	P_6.2.4
	$I_{RSTresl}$	2.4	–	–	µA	$V_{\overline{RST}}$ = 0.6 V, 1)	
Required Reset Duration time $\overline{RST}$	t_{RSTmin}	2	–	–	µs	1)	P_6.2.5
Enable Input Pin [EN]							
Low Level of EN	V_{ENl}	-0.3	-	V *0.2	V_{CC}*0.2	–	P_6.2.6
High Level of EN	V_{ENh}	V_{CC} *0.4	-	VCC	V	–	P_6.2.7
EN Switching Hysteresis	V_{ENhy}	20	60	300	mV	1)	P_6.2.8
Enable Pin pull-down Current	I_{ENresh}	5	35	85	µA	$V_{\overline{EN}}$ = 5V	P_6.2.9
	I_{ENresl}	2.4	–	–	µA	$V_{\overline{EN}}$ = 0.6V, 1)	
Enable Reaction Time (reaction of OUTx)	t_{ENrr}	–	4	–	µs	1)	P_6.2.10
Required Enable Duration time EN	t_{ENmin}	2	–	–	µs	1)	P_6.2.11

1) Parameter not subject to production test. Specified by design.

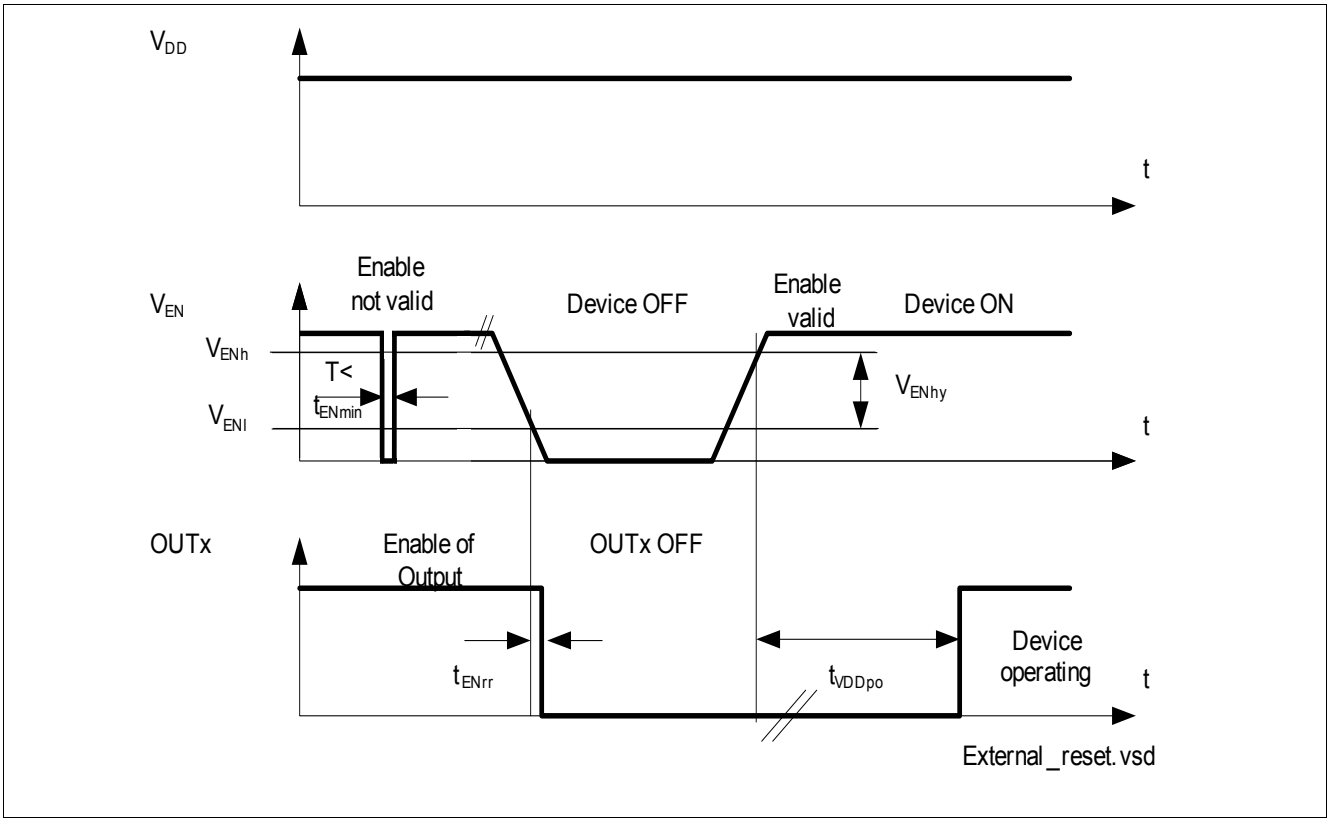

Figure 6 Timing

7 Power Outputs

7.1 Description Power Outputs

The TLE8110ED is a 10 channel low-side powertrain switch. The power stages are built by N-channel power MOSFET transistors. The device is a universal multichannel switch but mostly suited for the use in Engine Management Systems [EMS]. Within an EMS, the best fit of the channels to the typical loads is:

- Channel 1 to 4 for Injector valves or mid-sized solenoids with a nominal current requirement of 1.5A,
- Channel 5 to 6 for mid-sized solenoids or Injector valves with nominal current requirement of 1.7A,
- Channel 7 to 10 for small solenoids or relays with a nominal current requirement of 0.75A.

Channel 1 to 10 provide enhanced clamping capabilities of typically 55V best suited for inductive loads such as injectors and valves. It is recommended in case of an inductive load, to connect an external free wheeling- or clamping diode, where-ever possible to reduce power dissipation.

All channels can be connected in parallel. Channels 1 to 4, 5 to 6 and 7 to 10 are prepared by matching for parallel connection with the possibility to use a high portion of the capability of each single channel also in parallel mode (refer to **Chapter 7.4**).

Channel 5 and 6 have a higher current shut down threshold to allow to connect in parallel mode a load with high inrush-current, such as a lambda sensor heater.

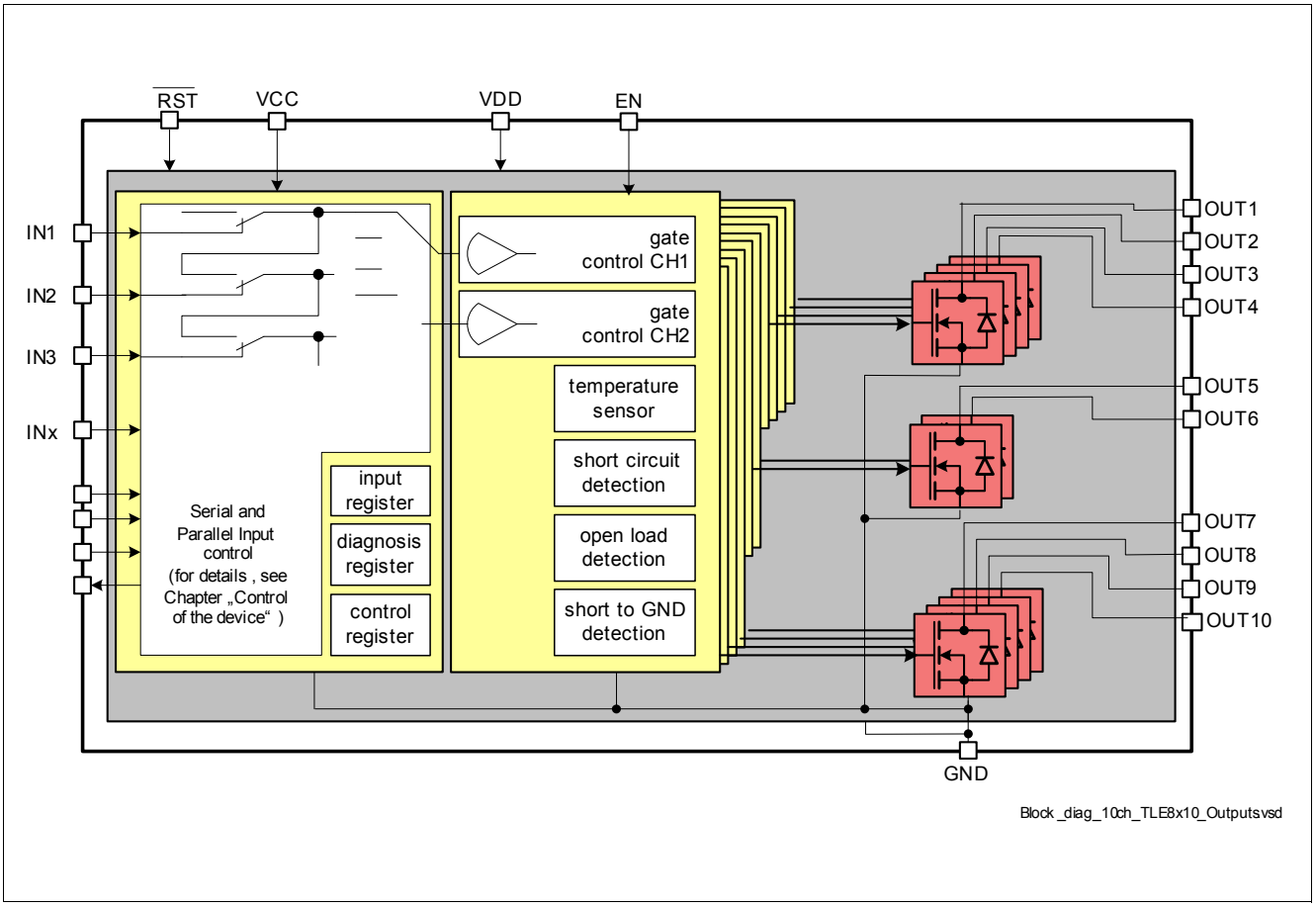

Figure 7 Block Diagram of Control and Power Outputs

7.2 Description of the Clamping Structure

When switching off inductive loads, the potential at pin OUT rises to $V_{DS(CL)}$ potential, because the inductance intends to continue driving the current. The clamping voltage is necessary to prevent destruction of the device, see **Figure 8** for the clamping circuit principle. Nevertheless, the maximum allowed load inductance is limited.

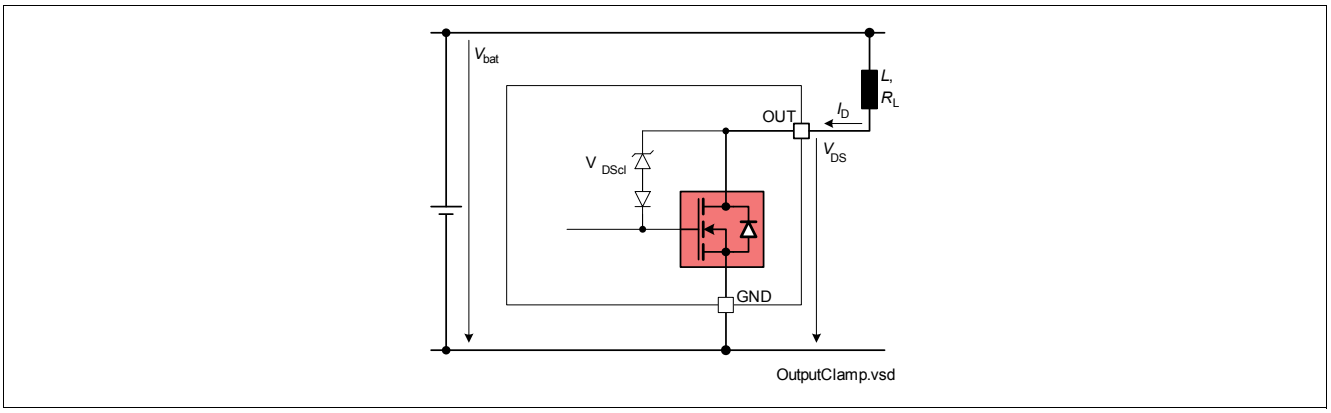

Figure 8 Internal Clamping Principle

Clamping Energy

During demagnetization of inductive loads, energy has to be dissipated in the device. This energy can be calculated with following equation:

$$E = V_{DS(CL)} \cdot \frac{L_L}{R_L} \cdot \left[I_L - \frac{V_{DS(CL)} - V_{BAT}}{R_L} \cdot \ln\left(1 + \frac{R_L \cdot I_L}{V_{DS(CL)} - V_{BAT}} \right) \right] \quad (7.1)$$

The maximum energy, which is converted into heat, is limited by the thermal design of the component.

Attention: ***It is strongly recommended to measure the load Energy and Current under operating conditions, example of measurement setup is shown in Figure 9. Load small-signal parameters might not reflect the real load behavior under operating conditions, see Figure 10. For more details please refer to the Application Note "Switching Inductive Loads".***

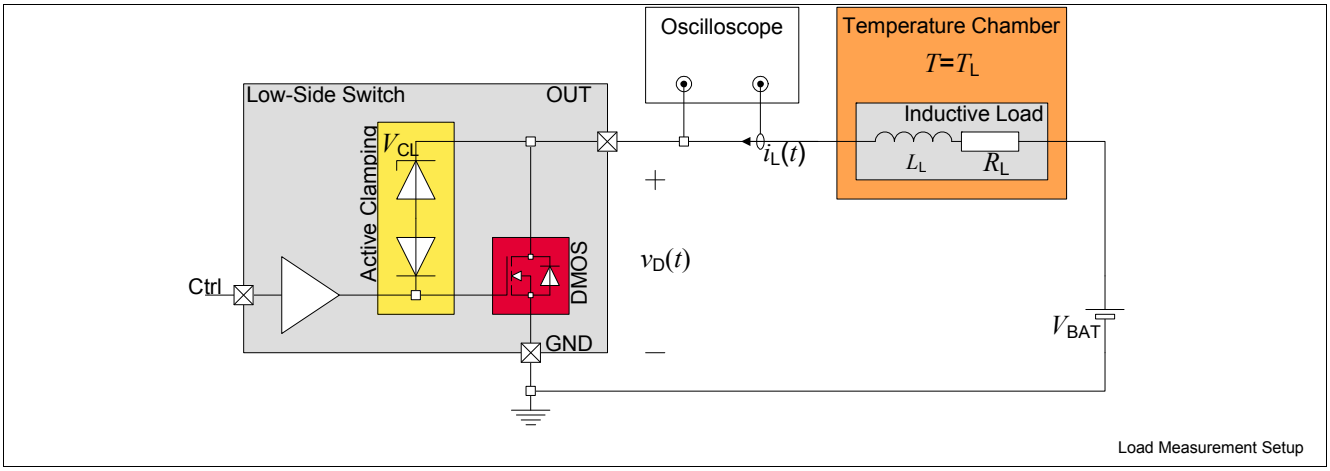

Figure 9 E_{CL} measurement setup

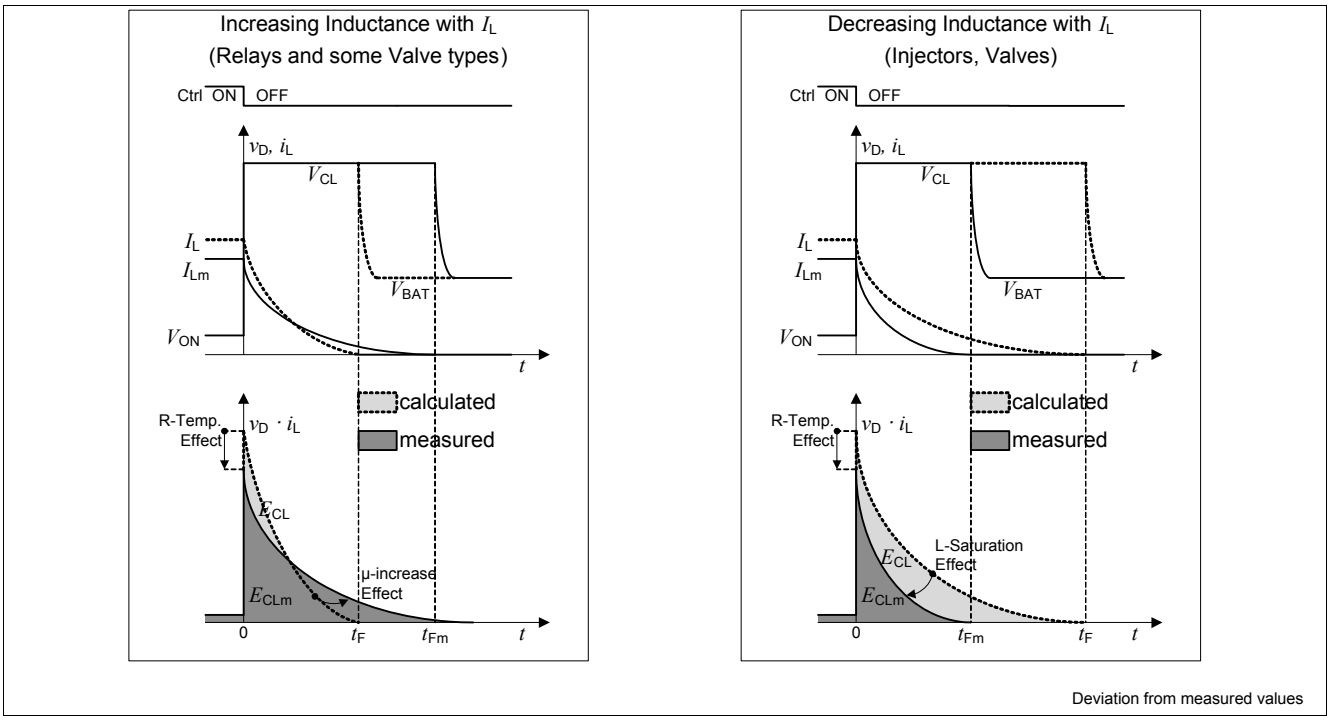

Figure 10 Deviation of calculation from measurement

7.3 Electrical Characteristics Power Outputs

Table 7 Electrical Characteristics: Power Outputs

3.0V < V_{CC} < 5.5V; 4.5V < V_{DD} < 5.5V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output Channel Resistance							
On State Resistance Channel Group 1-4	R_{DSon}	–	0.3	–	Ohm	I_{Dnom} = 1.5A, Tj = 25°C [1]	P_7.3.1
		–	0.45	0.6	Ohm	I_{Dnom} = 1.5A, T_j = 150°C	
On State Resistance Channel Group 5-6	R_{DSon}	–	0.25	–	Ohm	I_{Dnom} = 1.7A, T_j = 25°C [1]	P_7.3.2
		–	0.35	0.5	Ohm	I_{Dnom} = 1.7A, T_j = 150°C	
On State Resistance Channel Group 7-10	R_{DSon}	–	0.6	–	Ohm	I_{Dnom} = 0.75A, T_j = 25°C [1]	P_7.3.3
		–	0.85	1.2	Ohm	I_{Dnom}=0.75A, T_j = 150°C	
Clamping Energy - Repetitive[1)2)3)4)] Channel Group 1-4							
Repetitive Clamping Energy	E_{AR}	–	–	11	mJ	I_D = 1.0A, 10^9 cycles	P_7.3.4
		–	–	12	mJ	I_D = 2.1A, 10^4 cycles	
		–	–	15	mJ	I_D = 2.6A, 10 cycles [5]	
Channel 5-6							
Repetitive Clamping Energy	E_{AR}	–	–	13	mJ	I_D = 1.3A, 10^9 cycles	P_7.3.5
		–	–	15	mJ	I_D = 2.7A, 10^4 cycles	
		–	–	20	mJ	I_D = 3.2A, 10 cycles [5]	
Channel 7-10							
Repetitive Clamping Energy	E_{AR}	–	–	4	mJ	I_D = 0.7A, 10^9 cycles	P_7.3.6
		–	–	4	mJ	I_D = 1.4A, 10^4 cycles	
		–	–	5	mJ	I_D = 1.7A, 10 cycles [5]	

Table 7 Electrical Characteristics: Power Outputs (cont'd)

3.0V < V_{CC} < 5.5V; 4.5V < V_{DD} < 5.5V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Leakage Current							
Output Leakage Current in standby mode, Channel 1 to 4	I_{Doff}	–	–	3	µA	V_{DS} = 13.5V, V_{DD} = 5V, T_j = 85°C 1)	P_7.3.7
		–	–	8	µA	V_{DS} = 13.5V, V_{DD} = 5V, T_j = 150°C	
Output Leakage Current in standby mode, Channel 5 to 6	I_{Doff}	–	–	6	µA	V_{DS} = 13.5V, V_{DD} = 5V, T_j = 85°C 1)	P_7.3.8
		–	–	12	µA	V_{DS} = 13.5V, V_{DD} = 5V, T_j = 150°C	
Output Leakage Current in standby mode, Channel 7 to 10	I_{Doff}	–	–	2	µA	V_{DS} = 13.5V, V_{DD} = 5V, T_j = 85°C 1)	P_7.3.9
		–	–	5	µA	V_{DS} = 13.5V, V_{DD} = 5V, T_j = 150°C	
Clamping Voltage							
Output Clamping Voltage, Channel 1 to 10	V_{DScl}	45	55	60	V	–	P_7.3.10
Timing							
Output Switching Frequency	f_{OUTx}	–	–	20	kHz	1) resistive load, duty cycle > 25%	P_7.3.11
Turn-on Time	t_{dON}	–	5	10	µs	V_{DS} = 20% of Vbatt V_{batt} = 13.5V, I_{DS1} to I_{DS6} = 1A, I_{DS7} to I_{DS10} = 0.5A, resistive load	P_7.3.12
Turn-off Time	t_{dOFF}	–	5	10	µs	V_{DS} = 80% of V_{batt} V_{batt} = 13.5V, I_{DS1} to I_{DS6} = 1A, I_{DS7} to I_{DS10} = 0.5A, resistive load	P_7.3.13

1) Parameter is not subject to production test, specified by design.

2) Either one of the values has to be considered as worst case limitation. Cumulative scenario and wide range of operating conditions are treated in the Application Note "Switching Inductive Loads - TLE8110 addendum".

3) This lifetime statement is an anticipation based on an extrapolation of Infineon's qualification test results. The actual lifetime of a component depends on its form of application and type of use etc. and may deviate from such statement. The lifetime statement shall in no event extend the agreed warranty period.
4) Triangular Pulse Shape (inductance discharge): $I_D(t) = I_D(0) \cdot (1 - t / t_{pulse})$; $0 < t < t_{pulse}$.
5) Repetitive operation not allowed. Starting T_j must be kept within specs. In case of high energy pulse an immediate switch-off strategy is recommended.

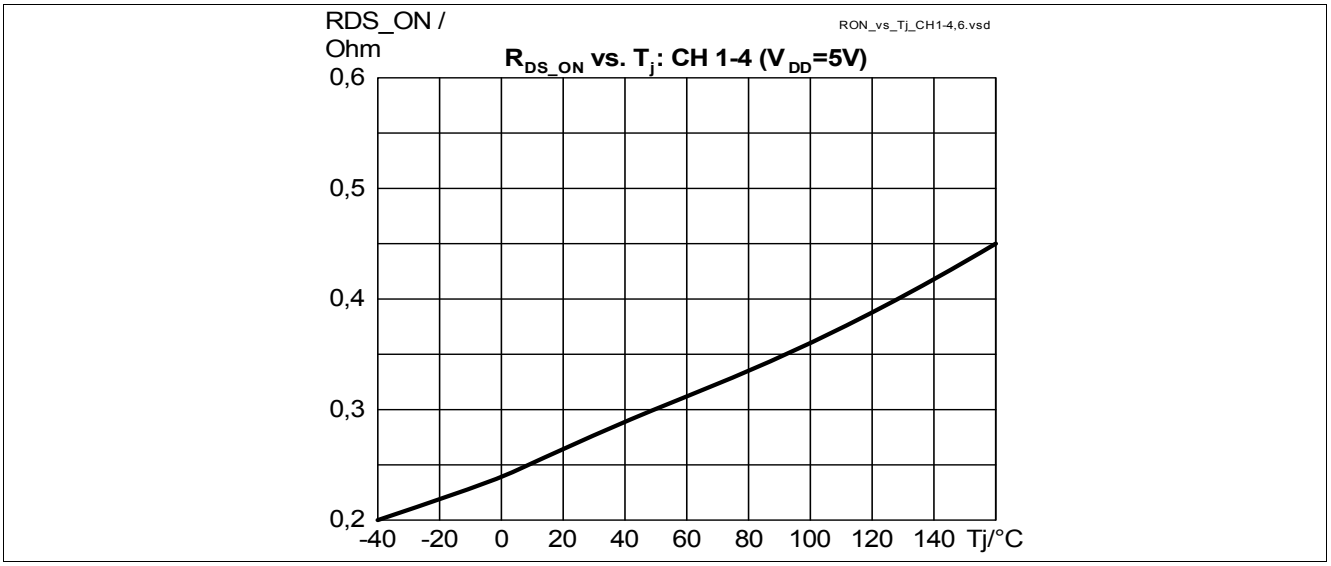

Figure 11 CH 1-4: typical behavior of RDS_ON versus the junction temperature Tj

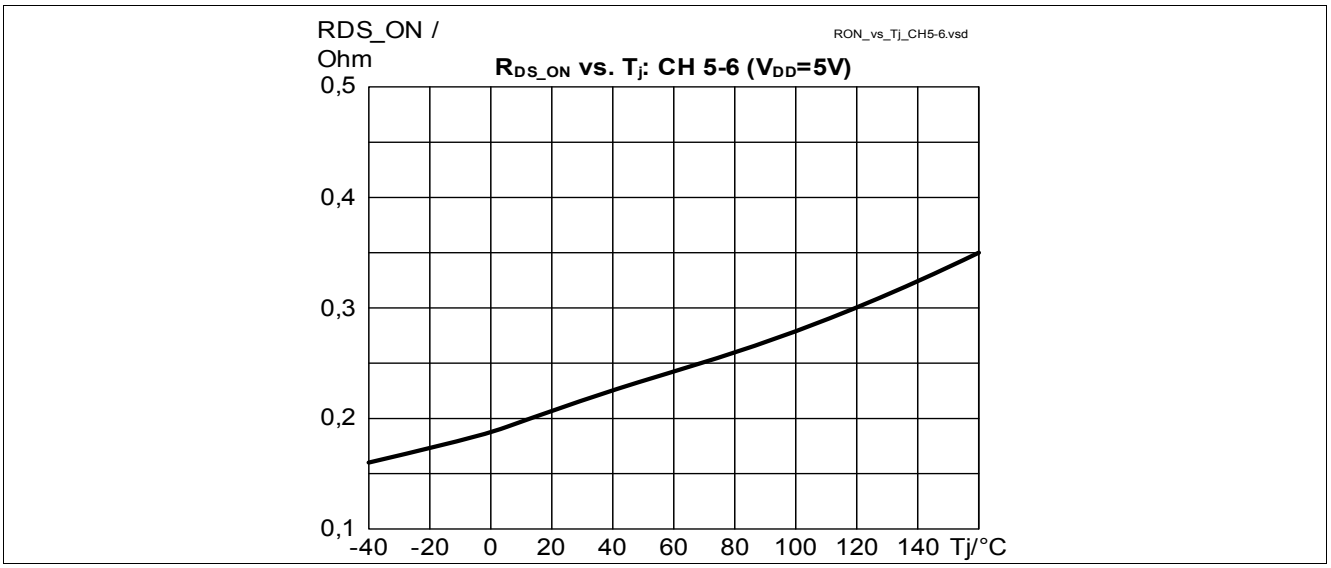

Figure 12 CH5-6: typical behavior of RDS_ON versus the junction temperature Tj

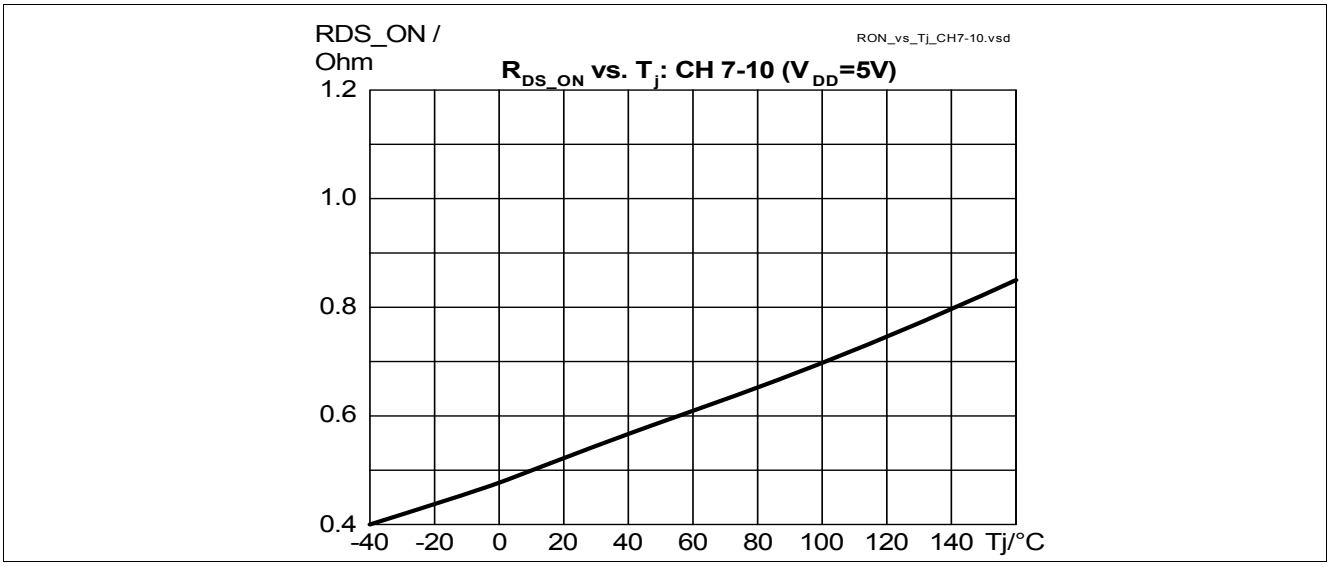

Figure 13 CH7-10: typical behavior of RDS_ON versus the junction temperature Tj

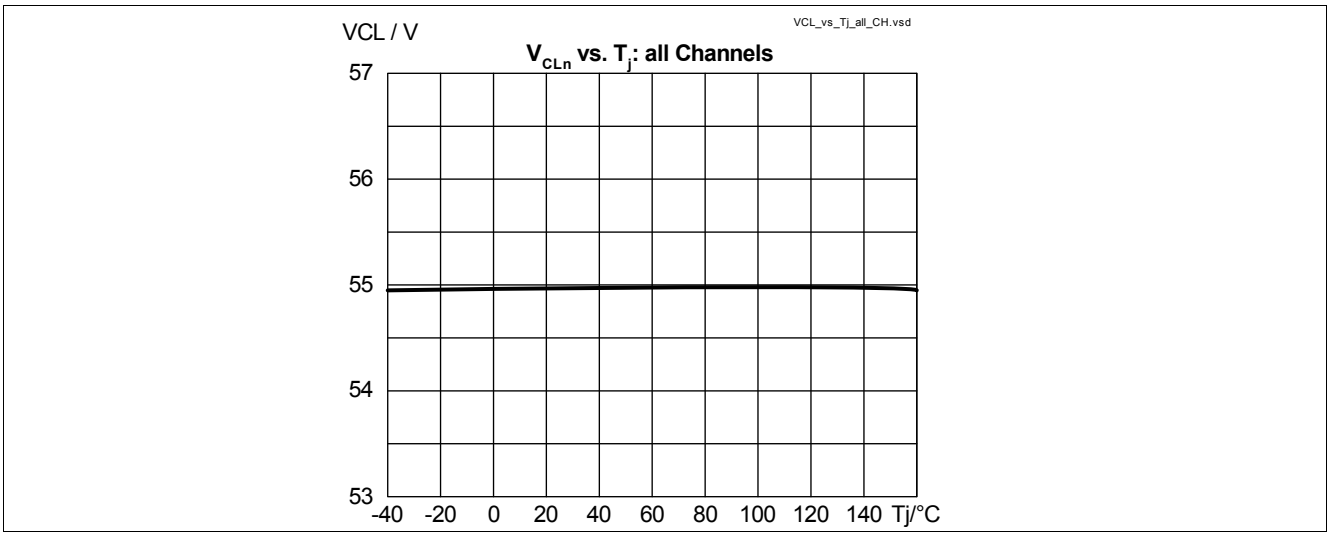

Figure 14 All Channels: typical behavior of the clamping voltage versus the junction temperature

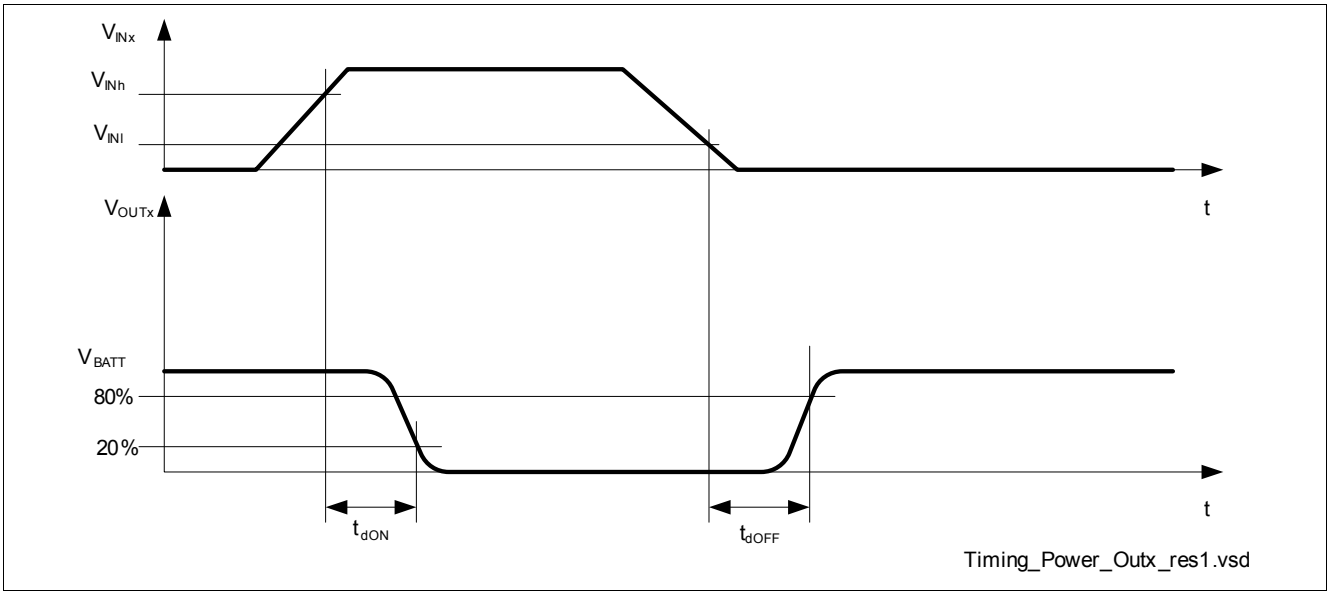

Figure 15 Timing of Output Channel switching (resistive load)

7.4 Parallel Connection of the Power Stages

The TLE8110ED is equipped with a structure which improves the capability of parallel-connected channels. The device can be “informed” via the PMx.PMx - bits (see chapter “Control of the device”) which of the channels are connected in parallel. The input channels can be mapped to the parallel connected output channels in order to apply the PWM signals. This feature allows a flexible adaptation to different load situations within the same hardware setup.

In case of overload the ground current and the power dissipation is increasing. The application has to take into account that all maximum ratings are observed (e.g. operating temperature T_J and total ground current I_{GND}, see Maximum Ratings). In case of parallel connection of channels with or w/o PM-bit set, the defined maximum clamping energy must not be exceeded.

All stages are switched on and off simultaneously. The µC has to ensure that the stages which are connected in parallel have always the same state (on or off). The PM-bit should be set according to the parallel connected power stages in order to achieve the best possible performance.

The PM-bit is set to its default value in case of a Reset event (Reset pin Low or at Digital Supply undervoltage), that means the improved Parallel Mode is no longer active. In the event of reset the channels will be switched off causing the clamping energy to be dissipated with low performance of the current sharing as without PM-bit set, for more details please refer to the Application Note *Switching Inductive Loads - TLE8110 addendum*.

The performance during parallel connection of channels is specified by design and not subject to the production test. All channels at the same junction temperature level.

ON-Resistance

The typical ON-Resistance $R_{DSsum(typ)}$ of parallel connected channels is given by:

$$R_{DSsum(typ)} = \left[\frac{1}{R_{DSon,\,n(typ)}} + \frac{1}{R_{DSon,\,n+1(typ)}}\right]^{-1} \quad (7.2)$$