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TLE8242-2

8 Channel Fixed Frequency Constant Current Control With Current Profile Detection

Automotive Power

Never stop thinking

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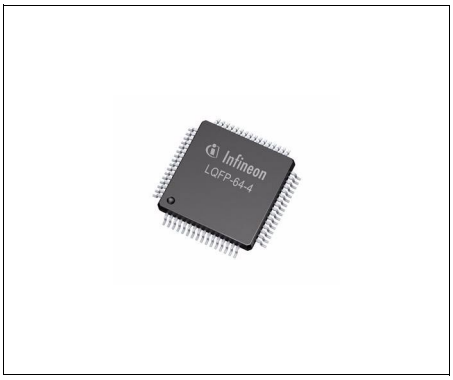
8 Channel Fixed Frequency Constant Current Control With Current Profile Detection **TLE8242-2**

AEC Qualified RoHS

1 Overview



PG-LQFP-64

1.1 Features

- Low side constant current control pre-driver integrated circuit
- Eight independent channels
- Output current programmable with 11 bit resolution
  - Current range = 0 to 1.2A (typ) with a 0.2 Ω sense resistor
  - Resolution = 0.78125 mA/bit (typ) with a 0.2 Ω sense resistor
  - +/- 2% full scale error over temperature when autozero is used
- Programmable PWM frequency via SPI from approximately 10 Hz to 4 kHz (typ)
- Programmable KP and KI coefficients for the PI controller for each channel
- Programmable superimposed dither
  - Dither programmed by setting a dither step size and the number of PWM periods in each dither period
  - Programmed via the SPI interface
  - The dither for each channel can be programmed independently
- Programmable synchronization of the PWM control signals
  - Phase delay time set via the SPI interface
  - Synchronization initiated via signal at the PHASE_SYNC input pin
  - Channels within one device and between multiple devices can be synchronized
- Each channel can be configured to for constant current control or for direct PWM control via SPI
- In Direct PWM mode, a current profile detection function is engaged
  - Verifies solenoid armature movement
  - Profile characteristics programmed via SPI
  - Pass / Fail Status can be read via SPI
- Interface and Control
  - 32 Bit SPI (Serial Peripheral Interface) - Slave only
  - ENABLE pin to disable all channels or freeze all channels
  - Active low RESET_B pin resets internal registers to their default state and disables all channels
  - Open drain FAULT pin can be programmed to transition low when various faults are detected
  - 5.0V and 3.3V logic compatible I/O
- Protection
  - Over current shutdown - monitored at POSx pin
  - Programmable over current threshold
  - Programmable over current delay time
  - Programmable over current retry time
  - Battery pin (BAT) overvoltage shutdown

Type	Package	Marking
TLE8242-2	PG-LQFP-64	TLE8242-2L

- Diagnostics
  - Over current
  - Open load in on state
  - Open load in off state
  - Short to ground
  - Test complete bit - indicates that fault detection test has completed
- Control loop monitor capabilities
  - The average current measurement over the last completed dither cycle for a selected channel can be accessed via SPI
  - The minimum and maximum current measurements over the last completed dither cycle for a selected channel can be accessed via SPI. This data can be used to measure the achieved dither amplitude
  - The duty cycle of each channel can be accessed via SPI
  - The auto zero values used to cancel the offsets of the input amplifiers can be accessed via SPI
- Required External Components:
  - N-Channel Logic level (5V) MOSFET transistor with typical Ron ≤ 100 mΩ (e.g. SPD15N06S2L-64)
  - Recirculation diode (ultrafast)
  - Sense resistor (0.2Ω for 1.2A average output current range)
- Green Product (RoHS compliant)
- AEC Qualified

1.2 Applications

- Variable Force Solenoids (e.g. automatic transmission solenoids)
- Other constant current solenoids
  - Idle Air Control
  - Exhaust Gas Recirculation
  - Vapor Management Valve
  - Suspension Control

1.3 General Description

The TLE8242G IC is an eight channel low-side constant current control predriver IC. Each channel can be configured to function either in direct PWM mode or in constant current mode by setting the appropriate CM bit in SPI message #1.

1.3.1 Direct PWM Mode Operation

For Direct PWM operation, the POSx and NEGx pins must be connected to the circuit in either of the configurations shown in **Figure 1**. If the sense resistor is included, the load current can be monitored by the microcontroller via a SPI command. The open load in on state fault detection feature is disabled in direct PWM mode.

Note: An external flyback clamp is required in this configuration otherwise the IC may be damaged.

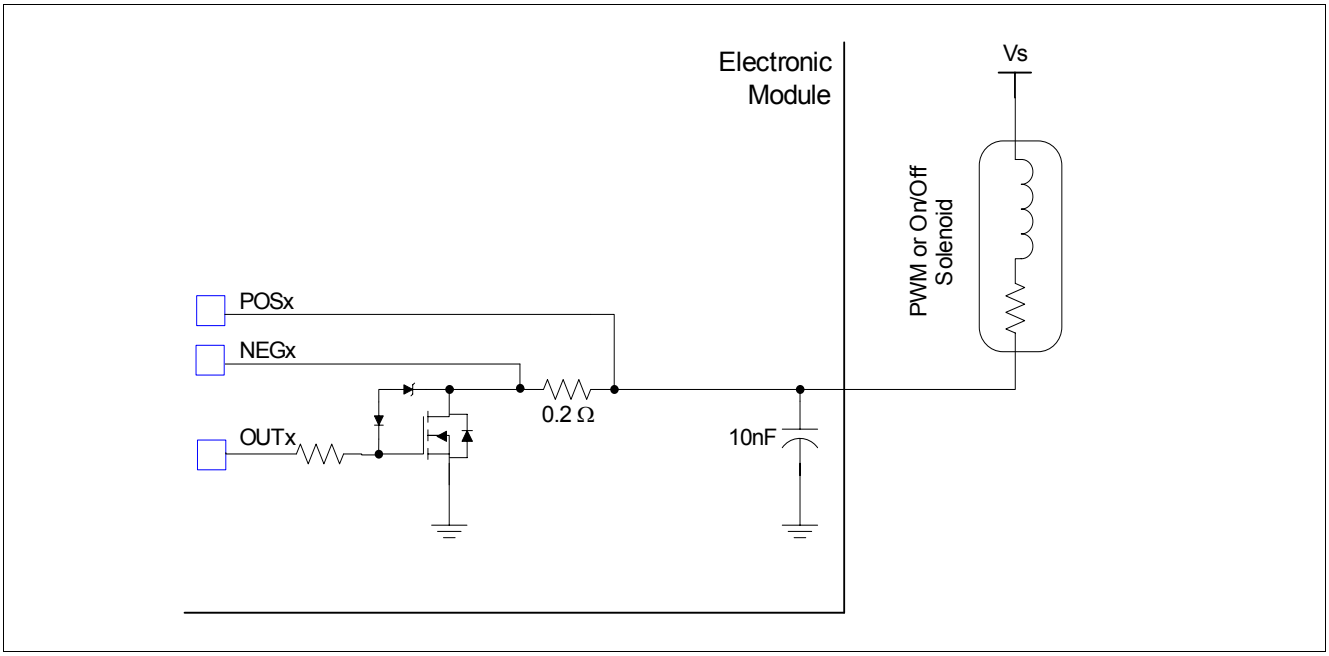


Figure 1 External Circuit Diagram for Direct PWM Mode Operation

1.3.2 Constant Current Mode Operation

During constant current operation, the POSx and NEGx pins must be connected to the circuit in the configuration shown in **Figure 2**.

Note: An external recirculation diode is required in this configuration otherwise the IC may be damaged.

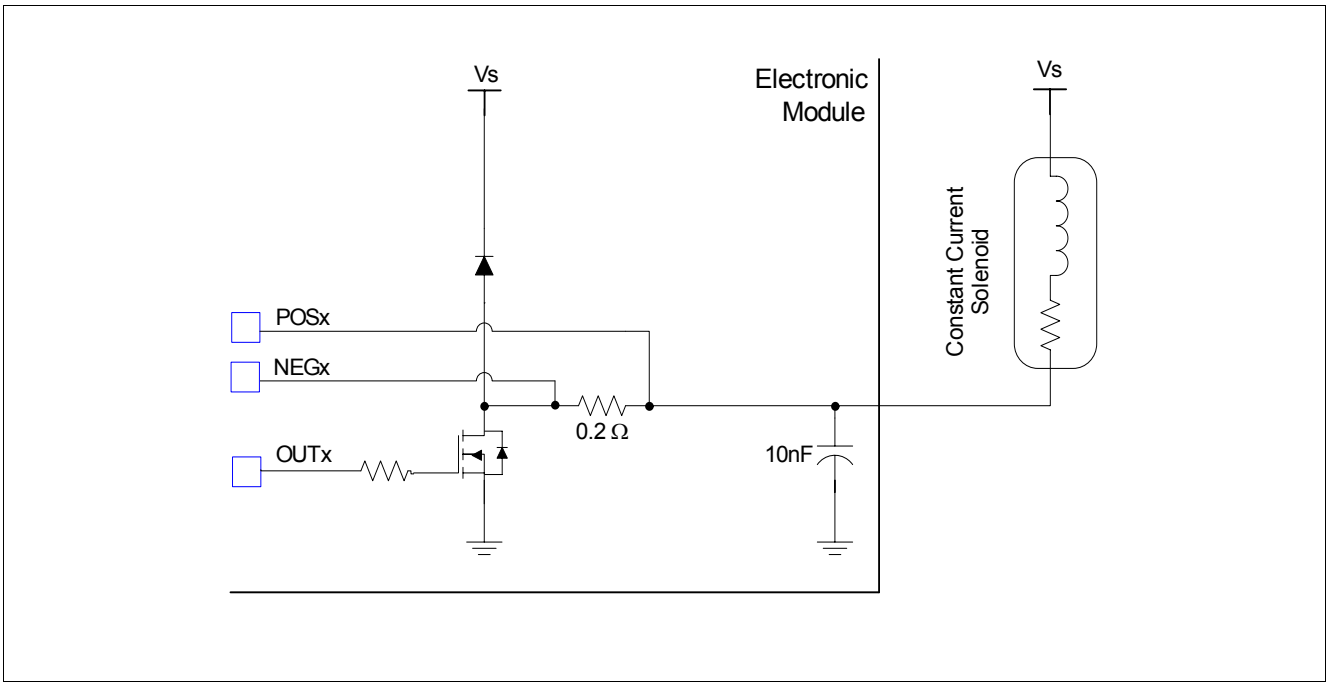


Figure 2 External Circuit Diagram for Constant Current Mode Operation

During constant current operation, the PWM control signal driven at the OUTx pin is controlled by the control loop shown in **Figure 3**. The PWM Frequency is programmed via the SPI message # 8. In this message the main period

divider, N, can be set to any value between 79 and 2^{14} -1 and the divider M can be set to 32, 64, or 128. In direct PWM mode, the value M can also be set to 512. The equation for calculating the PWM frequency is:

$$F_{PWM} = \frac{F_{CLK}}{M * N}$$

In constant current mode, the value of M is the number of A/D samples within one PWM period. Setting the SAM bit in SPI Message #8 to a “1” will cause the ADC samples immediately following a change in the state of the OUTx pin to be discarded. If the SAM bit is set to ‘0’, all M A/D samples are used in the average calculation.

The 11 bit Current Set Point is programmed via the SPI message #10. The equation for calculating the current setpoint is:

$$\text{CurrentSetpoint[mA]} = \frac{\text{setpoint(11bit)}}{2^{11}} * \frac{320[\text{mV}]}{R_{SENSE}[\text{ohm}]}$$

The Proportional coefficient (KP) and the Integral coefficient (KI) of the control loop are programmed in SPI message #9. The KP and KI values should be set to values that result in the desired transient response of the control loop. The duty cycle of the OUTx pin can be calculated from the difference equations:

$$DutyCycle(k) = KP * \frac{Rsense\ [Ohm]}{0.04 * M * N} * error(k-1)[A] + INT(k)$$

$$INT(k) = KI * \frac{Rsense\ [Ohm]}{0.04 * M * N} * error(k-1)[A] + INT(k-1)$$

where error is the difference between the commanded average current and measured average current in units of Amps.

where k indicates the integer number of PWM periods that have elapsed since current regulation was initiated.

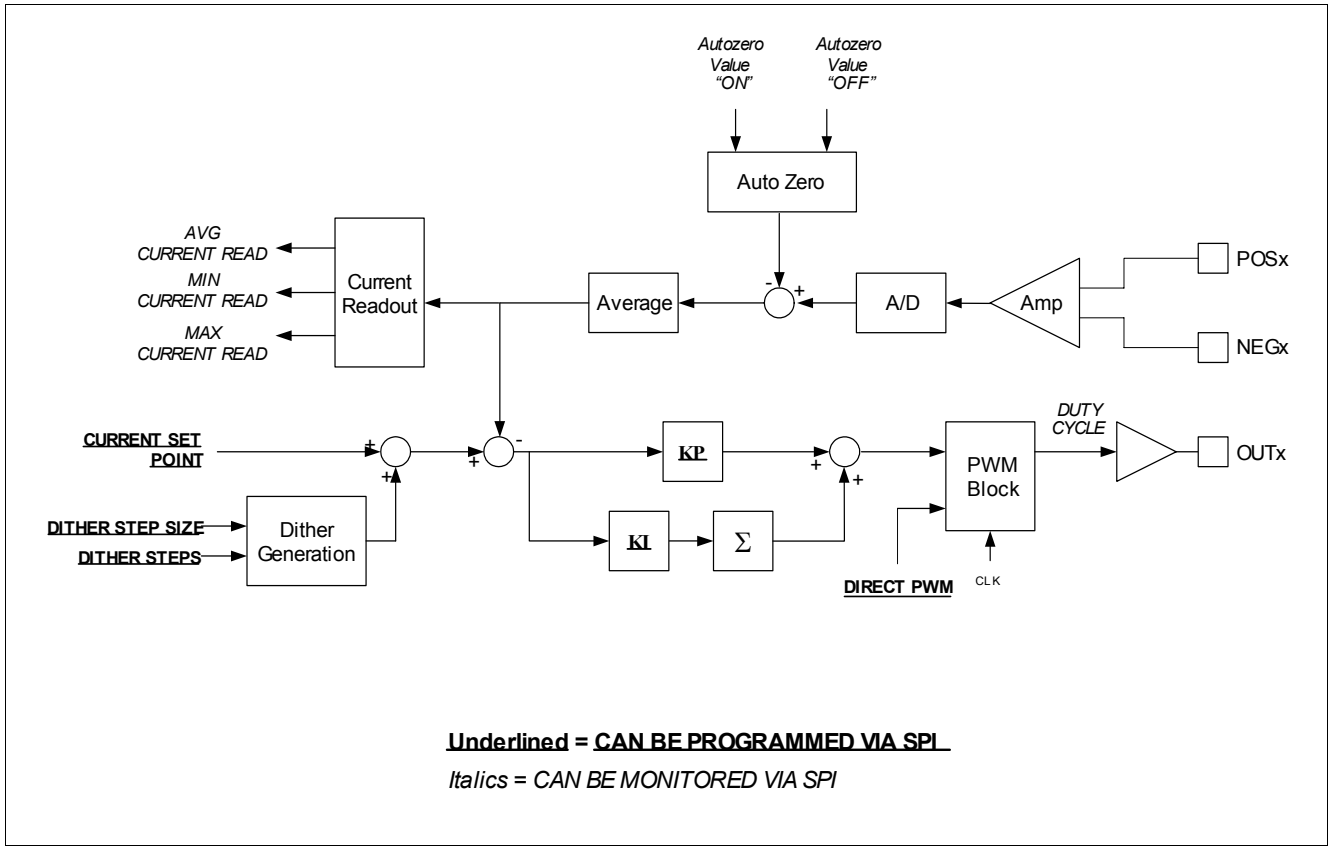


Figure 3 Control Loop - Simplified Diagram

Table 1 describes the effect on the integrator of the PI controller of several events.

Table 1 Control Loop Integrator Control

Condition	Action to Integrator
Reset Active	Cleared
V5D undervoltage	Cleared
V5Ax undervoltage	Cleared
ENABLE pin low (SPI message #10 bit EN = 0)	Cleared
ENABLE pin low (SPI message #10 bit EN = 1)	Remains Operational
VBAT overvoltage	Held at current value
Short to BAT	Cleared
Phase_Sync Transition	Remains Operational Integrator value for first PWM cycle = value from end of last complete PWM cycle.
Average Current set to 0	Cleared
Control Mode set to Direct PWM	Cleared
Main Period Set (N, M) Changed	Remains Operational
KP, KI settings Changed	Remains Operational

Auto Zero

The TLE8242 includes an autozero feature for each channel. When the setpoint of a channel is set to 0 mA and the autozero is triggered by an SPI command, the offset of the amplifiers and analog to digital converters are measured. The time required for the autozero sequence is calculated according to the formula:

$$T_{AZ} = \frac{4 * M * N}{F_{CLK}}$$

The measured offsets can be read via SPI message #14. these offsets will be subtracted from the A/D converter output as shown in **Figure 3** when the current set point is greater than 0.

Dither

A triangular dither waveform can be superimposed on the current set point by setting the amplitude and frequency parameters of the dither waveform via SPI messages #10 and #11. See the SPI message section for details.

The first programmed value is the step size of the dither waveform which is the number of bits added or subtracted from the setpoint per PWM period. One LSb of the dither step size is 1/4th the magnitude of the nominal setpoint current value. The second programmed value is the number of steps in one quarter of the dither waveform.

When dither is enabled, a new average current set point will not be activated until the current dither cycle has completed. The dither cycle is completed on the positive zero crossing of the dither waveform. A new dither amplitude setting or a new dither frequency setting will also not be activated until the current dither cycle has completed. See **Figure 4**.

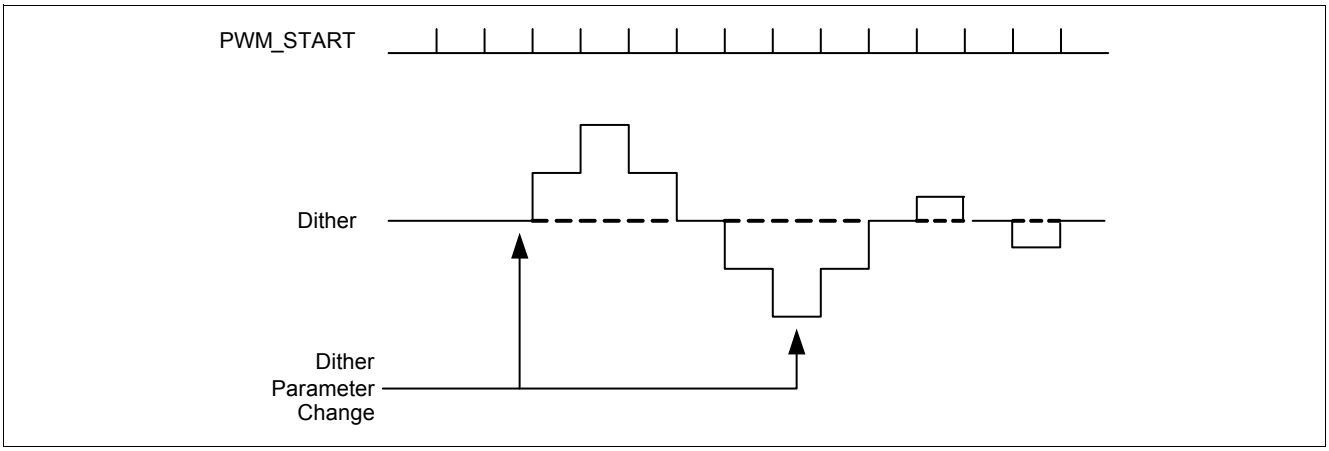


Figure 4 New Dither Values Programmed and the Resulting Waveform Timing

Note: The actual measured dither waveform is attenuated and phase shifted according to the frequency response of the control loop.

2 Block Diagram

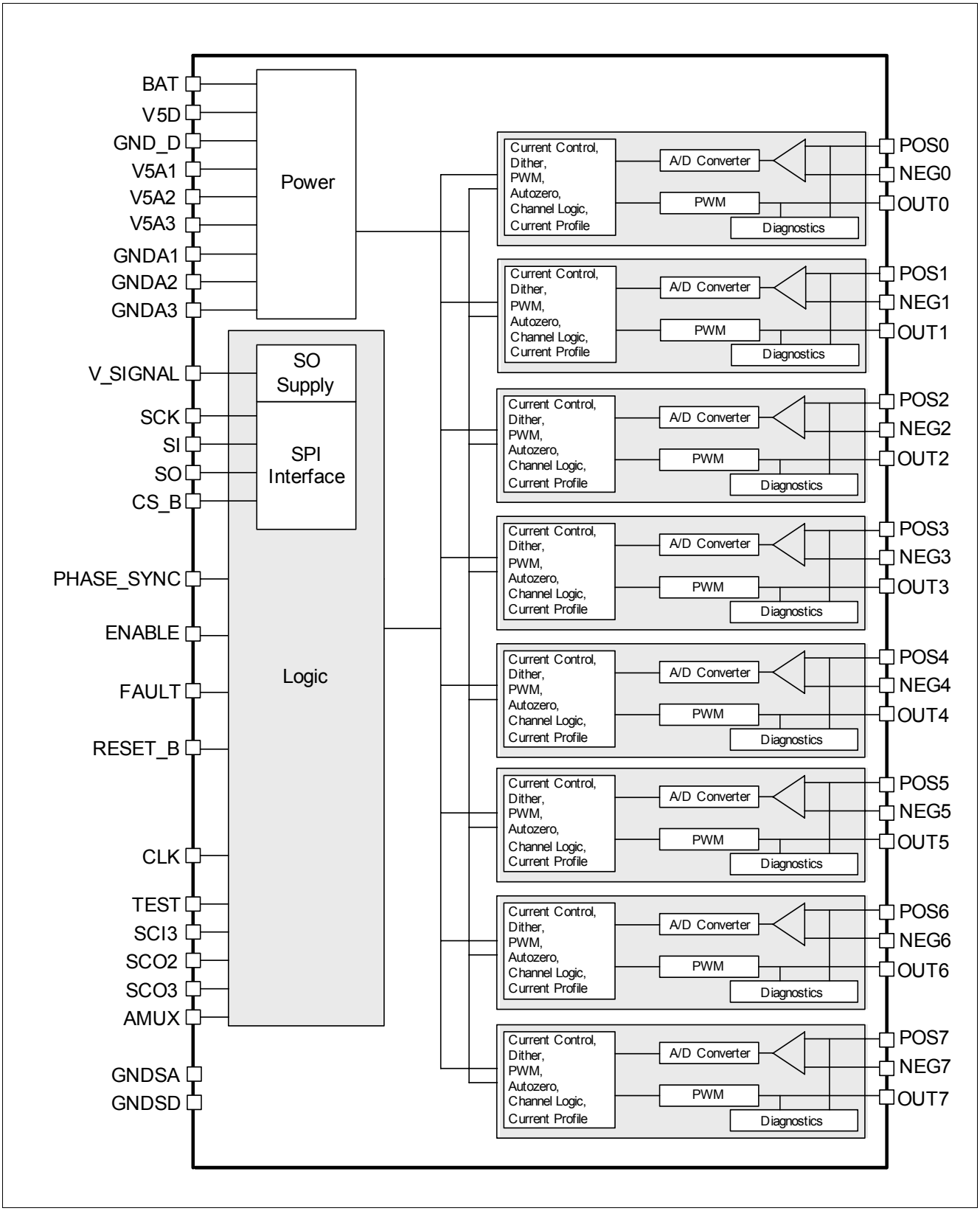


Figure 5 Block Diagram

3 Pin Configuration

3.1 Pin Assignment

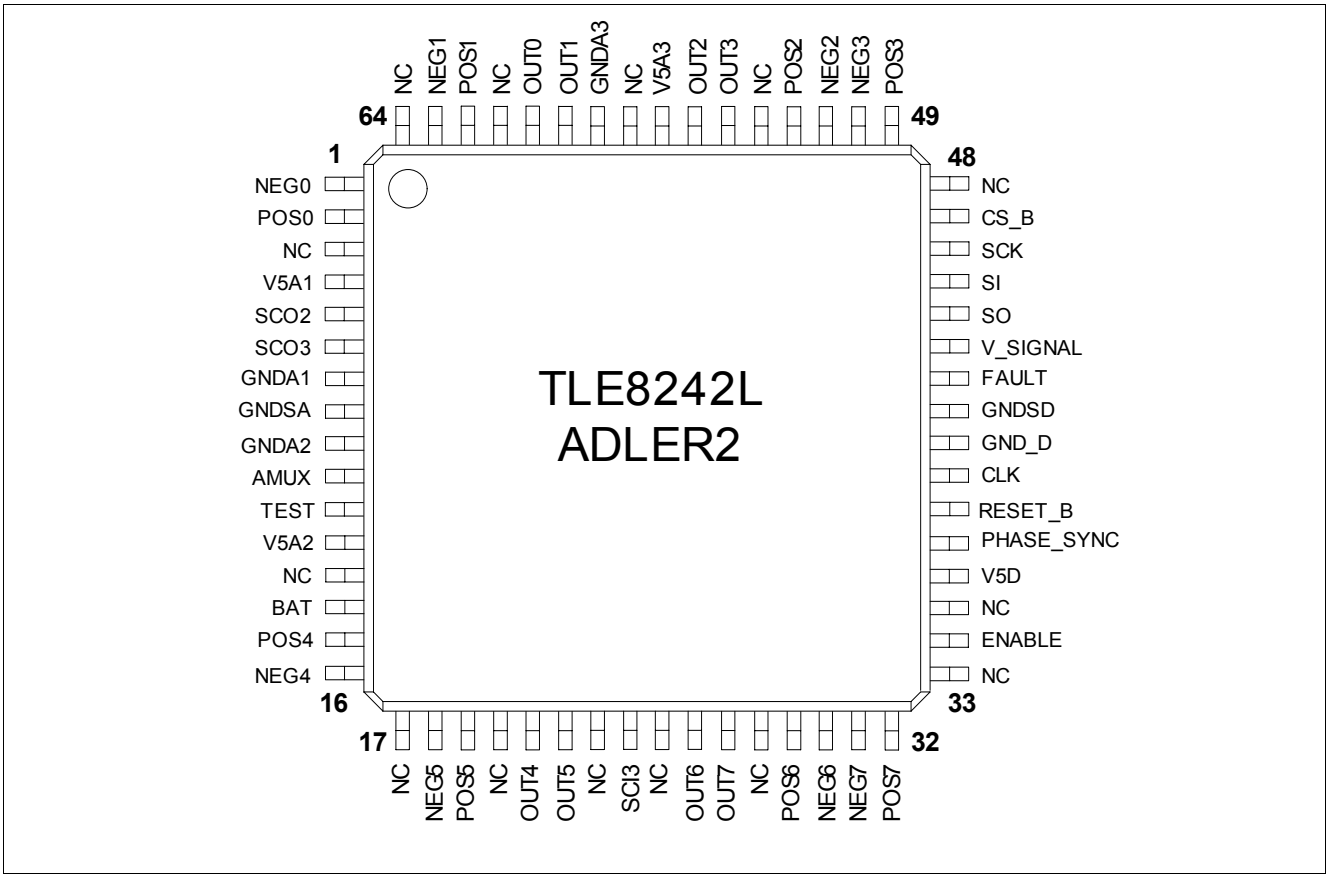


Figure 6 Pin Configuration

3.2 Pin Definitions and Functions

Pin	Symbol	Function
1	NEG0	**Channel #0 Negative sense pin;** Connect to the “FET” side of the external sense resistor
2	POS0	**Channel #0 Positive sense pin;** Connect to the “load” side of the external sense resistor
3	NC	**Not Connected;** do not connect to external supply, ground, or signal
4	V5A1	**Supply Voltage;** 5V input for analog circuits. An external capacitor is to be connected between this pin and GND_A near this pin
5	(T) SCO2	**Test Pin;** Used for IC test. Must be connected to GND_D for specified operation of the IC
6	(T) SCO3	**Test Pin;** Used for IC test. Must be connected to GND_D for specified operation of the IC
7	GND_A1	**Ground;** ground pin for analog circuits
8	GNDSA	**Ground;** ground pin for substrate connection near analog circuits

Pin	Symbol	Function
9	GND_A2	**Ground;** ground pin for analog circuits
10	(T) AMUX	**Test Pin;** Used for IC test. Must be connected to GND_D for specified operation of the IC
11	(T) TEST	**Test Pin;** Used for IC test. Must be connected to GND_D for specified operation of the IC
12	V5A2	**Supply Voltage;** 5V input for analog. An external capacitor is to be connected between this pin and GND_A near this pin
13	NC	**Not Connected;** do not connect to external supply, ground, or signal
14	BAT	**Battery Sense Input;** for over-voltage detection. Connect through a series resistor (e.g. 1 K ohm) to the solenoid supply voltage. A large electrolytic capacitor (e.g. 47uF) should be placed between the BAT supply and ground
15	POS4	**Channel #4 Positive sense pin**; Connect to the “load” side of the external sense resistor
16	NEG4	**Channel #4 Negative sense pin**; Connect to the “FET” side of the external sense resistor
17	NC	**Not Connected;** do not connect to external supply, ground, or signal
18	NEG5	**Channel #5 Negative sense pin**; Connect to the “FET” side of the external sense resistor
19	POS5	**Channel #5 Positive sense pin;** Connect to the “load” side of the external sense resistor
20	NC	**Not Connected;** do not connect to external supply, ground, or signal
21	OUT4	**Gate driver output for channel #4;** Connect to the gate of the external MOSFET
22	OUT5	**Gate driver output for channel #5;** Connect to the gate of the external MOSFET
23	NC	**Not Connected;** do not connect to external supply, ground, or signal
24	(T) SCI3	**Test Pin;** Used for IC test. Must be connected to GND_D for specified operation of the IC
25	NC	**Not Connected;** do not connect to external supply, ground, or signal
26	OUT6	**Gate driver output for channel #6**; Connect to the gate of the external MOSFET
27	OUT7	**Gate driver output for channel #7;** Connect to the gate of the external MOSFET
28	NC	**Not Connected;** do not connect to external supply, ground, or signal
29	POS6	**Channel #6 Positive sense pin;** Connect to the “load” side of the external sense resistor
30	NEG6	**Channel #6 Negative sense pin;** Connect to the “FET” side of the external sense resistor
31	NEG7	**Channel #7 Negative sense pin**; Connect to the “FET” side of the external sense resistor
32	POS7	**Channel #7 Positive sense pin**; Connect to the “load” side of the external sense resistor
33	NC	**Not Connected;** do not connect to external supply, ground, or signal

Pin	Symbol	Function
34	ENABLE	**ENABLE logic input;** When this input pin is low all channels are turned off (zero current) or remain in their last state, depending on how the channel is programmed to respond
35	NC	**Not Connected;** do not connect to external supply, ground, or signal
36	V5D	**Supply Voltage;** 5V input for digital circuits. An external capacitor is to be connected between this pin and GND_D near this pin
37	PHASE_SYNC	**Phase Synchronization Input:** Used to synchronize the rising edges of the PWM signal on the OUTx pins for each channel
38	RESET_B	**Reset Input;** When this input pin is low all channels are turned off and all internal registers are reset to the default state. The part must be held in reset by an external source until all supplies are stable and within tolerance
39	CLK	**CLOCK;** Main clock input for the chip. A clock input of 20 MHz to 40 MHz is required
40	GND_D	**Ground;** ground pin for digital circuits
41	GNDSD	**Ground;** ground pin for substrate connection near digital circuits
42	FAULT	**Fault Output Pin;** Open drain output pin is pulled low when a fault condition is detected. Certain faults can be masked via SPI
43	V_SIGNAL	**Supply Voltage;** Supply pin for the SPI SO output and the pull-up current sources of the digital inputs CS_B and RESET_B. An external capacitor must be connected between this pin and GND_D near this pin
44	SO	**SPI Serial Data Out**
45	SI	**SPI Serial Data In**
46	SCK	**SPI Serial Clock Input**
47	CS_B	**SPI Chip Select Bar;** active low signal
48	NC	**Not Connected;** do not connect to external supply, ground, or signal
49	POS3	**Channel #3 Positive sense pin**; Connect to the “load” side of the external sense resistor
50	NEG3	**Channel #3 Negative sense pin**; Connect to the “FET” side of the external sense resistor
51	NEG2	**Channel #2 Negative sense pin**; Connect to the “FET” side of the external sense resistor
52	POS2	**Channel #2 Positive sense pin**; Connect to the “load” side of the external sense resistor
53	NC	**Not Connected;** do not connect to external supply, ground, or signal
54	OUT3	**Gate driver output for channel #3**; Connect to the gate of the external MOSFET
55	OUT2	**Gate driver output for channel #2;** Connect to the gate of the external MOSFET
56	V5A3	**Supply Voltage;**5V input for analog. An external capacitor is to be connected between this pin and GND_A near this pin.
57	NC	**Not Connected;** do not connect to external supply, ground, or signal
58	GND_A3	**Ground;** ground pin for analog circuits
59	OUT1	**Gate driver output for channel #1**; Connect to the gate of the external MOSFET

Pin	Symbol	Function
60	OUT0	**Gate driver output for channel #0;** Connect to the gate of the external MOSFET
61	NC	**Not Connected;** do not connect to external supply, ground, or signal
62	POS1	**Channel #1 Positive sense pin;** Connect to the “load” side of the external sense resistor
63	NEG1	**Channel #1 Negative sense pin**; Connect to the “FET” side of the external sense resistor
64	NC	**Not Connected;** do not connect to external supply, ground, or signal

4 General Product Characteristics

4.1 Maximum Ratings

Absolute Maximum Ratings [1]

T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
Voltages						
4.1.1	Battery Input (VBAT)	V_{BAT}	-13	50	V	–
4.1.2	Supply Voltage (logic)	V_{5D}, V_{5A1} V_{5A2}, V_{5A3} V_{signal}	-0.3	6.0	V	–
4.1.3	POSx, NEGx	V_{pos}, V_{neg}	-0.3	50	V	–
4.1.4	POSx-NEGx	V_{pos}-V_{neg}	-0.2	13	V	–
4.1.5	OUTx	V_{out}	-0.3	min(V_{5D}+ 0.3; 6)	V	–
4.1.6	RESET_B, SI, SCK, CS_B, CLK, TEST, PHASE_SYNC, ENABLE	V_{io}	-0.3	min(V_{5D}+ 0.3; 6)	V	–
4.1.7	SO, FAULT	V_{io}	-0.3	min(V_{signal} + 0.3; 6)	V	–
4.1.8	Maximum difference between V5D and V5Ax pins		-500	500	mV	–
Currents						
4.1.9	Input Clamp Current ENABLE, PHASE_SYNC, RESET_B, SI, SCK, CS_B, CLK	I_{CLAMP}	5	–5	mA	[2]
Temperatures						
4.1.10	Storage Temperature	T_{stg}	-65	150	°C	–
4.1.11	Junction Temperature	T_j	-40	150	°C	–
ESD Susceptibility						
4.1.12	HBM		-2	2	kV	[3]
4.1.13	CDM all pins		-500	500	V	[4]
4.1.14	CDM corner pins		-750	750	V	[4]

1) Not subject to production test, specified by design.
2) Current needs to be limited only when maximum voltages are exceeded
3) ESD Susceptibility HBM according to EIA/JESD 22-A 114B
4) ESD Susceptibility CDM according to EIA/JESD22-C101

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

4.2 Functional Range

T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
4.2.1	Supply Voltage Range for Normal Operation - VBAT	V_{BAT}	5.5	42	V	–
4.2.2	Supply Voltage Range for Normal Operation - V5D, V5A1, V5A2, V5A3	V_{V5D} V_{V5A1}, V_{V5A2}, V_{V5A3}	4.75	5.25	V	–
4.2.3	Supply Voltage Range for Normal Operation -V_SIGNAL	V_{V_SIGNAL}	3.0	5.25	V	–
4.2.4	Clock Frequency	f_{CLK}	20	40	MHz	
4.2.5	PWM Frequency for Normal Operation	f_{PWM}	10	4000	Hz	
4.2.6	Extended PWM Frequency Range	f_{PWM}	10	8000	Hz	Parameter deviations possible
4.2.7	Common Mode Voltage Range for Normal Operation - POSx, NEGx pins.	V_{pos} , V_{neg}	0	30	V	–
4.2.8	Extended Common Mode Voltage Range for Operation - POSx, NEGx pins.	V_{pos} , V_{neg}	0	42	V	Parameter deviations possible

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

4.3 Thermal Resistance

T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
4.3.1	Junction to Ambient[1)]	R_{thJA}	–	38	–	K/W	[2)]

1) Not subject to production test, specified by design.

2) Specified R_{thJA} value is according to Jedec JESD51-2, -7 at natural convection on FR4 2s2p board; The Product (chip + Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70µm, 2 x 35 µm Cu).

5 Functional Description and Electrical Characteristics

Note: The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at T_A = 25 °C and the given supply voltage.

5.1 Supply and Reference

The device includes a power-on reset circuit. This feature will disable the channels and reset the internal registers to their default values when the voltage on V5A1, V5A2, V5A3, and/or V5D are below their respective reset thresholds.

The V5D pin and GND_D pin are the supply and ground pins for the digital circuit blocks. The current through these pins contain high frequency components. Decoupling with ceramic capacitors and careful PCB layout are required to obtain good EMC performance.

The V5A1, V5A2, V5A3 pins and GND_A pin are the supply and ground pins for the analog circuit blocks.

The V_SIGNAL pin supplies the SPI output pin (SO) and is the source voltage for the pull up currents on the CS_B and RESET_B pins. V_SIGNAL should be connected to the I/O supply of the microcontroller (3.3V or 5.0V).

The BAT pin is an input pin used to detect over voltage faults. This pin is not a power supply input. A series resistor should be connected between this pin and the solenoid supply voltage for transient protection.

Electrical Characteristics:

V5D = 4.75V to 5.25V, Vbat = 5.5V to 42V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.1.1	Undervoltage reset (internally generated) V5A1, V5A2, and V5A3	V_{V5A1}, V_{V5A2}, V_{V5A3}	3.5	–	4.5	V	Internal reset occurs if V5A1 V5A2, or V5A3 is below the undervoltage limit
5.1.2	Undervoltage reset (internally generated) V5D	V_{V5D}	1.0	–	4.5	V	Internal reset occurs if V5D is under the undervoltage limit
5.1.3	V5D supply current	I_{V5D}	–	–	75 40	mA mA	f_{CLK}=40MHz f_{CLK}=20MHz
5.1.4	V5A1 supply current	I_{V5A1}	–	–	20	mA	
5.1.5	V5A2 supply current	I_{V5A2}	–	–	20	mA	
5.1.6	V5A3 supply current	I_{V5A3}	–	–	5	mA	
5.1.7	V_SIGNAL supply current	I_{V_SIGNAL}	–	–	300	µA	V_{SIGNAL}=5.25V SO = Hi-Z state
5.1.8	VBAT current	I_{VBAT}	–	–	80	µA	full operating range
5.1.9	VBAT current - unpowered	I_{VBAT}	–	–	5	µA	V5D=V5Ax=0V, BAT=14V

5.2 Input / Output

All digital inputs are compatible with 3.3 V and 5 V I/O logic levels. The supply voltage for the SPI output SO is the V_SIGNAL pin. All digital inputs are pulled to a known state by a weak internal current source or current sink when not connected. However, unused digital input pins should be connected to ground or to V_SIGNAL (according to the desired functionality) by an external connection or resistor. All input pin weak internal current sources are supplied by the V_SIGNAL pin.

The RESET_B pin is an active low input pin. When this pin is low, all channels are off, and all internal registers are reset to their default states. The device must be held in reset by an external source until all the power supplies have stabilized. The IC contains an internal power on and undervoltage reset which becomes active when V5D, V5A1, V5A2, or V5A3 fall below the undervoltage reset thresholds.

The ENABLE pin is an active high input pin which must be held high for normal operation of the device. When this pin is held low all channels are either turned off or will remain in the last state, depending on how the enable behavior of the channel is programmed via SPI Message #10. The default condition is that all channels are turned off when the ENABLE pin is low.

The CLK pin is the main clock input for the device. The input thresholds are compatible with 3.3 V and 5.0 V logic levels. No synchronization is required between the clock signal connected to the CLK pin and the SPI clock signal (SCK). All internal clock signals of the TLE8242 (PWM signals, A/D sampling, diagnostics, etc.) are generated from the this clock input. Also, this clock is required for the device to accept and respond to SPI messages.

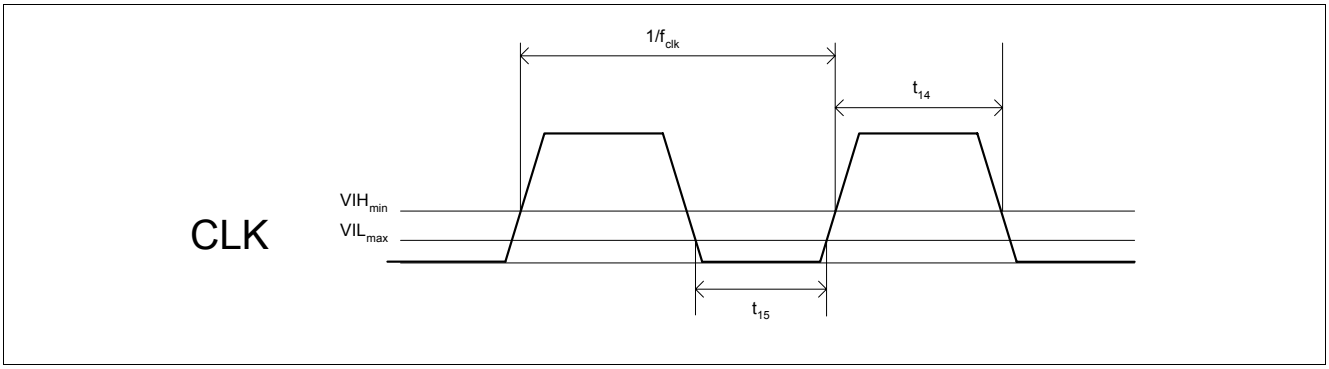


Figure 7 CLK Timing Diagram

The PHASE_SYNC pin is an input pin that can be used by the microcontroller to synchronize the PWM control signals of multiple channels. The desired phase delay between the rising edge of the signal applied to the PHASE_SYNC pin and the rising edge of the PWM signal of each channel can be programmed independently via SPI message #6. The equation for calculating the offset is:

$$T_{offset} = \frac{PhaseSynchOffset}{32 * F_{PWM}}$$

Each time a pulse is received on the PHASE_SYNC pin, the IC will latch a bit which is reported via the response to SPI message #19. (See SPI interface section for bit/message location.) This latch is cleared when the message is read.

Note: The PWM periods are restarted when a rising edge is detected on the PHASE_SYNC pin. A periodic pulse train on this pin will disturb the current regulation.

Note: After exiting the reset state, a pulse is needed on the PHASE_SYNC pin in order to synchronize the PWM periods of the channels

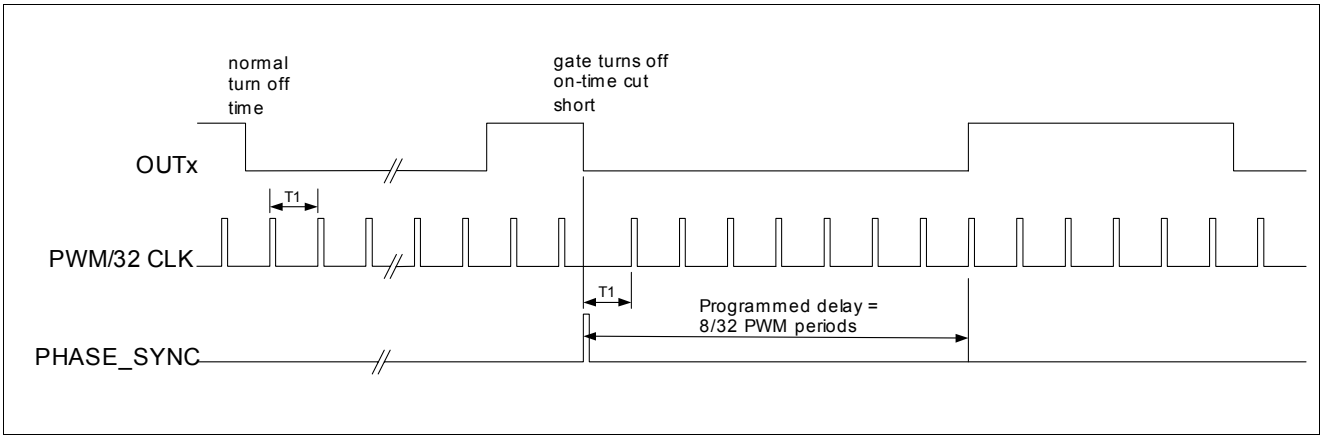


Figure 8 Phase Synchronization Diagram

The TEST, SCI3, SCO2, SCO3, and AMUX pins are used during IC level test. These pins should be connected directly to ground for normal device operation.

The FAULT pin is an open drain output pin. This pin will be pulled low by the device when an unmasked fault has been detected. The fault masks are programmed via SPI message #1.

Electrical Characteristics:

V5D = 4.75V to 5.25V, Vbat = 5.5V to 42V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.2.1	Logic input low voltage	V_{ILMAX}	–	–	0.8	V	
5.2.2	Logic input high voltage	V_{IHMIN}	2.0	–	–	V	
5.2.3	Logic output low voltage	V_{OLMAX}	–	–	0.2	V	I_L=200µA
5.2.4	Logic output high voltage	V_{OHMIN}	0.8*V_ SIGNAL	–	–	V	I_L=-200µA
5.2.5	Pull down digital input (SI, CLK, SCK, PHASE_SYNC, ENABLE)	I_{pd}	10	–	50	µA	V_{in}=V_SIGNAL
5.2.6	Pull up digital input (CS_B, RESET_B)	I_{pu}	-50	–	-10	µA	V_{in}=0V (Current drain from V_SIGNAL)
5.2.7	Fault pin voltage	$V_{fault.low}$	–	–	0.4	V	Active state; I_{fault}=2mA
5.2.8	Fault pin current	$I_{fault,max}$	2.0	–		mA	Active state; V_{fault}=0.4V
5.2.9	CLK high time (rise 2.0V to fall 2.0V)	t_{14}	8	–	–	ns	
5.2.10	CLK low time (fall 0.8V to rise 0.8V)	t_{15}	8	–	–	ns	

5.3 Diagnostics

The TLE8242 includes both on-state and off-state diagnostics. On-state diagnostics are active when the OUTx pin is driven high and off-state diagnostics are active when the OUTx pin is driven low. A detected fault can be used to activate the open drain FAULT pin on the IC. This pin can be used to interrupt the microcontroller when a fault is detected. Certain faults can be prevented from activating the FAULT pin by setting the fault mask register in SPI message #1.

Once a fault is detected it is latched into the respective fault register. The microcontroller can access the fault registers by SPI messages #4, #5, and #19.

If the RESET_B line transitions high-to-low, a RB_L bit is latched into the Generic Flag Bits register. This register is cleared after it is read from the SPI, and the RB_L bit will not be set again until the next high-to-low transition occurs on the RESET_B pin.

If the ENABLE pin voltage is low, the EN_L bit is latched in the Generic Flag Bits register. The ENL bit is cleared when the ENABLE pin returns to a high state and the Generic Flag Bits register is accessed by SPI message #19.

The diagnostic delay timers for the on-state and off-state diagnostic functions are derived from the master clock signal applied to the pin CLK using a programmable predivider. This predivider is programmable by the DIAG_TMR bits in SPI message #1.

Table 2 Timebase for Diagnostics

DIAG_TMR1	DIAG_TMR0	Pre-divider	nfault min ... max	Tested Timer and Fault Detection Timer Period.	
				f_{CLK}=20 MHz	f_{CLK}=40 MHz
0	0	128	10 ... 11	64 µsec	32 µsec
0	1	192	10 ... 11	96 µsec	48 µsec
1	0	128	2 ... 3	12.8 µsec	6.4 µsec
1	1	256	10 ... 11	128 µsec	64 µsec

$$t_{DIAG\_PERIOD} = \frac{n_{fault} * predivider}{F_{CLK}}$$

Three unique fault types are detected using 4 different fault bits

The fault bit is set to a “1“ if the fault is detected.

Table 3 Diagnostic Flags / Bits

Fault Type	Abr.	Gate is ON	Gate is OFF
Short to Ground Fault	SG	OL-ON-F reported (=0 in ON/OFF mode)	Bit SG-F
Short to Battery Fault	SB	Bit SB-F	
Open Load Fault	OL	BIT OL-ON-F (=0 in ON/OFF mode)	Bit OL-OFF-F

Note: In order to differentiate between a Short to Ground Failure and an Open Load Failure, the channel must be turned off (setpoint = 0ma).

Tested Diagnostic Bits

The tested bits allow the distinction between a a case when a fault bit is not set because the fault is not detected, and the case when a fault bit is not set because the diagnostic test has not completed. For instance, the calculated duty cycle is too low to complete the short to battery test.

Two fault tested bits are defined:

The tested bit is set to 1 when the fault test has completed successfully.

Table 4 Diagnostics Tested Bits / Flags

Tested Type	OUTx High	OUTx Low
Short to Ground and Open load OFF tested		Bit OFF-T
Short to Battery tested	Bit SB-T	

Each fault type can be described by the two bits: FAULT and TESTED.

Table 5 FAULT vs. TESTED Bits Matrix and Interpretation

FAULT	TESTED	Interpretation by microcontroller
0	0	This fault type has not been tested
0	1	No Fault - The fault type has been tested and no fault is present
1	0	This combination cannot occur
1	1	Fault - This particular fault type has occurred

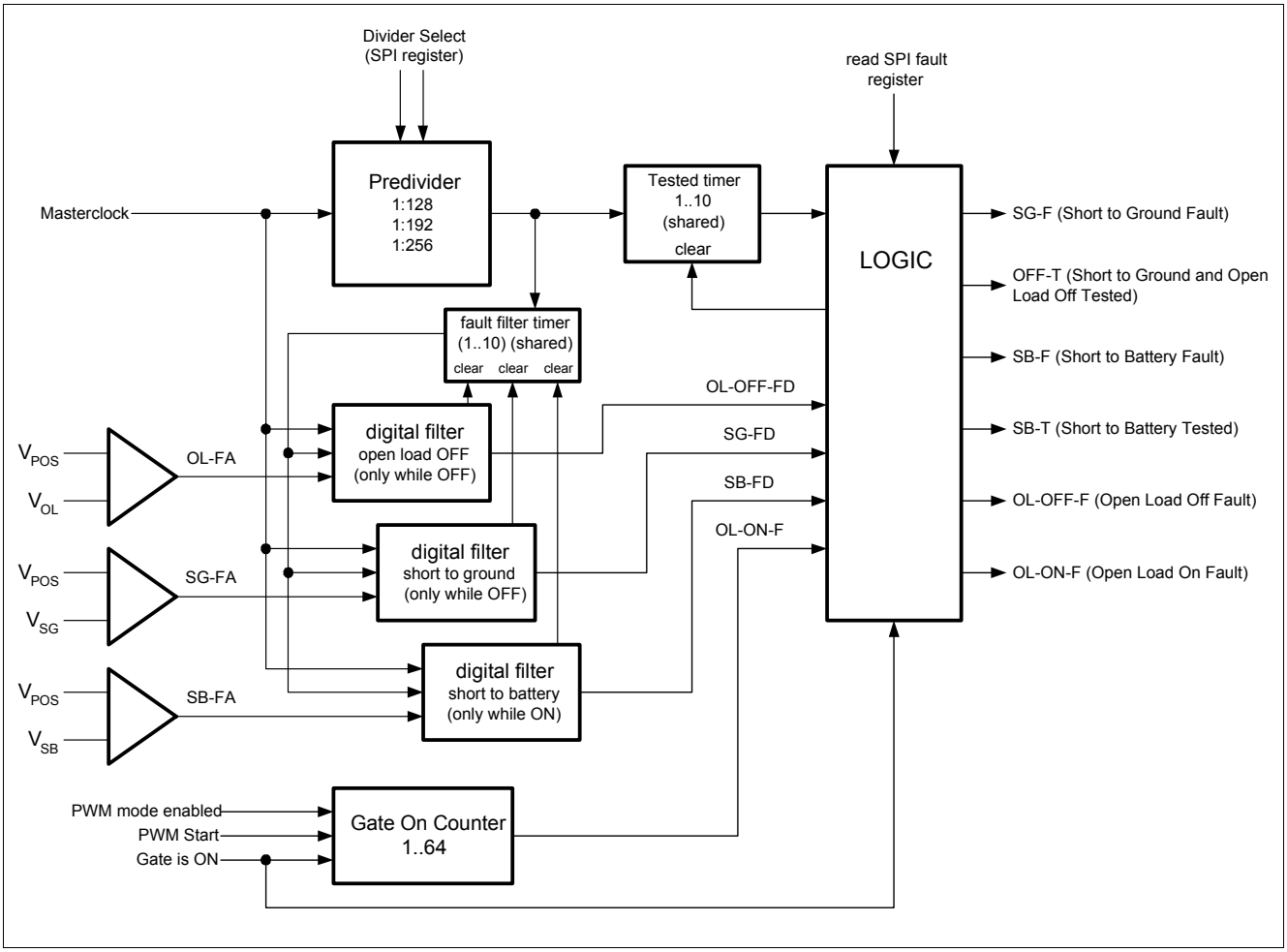


Figure 9 Diagnostic Block Diagram

5.3.1 On-State Diagnostics

When the OUTx pin transitions high, the fault timers are cleared to 0 and the tested timer starts. If the tested timer expires, the Bit SB-T (in the SPI registers #4 and #5) is set to 1. If the OUTx pin transitions low, the tested timer is cleared and then used for the off-state diagnostics.

If the analog SB fault signal (SB-FA) changes to 1, the fault filter timer starts. If the fault filter timer expires, the digitally filtered SB fault signal (SB-FD) is set to one. If SB-FA changes to 0, SB-FD changes immediately to 0 and the filter timer is cleared to 0.

A SB-FD=1 and SB-T=1 switches off the OUTx signal and the SB-F bit in the FAULT register will be set. The OUTx pin remains in the off state until the fault retry PWM period counter expires.

If the SPI message #3 or #4 is read, then the SB-F bit and the SB-FT bit in this register are cleared. Also, the tested timer is cleared to 0.

The Short to Battery (SB) detection functions in both direct PWM and constant current mode. The SG-FD and OL-OFF-FD signals are held to 0 while the OUTx pin is high.

If the TLE8242 IC is in direct PWM mode, Open Load ON detection is disabled (OL-ON-F = 0).

If the TLE8242 IC is not in direct PWM mode and the OUTx pin is high for 64 PWM periods, then the open load fault ON mode fault is detected, and the OL-ON-F bit in the diagnostic register is set. This bit will be cleared when SPI message #3 or #4 is read. If the OUTx pin remains in a high state, then the open load - on fault condition is detected again after another 64 PWM cycles.

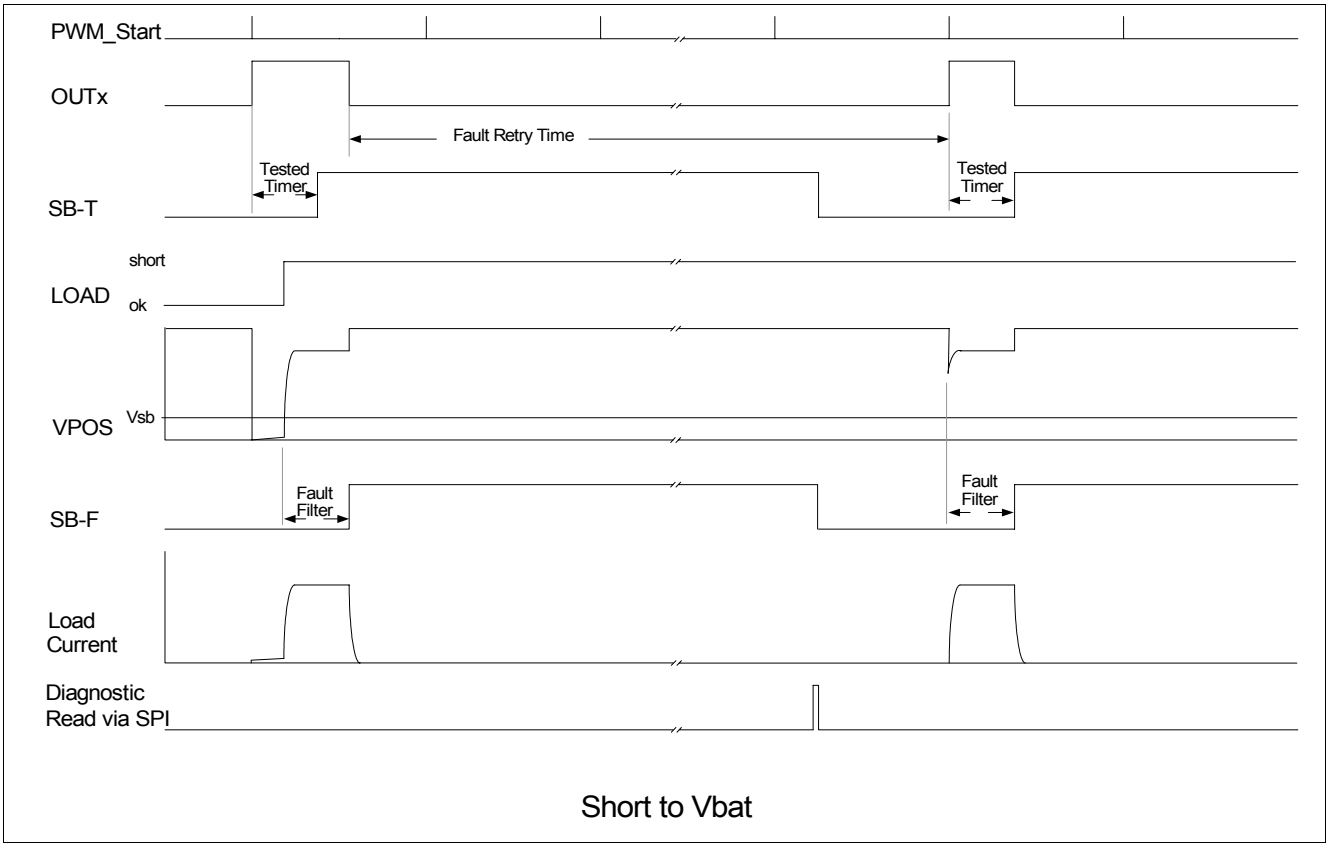


Figure 10 On-State Diagnostic Timing - Short to Vbat

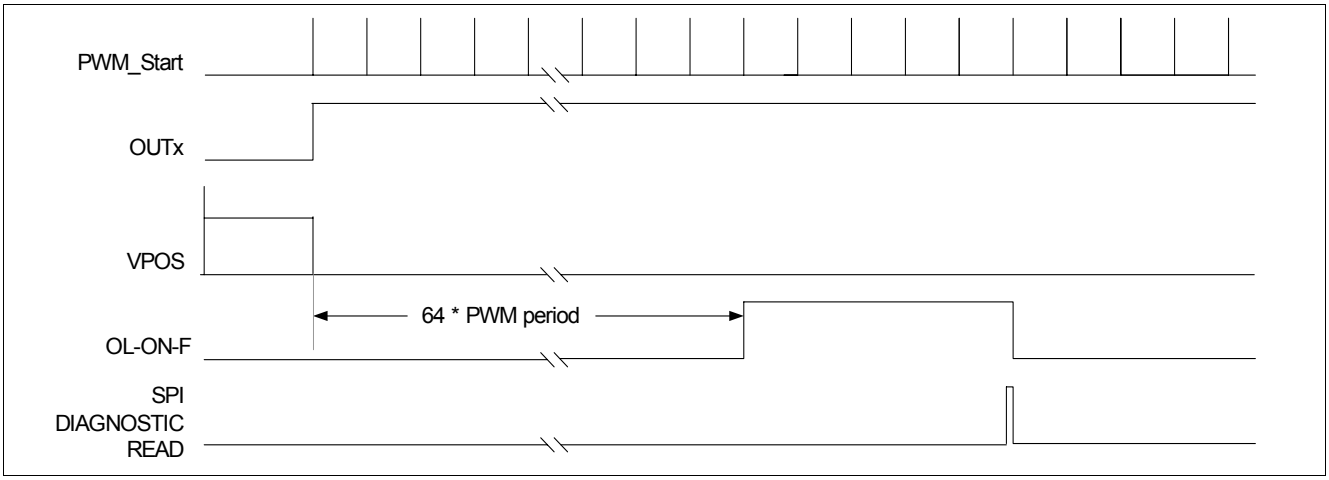


Figure 11 Open - On

5.3.2 Off-State Diagnostics

The off-state diagnostics function in both constant current mode and in direct PWM mode.

When the OUTx pin transitions low, the fault timers are cleared to 0 and the tested timer starts to count up. If the tested timer expires, the Bit OFF-T in the Diagnostic register is set. If a SPI diagnostic register read occurs, the tested timer is cleared to 0 and starts again to count up. If the OUTx pin transitions high, the tested-timer is cleared to zero and then used for on-state diagnostics.

If the analog OL fault signal (OL-FA) changes to 1, the fault filter timer starts to count up. If the fault filter timer expires, the digitally filtered OL fault signal (OL-ON-FD) is set to one.

If OL-FA changes to 0, OL-FD changes immediately to 0 and the fault filter timer is cleared to 0.

If the analog SG fault signal (SG-FA) changes to 1, the fault filter timer is cleared to 0 and starts to count up. If the fault filter timer expires, the digitally filtered SG fault signal (SG-FD) is set to one. If SG-FA changes to 0, SG-FD changes immediately to 0 and the fault filter timer is cleared to 0.

If SG-FD = 1 and the tested timer is expired then the SG-F bit in the FAULT register is set and the OL-OFF-F bit in the FAULT register remains unchanged (independently from OL-OFF-FD).

If SG-FD = 0 and OL-OFF-FD = 1 then the OL-F Bit in the FAULT register is set.

If a SPI fault read occurs, the OFF-T Bit, the SG-F Bit and the OL-F Bit in the SPI registers are cleared to zero (and the timers are cleared to 0).

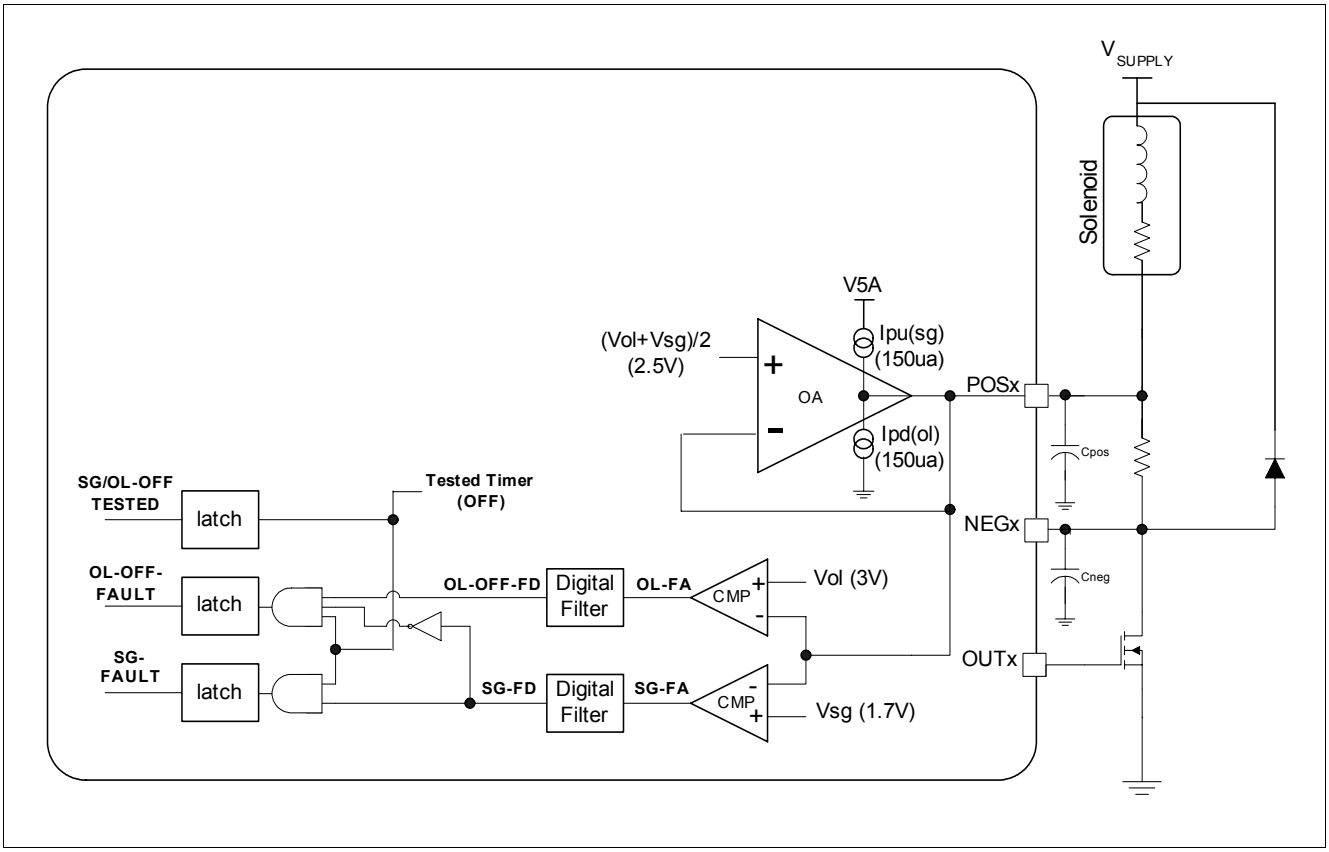


Figure 12 Off-State Diagnostics

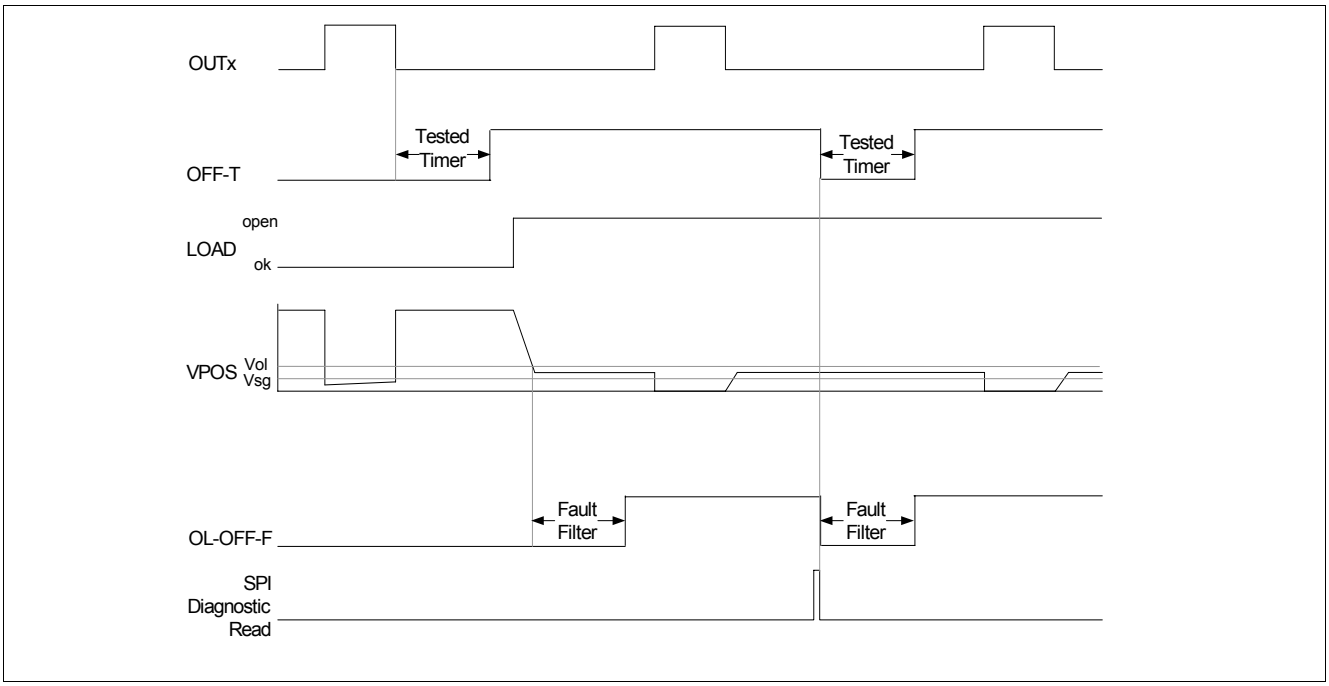


Figure 13 Off-State Diagnostics Timing Diagram - open