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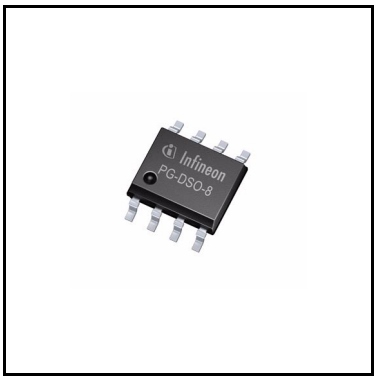
TLE8250

High Speed CAN Transceiver



1 Overview

Features

- Compatible to ISO 11898-2 (2016)
- Wide common mode range for electromagnetic immunity (EMI)
- Very low electromagnetic emission (EME)
- Excellent ESD robustness
- Guaranteed and improved loop delay symmetry to support CAN FD data frames up to 2 MBit/s
- Extended supply range on V_{CC} supply
- CAN short circuit proof to ground, battery and V_{CC}
- TxD time-out function
- Low CAN bus leakage current in power-down state
- Overtemperature protection
- Protected against automotive transients
- Receive-only mode and power-save mode
- Green Product (RoHS compliant)
- AEC Qualified
- Certified according to latest VeLIO (Vehicle LAN Interoperability & Optimization) test requirements for the Japanese market

Applications

- Engine Control Unit (ECUs)
- Transmission Control Units (TCUs)
- Chassis Control Modules
- Electric Power Steering

Description

The is a transceiver designed for HS CAN networks in automotive and industrial applications. As an interface between the physical bus layer and the CAN protocol controller, the drives the signals to the bus and protects the microcontroller against interferences generated within the network. Based on the high symmetry of the CANH and CANL signals, the provides a very low level of electromagnetic emission (EME) within a wide frequency range.
The TLE8250SJ fulfills or exceeds the requirements of the ISO11898-2.
The provides a receive-only mode and a power-save mode. It is designed to fulfill the enhanced physical layer

Overview

requirements for CAN FD and supports data rates up to 2 MBit/s.
On the basis of a very low leakage current on the HS CAN bus interface the provides an excellent passive behavior in power-down state. These and other features make the exceptionally suitable for mixed supply HS CAN networks.
Based on the Infineon Smart Power Technology SPT, the provides excellent ESD immunity together with a very high electromagnetic immunity (EMI). The and the Infineon SPT technology are AEC qualified and tailored to withstand the harsh conditions of the automotive environment.

Three different operating modes, additional fail-safe features like a TxD time-out and the optimized output slew rates on the CANH and CANL signals, make the the ideal choice for large HS CAN networks with high data transmission rates.

Type	Package	Marking
TLE8250SJ	PG-DSO-8	8250

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2 Block Diagram

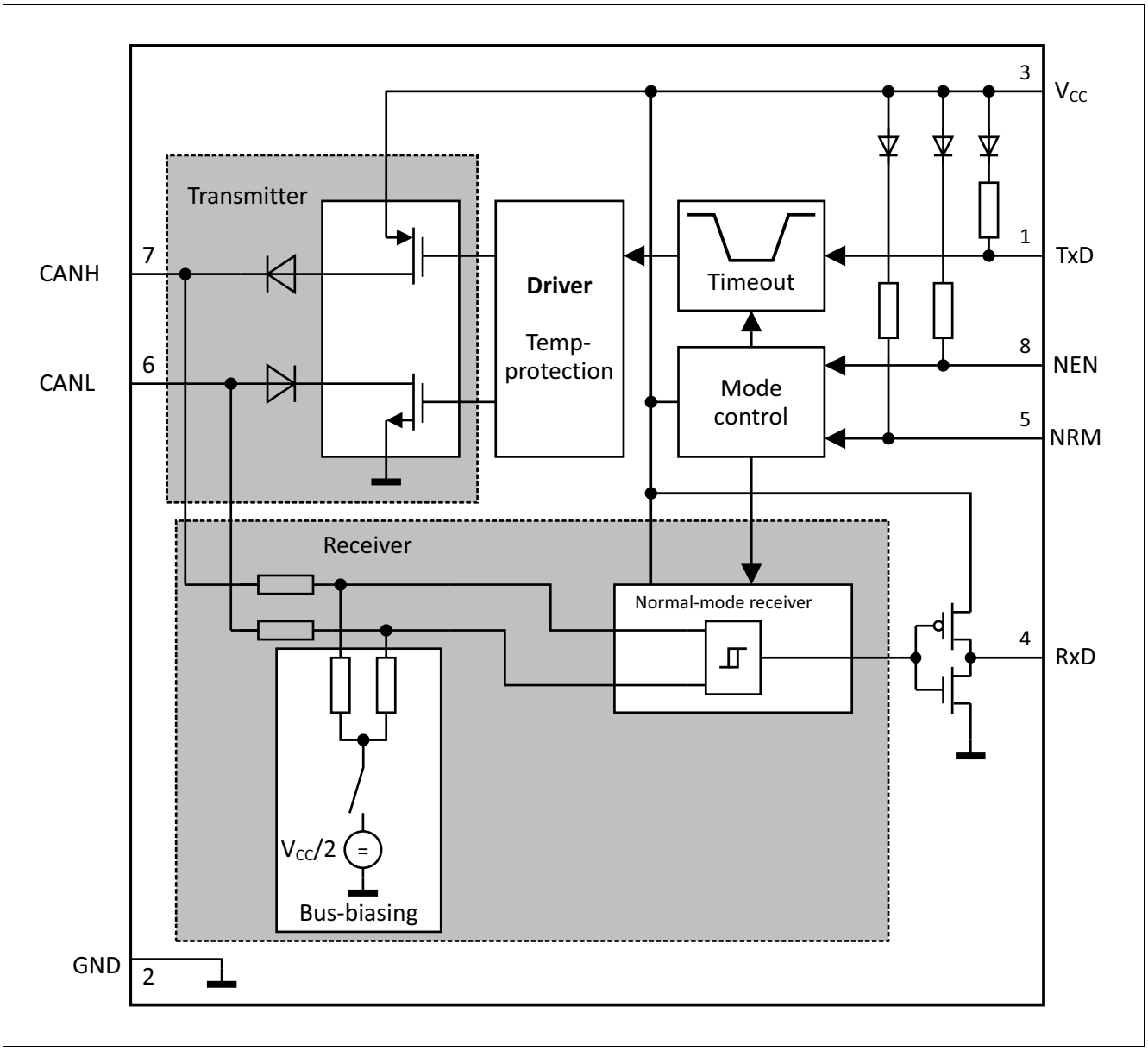

Figure 1 Functional block diagram

3 Pin Configuration

3.1 Pin Assignment

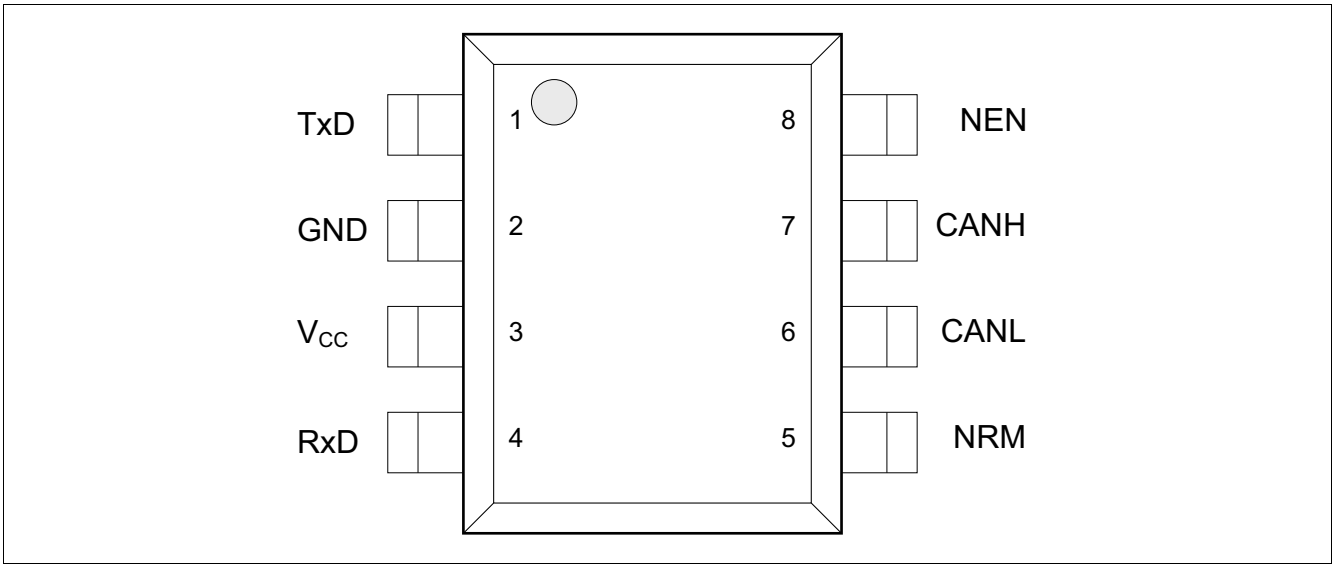

Figure 2 Pin configuration

3.2 Pin Definitions

Table 1 Pin definitions and functions

Pin No.	Symbol	Function
1	TxD	**Transmit Data Input;** internal pull-up to V_{CC}, “low” for dominant state.
2	GND	**Ground**
3	V_{CC}	**Transmitter Supply Voltage;** 100 nF decoupling capacitor to GND required.
4	RxD	**Receive Data Output;** “low” in dominant state.
5	NRM	**Not Receive-Only Mode Input;** control input for selecting receive-only mode, internal pull-up to V_{CC}, “low” for receive-only mode.
6	CANL	**CAN Bus Low Level I/O;** “low” in dominant state.
7	CANH	**CAN Bus High Level I/O;** “high” in dominant state.
8	NEN	**Not Enable Input;** internal pull-up to V_{CC}, “low” for normal-operating mode or receive-only mode.

4 Functional Description

HS CAN is a serial bus system that connects microcontrollers, sensors and actuators for real-time control applications. The use of the Controller Area Network (abbreviated CAN) within road vehicles is described by the international standard ISO 11898. According to the 7-layer OSI reference model the physical layer of a HS CAN bus system specifies the data transmission from one CAN node to all other available CAN nodes within the network. The physical layer specification of a CAN bus system includes all electrical and mechanical specifications of a CAN network. The CAN transceiver is part of the physical layer specification. Several different physical layer standards of CAN networks have been developed in recent years. The is a High Speed CAN transceiver without a wake-up function and defined by the international standard ISO11898-2.

4.1 High Speed CAN Physical Layer

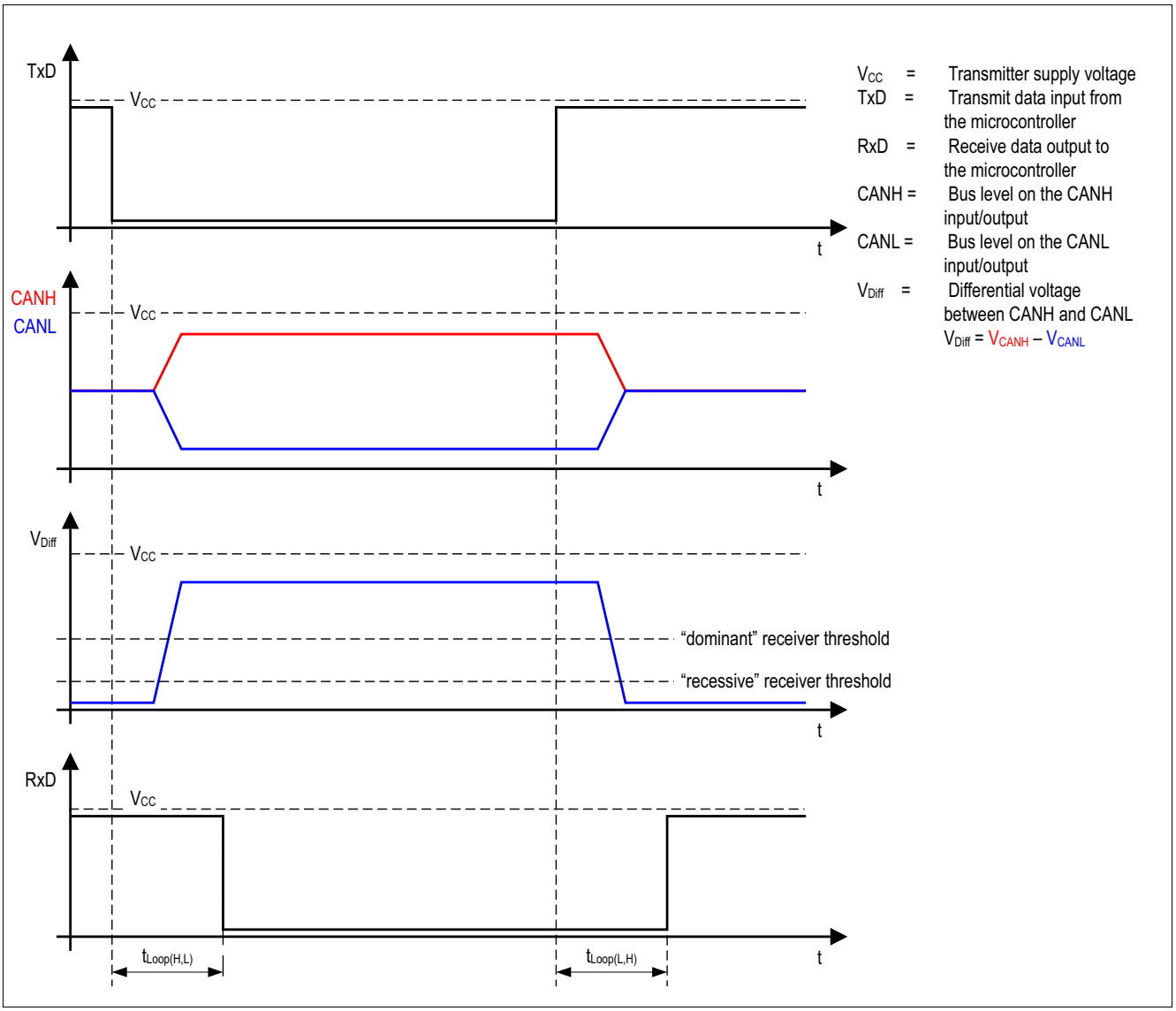

Figure 3 High speed CAN bus signals and logic signals

Functional Description

The is a High-Speed CAN transceiver, operating as an interface between the CAN controller and the physical bus medium. A HS CAN network is a two wire, differential network which allows data transmission rates for CAN FD frames up to 2 MBit/s. Characteristic for HS CAN networks are the two signal states on the HS CAN bus: dominant and recessive (see **Figure 3**).

V_{CC} and GND are the supply pins for the . The pins CANH and CANL are the interface to the HS CAN bus and operate in both directions, as an input and as an output. RxD and TxD pins are the interface to the CAN controller, the TxD pin is an input pin and the RxD pin is an output pin. The NEN and NRM pins are the input pins for the mode selection (see **Figure 4**).

By setting the TxD input pin to logical “low” the transmitter of the drives a dominant signal to the CANH and CANL pins. Setting TxD input to logical “high” turns off the transmitter and the output voltage on CANH and CANL discharges towards the recessive level. The recessive output voltage is provided by the bus-biasing (see **Figure 1**). The output of the transmitter is considered to be dominant, when the voltage difference between CANH and CANL is at least higher than 1.5 V ($V_{Diff} = V_{CANH} - V_{CANL}$).

Parallel to the transmitter the normal-mode receiver monitors the signal on the CANH and CANL pins and indicates it on the RxD output pin. A dominant signal on the CANH and CANL pins sets the RxD output pin to logical “low”, vice versa a recessive signal sets the RxD output to logical “high”. The normal-mode receiver considers a voltage difference (V_{Diff}) between CANH and CANL above 0.9 V as dominant and below 0.5 V as recessive.

To be conform with HS CAN features, like the bit to bit arbitration, the signal on the RxD output has to follow the signal on the TxD input within a defined loop delay $t_{Loop} \leq 255$ ns.

4.2 Modes of Operation

The supports three different modes of operation, power-save mode, receive-only mode and normal-operating mode while the transceiver is supplied according to the specified functional range. The mode of operation is selected by the NEN and the NRM input pins (see Figure 4).

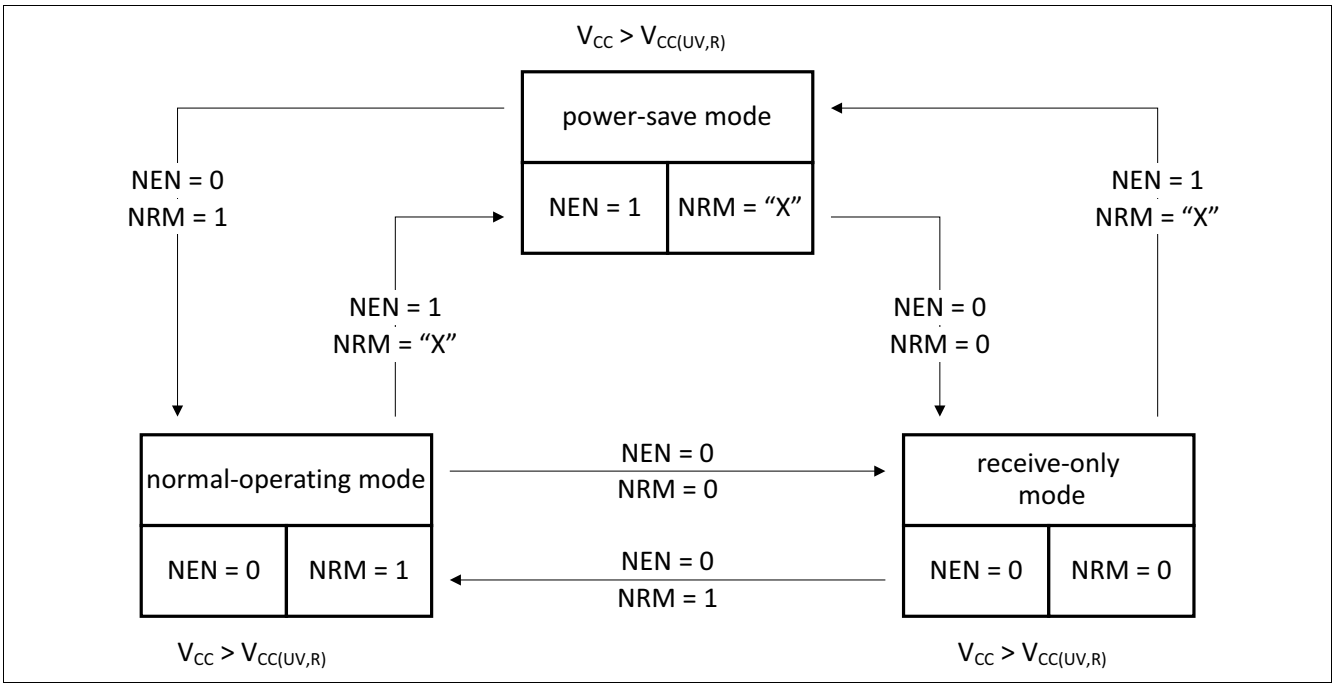

Figure 4 Mode state diagram

4.2.1 Normal-operating Mode

In normal-operating mode the transmitter and the receiver of the HS CAN transceiver are active (see Figure 1). The HS CAN transceiver sends the serial data stream on the TxD input pin to the CAN bus. The data on the CAN bus is displayed at the RxD pin simultaneously. A logical "low" signal on the NEN pin and a logical "high" signal on the NRM pin selects the normal-operating mode, while the transceiver is supplied by V_{CC} (see Table 2 for details).

4.2.2 Power-save Mode

The power-save mode is an idle mode of the with optimized power consumption. In power-save mode the transmitter and the normal-mode receiver are turned off. The can not send any data to the HS CAN bus nor receive any data from the HS CAN bus.

The RxD output pin is permanently "high" in the power-save mode.

A logical "high" signal on the NEN pin selects the power-save mode, while the transceiver is supplied by the transmitter supply V_{CC} (see Table 2 for details).

In power-save mode the bus input pins are not biased. Therefore the CANH and CANL input pins are floating and the HS CAN bus interface has a high resistance.

4.2.3 Receive-only Mode

In receive-only mode the normal-mode receiver is active and the transmitter is turned off. The can receive data from the HS CAN bus, but cannot send any data to the HS CAN bus.

A logical "low" signal on the NEN pin and a logical "low" signal on the NRM pin selects the receive-only mode, while the transceiver is supplied by V_{CC} (see Table 2 for details).

4.3 Power-up and Undervoltage Condition

By detecting an undervoltage event or by switching off the transmitter power supply V_{CC}, the transceiver changes the mode of operation (details see Figure 5).

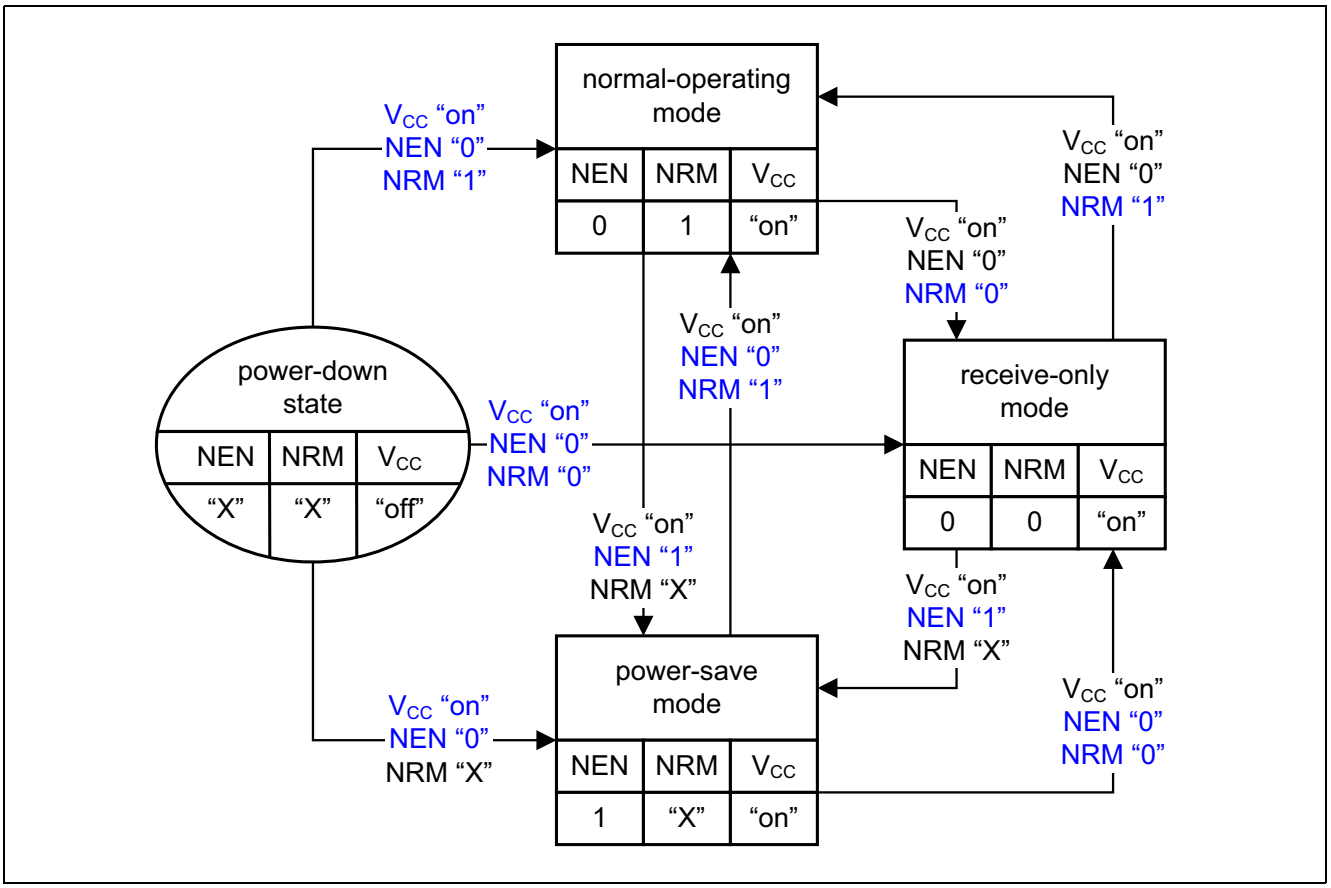

Figure 5 Power-up and undervoltage

Table 2 Modes of operation

Mode	NEN	NRM	V_{cc}	Bus-bias	Transmitter	Normal-mode Receiver	Low-power Receiver
Normal-operating	"low"	"high"	"on"	$V_{CC}/2$	"on"	"on"	not available
Power-save	"high"	"X"	"on"	floating	"off"	"off"	not available
Receive-only	"low"	"low"	"on"	$V_{CC}/2$	"off"	"on"	not available
Power-down state	"X[1)]"	"X"	"off"	floating	"off"	"off"	not available

1) "X": Don't care

4.3.1 Power-down State

Independent of the NEN and NRM input pins the is in power-down state when the transmitter supply voltage V_{CC} is turned off (see Figure 5).

In the power-down state the input resistors of the receiver are disconnected from the bus biasing $V_{CC}/2$. The CANH and CANL bus interface of the is floating and acts as a high-impedance input with a very small leakage current. The high-ohmic input does not influence the recessive level of the CAN network and allows an optimized EME performance of the entire HS CAN network (see also Table 2).

4.3.2 Power-up

The HS CAN transceiver powers up if the transmitter supply V_{CC} is connected to the device. By default the device powers up in power-save mode, due to the internal pull-up resistor on the NEN pin to V_{CC}.

In case the device needs to power-up to normal-operating mode, the NEN pin needs to be pulled active to logical “low” while the NRM pin is logical “high” (see Figure 5).

4.3.3 Undervoltage on the Transmitter Supply V_{CC}

In case the transmitter supply V_{CC} falls below the threshold $V_{CC} < V_{CC(UV,F)}$, the transceiver can not provide the correct bus levels to the CANH and CANL anymore. The normal-mode receiver is powered by the transmitter supply V_{CC}. In case of insufficient V_{CC} supply the can neither transmit the CANH and CANL signals correctly to bus nor can it receive them properly. Therefore the powers down and blocks both, the transmitter and the receiver.

The transceiver powers up again, when the transmitter supply V_{CC} recovers from the undervoltage condition.

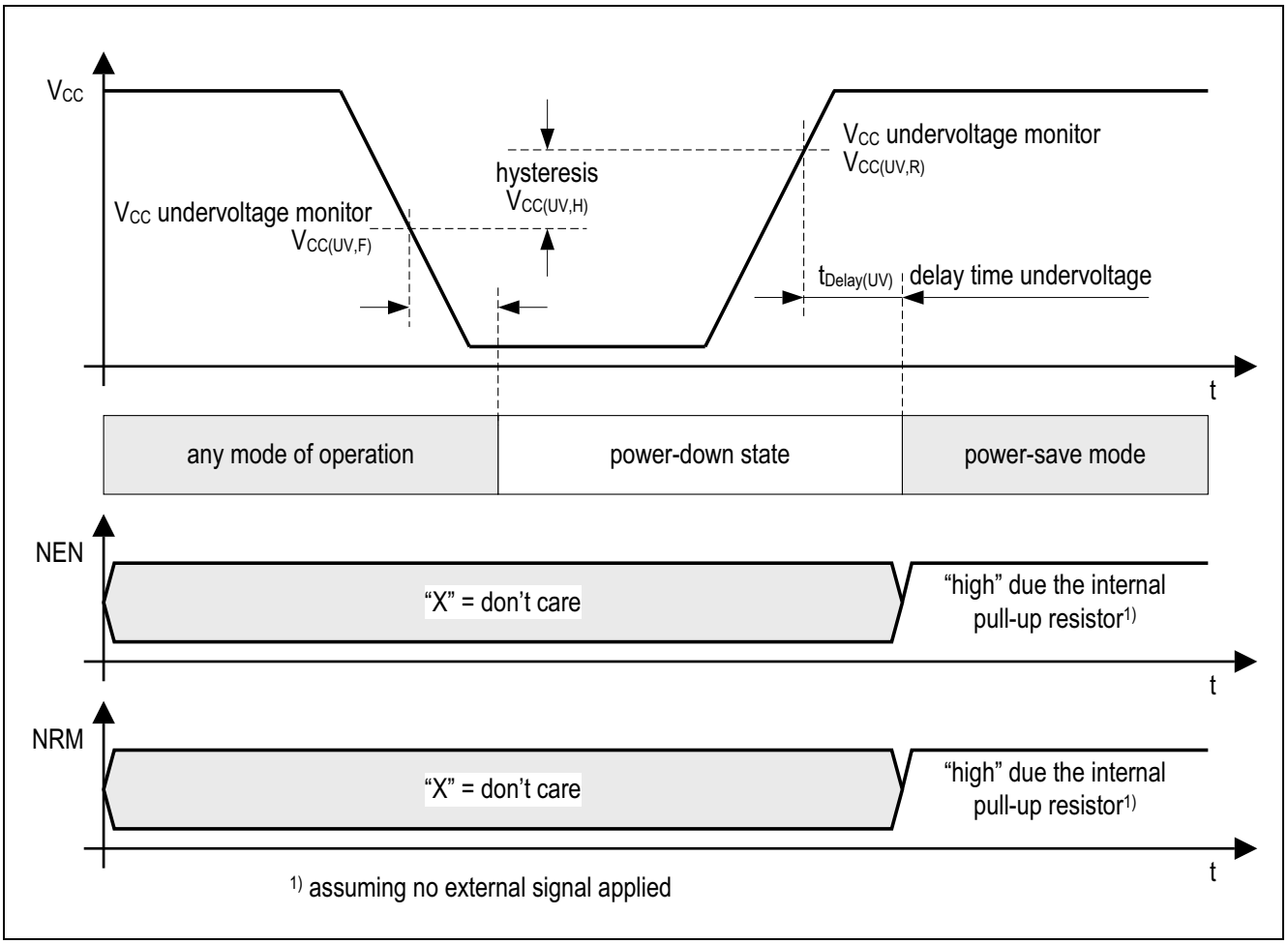

Figure 6 Undervoltage on the transmitter supply V_{CC}

5 Fail Safe Functions

5.1 Short Circuit Protection

The CANH and CANL bus outputs are short circuit proof, either against GND or a positive supply voltage. A current limiting circuit protects the transceiver against damages. If the device is heating up due to a continuous short on the CANH or CANL, the internal overtemperature protection switches off the bus transmitter.

5.2 Unconnected Logic Pins

All logic input pins have an internal pull-up resistor to V_{CC}. In case the V_{CC} supply is activated and the logical pins are open, the enters into the power-save mode by default. In power-save mode the transmitter of the is disabled and the bus bias is floating.

5.3 TxD Time-out Function

The TxD time-out feature protects the CAN bus against permanent blocking in case the logical signal on the TxD pin is continuously “low”. A continuous “low” signal on the TxD pin might have its root cause in a locked-up microcontroller or in a short circuit on the printed circuit board, for example. In normal-operating mode, a logical “low” signal on the TxD pin for the time $t > t_{TxD}$ enables the TxD time-out feature and the disables the transmitter (see Figure 7). The receiver is still active and the data on the bus continues to be monitored by the RxD output pin.

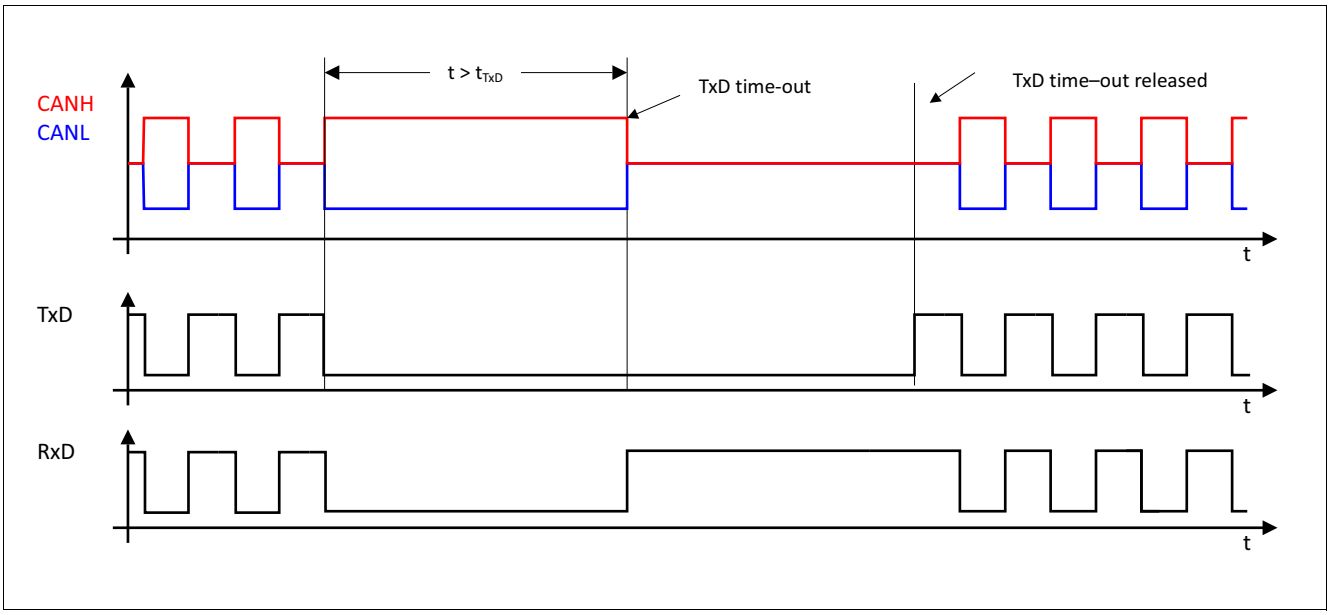

Figure 7 TxD time-out function

Figure 7 illustrates how the transmitter is deactivated and activated again. A permanent “low” signal on the TxD input pin activates the TxD time-out function and deactivates the transmitter. To release the transmitter after a TxD time-out event the requires a signal change on the TxD input pin from logical “low” to logical “high”.

5.4 Overtemperature Protection

The has an integrated overtemperature detection to protect the against thermal overstress of the transmitter. The overtemperature protection is active in normal-operating mode and disabled in power-save mode and receive-only mode. In case of an overtemperature condition, the temperature sensor will disable the transmitter (see Figure 1) while the transceiver remains in normal-operating mode.

After the device has cooled down the transmitter is activated again (see Figure 8). A hysteresis is implemented within the temperature sensor.

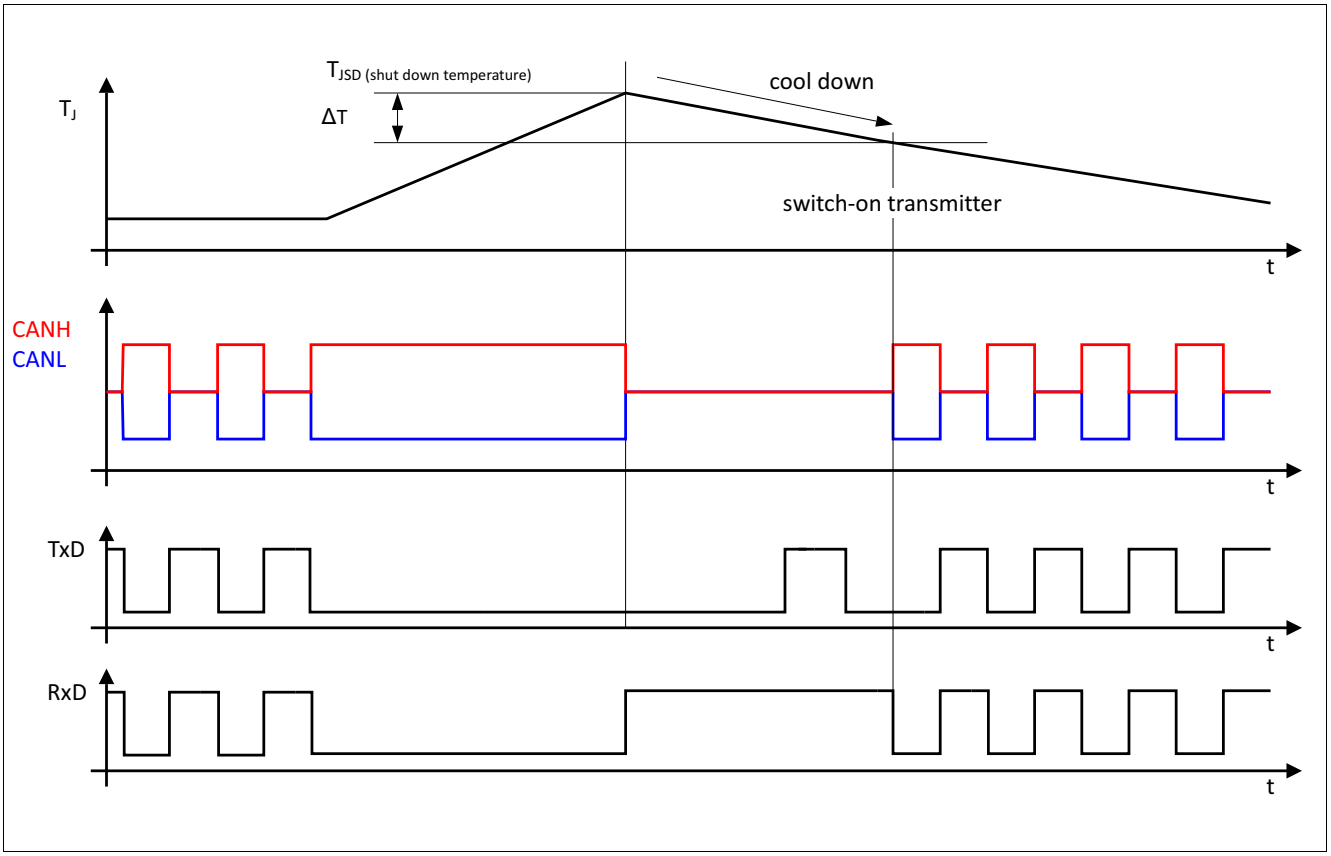

Figure 8 Overtemperature protection

5.5 Delay Time for Mode Change

The HS CAN transceiver changes the mode of operation within the time window t_{Mode}. Depending on the selected mode of operation, the RxD output pin is set to logical “high” during the mode change.
In this case the RxD output does not reflect the status on the CANH and CANL input pins (see as an example Figure 12 and Figure 13).

6 General Product Characteristics

6.1 Absolute Maximum Ratings

Table 3 Absolute maximum ratings voltages, currents and temperatures[1)]

All voltages with respect to ground; positive current flowing into pin;
(unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Voltages							
Transmitter supply voltage	V_{CC}	-0.3	–	6.0	V	–	P_6.1.1
CANH DC voltage versus GND	V_{CANH}	-40	–	40	V	–	P_6.1.2
CANL DC voltage versus GND	V_{CANL}	-40	–	40	V	–	P_6.1.3
Differential voltage between CANH and CANL	$V_{CAN\ SDiff}$	-40	–	40	V	–	P_6.1.4
Voltages at the input pins: NEN, NRM, TxD	V_{MAX_IN}	-0.3	–	6.0	V	–	P_6.1.5
Voltages at the output pin: RxD	V_{MAX_OUT}	-0.3	–	V_{CC}	V	–	P_6.1.6
Currents							
RxD output current	I_{RxD}	-20	–	20	mA	–	P_6.1.7
Temperatures							
Junction temperature	T_j	-40	–	150	°C	–	P_6.1.8
Storage temperature	T_S	-55	–	150	°C	–	P_6.1.9
ESD Resistivity							
ESD immunity at CANH, CANL versus GND	$V_{ESD\_HBM\_CAN}$	-10	–	10	kV	HBM (100 pF via 1.5 kΩ)[2)]	P_6.1.10
ESD immunity at all other pins	$V_{ESD\_HBM\_ALL}$	-2	–	2	kV	HBM (100 pF via 1.5 kΩ)[2)]	P_6.1.11
ESD immunity to GND	V_{ESD_CDM}	-750	–	750	V	CDM[3)]	P_6.1.12

1) Not subject to production test, specified by design
2) ESD susceptibility, Human Body Model “HBM” according to ANSI/ESDA/JEDEC JS-001
3) ESD susceptibility, Charge Device Model “CDM” according to EIA/JESD22-C101 or ESDA STM5.3.1

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal-operating range. Protection functions are not designed for continuos repetitive operation.

6.2 Functional Range

Table 4 Functional range

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Supply Voltages							
Transmitter supply voltage	V_{CC}	4.5	–	5.5	V	–	P_6.2.1
Thermal Parameters							
Junction temperature	T_j	-40	–	150	°C	1)	P_6.2.2

1) Not subject to production test, specified by design.

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

6.3 Thermal Resistance

Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, please visit www.jedec.org.

Table 5 Thermal resistance[1)]

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Thermal Resistances							
Junction to Ambient PG-DSO-8	R_{thJA}	–	130	–	K/W	2) TLE8250SJ	P_6.3.2
Thermal Shutdown (junction temperature)							
Thermal shutdown temperature	T_{JSD}	150	175	200	°C	–	P_6.3.3
Thermal shutdown hysteresis	ΔT	–	10	–	K	–	P_6.3.4

1) Not subject to production test, specified by design

2) Specified R_{thJA} value is according to Jedec JESD51-2,-7 at natural convection on FR4 2s2p board. The product ( ) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70µm Cu, 2 x 35µm Cu).

7 Electrical Characteristics

7.1 Functional Device Characteristics

Table 6 Electrical characteristics

4.5 V < V_{CC} < 5.5 V; R_L = 60 Ω; -40 °C < T_j < 150 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Current Consumption							
Current consumption at V_{CC} normal-operating mode	I_{CC}	–	2.6	5	mA	recessive state, $V_{TxD} = V_{NRM} = V_{CC}$, V_{NEN} = 0 V;	P_7.1.1
Current consumption at V_{CC} normal-operating mode	I_{CC}	–	38	60	mA	dominant state, $V_{TxD} = V_{NEN}$ = 0 V, $V_{NRM} = V_{CC}$;	P_7.1.2
Current consumption at V_{CC} receive-only mode	$I_{CC(ROM)}$	–	2	3	mA	$V_{NEN} = V_{NRM}$ = 0 V;	P_7.1.3
Current consumption at V_{CC} power-save mode	$I_{CC(PSM)}$	–	5	12	µA	$V_{TxD} = V_{NEN} = V_{NRM} = V_{CC}$;	P_7.1.4
Supply Resets							
V_{CC} undervoltage monitor rising edge	$V_{CC(UV,R)}$	3.8	4.0	4.3	V	–	P_7.1.5
V_{CC} undervoltage monitor falling edge	$V_{CC(UV,F)}$	3.65	3.85	4.3	V	–	P_7.1.6
V_{CC} undervoltage monitor hysteresis	$V_{CC(UV,H)}$	–	150	–	mV	1)	P_7.1.7
V_{CC} undervoltage delay time	$t_{Delay(UV)}$	–	–	100	µs	1) (see Figure 6);	P_7.1.8
Receiver Output RxD							
“High” level output current	$I_{RD,H}$	–	-4	-2	mA	$V_{RxD} = V_{CC}$ - 0.4 V, V_{Diff} < 0.5 V;	P_7.1.9
“Low” level output current	$I_{RD,L}$	2	4	–	mA	V_{RxD} = 0.4 V, V_{Diff} > 0.9 V;	P_7.1.10

Table 6 Electrical characteristics (cont'd)

4.5 V < V_{CC} < 5.5 V; R_L = 60 Ω; -40 °C < T_j < 150 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Transmission Input TxD							
"High" level input voltage threshold	$V_{TxD,H}$	–	0.5 × V_{CC}	0.7 × V_{CC}	V	recessive state;	P_7.1.11
"Low" level input voltage threshold	$V_{TxD,L}$	0.3 × V_{CC}	0.4 × V_{CC}	–	V	dominant state;	P_7.1.12
Pull-up resistance	R_{TxD}	10	25	50	kΩ	–	P_7.1.13
Input hysteresis	$V_{HYS(TxD)}$	–	450	–	mV	1)	P_7.1.14
Input capacitance	C_{TxD}	–	–	10	pF	1)	P_7.1.15
TxD permanent dominant time-out	t_{TxD}	4.5	–	16	ms	normal-operating mode;	P_7.1.16
Not Enable Input NEN							
"High" level input voltage threshold	$V_{NEN,H}$	–	0.5 ´ V_{CC}	0.7 ´ V_{CC}	V	power-save mode;	P_7.1.17
"Low" level input voltage threshold	$V_{NEN,L}$	0.3 ´ V_{CC}	0.4 ´ V_{CC}	–	V	normal-operating mode, receive-only mode;	P_7.1.18
Pull-up resistance	R_{NEN}	10	25	50	kW	–	P_7.1.19
Input capacitance	C_{NEN}	–	–	10	pF	1)	P_7.1.20
Input hysteresis	$V_{HYS(NEN)}$	–	200	–	mV	1)	P_7.1.21
Not Receive-only Input NRM							
"High" level input voltage threshold	$V_{NRM,H}$	–	0.5 ´ V_{CC}	0.7 ´ V_{CC}	V	normal-operating mode, power-save mode;	P_7.1.22
"Low" level input voltage threshold	$V_{NRM,L}$	0.3 ´ V_{CC}	0.4 ´ V_{CC}	–	V	receive-only mode, power-save mode;	P_7.1.23
Pull-up resistance	R_{NRM}	10	25	50	kW	–	P_7.1.24
Input capacitance	C_{NRM}	–	–	10	pF	1)	P_7.1.25
Input hysteresis	$V_{NRM(HYS)}$	–	200	–	mV	1)	P_7.1.26
Bus Receiver							
Differential receiver threshold dominant normal-operating mode and receive-only mode	V_{Diff_D}	–	0.75	0.9	V	2)	P_7.1.27
Differential receiver threshold recessive normal-operating mode and receive-only mode	V_{Diff_R}	0.5	0.66	–	V	2)	P_7.1.28
Differential range dominant Normal-operating mode	$V_{Diff\_D\_Range}$	0.9	–	8.0	V	1) 2)	P_7.1.29

Table 6 Electrical characteristics (cont'd)

4.5 V < V_{CC} < 5.5 V; R_L = 60 Ω; -40 °C < T_j < 150 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Differential range recessive Normal-operating mode	$V_{Diff\_R\_Range}$	-3.0	–	0.5	V	1) 2)	P_7.1.30
Common mode range	*CMR*	-12	–	12	V	V_{CC} = 5 V;	P_7.1.31
Differential receiver hysteresis normal-operating mode	$V_{Diff,hys}$	–	90	–	mV	1)	P_7.1.32
CANH, CANL input resistance	R_i	10	20	30	kΩ	recessive state;	P_7.1.33
Differential input resistance	R_{Diff}	20	40	60	kΩ	recessive state;	P_7.1.34
Input resistance deviation between CANH and CANL	ΔR_i	- 1	–	1	%	1) recessive state;	P_7.1.35
Input capacitance CANH, CANL versus GND	C_{In}	–	20	40	pF	1) V_{TxD} = V_{CC};	P_7.1.36
Differential input capacitance	C_{InDiff}	–	10	20	pF	1) V_{TxD} = V_{CC};	P_7.1.37
Bus Transmitter							
CANL/CANH recessive output voltage normal-operating mode	$V_{CANL/H}$	2.0	2.5	3.0	V	V_{TxD} = V_{CC}, no load;	P_7.1.38
CANH, CANL recessive output voltage difference normal-operating mode	V_{Diff_NM}	-500	–	50	mV	V_{TxD} = V_{CC}, no load;	P_7.1.39
CANL dominant output voltage normal-operating mode	V_{CANL}	0.5	–	2.25	V	V_{TxD} = 0 V;	P_7.1.40
CANH dominant output voltage normal-operating mode	V_{CANH}	2.75	–	4.5	V	V_{TxD} = 0 V;	P_7.1.41
CANH, CANL dominant output voltage difference normal-operating mode according to ISO 11898-2 V_{Diff} = V_{CANH} - V_{CANL}	V_{Diff}	1.5	–	3.0	V	V_{TxD} = 0 V, 50 Ω < R_L < 65 Ω, 4.75 < V_{CC} < 5.25 V;	P_7.1.42
CANH, CANL dominant output voltage difference normal-operating mode V_{Diff} = V_{CANH} - V_{CANL}	V_{Diff_EXT}	1.4	–	3.3	V	V_{TxD} = 0 V, 45 Ω < R_L < 70 Ω, 4.75 < V_{CC} < 5.25 V;	P_7.1.43
Differential voltage dominant high extended bus load Normal-operating mode	$V_{Diff\_HEX\_BL}$	1.5	–	5.0	V	V_{TxD} = 0 V, R_L = 2240Ω, 4.75 V < V_{CC} < 5.25 V, static behavior;1)	P_7.1.44

Table 6 Electrical characteristics (cont'd)

4.5 V < V_{CC} < 5.5 V; R_L = 60 Ω; -40 °C < T_j < 150 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Driver dominant symmetry normal-operating mode $V_{SYM} = V_{CANH} + V_{CANL}$	V_{SYM}	4.5	5	5.5	V	V_{CC} = 5.0 V, V_{TxD} = 0 V;	P_7.1.45
CANL short circuit current	I_{CANLsc}	40	75	100	mA	$V_{CANLshort}$ = 18 V, V_{CC} = 5.0 V, $t < t_{TxD}$, V_{TxD} = 0 V;	P_7.1.46
CANH short circuit current	I_{CANHsc}	-100	-75	-40	mA	$V_{CANHshort}$ = -3 V, V_{CC} = 5.0 V, $t < t_{TxD}$, V_{TxD} = 0 V;	P_7.1.47
Leakage current, CANH	$I_{CANH,lk}$	-5	–	5	µA	V_{CC} = 0 V, 0 V < V_{CANH} < 5 V, V_{CANH}=V_{CANL};	P_7.1.48
Leakage current, CANL	$I_{CANL,lk}$	-5	–	5	µA	V_{CC} = 0 V, 0 V < V_{CANL} < 5 V, V_{CANH}=V_{CANL};	P_7.1.49
Dynamic CAN-Transceiver Characteristics							
Propagation delay TxD-to-RxD "low" ("recessive to dominant)	$t_{Loop(H,L)}$	–	170	230	ns	C_L = 100 pF, 4.75 V < V_{CC} < 5.25 V, C_{RxD} = 15 pF;	P_7.1.50
Propagation delay TxD-to-RxD "high" (dominant to recessive)	$t_{Loop(L,H)}$	–	170	230	ns	C_L = 100 pF, 4.75 V < V_{CC} < 5.25 V, C_{RxD} = 15 pF;	P_7.1.51
Propagation delay TxD "low" to bus dominant	$t_{d(L),T}$	–	90	140	ns	C_L = 100 pF, 4.75 V < V_{CC} < 5.25 V, C_{RxD} = 15 pF;	P_7.1.52
Propagation delay TxD "high" to bus recessive	$t_{d(H),T}$	–	90	140	ns	C_L = 100 pF, 4.75 V < V_{CC} < 5.25 V, C_{RxD} = 15 pF;	P_7.1.53
Propagation delay bus dominant to RxD "low"	$t_{d(L),R}$	–	90	140	ns	C_L = 100 pF, 4.75 V < V_{CC} < 5.25 V, C_{RxD} = 15 pF;	P_7.1.54
Propagation delay bus recessive to RxD "high"	$t_{d(H),R}$	–	90	140	ns	C_L = 100 pF, 4.75 V < V_{CC} < 5.25 V, C_{RxD} = 15 pF;	P_7.1.55
Delay Times							
Delay time for mode change	t_{Mode}	–	–	20	µs	[1] (see Figure 12 and Figure 13);	P_7.1.56

Table 6 Electrical characteristics (cont'd)

4.5 V < V_{CC} < 5.5 V; R_L = 60 Ω; -40 °C < T_j < 150 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
CAN FD Characteristics							
Received recessive bit width at 2 MBit/s	$t_{Bit(RxD)\_2MB}$	430	500	530	ns	C_L = 100 pF, 4.75 V < V_{CC} < 5.25 V, C_{RxD} = 15 pF, t_{Bit} = 500 ns, (see **Figure 11**);	P_7.1.57
Transmitted recessive bit width at 2 MBit/s	$t_{Bit(Bus)\_2MB}$	450	500	530	ns	C_L = 100 pF, 4.75 V < V_{CC} < 5.25 V, C_{RxD} = 15 pF, t_{Bit} = 500 ns, (see **Figure 11**);	P_7.1.58
Receiver timing symmetry at 2 MBit/s $\Delta t_{Rec} = t_{Bit(RxD)} - t_{Bit(Bus)}$	Δt_{Rec_2MB}	-45	–	20	ns	C_L = 100 pF, 4.75 V < V_{CC} < 5.25 V, C_{RxD} = 15 pF, t_{Bit} = 500 ns, (see **Figure 11**);	P_7.1.59

1) Not subject to production test, specified by design.
2) In respect to the common mode range.

7.2 Diagrams

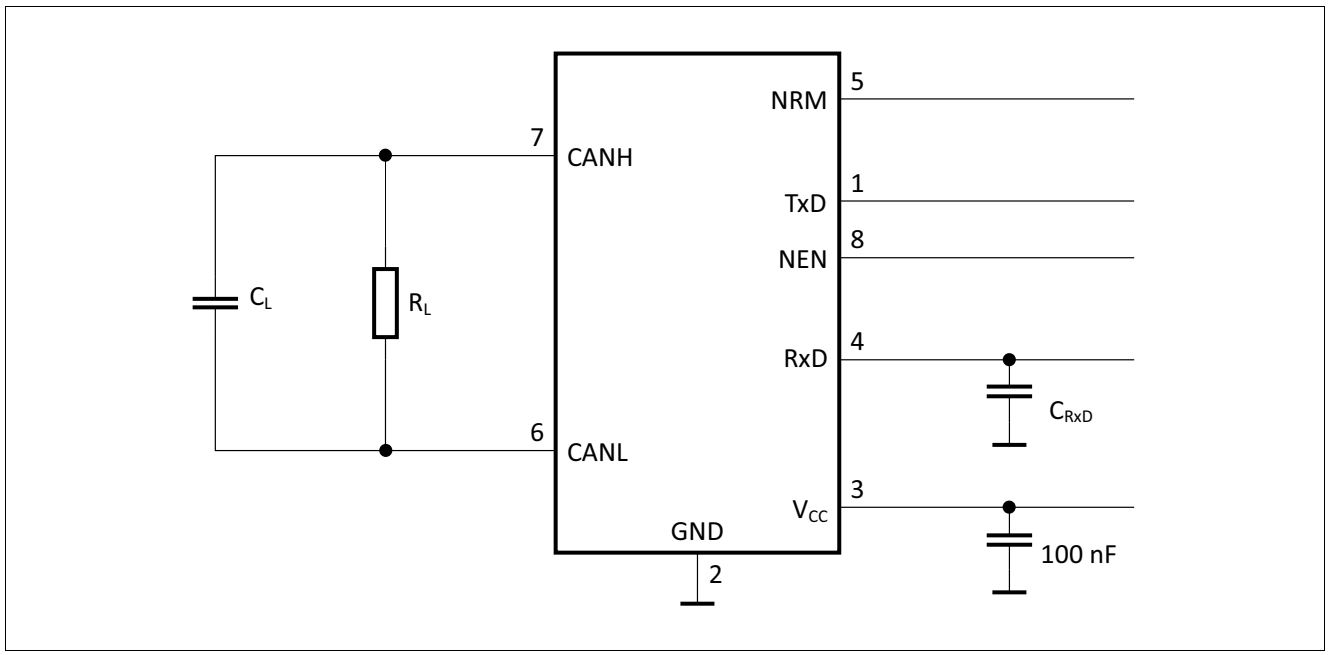

Figure 9 Test circuits for dynamic characteristics

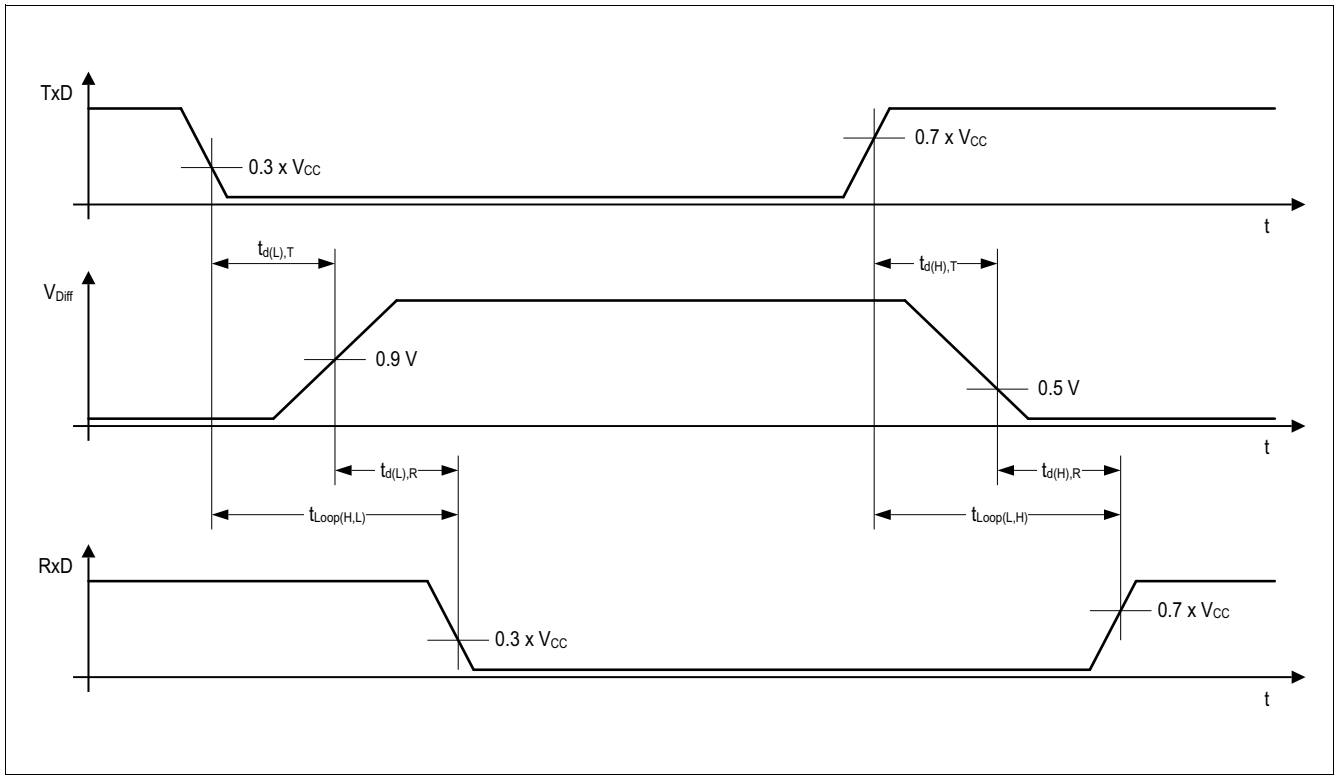

Figure 10 Timing diagrams for dynamic characteristics

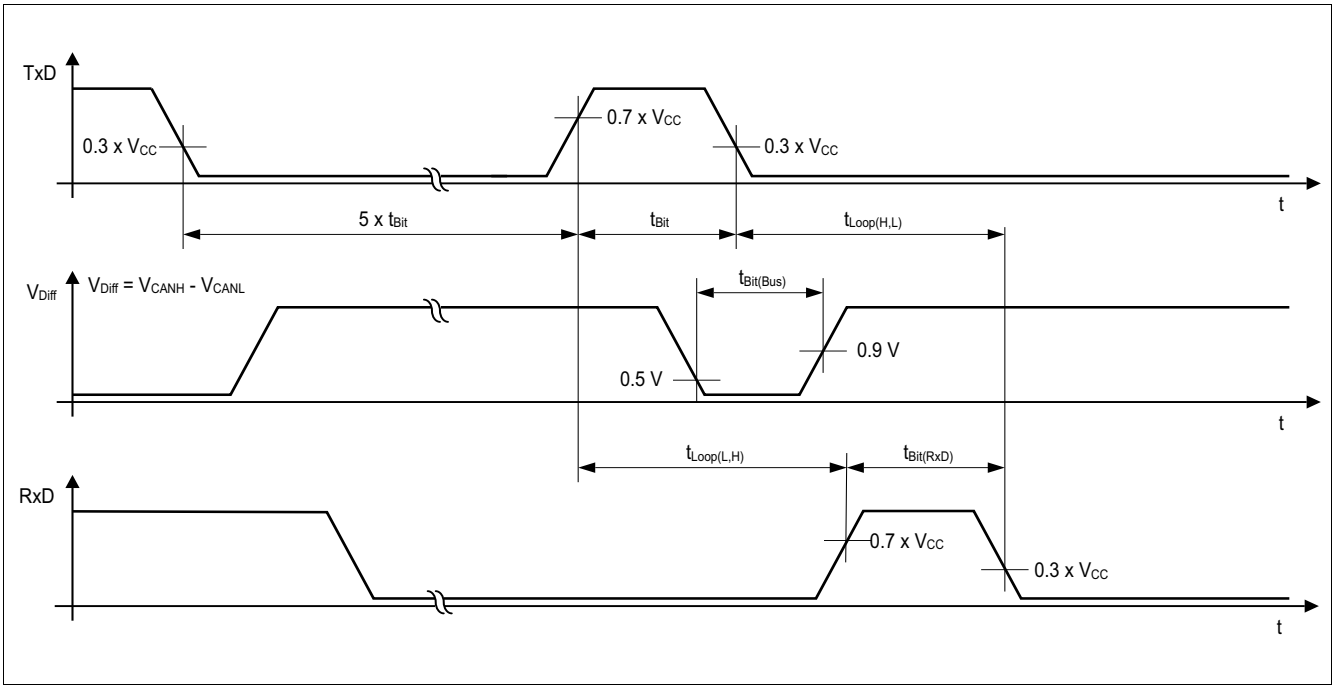

Figure 11 Recessive bit width - five dominant bits followed by one recessive bit

8 Application Information

8.1 ESD Robustness according to IEC61000-4-2

Tests for ESD robustness according to IEC61000-4-2 “Gun test” (150 pF, 330 Ω) have been performed. The results and test conditions are available in a separate test report.

Table 7 ESD robustness according to IEC61000-4-2

Performed Test	Result	Unit	Remarks
Electrostatic discharge voltage at pin CANH and CANL versus GND	≥ +8	kV	[1)]Positive pulse
Electrostatic discharge voltage at pin CANH and CANL versus GND	≤ -8	kV	[1)]Negative pulse

1) ESD susceptibility “ESD GUN” according to GIFT / ICT paper: “EMC Evaluation of CAN Transceivers, version 03/02/IEC TS62228”, section 4.3. (DIN EN61000-4-2)
Tested by external test facility (IBEE Zwickau, EMC test report no. TBD).

8.2 Application Example

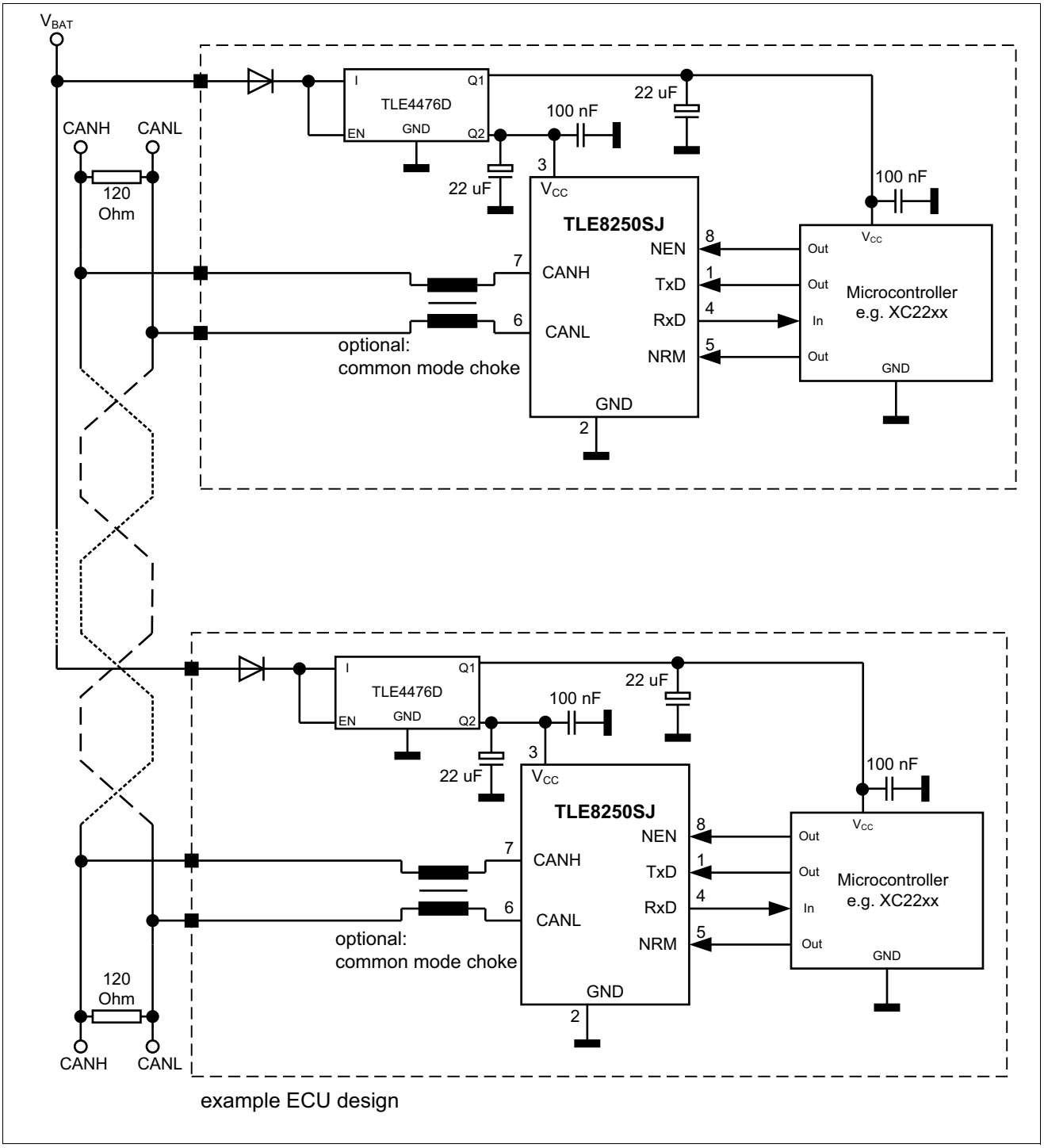

Figure 12 Application circuit

8.3 Examples for Mode Changes

- The mode change is executed independently of the signal on the HS CAN bus. The CANH, CANL inputs may be either dominant or recessive. They can be also permanently shorted to GND or V_{CC}.
- A mode change is performed independently of the signal on the TxD input. The TxD input may be either logical “high” or “low”.

Analog to that, changing the NEN input pin to logical “high” changes the mode of operation to the power-save mode. Changing the NEN input pin and the NRM input pin to logical “low” changes the mode of operation to the receive-only mode. Both mode changes are independent on the signals at the CANH, CANL and TxD pins.

Note: In case the TxD signal is “low” setting the NRM input pin to logical “high” and the NEN input pin to logical “low” changes the device to normal-operating mode and drives a dominant signal to the HS CAN bus”.

Note: The TxD time-out is only effective in normal-operating mode. The TxD time-out timer starts when the enters normal-operating mode and the TxD input is set to logical “low”.