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# TLE8264E

Universal System Basis Chip  
HERMES  
Rev. 1.0

Automotive Power



Never stop thinking

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## 1 HERMES Overview

### Scalable System Basis Chip Family

- Eight products for complete scalable application coverage
- Complete compatibility (hardware and software) across the family
- TLE8264-2E (3LIN), TLE8263-2E (2LIN) - 3 Limp Home outputs
- TLE8264E (3LIN), TLE8263E (2LIN) - 1 Limp Home output
- TLE8262-2E (1LIN), TLE8261-2E (no LIN) - 3 Limp Home outputs
- TLE8262E (1LIN), TLE8261E (no LIN) - 1 Limp Home output

### Basic Features

- Very low quiescent current in Stop and Sleep Modes
- Reset input, output
- Power on and scalable undervoltage reset generator
- Standard 16-bit SPI interface
- Overtemperature and short circuit protection
- Short circuit proof to GND and battery
- One universal wake-up input
- Wide input voltage and temperature range
- Cyclic wake in Stop Mode
- Green Product (RoHS compliant)
- AEC Qualified

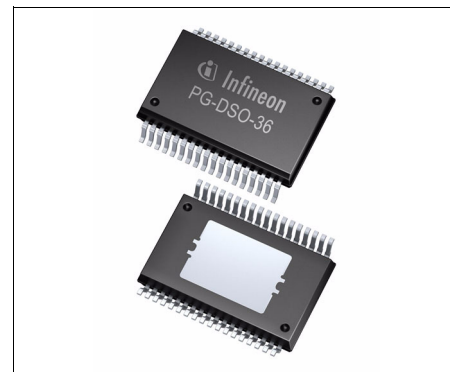
### Description

The devices of the SBC family are monolithic integrated circuits in an enhanced power package with identical software functionality and hardware features except for the number of LIN cells. The devices are designed for CAN-LIN automotive applications e.g. body controller, gateway applications.

To support these applications, the System Basis Chip (SBC) provides the main functions, such as HS-CAN transceiver and LIN transceivers for data transmission, low dropout voltage regulators (LDO) for an external 5 V supply, and a 16-bit Serial Peripheral Interface (SPI) to control and monitor the device. Also implemented are a Time-out or a Window Watchdog circuit with a reset feature, Limp Home circuitry output, and an undervoltage reset feature.

The devices offer low power modes in order to support application that are connected permanent to the battery. A wake-up from the low power mode is possible via a message on the buses or via the bi-level sensitive monitoring/wake-up input as well as from the SPI command. Each wake-up source can be inhibited.

The device is designed to withstand the severe conditions of automotive applications.



PG-DSO-36-38

Type	Package	Marking
TLE8264E	PG-DSO-36-38	TLE8264E

## HS CAN Transceiver

- Compliant to ISO 11898-2 and 11898-5 as well as SAE J2284
- CAN data transmission rate up to 1 MBaud
- Supplied by dedicated input  $V_{ccHSCAN}$
- Low power mode management
- Bus wake-up capability via CAN message
- Excellent EMC performance (very high immunity and very low emission)
- Bus pins are short circuit proof to ground and battery voltage
- 8 kV ESD gun test on CANH / CANL / SPLIT
- Bus failure detection

## LIN Transceiver

- LIN2.1 conformance, LIN2.1 is back compatible to LIN1.3 and LIN2.0
- SAE J2602-2 conformance
- Compatible to ISO 9141 (K-L-Line)
- Transmission rate up to 20 kBaud, LIN Flash Mode 115kBaud
- 8 kV ESD gun test on Bus pins

## Voltage Regulators

- Low-dropout voltage regulator
- $V_{cc1\mu C}$ , 200 mA, 5 V  $\pm 2\%$  for external devices, such as microcontroller and RF receiver
- $V_{cc2}$ , 200 mA, 5 V  $\pm 2\%$  for external devices or the internal HS CAN cell
- $V_{cc3}$ , current limitation by shunt resistor (up to 400 mA with 220 m $\Omega$  shunt resistor), 5 V  $\pm 4\%$  with external PNP transistor; for example: to supply additional external CAN transceivers
- $V_{cc1\mu C}$ , undervoltage Time-out

## Supervision

- Reset output with integrated pull-up resistor
- Time-out or Window Watchdog, SPI configured
- Watchdog Timer from 16 ms to 1024 ms
- Check sum bit for Watchdog configuration
- Reset due to Watchdog failure can be inhibited with Test pin (SBC SW Development Mode)

## Interrupt Management

- Complete enabling / disabling of interrupt sources
- Timing filter mechanism to avoid multiple / infinite Interrupt signals

## Limp Home

- Open drain Limp Home outputs
- Dedicated internal logic supply
- Maximum safety architecture for Safety Operation Mode
- Configurable Fail-Safe behavior
- Dedicated side indicators signal 1.25Hz 50% duty cycle
- Dedicated PWM signal 100Hz 20% duty cycle



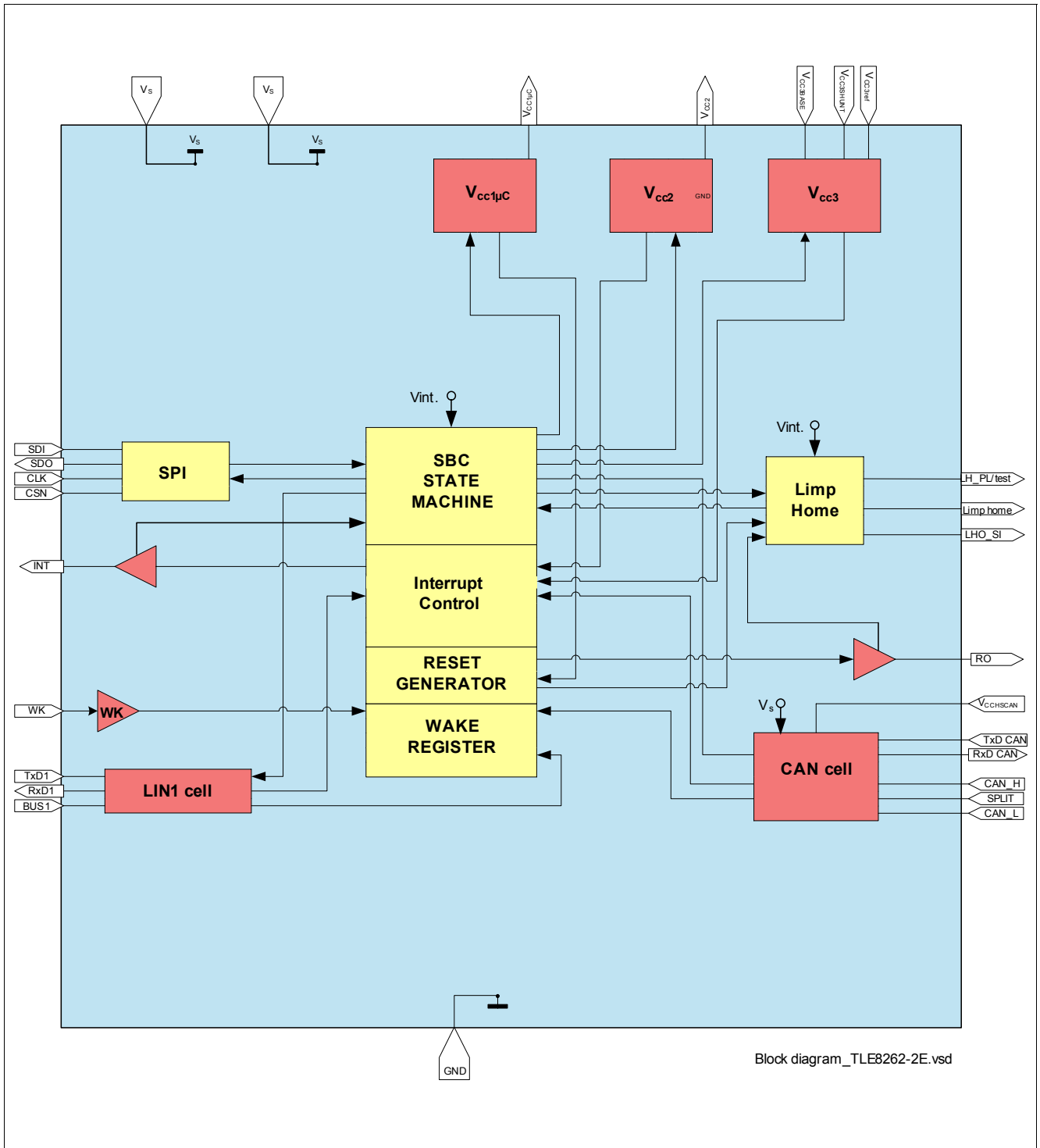


Figure 2 Simplified Block Diagram



### 3 Pin Configuration

#### 3.1 Pin Assignments

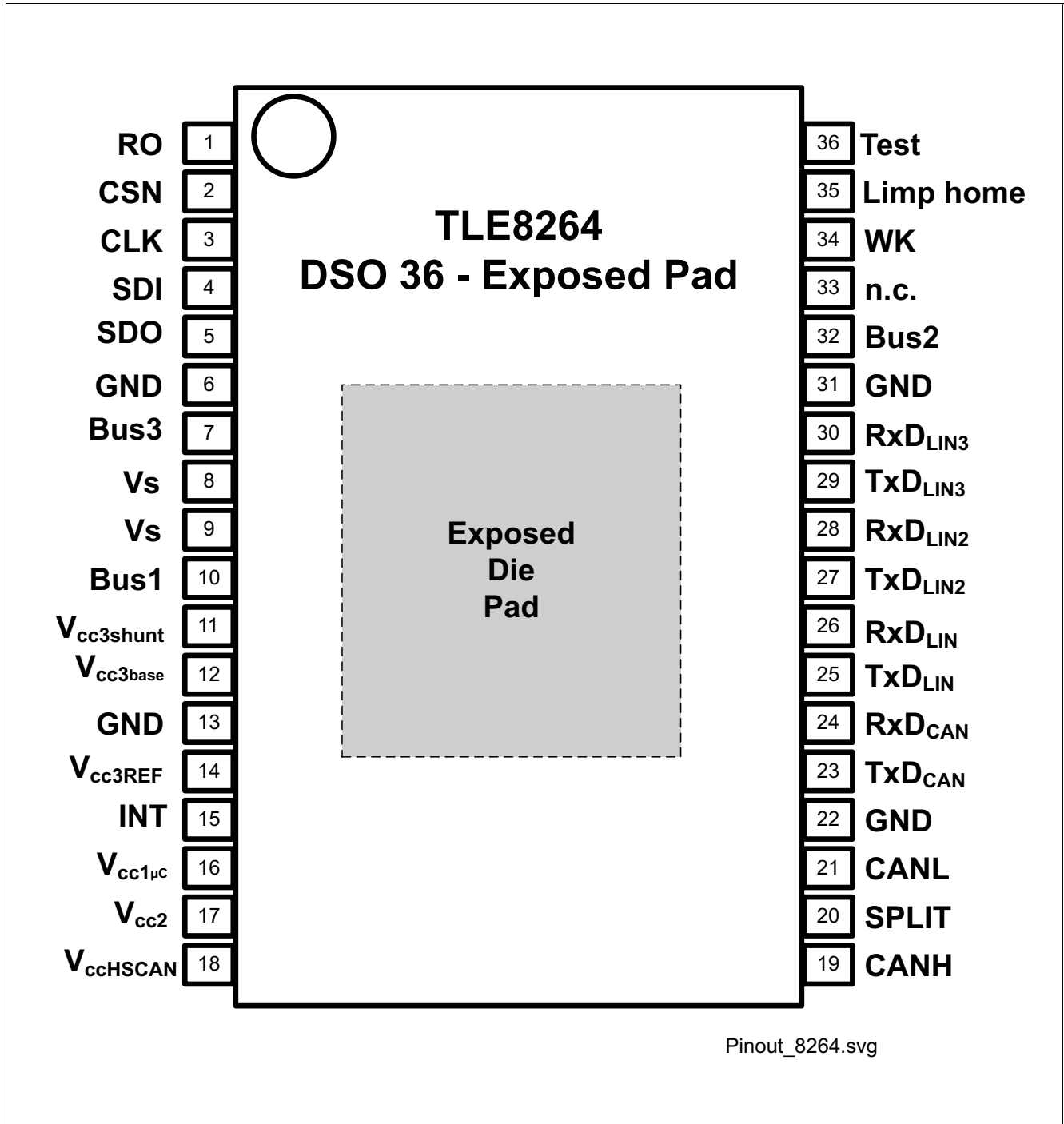


Figure 3 Pin Configuration

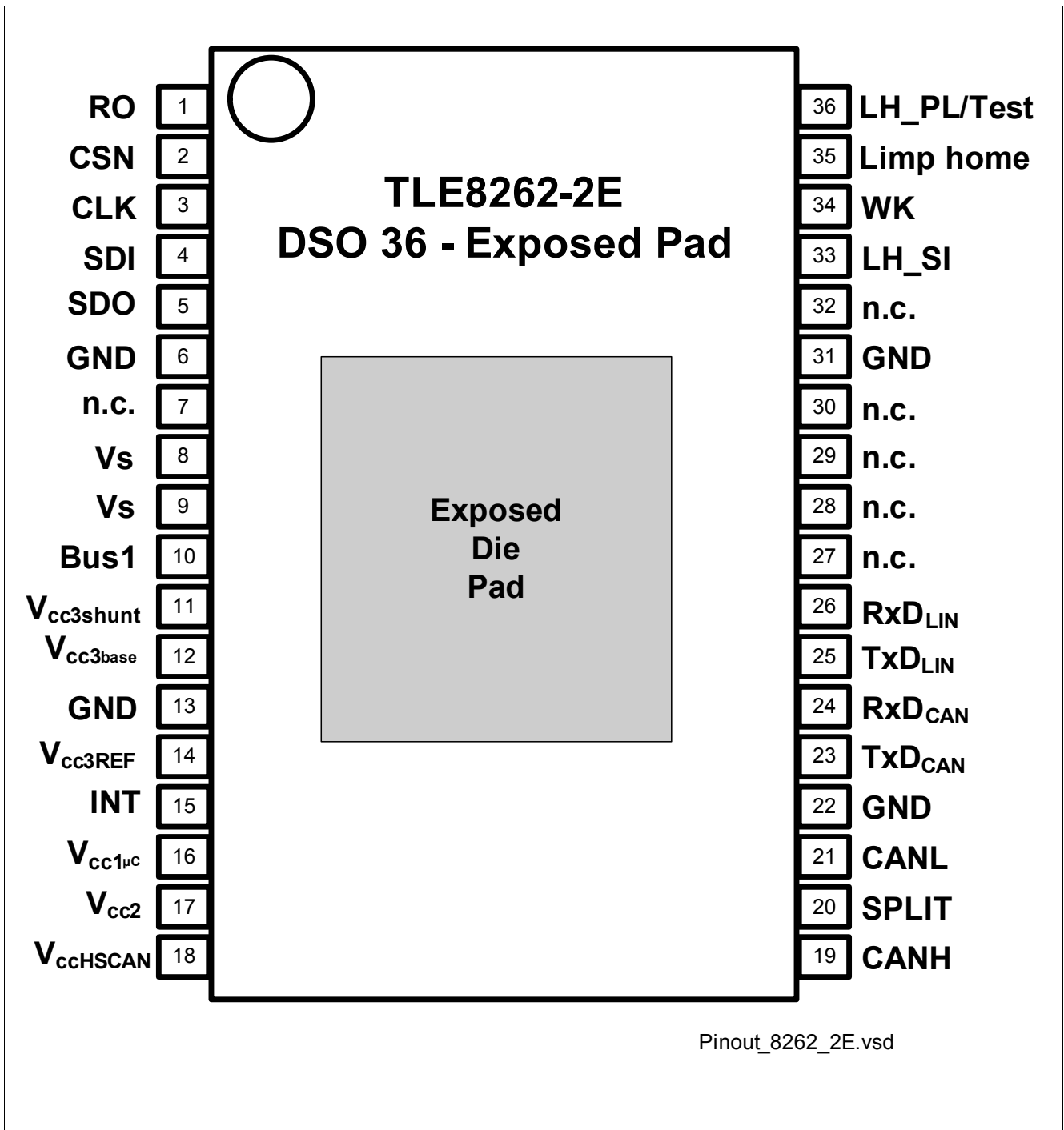


Figure 4 Pin Configuration

### 3.2 Pin Definitions and Functions

Pin	Symbol	Function
1	RO	<b>Reset Input/Output;</b> open drain output, integrated pull-up resistor; active low.
2	CSN	<b>SPI Chip Select Not Input;</b> CSN is an active low input; serial communication is enabled by pulling the CSN terminal low; CSN input should be set to low only when CLK is low; CSN has an internal pull-up resistor and requires CMOS logic level inputs.
3	CLK	<b>SPI Clock Input;</b> clock input for shift register; CLK has an internal pull-down resistor and requires CMOS logic level inputs.
4	SDI	<b>SPI Data Input;</b> receives serial data from the control device; serial data transmitted to SDI is a 16-bit control word with the Least Significant Bit (LSB) transferred first; the input has a pull-down resistor and requires CMOS logic level inputs; SDI will accept data on the falling edge of the CLK signal.
5	SDO	<b>SPI Data Output;</b> this tri-state output transfers diagnostic data to the control device; the output will remain tri-stated unless the device is selected by a low on Chip Select Not (CSN).
6	GND	<b>Ground</b>
7	Bus3	<b>LIN Bus 3;</b> Bus line for the LIN interface, according to ISO 9141 and LIN specification 2.1 as well as SAE J2602-2.
7	n.c.	<b>Not connected</b>
8	$V_s$	<b>Power Supply Input;</b> block to GND directly at the IC with ceramic capacitor. Ensure to have no current flow from PIN8 to PIN9. PIN8 and PIN9 can be directly connected.
9	$V_s$	<b>Power Supply Input;</b> block to GND directly at the IC with ceramic capacitor. Ensure to have no current flow from PIN8 to PIN9. PIN8 and PIN9 can be directly connected.
10	Bus1	<b>LIN Bus 1;</b> Bus line for the LIN interface, according to ISO. 9141 and LIN specification 2.1 as well as SAE J2602-2.
11	$V_{cc3\ shunt}$	<b>PNP Shunt;</b> External PNP emitter voltage.
12	$V_{cc3\ base}$	<b>PNP Base;</b> External PNP base voltage.
13	GND	<b>Ground</b>
14	$V_{cc3REF}$	External PNP Output Voltage
15	INT	<b>Interrupt Output, configuration Input;</b> used as wake-up flag from SBC Stop Mode and indicating failures. Active low. Integrated pull up. During start-up used to set the SBC configuration. External Pull-up sets config 1/3, no external Pull-up sets config 2/4.
16	$V_{cc1\ \mu c}$	<b>Voltage Regulator Output;</b> 5 V supply; to stabilize block to GND with an external capacitor.
17	$V_{cc2}$	<b>Voltage Regulator Output;</b> 5 V supply; to stabilize block to GND with an external capacitor.
18	$V_{ccHSCAN}$	<b>Supply Input;</b> for the internal HS CAN cell.
19	CANH	<b>CAN High Line;</b> High in dominant state.
20	SPLIT	<b>Termination Output;</b> to support recessive voltage level of the bus lines.
21	CANL	<b>CAN Low Line;</b> Low in dominant state.
22	GND	<b>Ground</b>
23	TxD <sub>CAN</sub>	<b>CAN Transmit Data Input;</b> integrated pull-up resistor.
24	RxD <sub>CAN</sub>	<b>CAN Receive Data Output</b>

**Pin Configuration**

Pin	Symbol	Function
25	TxD <sub>LIN</sub>	<b>LIN Transceiver Data input</b> ; according to ISO 9141 and LIN specification 2.1 as well as SAE J2602-2. integrated pull-up resistor.
26	RxD <sub>LIN</sub>	<b>LIN Transceiver Data Output</b> ; according to the ISO 9141 and LIN specification 2.1 as well as SAE J2602-2; push-pull output; LOW in dominant state.
27	TxD <sub>LIN2</sub>	<b>LIN Transceiver Data Input</b> ; according to ISO 9141 and LIN specification 2.1 as well as SAE J2602-2. integrated pull-up resistor.
28	RxD <sub>LIN2</sub>	<b>LIN Transceiver Data Output</b> ; according to the ISO 9141 and LIN specification 2.1 as well as SAE J2602-2; push-pull output; LOW in dominant state.
27	n.c.	<b>Not connected</b>
28	n.c.	<b>Not connected</b>
29	TxD <sub>LIN3</sub>	<b>LIN Transceiver Data Input</b> ; according to ISO 9141 and LIN specification 2.1 as well as SAE J2602-2. integrated pull-up resistor.
30	RxD <sub>LIN3</sub>	<b>LIN Transceiver Data Output</b> ; according to the ISO 9141 and LIN specification 2.1 as well as SAE J2602-2; push-pull output; LOW in dominant state.
29	n.c.	<b>Not connected</b>
30	n.c.	<b>Not connected</b>
31	GND	<b>Ground</b>
32	Bus2	<b>LIN Bus 2</b> ; Bus line for the LIN interface, according to ISO 9141 and LIN specification 2.1 as well as SAE J2602-2.
32	n.c.	<b>Not connected</b>
33	n.c.	<b>not connected</b>
33	LH_SI	<b>Limp Home side indicator</b> ; Side indicators 1.25Hz 50% duty cycle output; Open drain. Active LOW.
34	WK	<b>Monitoring / Wake-Up Input</b> ; bi-level sensitive input used to monitor signals coming from, for example, an external switch panel; also used as wake-up input;
35	Limp Home	<b>Fail-Safe Function Output</b> ; Open drain. Active LOW.
36	Test	<b>SBC SW Development Mode entry</b> ; Connect to GND for activation; Integrated pull-up resistor. Connect to $V_S$ or leave open for normal operation.
36	LH_PL/Test	<b>SBC SW Development Mode entry</b> ; Connect to GND for activation; Integrated pull-up resistor. Connect to $V_S$ or leave open for normal operation. <b>Limp Home Pulsed Light output</b> : Brake/rear light 100Hz 20% duty cycle output; Open drain. Active LOW.
EDP	-	<b>Exposed Die Pad</b> ; For cooling purposes only, do not use it as an electrical ground. <sup>1)</sup>

1) The exposed die pad at the bottom of the package allows better dissipation of heat from the SBC via the PCB. The exposed die pad is not connected to any active part of the IC and can be left floating or it can be connected to GND for the best EMC performance.

## 4 State Machine

### 4.1 Block Description

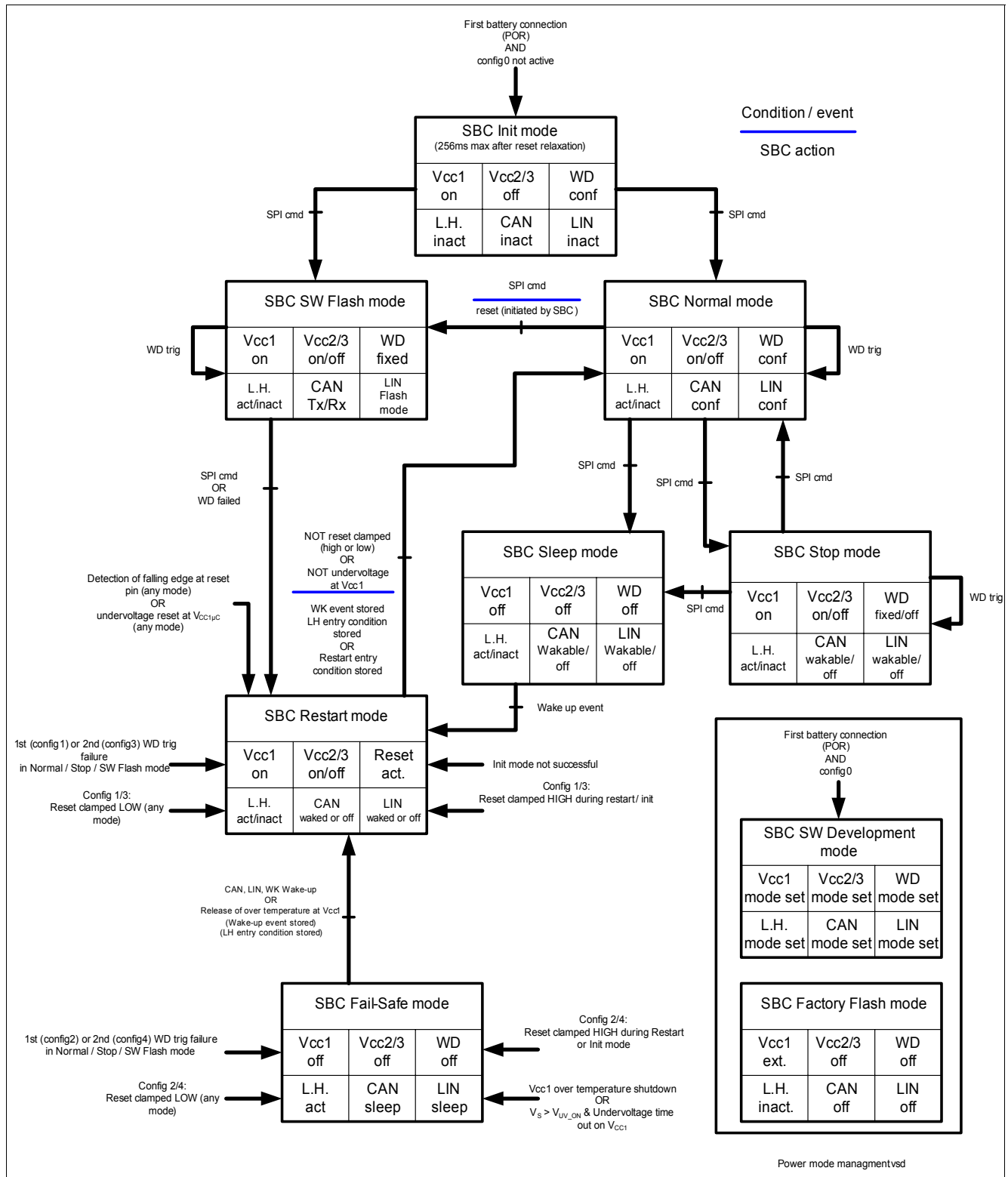


Figure 5 Power Mode Management

## 4.2 State Machine Description

The System Basis Chip (SBC) offers ten operating modes: Power On Reset, Init, Normal, Restart, Software Flash, Sleep, Stop, Fail-Safe, Software Development, and Factory Flash Mode. The modes are controlled with one test pin and via three mode select bits MS2..0, within the SPI. Additionally, the SBC allows five configurations, accessed via two external pins and one SPI bit.

### 4.2.1 Configuration Description

**Table 1** provides descriptions and conditions for entry to the different configurations of the SBC.

**Table 1 SBC Configuration**

Configuration	Description	Test pin	INT Pin	WD to LH bit
config 0	Software Development Mode	0V	n.a	n.a
config 1	After missing the WD trigger for the first time, the state of $V_{cc1\mu C}$ remain unchanged, LH pin is active, SBC in Restart Mode	Open / $V_S$	External pull-up	0
config 2	After missing the WD trigger for the first time, $V_{cc1\mu C}$ turns OFF, LH pin is active, SBC in Fail-Safe Mode		No ext. pull-up	0
config 3	After missing the WD trigger for the second time, the state of $V_{cc1\mu C}$ remain unchanged, LH pin is active, SBC in Restart Mode		External pull-up	1
config 4	After missing the WD trigger for the second time, $V_{cc1\mu C}$ turns OFF, LH pin is active, SBC in Fail-Safe Mode		No ext. pull-up	1

In SBC SW Development Mode, Config 1 to 4 are accessible.

### 4.2.2 SBC Power ON Reset (POR)

At  $V_S > V_{UVON}$ , the SBC starts to operate, by reading the test pin and then by turning ON  $V_{cc1\mu C}$ . When  $V_{cc1\mu C}$  reaches the reset threshold  $V_{RT1}$ , the reset output remains activated for  $t_{RD1}$  and the SBC enters then the Init Mode. In the event that  $V_S$  decreases below  $V_{UVOFF}$ , the device is completely disabled. For more details on the disable behavior of the SBC blocks, please refer to the chapter specific to each block.

### 4.2.3 SBC Init Mode

At entering the SBC Init Mode, the SBC starts to read the Test pin. The SBC starts-up in SBC Init Mode, and, after powering-up, waits for the microcontroller to finish its startup and initialization sequences.  $V_{cc2/3}$  are OFF and the Watchdog is configurable but not active. CAN and LIN modules are inactive and Limp Home output is inactive. From this transition mode, the SBC can be switched via SPI command to the desired operating mode, SBC Normal or Software Flash Mode. If the SBC does not receive any SPI command, or receive wrong SPI command (i.e. not send the device to SBC Normal or SBC SW Flash Mode) within a 256 ms time frame after the reset relaxation, it will enter into SBC Restart Mode and activate the Limp Home output.

*Note: In Init Mode it is recommended to send one SPI command that sets the device to Normal Mode, triggers the watchdog the first time and sets the required watchdog settings.*

#### 4.2.4 SBC Normal Mode

SBC Normal Mode is used to transmit and receive CAN and LIN messages. In this mode,  $V_{cc1\mu C}$  is always “ON”  $V_{cc2}$  and  $V_{cc3}$  can be turned-on or off by SPI command. In Normal Mode the watchdog needs to be triggered. It can be configured via SPI, window watchdog and time-out watchdog is possible (default value is time-out 256 ms). All the wake-up sources can be inhibited in this mode. The Limp Home output can be enabled or disabled via SPI command. Via SPI command, the SBC can enter Sleep, Stop or Software Flash Mode. A reset is triggered by the SBC when entering the Software Flash Mode. It is recommended to send at first SPI command the watchdog setting. Please refer to [Chapter 13.4](#).

#### 4.2.5 SBC Sleep Mode

During SBC Sleep Mode, the lowest power consumption is achieved by having the main and external voltage regulators switched-off. As the microcontroller is not supplied, the integrated Watchdog is disabled in Sleep Mode. The last Watchdog configuration is not stored. The CAN and LIN modules are in their respective Wake-capable or OFF modes and the Limp Home output is unchanged, as before entering the Sleep Mode. If a wake-up appears in this mode, the SBC goes into Restart Mode automatically. In Sleep Mode, not all wake-up sources should be inhibited, this is required to not program the device in a mode where it can not wake up. If all wake sources are inhibited when sending the SBC to Sleep Mode, the SBC does not go to Sleep Mode, the microcontroller is informed via the INT output, and the SPI bit “Fail SPI” is set. The first SPI output data when going to SBC Normal Mode will always indicate the wake up source, as well as the SBC Sleep Mode to indicate where the device comes from and why it left the state.

*Note: Do not change the transceiver settings in the same SPI command that sends the SBC to Sleep Mode.*

#### 4.2.6 SBC Stop Mode

The Stop Mode is used as low power mode where the  $\mu C$  is supplied. In this mode the voltage regulator  $V_{cc1\mu C}$  remains active. The other voltage regulator ( $V_{cc2/3}$ ) can be switched on or off.

The watchdog can be used or switched off. If the watchdog is used the settings made in Normal Mode are also valid in Stop Mode and can not be changed.

The CAN and LIN modules are not active. They can be selected to be off or used as wake-up source. If all wake up sources are disabled, (CAN, LIN, WK, cyclic wake) the watchdog can not be disabled, the SBC stays in Normal Mode and the watchdog continues with the old settings.

If a wake-up event occurs the INT pin is set to low. The  $\mu C$  can react on the interrupt and set the device into Normal Mode via SPI. There is no automatic transition to SBC Normal Mode.

There are 4 Options for SBC Stop Mode

- WD on (the watchdog needs to be served as in Normal Mode)
- WD off (special sequence required see [Chapter 11.2.4](#))
- Cyclic Wake up with acknowledge (interrupt is sent after set time and needs to be acknowledged by SPI read)
- Cyclic Wake-up, Watchdog off (interrupt is sent after set time)

#### Cyclic Wake-Up Feature

SBC Stop Mode supports the cyclic wake-up feature. By default, the function is OFF. It is possible to activate the cyclic wake-up via “Cyclic WK on/off” SPI bit. This feature is useful to monitor battery voltage, for example, during parking of the vehicle or for tracking RF data coming via the RF receiver. The Cyclic Wake-up feature sends an interrupt via the pin INT to the  $\mu C$  after the set time. The cyclic wake-up feature shares the same clock as the Watchdog. The time base set in the SPI for the Watchdog will be used for the cyclic wake-up. The timer has to be set before activating the function. With the cyclic wake-up feature the watchdog is not working as known from the other modes. In the case that both functions (Watchdog and cyclic wake-up) are selected, the cyclic wake-up is activated and each interrupt has to be acknowledged by reading the SPI Wake register before the next Cyclic Wake-Up comes. Otherwise, the SBC goes to SBC Restart Mode.

#### 4.2.7 SBC Software Flash Mode

SBC Software Flash Mode is similar to SBC Normal Mode regarding voltage regulators. In this mode, the Limp Home output can be set to active LOW via SPI and the communication on CAN and LIN modules is activated to receive flash data. In the LIN module the slope control mechanism is switched off. The Watchdog configuration is fixed to the settings used before entering the SBC SW Flash Mode. When the device comes from SBC Normal Mode, a reset is generated at the transition.

From the SBC Software Flash Mode, the SBC goes into SBC Restart Mode, the config setting has no influence on the behavior. A mode change to SBC Restart Mode can be caused by a SPI command, a time-out or Window Watchdog failure or an undervoltage reset. When leaving the SBC Software Flash Mode a reset is generated.

#### 4.2.8 SBC Restart Mode

There are multiple reasons to enter the SBC Restart Mode and multiple SBC behaviors described in [Table 2](#).

In any case, the purpose of the SBC Restart Mode is to reset the microcontroller.

- From SBC SW Flash Mode, it is used to start the new downloaded code.
- From SBC Normal, SBC Stop Mode and SBC SW Flash Mode it is reached in case of undervoltage on  $V_{cc1\mu C}$ , or due to incorrect Watchdog triggering.
- From SBC Sleep Mode it is used to ramp up  $V_{cc1\mu C}$  after wake
- From SBC Init Mode, it is used to avoid the system to remain undefined.
- From SBC Fail-safe Mode it is used to ramp up  $V_{cc1\mu C}$  after wake or cool down of  $V_{cc1\mu C}$ .

From SBC Restart Mode, the SBC goes automatically to SBC Normal Mode. The delay time  $t_{RDx}$  is programmable by the "Reset delay" SPI bit. The Reset output (RO) is released at the transition. SBC Restart Mode is left automatically by the SBC without any microcontroller influence. The first SPI output data will provide information about the reason for entering Restart Mode. The reason for entering Restart Mode is stored and kept until the microcontroller reads the corresponding "LH0..2" or "RM0..1" SPI bits. In case of a wake up from Sleep Mode the wake source is seen at the interrupt bits (Configuration select 000), an interrupt is not generated.

Entering or leaving the SBC Restart Mode will not result in deactivation of the Limp Home output (if activated).

The first SPI output data when going to SBC Normal Mode will always indicate the reason for the SBC Restart event.



**Table 2 SBC Restart Mode Entry Reasons and Actions**

SBC Mode and Configuration		Entering reason	Actions			
Mode	Config		LH output	$V_{cc1\mu C}$	RO	SPI Out Bits
Init Mode	n.a	Init Mode time-out	ON	remains ON	LOW	LH 0..2
	n.a.	Reset low from outside	Unchanged	remains ON	LOW	RM 0..1
	config 1/3	Reset clamped	ON	remains ON	LOW	LH 0..2
Normal <sup>1)</sup>	n.a	undervoltage reset	unchanged	ramping up	LOW	RM 0..1
	config 1	WD trigger failure	ON	remains ON	LOW	LH 0..2
	config 3		OFF after 1st ON after 2nd			RM 0..1 after 1st LH 0..2 after 2nd
	config 4		OFF after 1st			RM 0..1 after 1st <sup>2)</sup>
	n.a.	Reset low from outside	Unchanged	remains ON	LOW	RM 0..1
	config 1/3	Reset clamped	ON	remains ON	LOW	LH 0..2
Software Flash	n.a	undervoltage reset	unchanged	remains ON	LOW	RM 0..1
	n.a	SPI cmd	unchanged	remains ON	LOW	RM 0..1
	n.a	WD trigger failure	unchanged	remains ON	LOW	RM 0..1
	n.a.	Reset low from outside	Unchanged	remains ON	LOW	RM 0..1
	config 1/3	Reset clamped	ON	remains ON	LOW	LH 0..2
Sleep	n.a	Wake-up event	unchanged	ramping up	LOW	WK bits register
Stop <sup>1)</sup>	n.a	undervoltage reset	unchanged	ramping up	LOW	RM 0..1
	config 1	WD trigger failure	ON	remains ON	LOW	LH 0..2
	config 3		OFF after 1st ON after 2nd			RM 0..1 after 1st LH 0..2 after 2nd
	config 4		OFF after 1st			RM 0..1 after 1st <sup>2)</sup>
	n.a.	Reset low from outside	Unchanged	remains ON	LOW	RM 0..1
	config 1/3	Reset clamped	ON	remains ON	LOW	LH 0..2
Fail-Safe	n.a.	Wake-up event	ON	ramping up	LOW	LH 0..2
Software Development Mode	n.a	undervoltage reset	unchanged	ramping up	LOW	RM 0..1
	n.a.	Reset low from outside	Unchanged	remains ON	LOW	RM 0..1
	config 1/3	Reset clamped	ON	remains ON	LOW	LH 0..2

1) Config 2 will never enter Restart Mode in case of WD failure but directly Fail-Safe Mode

2) Goes to Fail-Safe Mode after the second consecutive failure

#### 4.2.9 SBC Fail-Safe Mode

In SBC Fail-Safe Mode, all voltage regulators are OFF and the transceivers are in Wake-Capable Mode. The Limp Home output is active.

Conditions to enter the SBC Fail-Safe Mode are:

- Watchdog trigger failure in configuration 2 or 4
- $V_{CC1\mu C}$  undervoltage time-out in any configuration if  $V_S$  is above  $V_{LHUV}$  range.
- Temperature shutdown of  $V_{CC1\mu C}$  in any configuration.
- Reset clamped in Config. 2/4

In case of  $V_{CC1\mu C}$  overtemperature shutdown, the SBC will latch and wait to cool down below the thermal hysteresis, and will go back to SBC Restart Mode.

In case of a wake-up event, the SBC will go to SBC Restart Mode (not in case of  $V_{CC1\mu C}$  overtemperature shutdown), storing the wake-up event and resetting the Watchdog trigger failure counter. The first SPI output data when going to SBC Normal Mode will always indicate the reason for the SBC Fail-Safe Mode.

#### 4.2.10 SBC Software Development Mode

If the Test pin is connected to GND (Config 0 active) during powering-up, the SBC enters SBC Software Development Mode. SBC Software Development Mode is a super set of the other modes so it is possible to use all the modes of the SBC with the following difference. In SBC Software Development Mode, no reset is generated and  $V_{CC1\mu C}$  is not switched off due to Watchdog trigger failure. If a Watchdog trigger failure occurs, it will be indicated by the INT output (reset bit). The SBC Fail-Safe Mode or SBC Restart Mode are not reached in case of wrong Watchdog trigger but the other reasons to enter these modes are still valid.

#### 4.2.11 SBC Factory Flash Mode

In this mode, the SBC is completely powered OFF and the microcontroller is supplied externally. The mode is detected when  $V_{CC1\mu C}$  is powered from external and the voltage on  $V_S$  is not powered from external. The current flow out of  $V_S$  must be limited to the maximum rating. The external supply voltage should be below the absolute maximum rating stated in [Chapter 5.1](#). The reset can be driven by an external circuit, or pulled high with a pull-up resistor.

*Note: Please respect the absolute maximum ratings when the device is in SBC Factory Flash Mode.*

## 5 General Product Characteristics

### 5.1 Absolute Maximum Ratings

#### Absolute Maximum Ratings <sup>1)</sup>

$T_j = -40\text{ °C}$  to  $+150\text{ °C}$ ; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Test Conditions
			Min.	Max.		
<b>Voltages</b>						
5.1.1	Supply Voltage	$V_S$	-0.3	40	V	–
5.1.2	Supply Voltage Slew Rate	$dV_{S/dt}$	-0.5	5	V/ $\mu$ s	–
5.1.3	Regulator Output Voltage	$V_{cc1\mu C/2/3}$	-0.3	5.5	V	–
5.1.4	CAN Bus Voltage (CANH, CANL)	$V_{CANH/L}$	-27	40	V	–
5.1.5	Differential Voltage CANH, CANL, SPLIT	$V_{diffESD}$	-40	40	V	CANH-CANL <  40 V ; CANH-SPLIT <  40 V  CANL-SPLIT <  40 V ;
5.1.6	Input Voltage at $V_{CCHSCAN}$	$V_{CCHSCAN}$	-0.3	5.5	V	–
5.1.7	Voltage at SPLIT, WK	$V_{SPLIT}$	-27	40	V	–
5.1.8	Voltage at LH_PL/Test	$V_{Test,max}$	-0.3	40	V	–
5.1.9	Voltage at $V_{cc3base}$ , $V_{cc3shunt}$ , $V_{cc3REF}$	$V_{cc3base}$	-0.3	40	V	–
5.1.10	Voltage at Limp Home (LH, LH_SI pin)	$V_{LH}$	-0.3	40	V	–
5.1.11	Logic Voltages Input Pin (SDI, CLK, CSN, TxDLINx, TxDCAN)	$V_I$	-0.3	$V_{CC1\mu C} + 0.3V$	V	$0\text{ V} < V_S < 28\text{ V}$ $0\text{ V} < V_{CC1\mu C} < 5.5\text{ V}$
5.1.12	Logic Voltage Output PIN (SDO, RO, INT, RxDLINx, RxDCAN)	$V_{DRI, RD}$	-0.3	$V_{CC1\mu C} + 0.3V$	V	$0\text{ V} < V_S < 28\text{ V}$ $0\text{ V} < V_{CC1\mu C} < 5.5\text{ V}$
5.1.13	LIN Line Bus Input Voltages	$V_{bus}$	-27	40	V	–
<b>Currents</b>						
5.1.14	Reverse current on pin Vs	$I_{VS}$	-500	–	mA	$V_S < V_{CC}$
<b>Temperatures</b>						
5.1.15	Junction Temperature	$T_j$	-40	150	°C	–
5.1.16	Storage Temperature	$T_{stg}$	-55	150	°C	–
<b>ESD Susceptibility</b>						
5.1.17	Electrostatic Discharge Voltage at BusX, CANH, CANL, SPLIT versus GND	$V_{ESD}$	-6	6	kV	<sup>2)</sup> HBM (100 pF via 1.5 k $\Omega$ )
5.1.18	Electrostatic Discharge Voltage	$V_{ESD}$	-2	2	kV	<sup>2)</sup> HBM (100 pF via 1.5 k $\Omega$ )
5.1.19	Electrostatic Discharge CDM Corner Pins (Pin 1, 18, 19, 36)	$V_{ESD\_CDM\_C}$	-750	750	V	<sup>3)</sup>
	Electrostatic Discharge CDM	$V_{ESD\_CDM}$	-500	500	V	<sup>3)</sup>

1) Not subject to production test; specified by design

2) ESD susceptibility Human Body Model "HBM" according to JESD22-A114

3) ESD susceptibility Charged Device Model "CDM" according to ESDA STM5.3.1

**General Product Characteristics**

*Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

*Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.*

**5.2 Functional Range**

Pos.	Parameter	Symbol	Limit Values		Unit	Test Conditions
			Min.	Max.		
5.2.1	Supply Voltage	$V_S$	$V_{UV\ OFF}$	28	V	After $V_S$ rising above $V_{UV\ ON}$ , <sup>1)</sup>
5.2.2	Supply Voltage	$V_S$	$V_{UV\ OFF}$	40	V	<sup>2)</sup> $t_{pulse} = 400\ ms$ 40 V load dump; $R_i = 2\ \Omega$
5.2.3	SPI Clock Frequency	$f_{clkSPI}$	–	4	MHz	<sup>3)</sup> $V_S > 5.5\ V$
5.2.4	SPI Clock Frequency	$f_{clkSPI}$	–	1	MHz	If $V_{UV\ ON} > V_S > V_{UV\ OFF}$ ;
5.2.5	Junction Temperature	$T_j$	-40	150	°C	–
5.2.6	Undervoltage “OFF”	$V_{UV\ OFF}$	3	4	V	- <sup>1)</sup>
5.2.7	Undervoltage “ON	$V_{UV\ ON}$	4.5	5.5	V	- <sup>1)</sup>
5.2.8	Supply Voltage for Limp Home Output Active	$V_{S\_LH}$	5.5	40	V	Pull up to $V_S$ $R_{LHO} = 40k\ \Omega$

1) In the case  $V_s < V_{UV\ OFF}$ , the SBC is switched OFF and will restart in INIT Mode at next  $V_s$  rising.

2) During load dump, the others pins remains in their absolute maximum ratings

3) Not subject to production test, specified by design

*Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.*

**5.3 Thermal Characteristics**

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
5.3.1	Junction Ambient	$R_{thJA\_1L}$	–	40		K/W	<sup>1) 3)</sup> 300 mm <sup>2</sup> cooling area
	Junction Ambient	$R_{thJA\_4L}$	–	25		K/W	<sup>2) 3)</sup> 2s2p + 600 mm <sup>2</sup> cooling area
5.3.2	Junction to Soldering Point	$R_{thJSP}$	–	5	–	K/W	<sup>3)</sup>
<b>Thermal Prewarning and Shutdown Junction Temperatures;</b>							
5.3.3	$V_{CC1\mu C}$ , Thermal Pre-warning ON Temperature	$T_{jPW}$	120	145	170	°C	<sup>3)</sup>
5.3.4	$V_{CC1\mu C}$ , Thermal Prewarning Hysteresis	$\Delta T_{PW}$	–	25	–	K	<sup>3)</sup>
5.3.5	$V_{CC1\mu C}$ , $V_{CC2}$ Thermal Shutdown Temperature	$T_{jSDVcc}$	150	185	200	°C	<sup>3)</sup>
5.3.6	$V_{CC1\mu C}$ , $V_{CC2}$ Thermal Shutdown Hysteresis	$\Delta T_{SDVcc}$	–	35	–	K	<sup>3)</sup>
5.3.7	$V_{CC1\mu C}$ , Ratio of SD to PW Temperature	$\frac{T_{jSDVcc}}{T_{jPW}}$	–	1.20	–	–	<sup>3)</sup>
5.3.8	CAN Transmitter Thermal Shutdown Temperature	$T_{jSDCAN}$	150	–	200	°C	<sup>3)</sup>
5.3.9	CAN Transmitter Thermal Shutdown Hysteresis	$\Delta T_{CAN}$	–	10	–	K	<sup>3)</sup>
5.3.10	LIN Transmitter Thermal Shutdown Temperature	$T_{jSDLIN}$	150	–	200	°C	<sup>3)</sup>
5.3.11	LIN Transmitter Thermal Shutdown Hysteresis	$\Delta T_{LIN}$	–	10	–	K	<sup>3)</sup>

1) Specified Rthja value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 single layer. The product (chip + package) was simulated on a 76.4 x 114.3 x 1.5 mm board.

2) According to Jedec JESD51-2,-5,-7 at natural convection on 2s2p board for 2W. Board: 76.2x114.3x1.5mm<sup>3</sup> with 2 inner copper layers (35µm thick)., with thermal via array under the exposed pad contacted the first inner copper layer and 600mm<sup>2</sup> cooling are on the top layer (70µm)

3) Not subject to production test; specified by design;

### 5.4 Current Consumption

$V_s = 5.5\text{ V to }28\text{ V}$ ; all outputs open; Without  $V_{CC3}$ ;  $T_j = -40\text{ °C to }+150\text{ °C}$ ; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Pos.	Parameter	Symbol	Limit Values			Unit	Test Condition
			Min.	Typ.	Max.		
<b>Normal Mode;</b>							
5.4.1	Current Consumption for Internal Logic	$I_{VS\_logic}$	–	–	2	mA	SBC Normal Mode $I_{CC1\mu C} = I_{CC2} = 0\text{ mA}$ ; CAN OFF mode; LIN OFF mode
5.4.2	Additional current Consumption for CAN Cell	$I_{VS\_CAN}$	–	–	10	mA	CAN Normal Mode; Recessive state; $V_{CC2}$ connected to $V_{CCHSCAN}$ $V_{TXD} = V_{cc1\mu C}$ ; without $R_L$
			–	–	12	mA	CAN Normal Mode; dominant state; $V_{CC2}$ connected to $V_{CCHSCAN}$ $V_{TXD} = \text{low}$ ; without $R_L$ ;
5.4.3	Additional Current Consumption per LIN Cell	$I_{VS\_LIN}$	–	–	3.0	mA	LIN Normal Mode; recessive state; without $R_L$ ; $V_{TXD} = V_{cc1\mu C}$
			–	–	5.0	mA	LIN Normal Mode; dominant state; without $R_L$ ; $V_{TXD} = \text{low}$
<b>Stop Mode</b>							
5.4.4	Current Consumption	$I_{VS}$	–	58	75	$\mu\text{A}$	SBC Stop Mode; $V_s = 13.5\text{ V}$ ; $V_{CC1\mu C}$ "ON"; $V_{CC2/3}$ "OFF" CAN/LIN wake capable; $T_j = 25\text{ °C}$
				65	85		
			–	70	90	$\mu\text{A}$	SBC Stop Mode; $V_s = 13.5\text{ V}$ ; $V_{CC1\mu C/2}$ "ON"; $V_{CC3}$ "OFF" CAN/LIN wake capable; $T_j = 25\text{ °C}$
				78	100		

### 5.4 Current Consumption (cont'd)

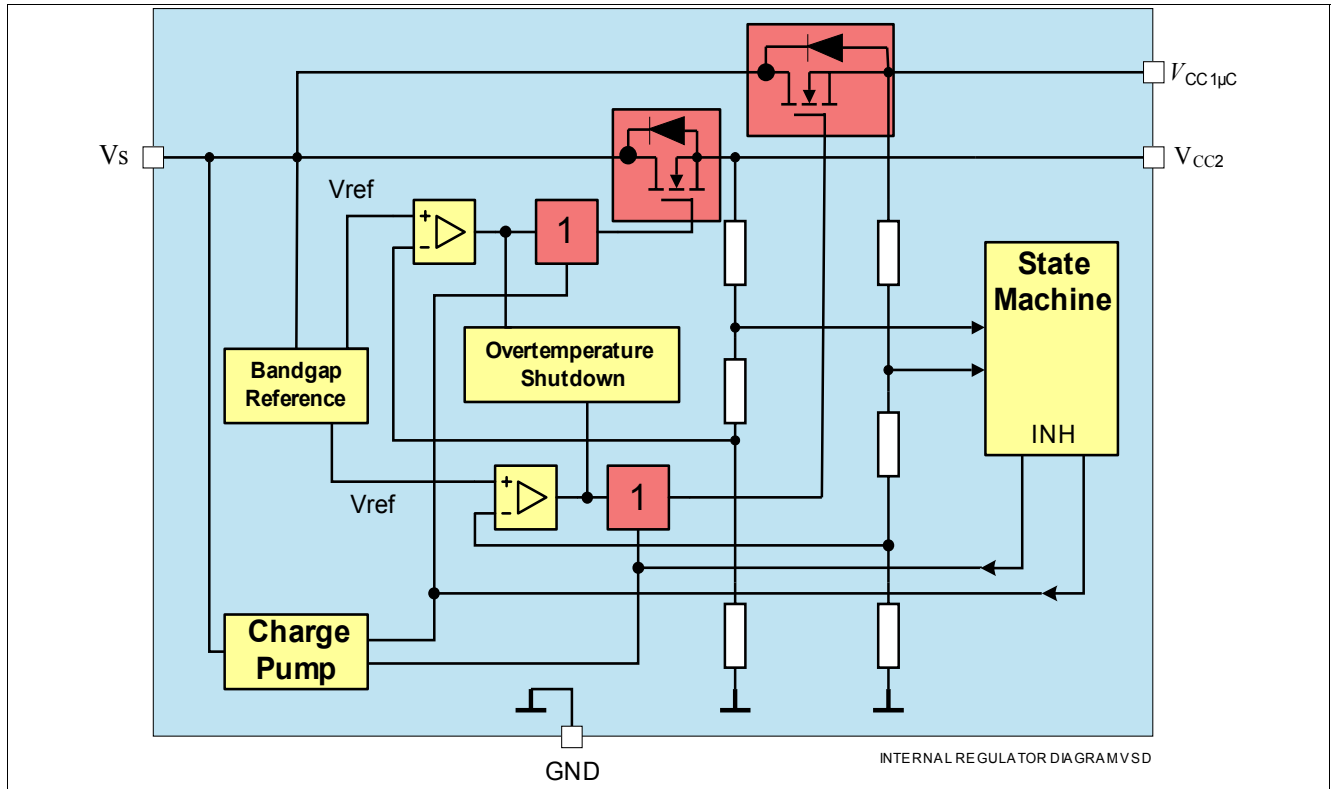
$V_S = 5.5\text{ V to }28\text{ V}$ ; all outputs open; Without  $V_{CC3}$ ;  $T_j = -40\text{ °C to }+150\text{ °C}$ ; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Pos.	Parameter	Symbol	Limit Values			Unit	Test Condition
			Min.	Typ.	Max.		
<b>Sleep Mode</b>							
5.4.5	Current consumption, all Wake Up Sources available.	$I_{VS\_sleep\_SBC}$	–	28	40	μA	SBC Sleep Mode; $T_j = 25\text{ °C}$ $V_S = 13.5\text{ V}$ ; $V_{CC1\mu C/2/3}$ "OFF" CAN/LIN wake capable; $T_j = 85\text{ °C}^{1)}$
				32	50		
5.4.6	Quiescent Current Reduction when one Wake Capable LIN Cell Disabled	$I_{VS\_sleep\_LIN}$	0.5	1	–	μA	<sup>1)</sup> SBC Sleep Mode; $T_j = 25\text{ °C}$ ; $V_S = 13.5\text{ V}$ ; $V_{CC1\mu C/2/3}$ "OFF" CAN/LIN 1_2 wake capable; LIN3 OFF
5.4.7	Quiescent Current Reduction when Wake Capable CAN Cell Disabled	$I_{VS\_sleep\_CAN}$	5	12	–		

1) Not subject to production test; specified by design

## 6 Internal Voltage Regulator

### 6.1 Block Description



**Figure 6 Functional Block Diagram**

The internal voltage regulators are dual low-drop voltage regulators that can supply loads up to  $I_{CC1\mu C/2\_max}$ . An input voltage up to  $V_{S\_MAX}$  is regulated to  $V_{cc1\mu C/2\_nom} = 5.0\text{ V}$  with a precision of  $\pm 2\%$ . Due to its integrated reset circuitry, featuring two SPI configurable power-on timing ( $t_{RDx}$ ) and three SPI configurable output voltages ( $V_{RTx}$ ) monitoring, the device is well suited for microcontroller supply. The design enables stable operation even with ceramic output capacitors down to 470nF, with  $ESR < 1\ \Omega @ f = 10\text{ kHz}$ . The device is designed for automotive applications, therefore it is protected against overload, short circuit, and overtemperature conditions. **Figure 6** shows the functional block diagram. If the  $V_S$  voltage is lower than  $V_{UV\_OFF}$ , the DMOS of the voltage regulator is switched to high impedance. The body diodes of the DMOS might go into conduction when  $V_{CC1\mu C}$  or  $V_{CC2} > V_S$  (no reverse protection).

### 6.2 Internal Voltage Regulator Modes

It is possible to turn  $V_{cc1\mu C}$  via SBC Modes and  $V_{cc2}$  activity ON or OFF via SPI command or by entering SBC modes. The limiting current for the both regulators is  $I_{CC1\mu C\_max}/I_{CC2}$ .

### 6.3 Internal Voltage Regulator Modes with SBC Mode

Depending on the SBC Mode in use,  $V_{cc1\mu C}$  and  $V_{cc2}$  can be either ON or OFF by definition,  $V_{cc2}$  can be also turned ON or OFF, via SPI. **Table 3** identifies the possible states of the voltage regulators, based on the various SBC modes.



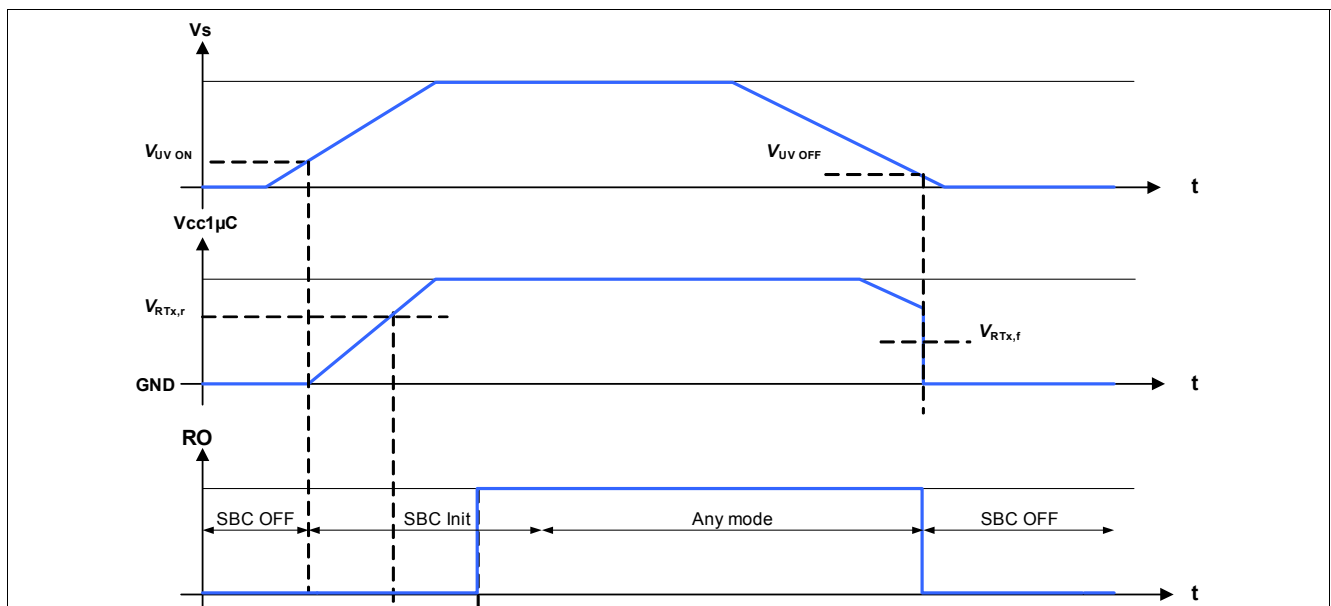
**Table 3 Internal Voltage Regulators States**

SBC Mode	Vcc1 $\mu$ C	Vcc2	
INIT Mode	ON	OFF	
Normal Mode	ON	ON	OFF
Sleep Mode	OFF	OFF	
Restart Mode	ON	unchanged	
Software Flash Mode	ON	ON	OFF
Stop Mode	ON	ON	OFF
Fail-Safe Mode	OFF	OFF	

## 6.4 Application information

### 6.4.1 Timing Diagram

**Figure 7** shows the ramp up and down of the  $V_S$ , and the dependency of  $V_{cc1\mu C}$ . At the first ramp up from SBC Init Mode, the reset threshold  $V_{RT}$  and time  $t_{RO}$  are set to the default value. See [Chapter 11.1](#)



**Figure 7 Ramp up / Down of Main Voltage Regulator**

An undervoltage time-out on  $V_{cc1\mu C}$  is implemented. Refer to [Chapter 13](#) for more information on this function.

### 6.4.2 Under voltage detection at $V_{cc2}$

The  $V_{cc2}$  voltage regulator integrates an under voltage detection. When  $V_{cc2}$  voltage goes below  $V_{UV\_VCC2}$ , the failure is indicated by an interrupt and the failure is reported into the diagnosis frame of the SPI.

## 6.5 Electrical Characteristics

$V_S = 5.5 \text{ V to } 28 \text{ V}$ ;  $C_{CC1\mu C} = C_{CC2} = 470 \text{ nF}$ ; all outputs open; SBC Normal Mode;

$T_j = -40 \text{ }^\circ\text{C to } +150 \text{ }^\circ\text{C}$ ; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Pos.	Parameter	Symbol	Limit Values			Unit	Test Condition
			Min.	Typ.	Max.		
<b>Voltage Regulator; Pin <math>V_{cc1\mu C}</math></b>							
6.5.1	Output Voltage	$V_{CC1\mu C}$	4.9	5.0	5.1	V	$0 \text{ mA} < I_{CC1\mu C} < 200 \text{ mA}$ ; $5.5 \text{ V} < V_S < 28 \text{ V}$ ;
6.5.2	Line Regulation	$\Delta V_{CC1\mu C, Li}$	–	–	20	mV	$6 \text{ V} < V_S < 16 \text{ V}$ ; $I_{CC1\mu C} = 0 \text{ A}$
6.5.3	Load Regulation	$\Delta V_{CC1\mu C, Lo}$	–	–	50	mV	$5 \text{ mA} < I_{CC1\mu C} < 200 \text{ mA}$ ; $V_S = 6 \text{ V}$
6.5.4	Power Supply Ripple Rejection	PSRR	–	40	–	dB	$V_r = 1 \text{ Vpp}$ ; $f_r = 100 \text{ Hz}$ ; <sup>1)</sup>
6.5.5	Output Current Limit	$I_{cc1\mu C \text{ max}}$	200	–	500	mA	$V_{cc1\mu C} = 4.5 \text{ V}$ ; power transistor thermally monitored;
6.5.6	Drop Voltage	$V_{DR \text{ } V_{cc1\mu C}}$	–	–	0.5	V	$I_{CC1\mu C} = 150 \text{ mA}$ ; <sup>2)</sup>
<b>Voltage Regulator; Pin <math>V_{cc2}</math></b>							
6.5.7	Output Voltage	$V_{CC2}$	4.9	5.0	5.1	V	$0 < I_{CC2} < 200 \text{ mA}$ ; $5.5 \text{ V} < V_S < 28 \text{ V}$ ;
6.5.8	Line Regulation	$\Delta V_{CC2, Li}$	–	–	20	mV	$6 \text{ V} < V_S < 16 \text{ V}$ ; $I_{CC2} = 0 \text{ A}$ ;
6.5.9	Load Regulation	$\Delta V_{CC2, Lo}$	–	–	50	mV	$5 \text{ mA} < I_{CC2} < 200 \text{ mA}$ ; $V_S = 6 \text{ V}$
6.5.10	Power Supply Ripple Rejection	PSRR	–	40	–	dB	$V_r = 1 \text{ Vpp}$ ; $f_r = 100 \text{ Hz}$ ; <sup>1)</sup>
6.5.11	Output Current Limit	$I_{cc2}$	200	–	500	mA	$V_{cc2} = 4.5 \text{ V}$ ; power transistor thermally monitored;
6.5.12	Drop Voltage	$V_{DR \text{ } V_{cc2}}$	–	–	0.5	V	$I_{CC2} = 150 \text{ mA}$ ; <sup>2)</sup>
6.5.13	Under voltage detection on $V_{cc2}$	$V_{UV \text{ } V_{CC2}}$	4.5	4.65	4.8	V	$V_{CC2}$ falls until INT = LOW

1) specified by design; not subject to production test.

2) Measured when the output voltage has dropped 100 mV from the nominal Value obtained at  $V_S = 13.5 \text{ V}$ . Specified drop voltage for  $V_S > 4 \text{ V}$ .