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TLE8888-1QK

Engine Machine System IC

AEC Qualified RoHS

1 Overview

Quality Requirement Category: Automotive

Features

- Voltage pre-regulator
- Integrated 5 V regulator
- 2 integrated 5 V trackers
- Standby regulator
- Separate internal supply
- Voltage monitoring
- High speed CAN interface with wake-up by bus
- LIN interface with high speed mode for K-Line operation
- Variable reluctance sensor interface
- Microsecond Channel interface (MSC) with low voltage differential signal (LVDS) inputs pads for low EME
- SPI and direct control inputs for high flexibility
- Main relay driver
- Ignition Key detection with key off delay output
- Wake-up input
- Engine off timer
- 4 low-side power stages especially to drive injectors (R_{on} = 550 mΩ) with enable input
- 3 low-side power stages (R_{on} = 350 mΩ)
- 6 push pull stages for driving on-board MOSFET with drain feedback
- 7 low-side power stages especially to drive relays (R_{on} = 1.5 Ω), one with delayed switch off functionality
- 4 half bridge stages for high flexibility, one with delayed switch off functionality
- 4 push pull stages for driving on- and off- board IGBT with back supply suppression and high voltage capability
- Open-load, short-to-GND and short-to-BAT diagnostic
- Overtemperature and short-to-BAT protection
- Monitoring watchdog module
- AEC Qualified

Overview

Description

The TLE8888-1QK is a U-Chip suitable for automotive engine management systems. It contains the basic functionality to supply the microcontroller and the ECU, establish the communication on- and off- board and drive EMS typical actuators. Furthermore it controls the main relay driver.

Type	Package	Marking
TLE8888-1QK	LQFP-100	TLE8888-1QK
TLE8888QK	LQFP-100	TLE8888QK
TLE8888-2QK	LQFP-100	TLE8888-2QK

Device Variants TLE8888QK and TLE8888-2QK

The device variants TLE8888QK and TLE8888-2QK differ from the main version TLE8888-1QK in the watchdog functionality.

The TLE8888QK has a fixed set of parameter for the watchdog (see datasheet addendum “TLE8888QK - Addendum”).

For the TLE8888-2QK the watchdog function is disabled (see datasheet addendum “TLE8888-2QK - Addendum”).

Only the main version TLE8888-1QK is described in this datasheet.

For order conditions please contact the nearest Infineon Technologies office.

Abbreviations

Symbol	Explanation
MSC	Microsecond channel
SPI	Serial peripheral interface
LVDS	Low voltage differential signal
EME	Electromagnetic emission
EMI	Electromagnetic interference
LIN	Local interconnect network
HS CAN	High speed controller area network

Table of Contents

2 Block Diagram

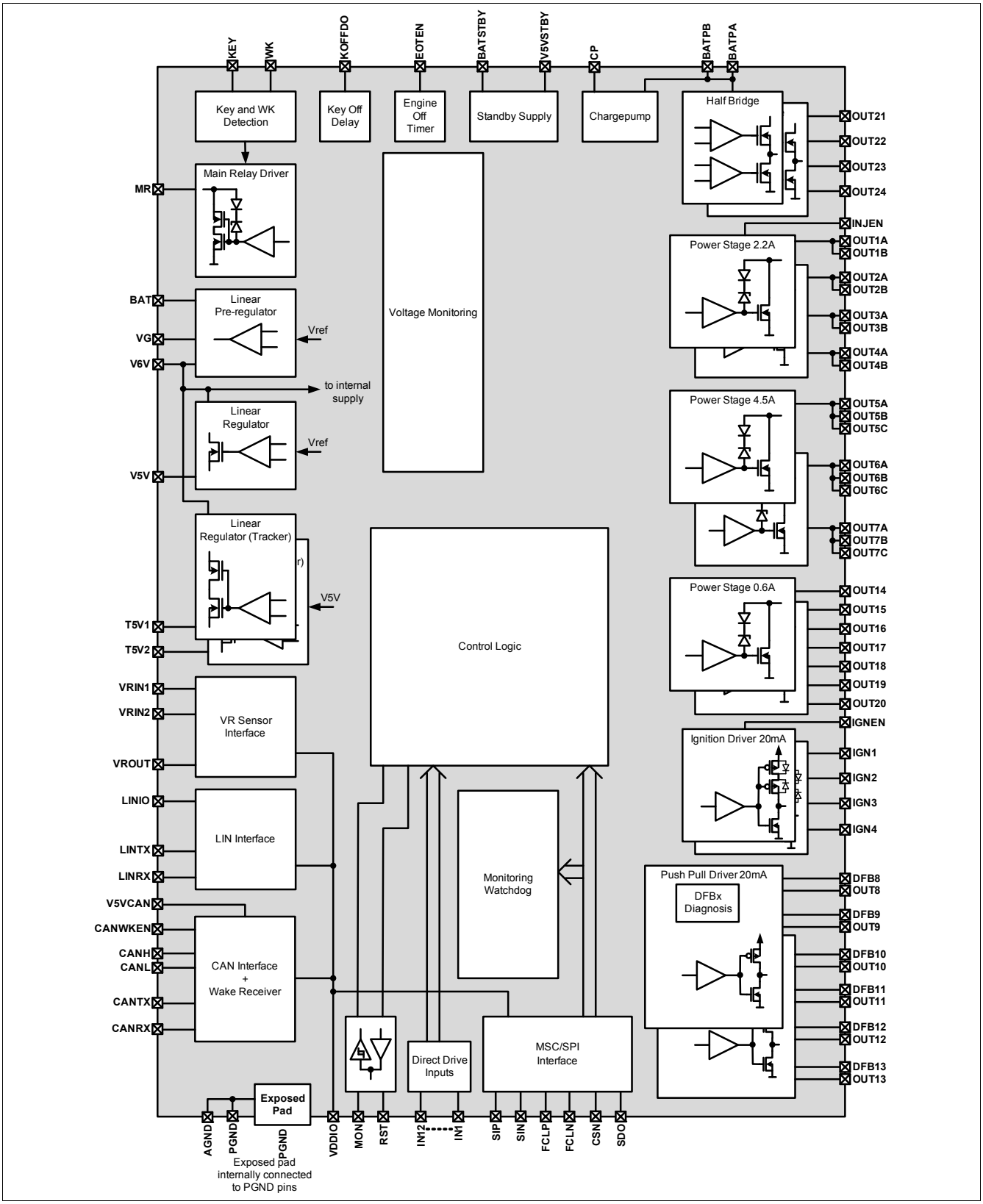

Figure 1 Block Diagram

3 Pin Configuration

3.1 Pin Assignment

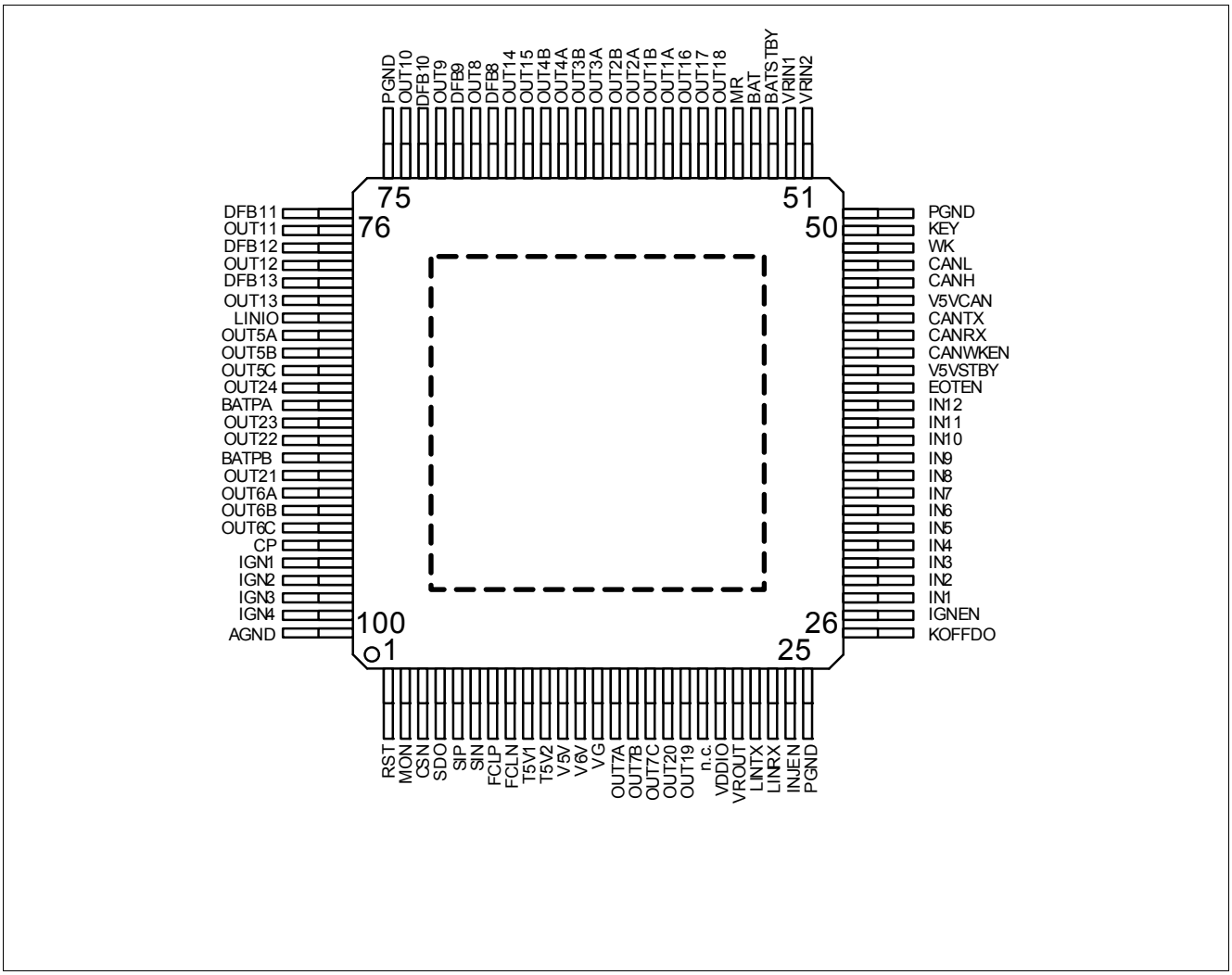

Figure 2 Pin Configuration

3.2 Pin Definitions and Functions

Pin	Symbol	Function	Function
1	*RST*	IN/OUT	**Reset;** Bidirectional pin for reset functions
2	*MON*	IN/OUT	**Monitor;** Bidirectional pin for monitoring functions
3	*CSN*	IN	**MSC/SPI slave chip select;** Single ended chip select for MSC and SPI
4	*SDO*	OUT	**MSC/SPI serial data output;** Output for MSC and SPI
5	*SIP*	IN	**MSC/SPI Data input;** positive data input of LVDS in MSC mode or single ended data input in SPI mode

Pin	Symbol	Function	Function
6	*SIN*	IN	**MSC data input or select input;** negative data input of LVDS in MSC mode or select input for SPI mode
7	*FCLP*	IN	MSC/SPI Clock input; positive clock input of LVDS in MSC mode or single ended clock input in SPI mode
8	*FCLN*	IN	**Select input or MSC clock input;** negative clock input of LVDS in MSC mode or select input for single ended mode (SPI or MSC)
9	*T5V1*	OUT	**5 V tracker;** Supply voltage for off- board sensors
10	*T5V2*	OUT	**5 V tracker;** Supply voltage for off- board sensors
11	*V5V*	OUT	**5 V supply;** Supply voltage for main functions of the ECU
12	*V6V*	IN	**Source of external pre-regulator**
13	*VG*	OUT	**Gate of external pre-regulator**
14	*OUT7A*	OUT	**Low-side power stage;** Must be connected to *OUT7B* and *OUT7C* without any parasitic
15	*OUT7B*	OUT	**Low-side power stage;** Must be connected to *OUT7A* and *OUT7C* without any parasitic
16	*OUT7C*	OUT	**Low-side power stage;** Must be connected to *OUT7A* and *OUT7B* without any parasitic
17	*OUT20*	OUT	**Low-side small signal stage;**
18	*OUT19*	OUT	**Low-side small signal stage;**
19	n.c.		leave open or connect to GND
20	*VDDIO*	Supply	**Supply input for logic level inputs and outputs**
21	*VROUT*	OUT	**Output of variable reluctance sensor interface;** Digital output to microcontroller
22	*LINTX*	IN	**Transmit digital input for LIN interface;**
23	*LINRX*	OUT	**Receive digital output for LIN interface;**
24	*INJEN*	IN	**Injector enable input;**
25	*PGND*	GND	**Power ground;** internally connected to cooling tab
26	*KOFFDO*	OUT	**Key off delay output;**
27	*IGNEN*	IN	**Ignition enable input;**
28	*IN1*	IN	**Parallel input;** Input pin for direct control of power stage OUT1,
29	*IN2*	IN	**Parallel input;** Input pin for direct control of power stage OUT2
30	*IN3*	IN	**Parallel input;** Input pin for direct control of power stage OUT3
31	*IN4*	IN	**Parallel input;** Input pin for direct control of power stage OUT4
32	*IN5*	IN	**Parallel input;** Input pin for direct control of push pull state IGN1
33	*IN6*	IN	**Parallel input;** Input pin for direct control of push pull state IGN2
34	*IN7*	IN	**Parallel input;** Input pin for direct control of push pull state IGN3
35	*IN8*	IN	**Parallel input;** Input pin for direct control of push pull state IGN4
36	*IN9*	IN	**Parallel input;** Input pin for direct control of power stages, could be multiplexed to various stages

Pin	Symbol	Function	Function
37	*IN10*	IN	**Parallel input;** Input pin for direct control of power stages, could be multiplexed to various stages
38	*IN11*	IN	**Parallel input;** Input pin for direct control of power stages, could be multiplexed to various stages
39	*IN12*	IN	**Parallel input;** Input pin for direct control of power stages, could be multiplexed to various stages
40	*EOTEN*	IN	**Engine off timer enable input;**
41	*V5VSTBY*	OUT	**5 V standby supply;** Supply voltage in sleep mode
42	*CANWKEN*	IN	**Enable input for remote CAN wake-up;**
43	*CANRX*	OUT	**Receive digital output for CAN;**
44	*CANTX*	IN	**Transmit digital input for CAN;**
45	*V5VCAN*	Supply	**5 V supply input for CAN;**
46	*CANH*	IN/OUT	**CAN bus high;**
47	*CANL*	IN/OUT	**CAN bus low;**
48	*WK*	IN	**Wake-up input;** Input signal and supply for MR
49	*KEY*	IN	**Key input;** Input signal and supply for MR
50	*PGND*	GND	**Power ground;** internally connected to cooling tab
51	*VRIN2*	IN	**Differential input of variable reluctance sensor;** Analog input from sensor
52	*VRIN1*	IN	**Differential input of variable reluctance sensor;** Analog input from sensor
53	*BATSTBY*	Supply	**Battery input for standby supply;** Battery supply voltage standby supply regulator
54	*BAT*	Supply	**Battery;** Supply voltage for main functions of the device.
55	*MR*	OUT	**Low-side power stage for main relay;**
56	*OUT18*	OUT	**Low-side power stage;**
57	*OUT17*	OUT	**Low-side power stage;**
58	*OUT16*	OUT	**Low-side power stage;**
59	*OUT1A*	OUT	**Low-side power stage;** Must be connected to *OUT1B* without any parasitic
60	*OUT1B*	OUT	**Low-side power stage;** Must be connected to *OUT1A* without any parasitic
61	*OUT2A*	OUT	**Low-side power stage;** Must be connected to *OUT2B* without any parasitic
62	*OUT2B*	OUT	**Low-side power stage;** Must be connected to *OUT2A* without any parasitic
63	*OUT3A*	OUT	**Low-side power stage;** Must be connected to *OUT3B* without any parasitic
64	*OUT3B*	OUT	**Low-side power stage;** Must be connected to *OUT3A* without any parasitic

Pin	Symbol	Function	Function
65	*OUT4A*	OUT	**Low-side power stage;** Must be connected to *OUT4B* without any parasitic
66	*OUT4B*	OUT	**Low-side power stage;** Must be connected to *OUT4A* without any parasitic
67	*OUT15*	OUT	**Low-side power stage;**
68	*OUT14*	OUT	**Low-side power stage;**
69	*DFB8*	IN	**Drain Feedback;** Related to OUT8
70	*OUT8*	OUT	**Push pull stage;** To control on- board MOSFET
71	*DFB9*	IN	**Drain Feedback;** Related to OUT9
72	*OUT9*	OUT	**Push pull stage;** To control on- board MOSFET
73	*DFB10*	IN	**Drain Feedback;** Related to OUT10
74	*OUT10*	OUT	**Push pull stage;** To control on- board MOSFET
75	*PGND*	GND	**Power ground;** internally connected to cooling tab
76	*DFB11*	IN	**Drain Feedback;** Related to OUT11
77	*OUT11*	OUT	**Push pull stage;** To control on- board MOSFET
78	*DFB12*	IN	**Drain Feedback;** Related to OUT12
79	*OUT12*	OUT	**Push pull stage;** To control on- board MOSFET
80	*DFB13*	IN	**Drain Feedback;** Related to OUT13
81	*OUT13*	OUT	**Push pull stage;** To control on- board MOSFET
82	*LINIO*	IN/OUT	**BUS for LIN interface;**
83	*OUT5A*	OUT	**Low-side power stage;** Must be connected to *OUT5B* and *OUT5C* without any parasitic
84	*OUT5B*	OUT	**Low-side power stage;** Must be connected to *OUT5A* and *OUT5C* without any parasitic
85	*OUT5C*	OUT	**Low-side power stage;** Must be connected to *OUT5A* and *OUT5B* without any parasitic
86	*OUT24*	OUT	**Half bridge stage;**
87	*BATPA*	Supply	**Battery;** Supply voltage for half bridges and the charge pump; must be connected to *BATPB* without any parasitic
88	*OUT23*	OUT	**Half bridge stage;**
89	*OUT22*	OUT	**Half bridge stage;**
90	*BATPB*	Supply	**Battery;** Supply voltage for half bridges and the charge pump; must be connected to *BATPA* without any parasitic
91	*OUT21*	OUT	**Half bridge stage;**
92	*OUT6A*	OUT	**Low-side power stage;** Must be connected to *OUT6B* and *OUT6C* without any parasitic
93	*OUT6B*	OUT	**Low-side power stage;** Must be connected to *OUT6A* and *OUT6C* without any parasitic
94	*OUT6C*	OUT	**Low-side power stage;** Must be connected to *OUT6A* and *OUT6B* without any parasitic
95	*CP*	OUT	**Charge pump;** add external capacitance to stabilise charge pump voltage

Pin Configuration

Pin	Symbol	Function	Function
96	*IGN1*	OUT	**Push pull stage;** To control on- or off- board IGBT
97	*IGN2*	OUT	**Push pull stage;** To control on- or off- board IGBT
98	*IGN3*	OUT	**Push pull stage;** To control on- or off- board IGBT
99	*IGN4*	OUT	**Push pull stage;** To control on- or off- board IGBT
100	*AGND*	GND	**Signal ground;** internally connected to *PGND* and cooling tab
Cooling tab[1)]	*PGND*	GND	**Power ground;** internally connected PGND pins

1) Cooling tab is also called exposed pad

4 General Product Characteristics

General definition:

V_S is the short cut for all battery supplies of the TLE8888-1QK (*BAT*, *BATPA*, *BATPB*, *BATSTBY*) unless otherwise specified

GND is the short cut for all grounds of the TLE8888-1QK (*AGND*, *PGND*) unless otherwise specified.

Table 1 Absolute Maximum Ratings[1)]

T_j = -40°C to +150°C, all voltages with respect to GND, positive current flowing into pin, (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Voltages							
BATPA, BATPB, OUT8…13, DFB8…13	$V_{BATPA,MR}$, $V_{BATPB,MR}$, $V_{OUT8…13,MR}$, $V_{DFB8…13,MR}$,	-0.3	–	40	V	–	P_4.1
CP	$V_{CP,MR}$	-0.3	–	45	V	-0.3 V < V_{CP} - V_{BATPA} < 5 V	P_4.2
OUT1…7, OUT14…20	$V_{OUT1…7,MR}$, $V_{OUT14…20,MR}$	-0.3	–	50	V	OUTn is switched off, clamping is allowed according **Chapter 9.6**	P_4.3
V6V	$V_{V6V,MR}$	-0.3	–	10	V	–	P_4.4
VG	$V_{VG,MR}$	-0.3	–	12	V	V_{VG} - V_{V6V} < 5 V	P_4.5
V5V, V5VSTBY, VDDIO, V5VCAN	$V_{V5V,MR}$, $V_{V5STBY,MR}$, $V_{VDIO,MR}$, $V_{V5VCAN,MR}$	-0.3	–	5.5	V	–	P_4.6
T5V1, T5V2, IGN1…4	$V_{T5V1,MR}$, $V_{T5V2,MR}$, $V_{IGN1…4,MR}$	-1	–	40	V	–	P_4.7
BAT, BATSTBY, KEY, WK, MR	$V_{BAT,MR}$, $V_{KEY,MR}$, $V_{WK,MR}$, $V_{BATSTBY,MR}$, $V_{MR,MR}$,	-16	–	40	V	–	P_4.8

Table 1 Absolute Maximum Ratings[1)] (cont'd)

T_j = -40°C to +150°C, all voltages with respect to GND, positive current flowing into pin, (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
IN1…12, SIP, SIN, FCLP, FCLN, CSN, LINTX, CANTX, IGNEN, INJEN, CANWKEN, EOTEN	$V_{IN1...12,MR}$, $V_{FCLP,MR}$, $V_{FCLN,MR}$, $V_{SIP,MR}$, $V_{SIN,MR}$, $V_{CSN,MR}$, $V_{LINTX,MR}$, $V_{CANTX,MR}$, $V_{IGNEN,MR}$, $V_{INJEN,MR}$, $V_{EOTEN,MR}$, $V_{CANWKEN,MR}$	-0.3	–	5.5	V	–	P_4.9
SDO, RST,VROUT, LINRX, CANRX	$V_{SDO,MR}$, $V_{RST,MR}$,	-0.3	–	*VDDIO*+ 0.3	V	both conditions must be observed	P_4.31
	$V_{VROUT,MR}$, $V_{LINRX,MR}$, $V_{CANRX,MR}$	-0.3	–	5.5	V		
MON, KOFFDO	$V_{MON,MR}$,	-0.3	–	*V5V*+0.3	V	both conditions must be observed	P_4.10
	$V_{KOFFDO,MR}$	-0.3	–	5.5	V		
VRIN1	$V_{VRIN1,MR}$	-0.3	–	40	V	VRIN2 open	P_4.11
VRIN2	V_{VRIN2_MR}	-0.3	–	40	V	VRIN1 open	P_4.12
LINIO, CANH, CANL	$V_{LINIO,MR}$, $V_{CANH,MR}$, $V_{CANL,MR}$	-40	–	40	V	–	P_4.13
OUT21…24	$V_{OUT21...24,MR}$	-0.3	–	BATPx+0 .3	V	–	P_4.14
Currents							
DFB8…13	$I_{DFB8...13,MR}$	-5	–	5	mA	[2)]	P_4.15
Common Mode Input Current of VRIN1 and VRIN2	$I_{VRIN,CM,MR}$	-5	–	5	mA	$I_{VRIN,CM,MR} = I_{VRIN1} + I_{VRIN2}$ [2)]	P_4.16
Common Mode Input Current of VRIN1 and VRIN2, non permanent	$I_{VRIN,CM,MR}$	-15	–	15	mA	$I_{VRIN,CM,MR} = I_{VRIN1} + I_{VRIN2}$ [2)], maximum duty cycle 60% and maximum on time of 1 ms, 100 h	P_4.34
Differential Current of VRIN1 and VRIN2	$\Delta I_{VRIN,MR}$	-50	–	50	mA	$\Delta I_{VRIN,MR} = (I_{VRIN1} - I_{VRIN2})/2$ [2)]	P_4.17
PGND	$I_{PGND,MR}$	-25	–	25	A	–	P_4.18
IGN1…4	$I_{IGN1...4,MR}$	-50	–	–	mA	[2)]	P_4.19
Temperatures							

Table 1 Absolute Maximum Ratings[1)] (cont'd)

T_j = -40°C to +150°C, all voltages with respect to GND, positive current flowing into pin, (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction Temperature	T_j	-40	–	150	°C	3)	P_4.20
Storage Temperature	T_{stg}	-55	–	150	°C	–	P_4.21
ESD Susceptibility							
ESD Susceptibility	V_{ESDHBM}	-2	–	2	kV	HBM[4)]	P_4.22
ESD Susceptibility BAT, BATPA, BATPB, T5V1, T5V2, BATSTBY, KEY, WK, MR, OUT1…7, OUT14…24, DFB8…13, IGN1…4, CANH, CANL, LINIO, VRIN1, VRIN2 to PGND	$V_{ESD,HBM}$	-4	–	4	kV	HBM[4)]	P_4.23
ESD Susceptibility	V_{ESDCDM}	-500	–	500	V	CDM[5)]	P_4.24
ESD Susceptibility Pin 1, 25, 26, 50, 51, 75, 76, and 100 (corner pins)	$V_{ESD1, 25, 26, 50, 51, 75, 76, 100}$	-750	–	750	V	CDM[5)]	P_4.25

1) not subject to production test
2) Current has to be limited when maximum voltages are exceeded
3) according to qualification
4) ESD susceptibility, HBM according to EIA/JESD 22-A114F (1.5k Ω, 100 pF)
5) ESD susceptibility, Charged Device Model "CDM" EIA/JESD22-C101 or ESDA STM5.3.1

Notes

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.*

Table 2 Functional Range

T_j = -40°C to +150°C, all voltages with respect to GND, positive current flowing into pin, (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Supply Voltage - Reduced Operation	$V_{BAT,ro}$	4.5	–	6	V	reduced operation range, main relay and delayed off power stages are on if enabled, remaining functions not working	P_4.26
Supply Voltage - Low Drop Range	$V_{BAT,ld}$	6	–	9	V	low drop operation range, supply regulators working with supply out of the charge pump, standby supply regulator out of operation range	P_4.27
Supply Voltage - Normal Operation range	$V_{BAT,nop}$	9	–	28	V	normal operation range[1)]	P_4.28
Supply Voltage - Overvoltage Range	$V_{BAT,ov}$	28	–	40	V	overvoltage, power stages are switched off	P_4.29
Supply Voltage transients[2)]	d_{VBAT}/d_t	-1	–	1	V/µs	–	P_4.30

1) overtemperature due to bad R_{thJA} of the ECU or overload can happen
2) not subject to production test, specified by design

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

Table 3 Thermal Resistance

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction to Case[1)]	R_{thJC}	–	2.4	–	K/W	–	P_4.32
Junction to Ambient	R_{thJA}	–	–	–	K/W	[2)]	P_4.33

1) Not subject to production test, specified by design.
2) EIA/JESD 52_2, FR4, 80 × 80 × 1.5 mm; 35 × Cu, 5 × Sn; 300 mm^2

5 Operation Behavior

The TLE8888-1QK has implemented the whole supply of an ECU. Therefore a complex control logic is implemented to provide several operation states.

In this chapter

- the ramp up and down behavior and
- the status of the TLE8888-1QK during special conditions like 5 V undervoltage

is described. For the description of the monitoring watchdog module see **Chapter 6**.

In **Figure 3** the block diagram with all blocks affecting the status of the device and the ECU are shown. Following blocks are influenced during the different operation states and reset functions:

- Serial Interface MSC/SPI: with the serial interface the setup of the device is done
- Key input detection: start signal from key switch (KL15)
- Wake-up input detection: additional start signal e.g. from external CAN with wake-up by bus function
- Engine off timer: wake-up signal in comparator mode
- Power supply: ECU 5 V supply and 5 V sensor supplies, 5 V standby supply
- Voltage monitoring: supervision of all supplies (BAT, V5V, T5V1, T5V2)
- Main relay driver: controls external main relay to switch battery voltage to an ECU supply pin (see also application setups in **Chapter 17**)
- Power stages and half-bridges control block
- LIN/K-Line: transmission mode depends on operation state of the ECU
- CAN: transmission mode depends on operation state of the ECU, remote wake-up function
- Reset outputs MON and RST
- Monitoring watchdog module: signature watchdog for safety applications
- Operation Mode Control

The operation mode control block consists of:

- ramp up and down sequence control logic
- the reset control logic and
- status output logic.

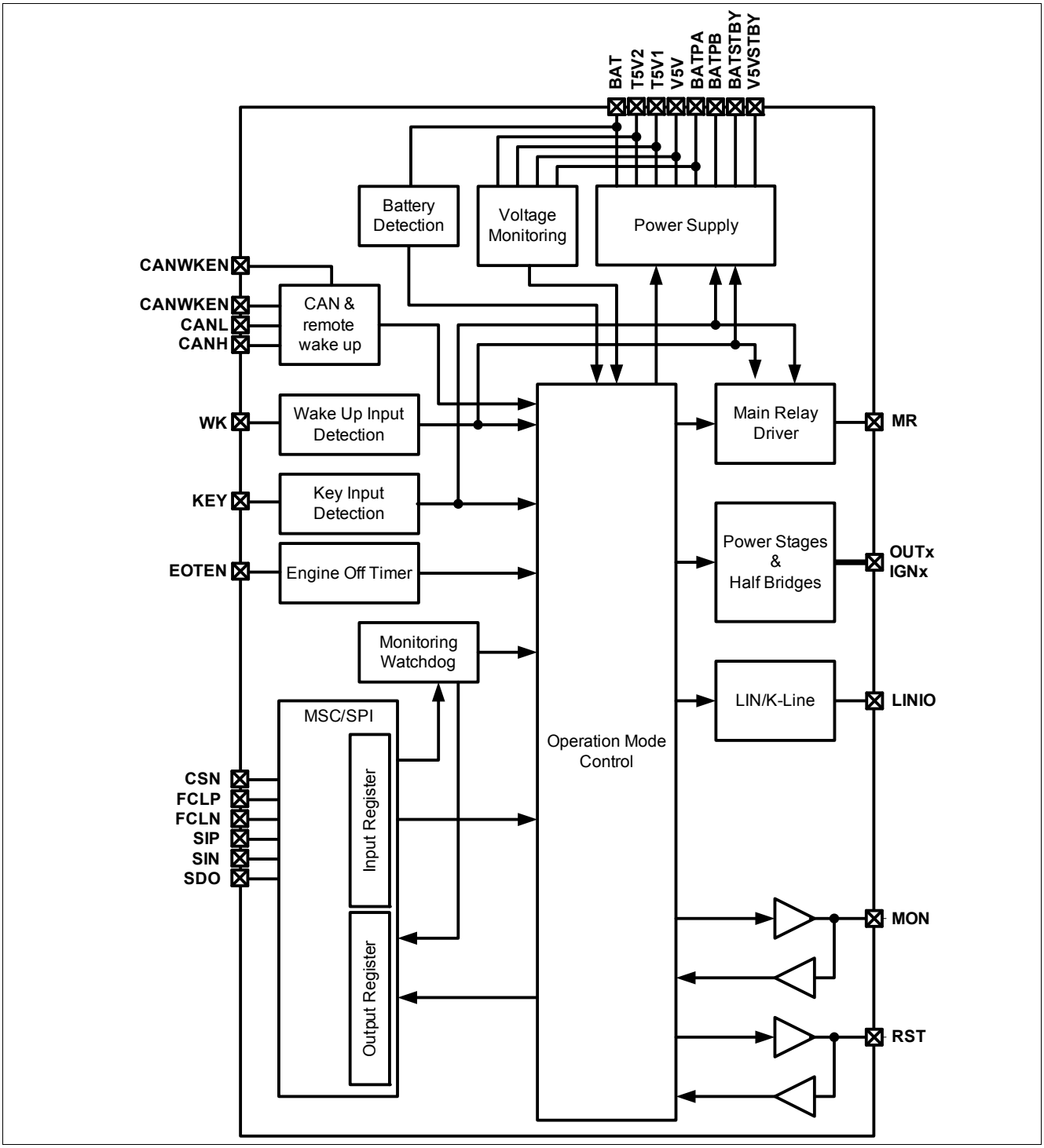

Figure 3 Block diagram operation mode control

5.1 Operation States

In **Figure 4** the state diagram of the whole ramp up and down sequence is shown. There are seven operation states:

- ECU sleep state: *KEY* and *WK* input are “low”, no wake-up signals from engine off timer or CAN are active, main relay is off, the whole ECU inclusive TLE8888-1QK is not supplied, 5 V standby supply is working if pin *BATSTBY* is supplied, engine off timer and CAN wake-up circuits are active if enabled and supplied.

- Supply ramp up state: *KEY* input or wake[1)] are “high” and the supply of the TLE8888-1QK starts working, the voltage of V6V, V5V, T5V1 and T5V2 are ramping up but the voltage levels are below the undervoltage threshold. For wake-up by wake[1)] the ramp up of the main supply has to be finished before the ramp up timer overflow. The main relay is switched on depending on the voltage level at the pin *BAT* (see **Chapter 7.2**)
- Normal operation state: *KEY* input or wake are “high” and main relay is switched on depending on the voltage level at the pin *BAT* or the status of bit **MR** in the status register **OpStat0** (see **Chapter 7.2**), the whole ECU is supplied and the status of the different functions and registers is according **Table 5** and **Table 6**.
- Afterrun state: *KEY* is “low” but afterrun enable bit is set and therefore the whole ECU is supplied, the status of the different functions and registers is according **Table 5** and **Table 6** and the microcontroller can execute afterrun routines
- Afterrun reset state: the reset procedure before direct reentry in normal operation is executed if bit **AR** =1 in the configuration register **OpConfig0**
- General power-down state: the supplies of the ECU (*V5V*, *T5V1*, *T5V2*) are disabled and the power-down timer is counting, main relay remains in the switching status and the TLE8888-1QK is supplied to ensure the power-down (V5V drops down to 0 V) of the ECU, *V5VSTBY* is working if *BATSTBY* is supplied, all functions to external are disabled.
- Wake clear state: this state avoids permanent wake-up in failure cases. The wake clear command is executed (function according setting bit **WKCLR** in the command register **Cmd0**). All wake signals which are active after the supply ramp up and the general power-down state are reset.

1) description see **Figure 4**, **Chapter 7.2**, **Chapter 7.4** and **Chapter 12.2.4**

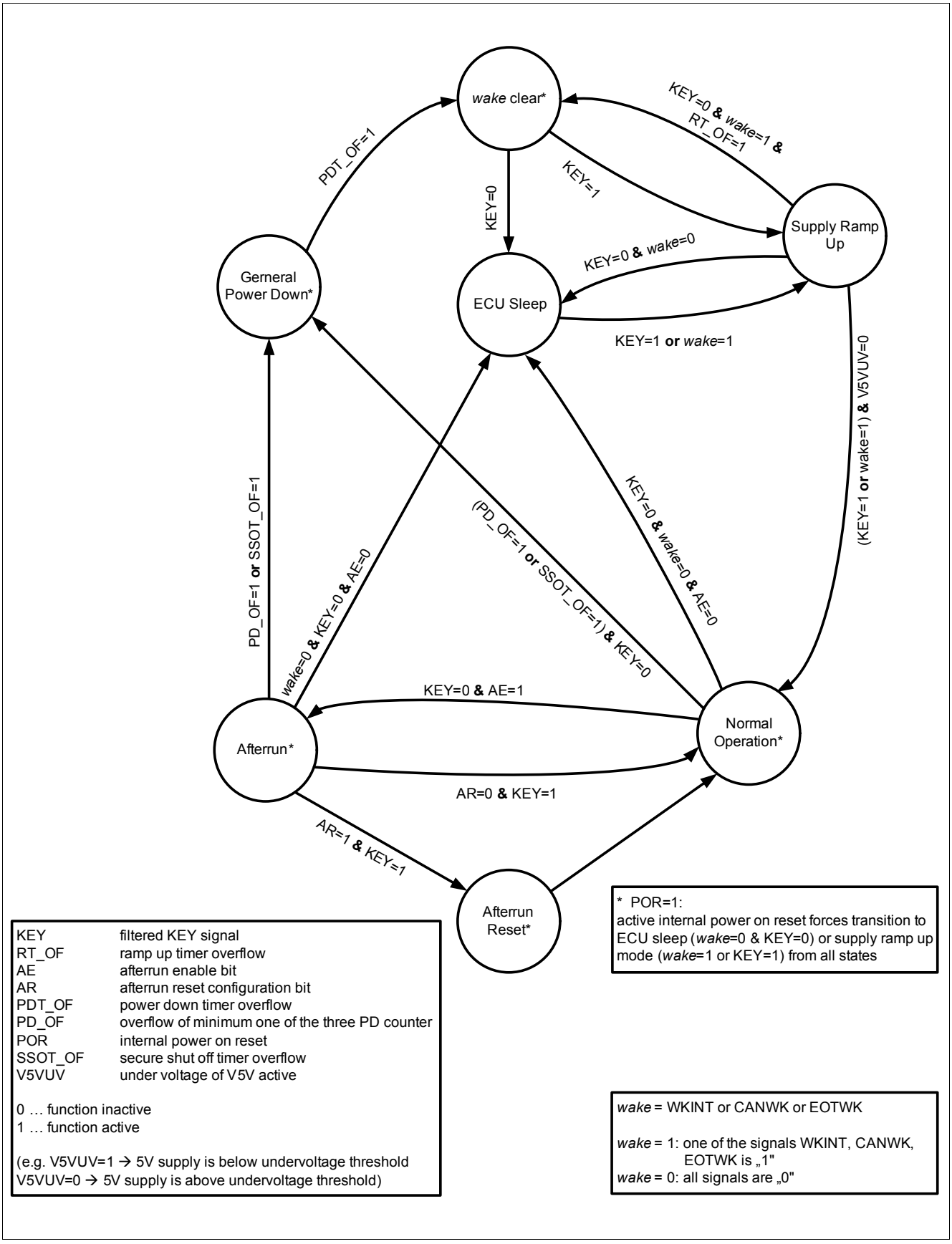

Figure 4 Operation state diagram

Description of the transitions:

Table 4 Operation State Transitions

Transition	Condition	Description
from all states to ECU sleep state	internal supply voltage < internal por threshold and *KEY* = 0 and wake[1)]=0[2)]	internal power on reset is active and reset the whole digital logic, ECU sleep state is entered due to no wake-up signal at *KEY* or wake
from all states to supply ramp up state	internal supply voltage < internal por threshold and *KEY* = 1 or wake = 1[2)]	internal power on reset is active and reset the whole digital logic, supply ramp up state is entered due to a wake-up signal at *KEY* or wake
ECU sleep state to supply ramp up state	*KEY* > $V_{KEY,th}$ or wake = 1	With a “high” voltage at *KEY* or wake the wake-up of the TLE8888-1QK starts
Supply ramp up state to ECU sleep state	*KEY* < $V_{KEY,th}$ and wake = 0[2)]	The external supply ramp up is not finished but the wake-up signals are low
Supply ramp up state to wake clear state	*KEY* < $V_{KEY,th}$ and wake = 1[2)] and RT_OF = 1	The *KEY* signal is low and the wake-up signals are active. The ramp up timer has an overflow which indicates a ramp up problem of the external supply (e.g. short to GND). To avoid permanent high current consumption the internal wake signals must be reset to enter the ECU sleep state.
Supply ramp up state to normal operation state	(*KEY* > $V_{KEY,th}$ or wake = 1) and V5V > $V_{uv,V5V}$[2)]	normal operation state is entered if the main supply voltage *V5V* is above the undervoltage threshold, *KEY* is high or one of the wake-up conditions are active
Normal operation state to afterrun state	*KEY* < $V_{KEY,th}$ and AE = 1[2)]	*KEY* is “low” and afterrun function is enabled: no changes in the setup of the TLE8888-1QK
Normal operation state to ECU sleep state	AE = 0 and KEY < $V_{KEY,th}$ and wake = 0[2)]	normal shut off
Normal operation state to general power-down state	(PD_OF = 1 or SSOT_OF = 1) and KEY < $V_{KEY,th}$[2)]	*KEY* is low and watchdog error shut off with overflow of the power-down counter or secure shut off due to expired secure shut off timer
Afterrun state to ECU sleep state	AE = 0 and KEY < $V_{KEY,th}$ and wake = 0[2)]	normal shut off in afterrun mode with the reset of the afterrun enable bit AE by the microcontroller
Afterrun state to general power-down state	PD_OF = 1 or SSOT_OF = 1	watchdog error shut off with overflow of the power-down counter or secure shut off due to expired secure shut off timer
Afterrun state to normal operation state	*KEY* > $V_{KEY,th}$ and AR = 0[2)]	reentry of normal operation with *KEY* on during afterrun operation, no reset is performed (AR = 0)
Afterrun state to afterrun reset state	*KEY* > $V_{KEY,th}$ and AR = 1[2)]	reentry of normal operation with *KEY* on during afterrun operation with reset (AR = 1)
Afterrun reset state to normal operation state		transition to normal operation with the next active internal clock edge after entry to the afterrun reset state

Table 4 Operation State Transitions (cont'd)

Transition	Condition	Description
General power-down state to wake clear state	PDT_OF = 1	with the power-down timer overflow the reset of the internal wake signals must be performed
Wake clear state to ECU sleep state	*KEY* < $V_{KEY,th}$	after reset of the internal wake signals and *KEY* is low the ECU sleep state is entered, no unwanted wake-up due to a failure condition will occur
Wake clear state to supply ramp up state	*KEY* > $V_{KEY,th}$	after reset of the internal wake signals and *KEY* is high the supply ramp up state is entered, no unwanted wake-up due to a failure condition at the CAN bus and pin *WK* will occur

1) wake = WKINT or CANWK or EOTWK (see **Chapter 7.2**, **Chapter 7.4** and **Chapter 12.2.4**)
2) including defined filter times

The two states:

- normal operation
- afterrun

are reflected in the bit **OM** of the status register **OpStat0**.

The power-down time is defined with the bits **PDT** of the configuration register **OpConfig0**.

In **Figure 5** a sequence with wake-up by *KEY* and go to sleep with afterrun mode is shown.

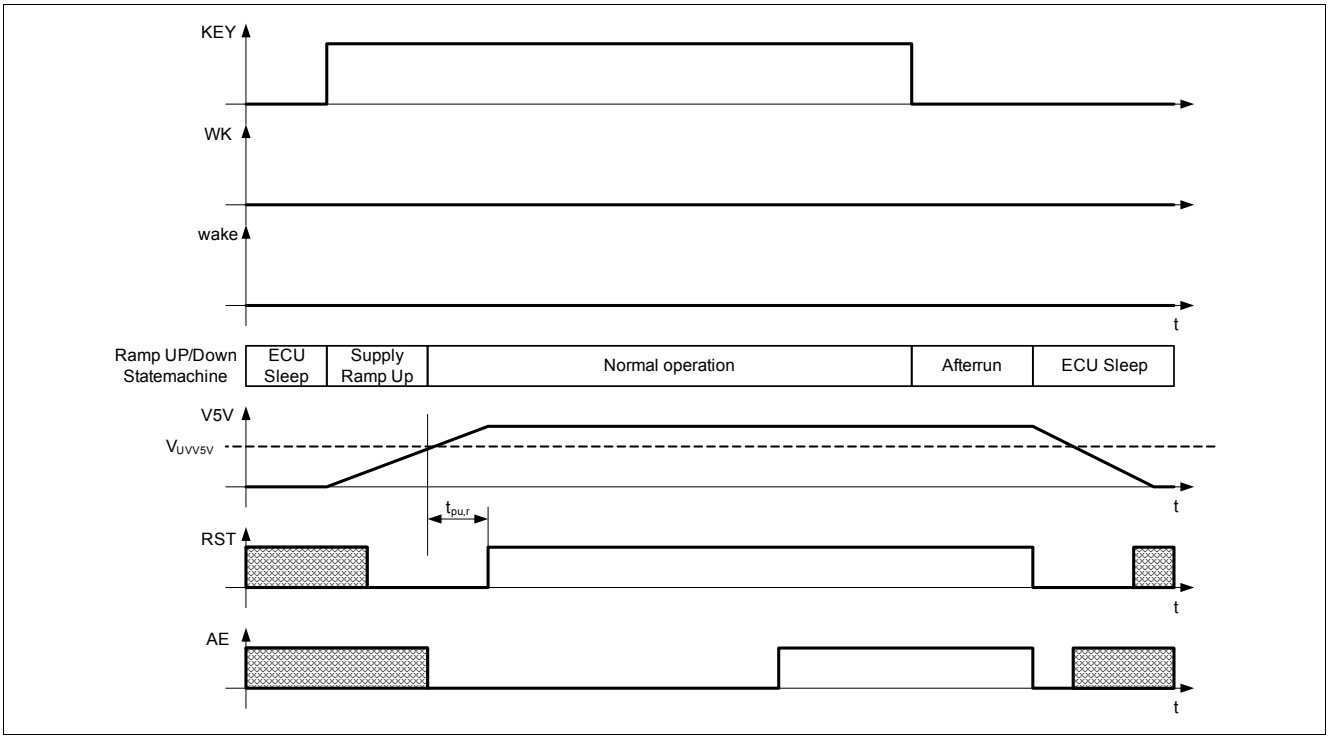

Figure 5 Ramp up and down sequence diagram with wake-up by *KEY* and afterrun mode

5.2 Reset and Operation Modes

Operation Behavior

The TLE8888-1QK provides several supervision functions which lead to some dedicated reset states and special operation modes of the device and the ECU.

There are two bidirectional reset pins MON and RST implemented. For the behavior during reset of the reset pins MON and RST and the other status of the TLE8888-1QK see **Table 5** and **Table 6**.

Following reset functions and special states are implemented:

- Internal power on reset: the internal power on reset detection circuit monitors the voltage level of the internal supply. For an internal supply voltage below the internal power on reset threshold the whole digital logic of the TLE8888-1QK is reset which results in the ECU sleep state or supply ramp up state depending on the state of *KEY* and wake. If the voltage level for operation is high enough the 6 V pre regulator is working. The 5 V supplies are disabled till the internal supply level is over the power on threshold level.
- ECU power on reset: this is the reset at ramp up of the power supplies and the beginning of the operation. The pins *RST* and *MON* are pulled to GND to reset the microcontroller and all devices connected to the pin *MON*. The device is reset to the initial reset status. The reset is released with a voltage at pin *V5V* higher than the **V5V Undervoltage Detection Hysteresis** after **tpu,r**.
- Reset during undervoltage of the 5 V supply V5V: this reset occurs during undervoltage of the 5 V ECU supply. The pins *RST* and *MON* are pulled to GND to reset the microcontroller and all devices connected to the pin *MON*. The delayed switch off function is active regarding the configuration setup. The status of the main relay is according to the status of the wake-up pins *KEY* and *WK* and the voltage level of the supply pin *BAT*.
- State during undervoltage of the 5 V supplies T5V1 and T5V2: with the undervoltage detection of the tracker supplies diagnosis bits are set but there is no effect to the behavior of the device.
- Reset during overvoltage of the 5 V supply V5V: with the overvoltage detection of the 5 V ECU supply all functions of the device which have an effect externally or can lead to overcurrent or overtemperature are disabled (e.g. power stages, LIN/CAN/MSC/SPI communication). The pins *RST* and *MON* are low.
- State during overvoltage of the 5 V supplies T5V1 and T5V2: with the detection of overvoltage of the tracker supplies diagnosis bits are set but there is no effect to the behavior of the device.
- Power stages switch off during overvoltage of the battery supply *BAT*: For voltages at the supply pin *BAT* higher than the overvoltage threshold the power stages are disabled to avoid too high clamping energy during switch off. Damage of the switches is prevented.
- Watchdog reset: If the reset counter is incremented and the reset is enabled (bit **WDREN** = 1) the microcontroller is reset with a “low” at the pin *RST*. The power stages are disabled and the LIN/CAN communication is set to receive only mode.
- Software reset from microcontroller: with the software reset command (command register **CmdSR**) the software reset is activated. The device is reset to the reset status defined in **Table 5** and **Table 6**. The activation of the software reset triggers an increase of the power-down counter by 1.
- Reset with an external forced “low” at *RST*: With a detected “low” at the *RST* pin the TLE8888-1QK is reset to the reset status defined in **Table 5** and **Table 6**.
- Power stages switch off with an external forced “low” at *MON*: With a detected “low” at the *MON* pin the power stages are disabled (**O1E** to **O24E**, **IGN1E** to **IGN4E** are set to “0”). After *MON*=0 event the power stages must be enabled again.
- State with time out of the MSC communication: With the time out of the MSC communication the power stages are disabled (**O1E** to **O24E**, **IGN1E** to **IGN4E** are set to “0”). After the next valid received data frame the power stages must be enabled again.
- Afterrun reset: This reset is executed if the bit **AR** of register **OpConfig0** is 1 and the transition from afterrun state to normal operation is triggered (definition see **Table 6**).

Table 5 Overview Behavior at Reset and Operation Conditions (part 1)

Effect to functions:	Conditions						
	Internal power on reset	**ECU power on reset**	**Undervoltage V5V**	**Undervoltage T5V1, T5V2**	**Overvoltage V5V[1)]**	**Overvoltage T5V1, T5V2**	**Overvoltage BAT**
notes	forces state change	only after transition from Supply Ramp Up to Normal Operation state for **tpu,r**	timing see **Chapter 8.7** and **Table 7**	timing see **Chapter 8.7**	timing see **Chapter 8.7** and **Table 7**	timing see **Chapter 8.7**	timing see **Chapter 8.7**
V5VSTBY, *V6V*	en.	en.	en.	en.	en.	en.	en.
V5V, *T5V1*, *T5V2*	dis.	en.	en.	en.	en.	en.	en.
MSC/SPI communication	dis.	dis.	dis.	en.	dis.	en.	en.
Main relay	en.[2)]	en.[2)]	en.[2)]	en.[2)]	en.[2)]	en.[2)]	en.[2)]
Low-side switches / Half bridges / Push Pull Driver	off/dis./off	off/dis./off	off/dis./off	no change	off/dis./off	no change	off/dis./off
OUT17 and *OUT21* with delayed switch off function	dis.	dis.	delayed switch off activated	en.	delayed switch off activated	en.	dis.
LIN/CAN communication	dis.	rec. only, after release setup acc. bits **CAN**, **LIN**, **CANWE**, **LINWE**[3)]	rec. only, after release setup acc. bits **CAN**, **LIN**, **CANWE**, **LINWE**[3)]	acc. bits **CAN**, **LIN**, **CANWE**, **LINWE**	dis., after release setup acc. bits **CAN**, **LIN**, **CANWE**, **LINWE**	acc. bits **CAN**, **LIN**, **CANWE**, **LINWE**	acc. bits **CAN**, **LIN**, **CANWE**, **LINWE**
MON (output function)	“low”[4)]	“low”	“low”	no effect[5)]	“low”	no effect[5)]	no effect[5)]
RST (output function)	“low”[4)]	“low”	“low”	no effect[5)]	“low”	no effect[5)]	no effect[5)]
Watchdog Sequence, Heartbeat Timer[6)]	reset	reset	reset	no effect	reset	no effect	no effect

Table 5 Overview Behavior at Reset and Operation Conditions (part 1) (cont'd)

Effect to functions:	Conditions						
	Internal power on reset	**ECU power on reset**	**Undervoltage V5V**	**Undervoltage T5V1, T5V2**	**Overvoltage V5V[1)]**	**Overvoltage T5V1, T5V2**	**Overvoltage BAT**
WWD Error Counter, FWD pass counter, Total error counter	reset	reset	reset	no effect	reset	no effect	no effect
PD Counter	reset	reset	reset	no effect	reset	no effect	no effect
Reset Counter; SSOT	reset	reset	reset	no effect	reset	no effect	no effect
AR; **CANWE**; **LINWE**; **FWDQUEST**	reset	reset	reset	no effect	reset	no effect	no effect
AE; **WWDConfig0**; **WDConfig0**; watchdog diagnosis bits	reset	reset	reset	no effect	reset	no effect	no effect
Logic and MSC/SPI register bits[7)8)]	reset	reset	reset, diagnosis bit is set	diagnosis bits are set	no effect	diagnosis bits are set	diagnosis bit is set
EOTWK, **CANWK**, **WKINT**	no effect	no effect	reset	no effect	no effect	no effect	no effect

1) for voltages greater than the maximum ratings of pin *V5V* behavior is not guaranteed
2) according the definition in **Chapter 7**
3) after release of RST (transition from low to high) there is a time delay of **tdel,r** before configuration is enabled
4) active pull down if supply voltage is high enough
5) pull up of open drain output is active
6) start of watchdog sequence after release of reset
7) valid for all register bits which are not described in **Table 5** or **Table 6**
8) During active delayed switch off mode some register bits related to the power stages are not reset, see **Chapter 9.4**

Table 6 Overview Behavior at Reset and Operation Conditions (part 2)

Effect to functions:	Conditions							
	Watchdog reset	Safe State	SW reset from micro-controller	MON switch off (input function)	RST reset (input function)	MSC time out	afterrun reset	
							no reset AR=0	reset AR=1
note	status during reset pulse **top,r**		status during reset pulse **tint,r**	masked by MON output function	masked by RST output function	status till next valid MSC communication		
V5VSTBY, *V6V*	en.	en.	en.	en.	en.	en.	en.	en.
V5V, *T5V1*, *T5V2*	en.	en.	en.	en.	en.	en.	en.	en.
MSC/SPI communication	dis.	en.	en.	en.	dis.	en.	en.	dis.
Main relay	en.[1)]	en.	en.[1)]	en.[1)]	en.[1)]	en.[1)]	en.[1)]	en.[1)]
Low-side switches / Half bridges / Push Pull Driver	off/dis./off	off/dis./off	off/dis./off[3)]	off/dis./off	off/dis./off	off/dis./off	no change	off/dis./off
OUT17 and *OUT21* with delayed switch off function	no trigger if termination of delayed switch off function	no trigger if termination of delayed switch off function	dis.[3)]	delayed switch off activated	delayed switch off activated	delayed switch off activated	en.	dis.