Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

TLE9221SX

FlexRay Transceiver

Data Sheet

Rev. 1.3, 2015-09-21

Automotive Power

Table of Contents

Table of Contents 2

1 Overview 5
1.1 Features 5
1.2 Description 6

2 Block Diagram 8

3 Pin Configuration 9
3.1 Pin Assignment 9
3.2 Pin Definitions 9

4 Functional Overview 11
4.1 Functional Description 11
4.2 Modes of Operation 12
4.3 Behavior of Unconnected Digital Input Pins 12

5 Overview Functional Blocks 14
5.1 Transmitter 14
5.2 Receiver 14
5.3 Communication Controller Interface 15
5.4 Bus Guardian Interface 17
5.5 Host Interface 19
5.6 Wake-up Detector 20
5.7 Power Supply Interface 20
5.8 Bus Failure Detector 20
5.9 Central State Machine 20

6 Host Interface and Status Information Register 21
6.1 Host Commands 21
6.2 Status Information Register 22
6.2.1 Definition of the Status Information Register 22
6.2.2 SIR Readout Mechanism 22
6.2.3 Clearing Sequence of SIR 25
6.3 Status Information at the ERRN Output Pin 25
6.3.1 Reset the ERRN Output Pin 26

7 Wake-up Detector 27
7.1 Local Wake-up 27
7.1.1 Local Wake-up Falling Edge 28
7.1.2 Local Wake-up Rising Edge 29
7.2 Remote Wake-up 29
7.2.1 Standard Wake-up Pattern 30
7.2.2 Alternative Wake-up Pattern. 31
7.2.3 Wake-up by Payload 31
7.3 Wake-up Flag and Wake-up Bits 32

8 Power Supply Interface 34
8.1 INH Output 35
8.2 BD_Off and Undervoltage 35

8.3 Undervoltage Events ... 37
8.3.1 Undervoltage Flags and Undervoltage Bits ... 37
8.3.2 Undervoltage Event at uV_{BAT} ... 38
8.3.3 Undervoltage Event at uV_{CC} ... 39
8.3.4 Undervoltage Event at uV_{IO} ... 40
8.4 Power-up and Power-down ... 41
8.4.1 BD_Off State ... 41
8.4.2 Power-up ... 42
8.4.3 Interim BD_Standby Mode ... 43

9 Operating Mode Description ... 45
9.1 Operating Mode Transitions Overview ... 45
9.2 Operating Mode Change by Host Command ... 46
9.2.1 Entering BD_Sleep Mode via the BD_GoToSleep Command ... 51
9.2.2 Quitting BD_Sleep by Host Command ... 52
9.3 Operating Mode Changeover by Undervoltage Flag ... 52
9.3.1 Priorities of Undervoltage Events ... 56
9.4 Operating Mode Changes by Undervoltage Recovery ... 56
9.4.1 BD_Sleep Mode Entry Flag ... 56
9.5 Operation Mode Changes by the Wake-up Flag ... 61

10 Bus Error Indication ... 63
10.1 Setting the Bus Error Bit by uV_{CC} Undervoltage ... 63
10.2 Setting the Bus Error Bit by RxD and TxD Comparison ... 63
10.3 Setting the Bus Error Bit by Overcurrent Detection ... 63

11 Overtemperature Protection ... 64

12 Transmitter Time-out ... 65

13 Mode Indication, Power-up and Parity Information ... 66
13.1 Power-up Bit ... 66
13.2 Mode Indication Bit EN and Mode Indication Bit STBN ... 66
13.3 Even Parity Bit ... 66

14 General Product Characteristics ... 67
14.1 Absolute Maximum Ratings ... 67
14.2 Functional Range ... 69
14.3 Thermal Resistance ... 70

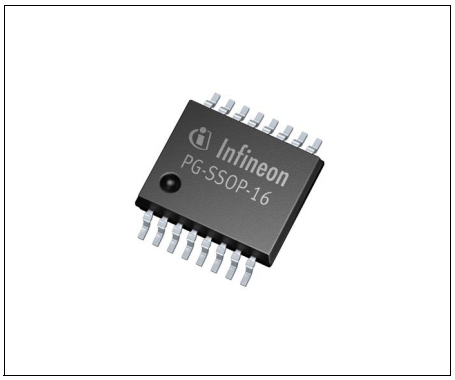
15 Electrical Characteristics ... 71
15.1 Functional Device Characteristics ... 71
15.2 Diagrams ... 87

16 Application Information ... 92
16.1 ESD Robustness according to IEC61000-4-2 ... 92
16.2 Bus Interface Simulation Model Parameter ... 92
16.3 Typical RxD Output Signals ... 92
16.4 Operating Temperature ... 94
16.5 Application Example ... 95
16.6 Further Application Information ... 95

17 Package Outlines ... 96

18 Revision History 97

1 Overview



PG-SSOP-16

1.1 Features

General Features

- Compliant with the FlexRay Electrical Physical Layer Specification, version 3.0.1 and ISO 17458
- Optimized for time-triggered in-vehicle networks with data transmission rates from 1 Mbit/s up to 10 Mbit/s
- Optimized electromagnetic immunity (EMI)
- Very low electromagnetic emission (EME), supporting large networks and complex bus topologies
- Very high level of ESD robustness, 11 kV according to IEC-61000-4-2
- Supports 60 ns minimum bit time
- Optimized digital inputs to minimize jitter
- Integrated Bus Guardian Interface
- Bus failure protection and error detection
- Automatic voltage adaptation on the digital interface pins
- High current digital outputs, optimized to drive long wires and high capacitive loads
- Green Product (RoHS compliant)
- AEC Qualified

Modes of Operation and Wake-up Features

- Sleep and stand-by operation mode with very low quiescent current
- Receive-only mode
- Separate INH output to control external circuitry
- Local wake-up input
- Remote wake-up via a dedicated wake-up symbol
- Alternative remote wake-up
- Remote wake-up via payload
- Wake-up source recognition and indication

Type	Package	Marking
TLE9221SX	PG-SSOP-16	9221

Protection and Diagnostics

- Short-circuit protection
- Overtemperature protection
- Undervoltage detection on all power supplies
- Transmitter time-out
- Error and wake-up indication on the ERRN output
- Status Information Register to indicate error bits and wake-up bits
- High Impedance bus input in BD_Off condition

1.2 Description

FlexRay is a serial, deterministic bus system for real-time control applications. It is designed for future requirements of in-vehicle control applications, providing data transmission rates up to 10 Mbit/s. FlexRay is designed for collision-free data communication. The nodes do not arbitrate and the FlexRay Communication Controller (CC) guarantees a collision-free bus access during normal operation.

The TLE9221SX FlexRay transceiver is a FlexRay bus driver (BD) and it accomplishes the physical interface between the Communication Controller and the bus medium. Fully compliant with the FlexRay Electrical Physical Layer Specification, version 3.0.1 (acronym EPL) and ISO 17458.

The TLE9221SX supports the following functional classes:

- Functional class “bus driver voltage regulator control”
- Functional class “bus driver bus guardian interface”
- Functional class “bus driver logic level adaption”
- Functional class “bus driver remote wake-up”

The TLE9221SX supports data transmission rates from 1 Mbit/s up to 10 Mbit/s. Besides the transmit and receive capability of the bus, the TLE9221SX provides arrangements for low power supply management, supply voltage monitoring and bus failure detection.

In BD_Sleep mode, the TLE9221SX quiescent current decreases to a typical, total current consumption of 47.5 µA, while the device is still able to wake up by a dedicated wake-up pattern on the FlexRay data bus or by a local wake-up event on the pin WAKE. The INH output pin allows the control of external circuitry depending on the selected mode of operation.

Fail-safe features, like bus failure detection or the power supply monitoring, combined with an easy accessible Status Information Register support the requirements of safety-related applications with extended diagnostic features.

The TLE9221SX is internally protected against transients on all global pins. Global pins are BP, BM, WAKE and V_{BAT}. It is possible to use the TLE9221SX without any additional external protection circuitry while the TLE9221SX meets the ESD and ISO pulse requirements of the car manufactures.

The TLE9221SX is designed on the latest Infineon Smart Power Technology SPT, which combines power devices with a highly integrated logic process. Based on its digital design concept, the TLE9221SX provides very high immunity against RF disturbances over a wide frequency range.

Based on the high symmetry of the BP and BM signals, the TLE9221SX provides the lowest level of electromagnetic emission (EME) within a wide frequency range.

Overview

The TLE9221SX is integrated in a RoHS compliant PG-SSOP-16 package. The TLE9221SX and the Infineon Smart Power Technology SPT are especially tailored to withstand the harsh conditions of the automotive environment and qualified according to the AEC-Q100 standard.

2 Block Diagram

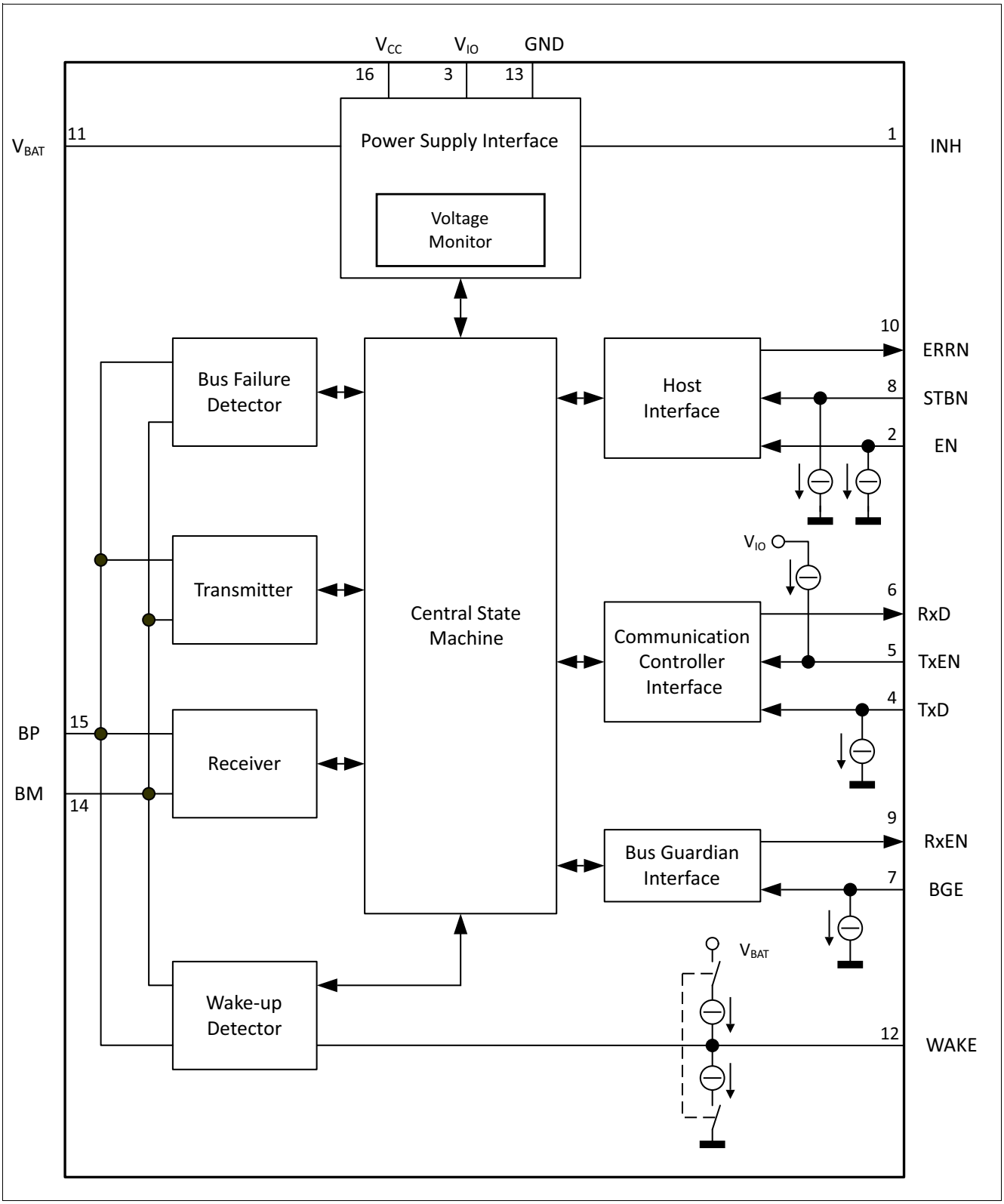


Figure 1 Block diagram

3 Pin Configuration

3.1 Pin Assignment

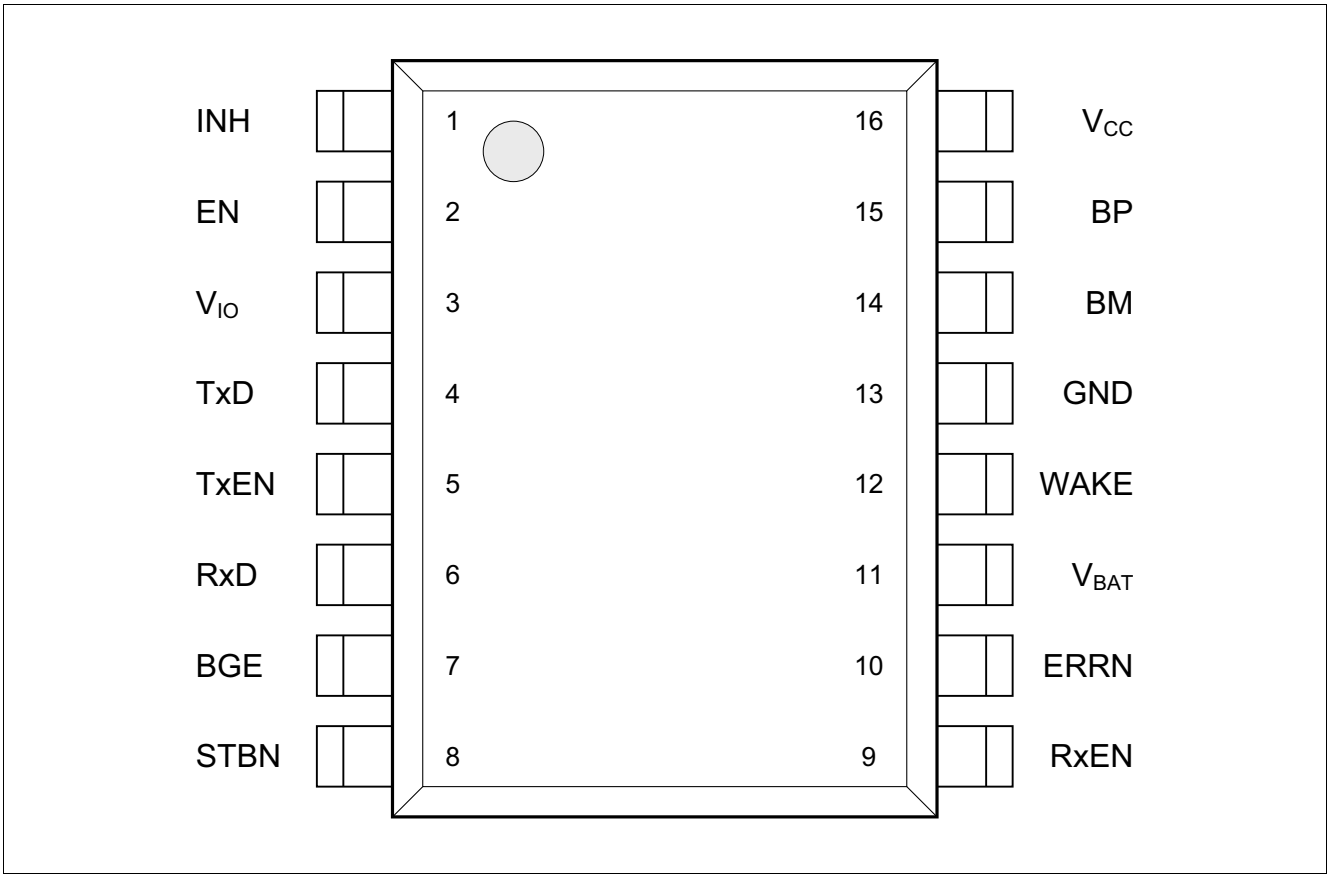


Figure 2 Pin configuration

3.2 Pin Definitions

Table 1 Pin definition and functions

Pin	Symbol	Function
1	INH	**Inhibit Output;** open drain output to control external circuitry, “high” impedance in BD_Sleep mode.
2	EN	**Enable Mode Control Input;** digital input for the mode selection, integrated “pull-down” resistor to GND.
3	V_{IO}	**Level Shift Input;** reference voltage for the digital input and output pins, 100 nF decoupling capacitor to GND recommended.

Pin Configuration

Table 1 Pin definition and functions

Pin	Symbol	Function
4	TxD	**Transmit Data Input;** integrated “pull-down” current source to GND, logical “low” to drive “Data_0” to the FlexRay bus.
5	TxEN	**Transmitter Enable Not Input;** integrated “pull-up” current source to V_{IO}, logical “low” to enable the Transmitter.
6	RxD	**Receive Data Output;** logical “low” while “Data_0” is on the FlexRay bus, output voltage adapted to the voltage on the V_{IO} level shift input.
7	BGE	**Bus Guardian Enable Input;** logical “high” to enable the Transmitter, integrated “pull-down” current source to GND.
8	STBN	**Stand-by Not Mode Control Input;** digital input for the mode selection, integrated “pull-down” current source to GND.
9	RxEN	Receive Data Enable Not Output; logical “low” indicates activity on the FlexRay bus, logical “high” in case the FlexRay Bus is “Idle”, output voltage adapted to the voltage on the V_{IO} level shift input.
10	ERRN	Error Not Diagnosis Output; logical “low” in failure case, output voltage adapted to the voltage on the V_{IO} level shift input.
11	V_{BAT}	Battery Voltage Supply; 100 nF decoupling capacitor to GND recommended.
12	WAKE	Wake-up Input; local wake-up input, terminated against GND and V_{BAT}, wake-up input sensitive to signal changes in both directions.
13	GND	Ground;
14	BM	Bus Line Minus; negative input/output to the FlexRay bus.
15	BP	Bus Line Plus; positive input/output to the FlexRay bus.
16	V_{CC}	Supply Voltage; Transmitter supply voltage, 100 nF decoupling capacitor to GND recommended.

4 Functional Overview

4.1 Functional Description

FlexRay is a differential bus system. The data is exchanged via a dual wire bus medium on the wires BP (Bus Line Plus) and BM (Bus Line Minus).

Three different bus symbols are supported: “Data_0”, “Data_1” and bus “Idle”. An active Transmitter of the TLE9221SX drives “Data_0” or “Data_1” to the bus medium, depending on the TxD input signal. To sustain an “Idle” signal on the FlexRay bus, the Transmitter is turned off, the voltage difference between BP and BM is below 30 mV, and the absolute voltage level on both bus lines, BP and BM depends on the Bus Biasing (see **Figure 3**):

- “Data_1”: uBus = uBP - uBM ≥ 300 mV → positive voltage between BP and BM
- “Data_0”: uBus = uBP - uBM ≤ - 300 mV → negative voltage between BP and BM
- “Idle”: |uBus| = |uBP - uBM| ≤ 30 mV

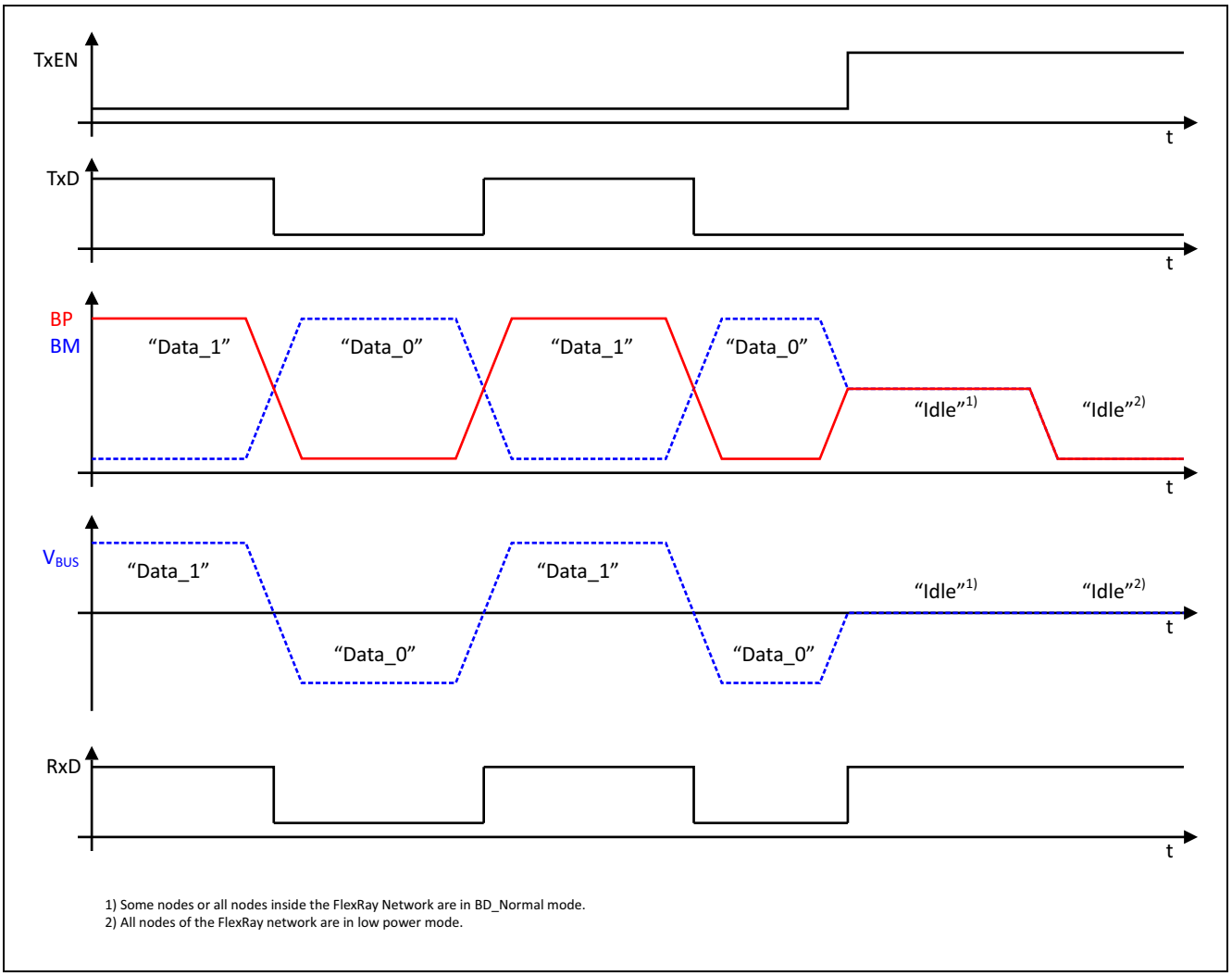


Figure 3 FlexRay EPL bus signals without Bus Guardian Interface

4.2 Modes of Operation

The FlexRay bus driver TLE9221SX supports four different modes of operation:

- BD_Normal mode
- BD_ReceiveOnly mode
- BD_Standby mode
- BD_Sleep mode

Each mode has specific characteristics in terms of quiescent current, data transmission or failure diagnostic. To enter the BD_Sleep mode, the TLE9221SX provides an intermediate mode, the so-called BD_GoToSleep command.

Mode changes on the TLE9221SX are either triggered by:

- The Host Interface and a host command on the input pins EN and STBN.
- The Power Supply Interface and an undervoltage event on one of the two power supplies or the reference supply uV_{IO}.
- The Wake-up Detector and wake-up events either on the FlexRay bus or on the local wake-up pin WAKE.

While all power supplies are turned off, the transceiver TLE9221SX is in BD_Off condition or also called “without supply”.

In BD_Sleep mode and in BD_Standby mode the quiescent current consumption at all three supplies is tailored to reach the minimum, and therefore only a limited set of the functions of the TLE9221SX is available. BD_Sleep mode and BD_Standby mode are also called low power modes. Conversely the modes BD_Normal and BD_ReceiveOnly are called non-low power modes.

4.3 Behavior of Unconnected Digital Input Pins

The integrated pull-up and pull-down resistors at the digital input pins force the TLE9221SX into a secure, fail safe behavior if the input pins are not connected and floating (see **Table 2** for details).

If the TxEN pin or the BGE pin is not connected in BD_Normal mode, the Transmitter is disabled. If the TxD input pin is open in BD_Normal mode and the Transmitter is active, the transceiver TLE9221SX drives a “Data_0” signal to the bus.

If the mode control input pins of the Host Interface are not connected, the pull-down resistors on the EN pin and on the STBN pin set the TLE9221SX by default to BD_Standby mode.

Table 2 Logical inputs when unconnected

Input Signal	Default State	Comment
TxD[1)]	“low”	pull-down to GND
TxEN[1)]	“high”	pull-up to uV_{IO}
STBN	“low”	pull-down to GND
EN	“low”	pull-down to GND
BGE[1)]	“low”	pull-down to GND

1) In BD_Sleep, BD_Standby, and also in BD_ReceiveOnly mode, the inputs TxD, TxEN and BGE are blocked by the internal logic. To optimize the total quiescent current consumption, the pull-up and pull-down structures are disabled in BD_Sleep mode, BD_Standby mode and BD_ReceiveOnly mode.

Functional Overview

The Power Supply Interface detects missing supply voltages or a missing reference supply. The Central State Machine sets the TLE9221SX into a fail safe mode when a supply is not available (details see **Chapter 8.3**).

5 Overview Functional Blocks

5.1 Transmitter

The Transmitter is the output driver for the FlexRay bus. It is based on a “high” side and “low” side push-pull unit. The push-pull units are supplied by the power supply uV_{CC} (see **Figure 1**).

While driving a “Data_1” or “Data_0” signal on to the FlexRay bus, the transceiver is active and enabled. During an “Idle” signal, the transceiver is turned off.

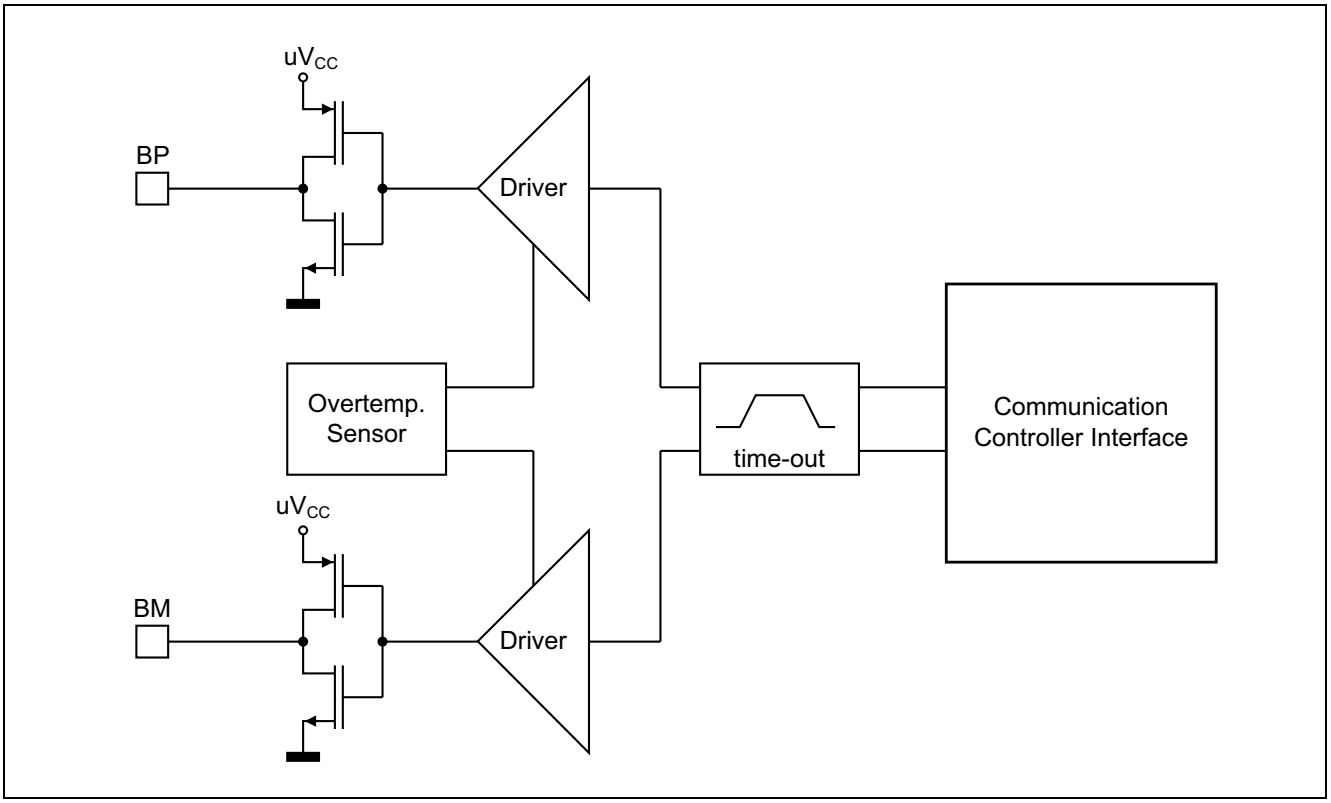


Figure 1 Block diagram of the Transmitter

The Transmitter is protected by an internal temperature sensor against overheating in terms of a short circuit on the bus lines BM or BP. The Transmitter is controlled by the Communication Controller Interface (see **Chapter 5.3**). The Transmitter is only active in BD_Normal mode.

5.2 Receiver

The Receiver detects communication elements, like “Idle”, “Data_1” and “Data_0”, when it is not in low power mode. It is connected to the BP and BM I/O pins of the TLE9221SX, together with the Transmitter, the Bus-Failure Detector, and the Wake-up Detector (see **Figure 1**). Based on a digital sampling concept, the Receiver is optimized to withstand the RF immunity requirements of the automotive industry.

The low pass input filter is tailored to support analog bit times down to 60 ns. Data bits below 60 ns may not be detected as valid communication elements. When the Receiver detects activity on the FlexRay bus behind the input filter, the differential Receiver distinguishes whether “Data_0” or “Data_1” is signaled by the differential bus voltage. The bus activity information is provided to the Bus Guardian Interface. The information regarding the FlexRay data bits is provided to the Communication Controller (see **Figure 2**).

The thresholds and the timings of the Receiver are available in **Figure 38** and **Figure 39**.

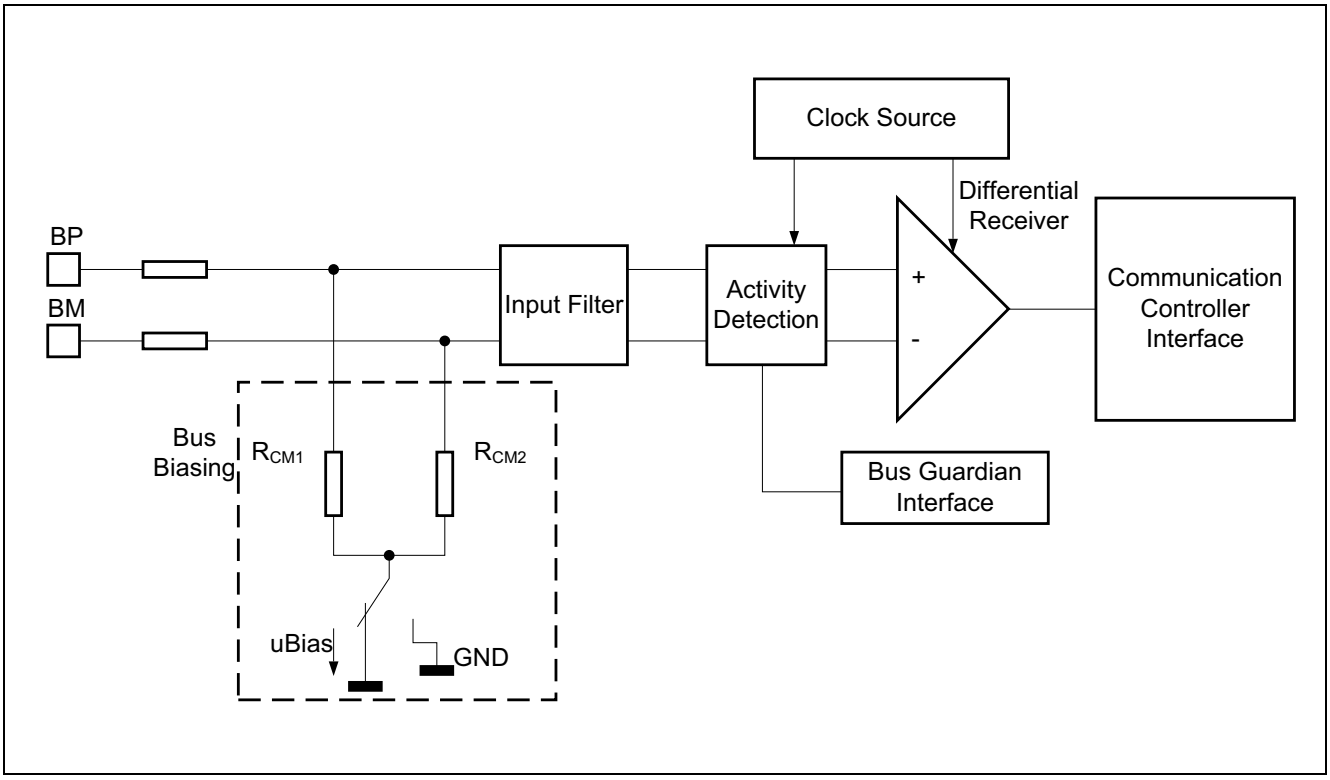


Figure 2 Block diagram of the Receiver

Apart from receiving data, the Receiver is responsible for biasing the FlexRay bus. The biasing of the FlexRay bus depends on the selected mode of operation.

In BD_Normal mode and BD_ReceiveOnly mode, the voltage uBias is connected to the BP and BM pins across the common mode resistors R_{CM1} and R_{CM2}. In BD_Sleep mode, BD_Standby mode and in the BD_GoToSleep command the I/O pins BP and BM are connected to GND via the common mode resistors R_{CM1} and R_{CM2}.

When TLE9221SX is not supplied, the bus biasing is open and is neither switched to uBias nor to GND, the BP and BM pins appear to the FlexRay bus as a high-impedance input (see **Table 3** and **Figure 2**).

Table 3 Bus biasing

Mode of Operation	Bus Biasing	Transmitter
BD Normal	uBias	active or disabled
BD_ReceiveOnly	uBias	disabled
BD_Standby	GND	disabled
BD_GoToSleep command	GND	disabled
BD_Sleep	GND	disabled
BD_Off condition	Open	disabled

5.3 Communication Controller Interface

The Communication Controller Interface is the interface between the FlexRay transceiver TLE9221SX and the FlexRay Communication Controller (CC). It comprises three digital signals:

- The TxEN (Transmit Data Enable Not) input pin
- The TxD (Transmit Data) input pin
- The RxD (Receive Data) output pin

Overview Functional Blocks

The logical I/O levels of all three digital pins are adapted to the reference voltage uV_{IO}. In case uV_{IO} is not available or in an undervoltage condition, the RxD output is set to logical “low” and the input pins TxD and TxEN are set to their default condition (see **Table 2**).

The Communication Controller logic block handles the interlock between TxD and TxEN. The Central State Machine provides the interface to other TLE9221SX function blocks and handles the dependency based on the selected mode of operation (see **Figure 3**).

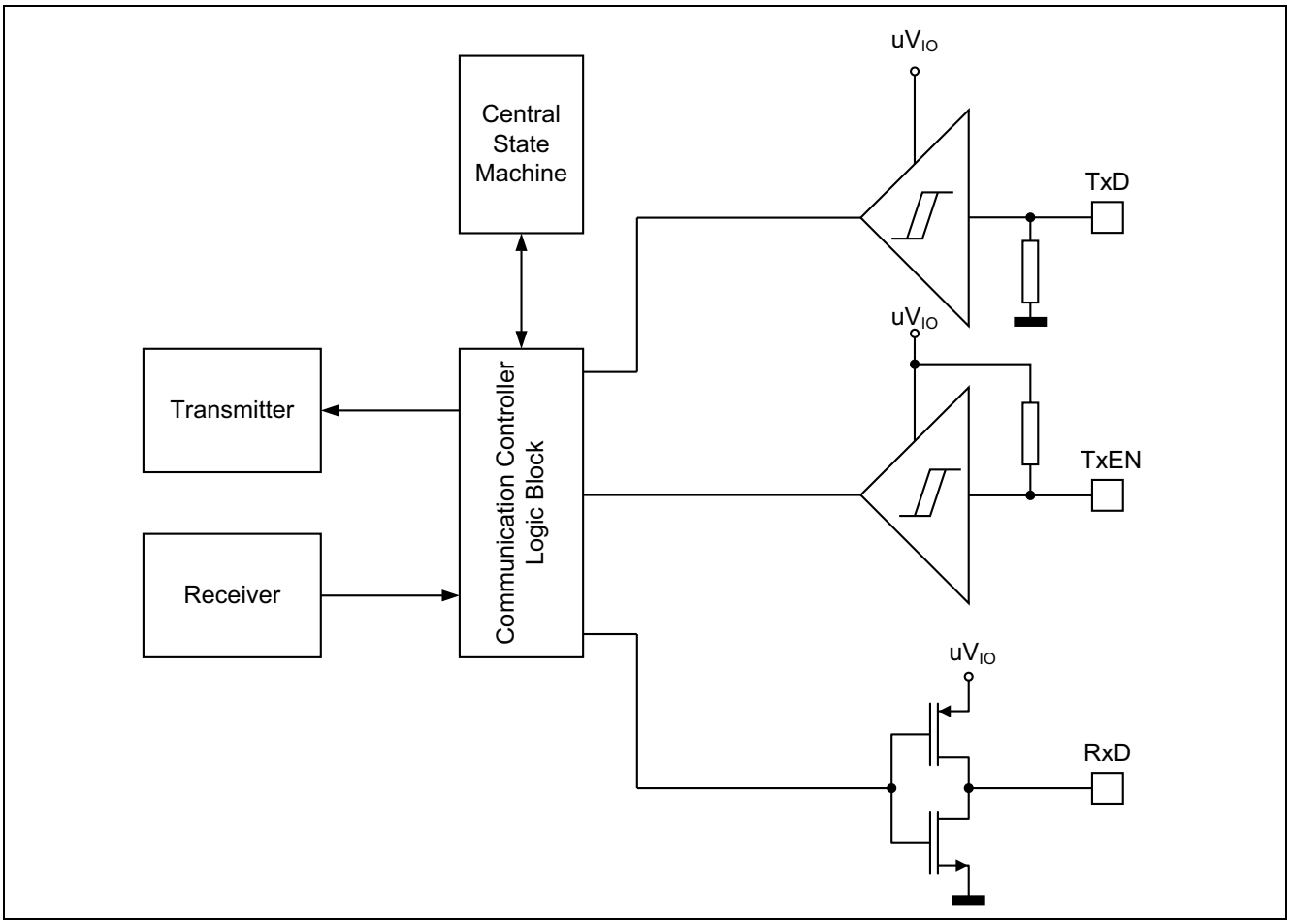


Figure 3 Block diagram of the Communication Controller Interface

The TxD input of the Communication Controller Interface is active only when the Transmitter is activated. To activate the Transmitter, the transceiver TLE9221SX needs to be in BD_Normal mode, the TxEN input must be at logical “low” and the BGE input pin must be at logical “high” (see **Table 4**).

The FlexRay transceiver shall never start data transmission with the communication element “Data_1”. Therefore, the activation of the Transmitter via the TxEN signal is only possible while the TxD signal is at logical “low” (see **Figure 4**).

While the Transmitter is enabled, the Communication Controller Interface drives the serial digital data stream available at the TxD input pin to the FlexRay bus via the Transmitter. A logical “high” signal at the TxD pin drives a “Data_1” signal to the FlexRay bus and a logical “low” signal drives a “Data_0” signal (see **Table 4**).

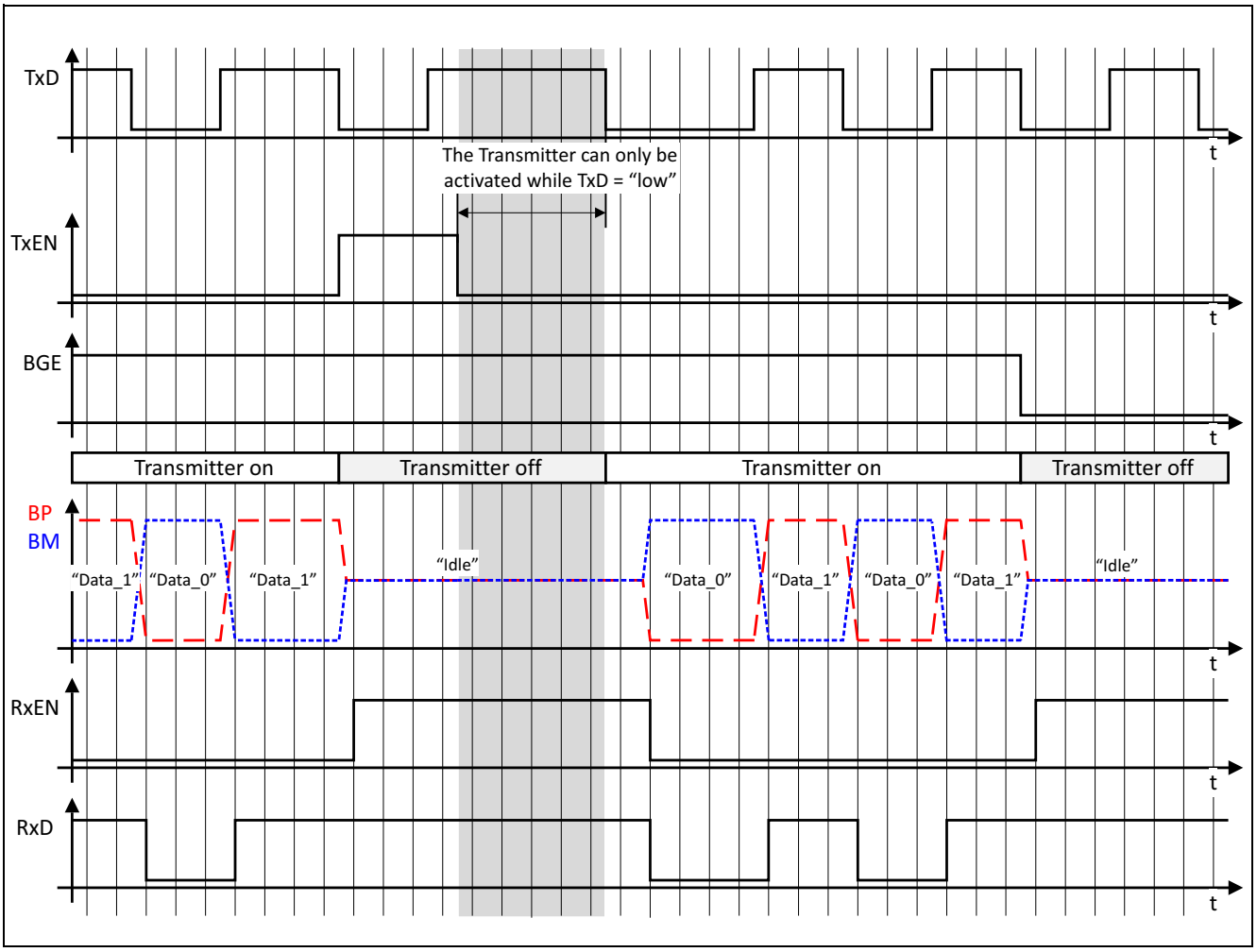


Figure 4 FlexRay physical layer bus signals with Bus Guardian Interface

The Receiver of the TLE9221SX is active in all non-low power operating modes. Similar to the TxD input, the RxD output indicates a “Data_1” signal on the FlexRay bus by a logical “high” signal and the “Data_0” signal by a logical “low” signal.

In every low power mode, the TxD and TxEN input pins are disabled. The RxD output pin is used to indicate the wake-up flag, while the transceiver is in low power mode (see **Table 5**).

5.4 Bus Guardian Interface

The Bus Guardian Interface comprises two digital signals:

- The BGE (Bus Guardian Enable) input pin.
- The RxEN (Receive Enable Not) output pin.

The logical I/O levels of the input and the output pin are adapted to the reference voltage uV_{IO}. In case uV_{IO} is not available or in undervoltage condition, the RxEN output is set to logical “low” and the input pin BGE is set to its default condition (see **Table 2**).

The Bus Guardian logic block handles the connection to the Transmitter and the Receiver. The Central State Machine provides the interface to other TLE9221SX function blocks and handles the dependency on the selected mode of operation (see **Figure 5**).

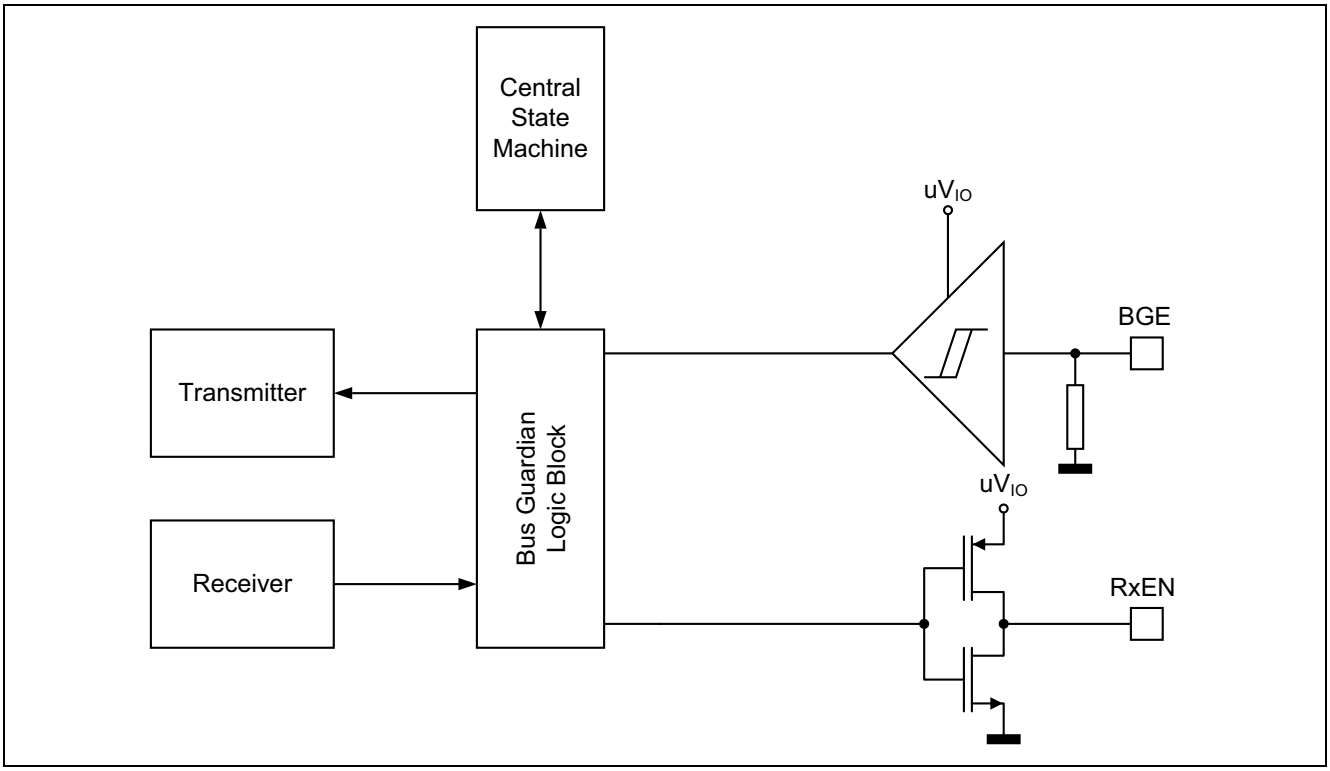


Figure 5 Block diagram of the Bus Guardian Interface

The BGE input is an additional fail safe input, allowing external hardware to block the data stream driven to the FlexRay bus medium. Switching the BGE input to logical “low” disables the Transmitter of TLE9221SX regardless of the signals on all the other digital input pins. The BGE input is active only in BD_Normal mode (see **Table 4** and **Figure 4**).

Table 4 TxD/TxEN interface, acting as a Transmitter

Mode of Operation	TxEN	BGE	TxD	Resulting Signal on the Bus
BD_Normal	“high”	X[1)]	X	“Idle”
	X	“low”	X	“Idle”
	“low”	“high”	“low”	“Data_0”
	“low”	“high”	“high”	“Data_1”
All other modes	X	X	X	“Idle”

1) X = don’t care

The RxEN (Receive Enable Not) indicates the activity on the FlexRay bus. In case the FlexRay bus is “Idle”, the logical signal on the RxEN is “high”. Any active data signal on the FlexRay bus, regardless of whether it is “Data_0” or “Data_1”, is indicated by a logical “low” signal on the RxEN output pin. Like the RxD output pin, the RxEN output pin indicates also the wake-up flag while the transceiver is in low power mode (see **Table 5** and **Figure 4**).

Table 5 RxD/RxEN interface, acting as Receiver with Bus Guardian Interface

Mode of Operation	Signal on the Bus Wires	Wake-up Flag	RxD	RxEN
BD_Normal, BD_ReceiveOnly	“Idle”	X[1)]	“high”	“high”
	“Data_0”	X	“low”	“low”
	“Data_1”	X	“high”	“low”

Table 5 RxD/RxEN interface, acting as Receiver with Bus Guardian Interface

Mode of Operation	Signal on the Bus Wires	Wake-up Flag	RxD	RxEN
BD_Sleep, BD_StandBy	X	“low” (set)	“low”	“low”
	X	“high” (not set)	“high”	“high”

1) X = don’t care

5.5 Host Interface

The Host Interface is the interface between the FlexRay transceiver TLE9221SX and the FlexRay host controller. It allows the host to control the operating modes and to read status and diagnostics information. It comprises three digital signals:

- The EN (Enable) input pin
- The STBN (Stand-By Not) input pin
- The ERRN (Error Not) output pin

The logical I/O levels of the pins are adapted to the reference voltage uV_{IO}. In case uV_{IO} is not available or in undervoltage condition, the ERRN output is set to logical “low” and the input pins EN and STBN are set to their default condition (see **Table 2**).

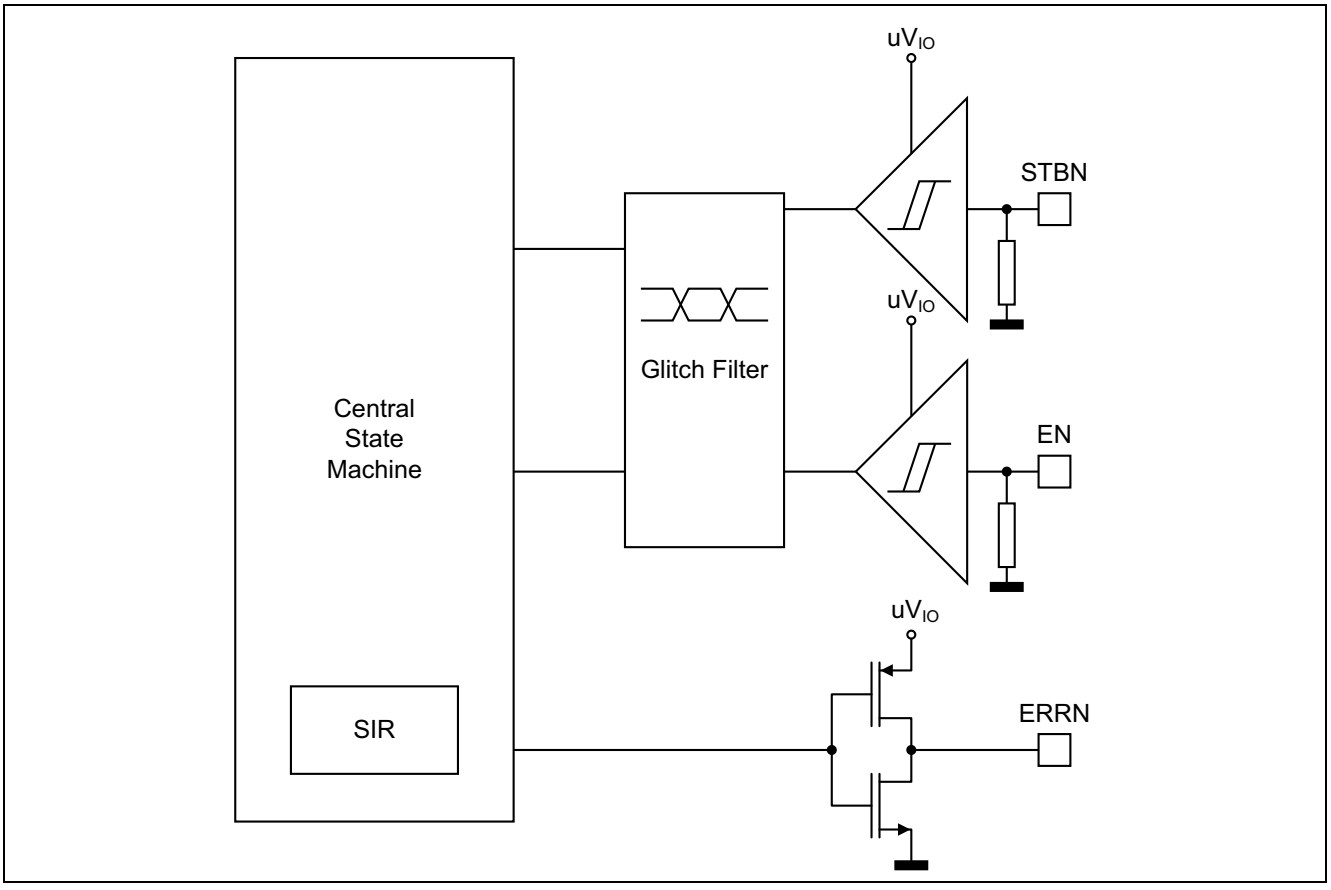


Figure 6 Block diagram of the Host Interface

The EN and STBN pins control the modes of operation. The pins are connected to the Central State Machine via an input filter. The input filter protects the transceiver TLE9221SX against unintentional mode changes caused by spikes on the EN and STBN.

The ERRN output signals failures, diagnostic and status information to the external host controller. The TLE9221SX also contains a Status Information Register. Access to the Status Information Register is given by the Host Interface (see details **Chapter 6**).

Table 6 Modes of operation[1)]

STBN	EN	Mode of Operation
“high”	“high”	BD_Normal
“high”	“low”	BD_ReceiveOnly
“low”	“high”	BD_GoToSleep, automatically transferred to BD_Sleep
“low”	“low”	BD_Standby

1) No undervoltage flag and no wake-up flag is set.

5.6 Wake-up Detector

The Wake-up Detector is a separate internal function block to detect wake-up events, be it a local or a remote wake-up event. The Wake-up Detector also enables the filtering unit to differentiate between real wake-up signals and floating signals or glitches on the wake-up lines. Active in every operation mode, and also in the BD_Normal or BD_ReceiveOnly mode, the Wake-up Detector ensures that no wake-up signal gets lost due to a concurrent change of the operating mode. The Wake-up Detector provides feedback on the wake-up information to the Central State Machine for further processing (details see **Chapter 7**).

5.7 Power Supply Interface

The Power Supply Interface is the interface from the bus driver to the external supply voltages. It hosts the inputs to the power supplies V_{BAT} and V_{CC} and also the level shift input to the reference voltage V_{IO}.

To enable the control of external circuitry, like a voltage regulator for example, the Power Supply Interface of the TLE9221SX provides an INH output.

All power supplies and the reference voltage are monitored and undervoltage conditions are indicated via the ERRN output on the Host Interface (details see **Chapter 8**).

5.8 Bus Failure Detector

The Bus Failure Detector monitors the data stream on the BM and BP I/O pins and compares the bus data with the digital data stream available at the Communication Controller Interface. Discrepancies between the bus data and the digital data are interpreted as a bus failure. The Bus Failure Detector is active only in BD_Normal mode. All detected failures are signaled on the ERRN output by the Host Interface (see **Chapter 10**).

5.9 Central State Machine

The Central State Machine is the main logic block of the TLE9221SX. It controls all functions of the TLE9221SX, the failure management as well as the power-up and power-down operations. The Central State Machine also provides some internal registers to store status, diagnostic and failure information.

- Information about the operating mode handling (see **Chapter 9**)
- Information about the Status Information Register (see **Chapter 6**)
- Information about the power management (see **Chapter 8**)
- Information about the bus failure flag (see **Chapter 10**)

6 Host Interface and Status Information Register

The Host Interface is the main interface for:

- Selecting and controlling the operation modes of the TLE9221SX by host commands.
- Receiving status information of the TLE9221SX at the ERRN output pin.
- Retrieving diagnostics information of the TLE9221SX by reading the Status Information Register.

The Host Interface is operational when the reference voltage uV_{IO} is in its functional range. In case the supply uV_{IO} is in undervoltage condition, the Host Interface is blocked and the operating mode of the TLE9221SX FlexRay transceiver is automatically set to BD_Sleep mode (compare with **Chapter 9.3**).

6.1 Host Commands

The digital inputs EN and STBN have dual functionality:

- EN and STBN are used to select the operating mode.
- EN and STBN are used to trigger the read-out of the Status Information Register.

The STBN, EN and all other digital inputs of the TLE9221SX are level-triggered and protected with a glitch input filter. Additionally, a digital input filter is provided at the mode selection pins STBN and EN.

To get a valid host command, which triggers a change of the operating mode, the external signals at the pins EN and STBN need to be stable at least for time $t \geq dBDLogic_{Filter}$. Signal changes with a smaller pulse width than the internal filter time $t < dBDLogic_{Filter}$ are not considered valid host commands and the TLE9221SX remains in its previous operating mode.

Within the time for mode change $t = dBD_{ModeChange}$ the FlexRay transceiver TLE9221SX changes to the selected mode of operation (see **Figure 4**). All output signals are valid after the mode transition and when the time for mode change $t = dBD_{ModeChange}$ has expired.

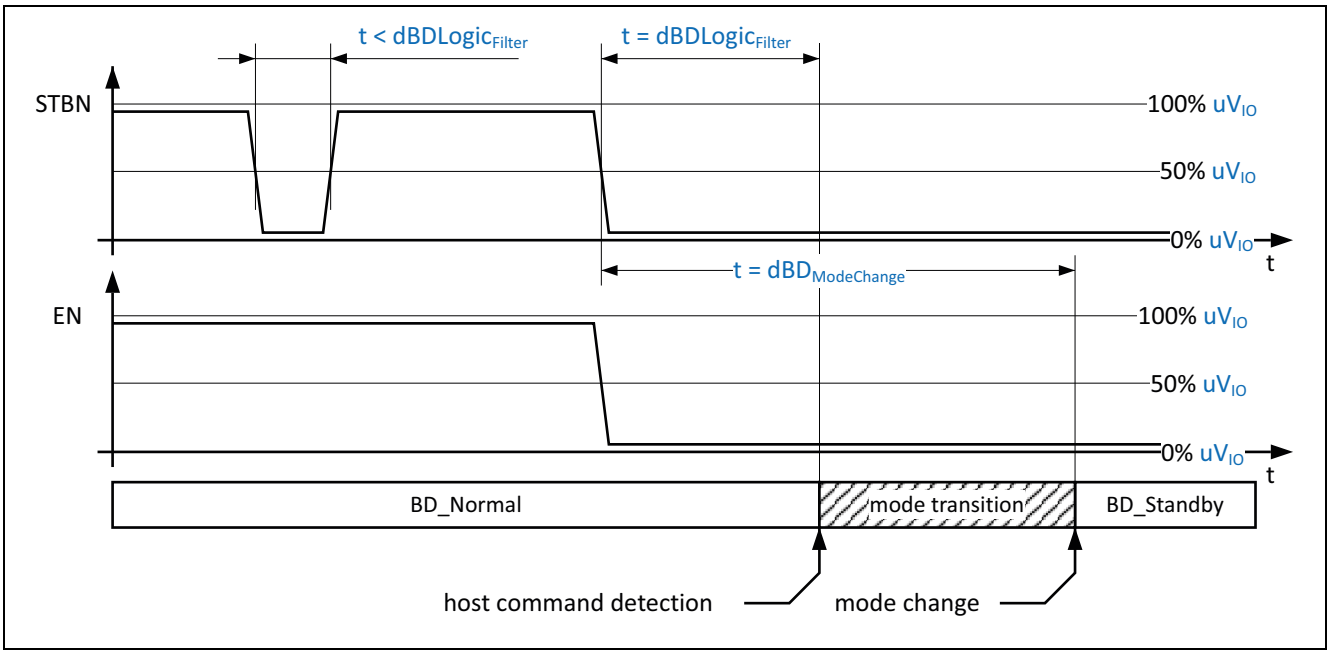


Figure 4 Example of a valid host command

Note: The time for mode change has to be considered for every change of the operation mode. All definitions in this data sheet are made considering the time for mode change $dBD_{ModeChange}$, even if the time for mode

change is not explicitly mentioned, for example in logical status tables, mode diagrams or in elementary timing diagrams.

6.2 Status Information Register

6.2.1 Definition of the Status Information Register

Failure, wake-up and diagnostic information is stored internally in a 16-bit wide register in the TLE9221SX, the so-called Status Information Register, or abbreviated to SIR (see **Table 7**).

Table 7 Bit definition of the Status Information Register[1)]

Bit	Description	Summary Flag / Bit
Bit 0	local wake-up bit	wake-up flag
Bit 1	remote wake-up bit	wake-up flag
Bit 2	reserved, always “high”	–
Bit 3	power-up bit	–
Bit 4	bus error bit	error bit
Bit 5	overtemperature error bit	error bit
Bit 6	overtemperature warning bit	error bit
Bit 7	Transmitter time-out bit	error bit
Bit 8	V_{BAT} undervoltage bit	error bit
Bit 9	V_{CC} undervoltage bit	error bit
Bit 10	V_{IO} undervoltage bit	error bit
Bit 11	error bit	–
Bit 12	wake-up source bit	–
Bit 13	EN mode indication bit	–
Bit 14	STBN mode indication bit	–
Bit 15	even parity bit	–

1) The bits are “low” active. For example bit = 0, when set.

6.2.2 SIR Readout Mechanism

The SIR is a “read-only” register and the data can be read out serially by using EN input as a data clock. While the SIR readout procedure is running, no operation mode change applies to the TLE9221SX. This allows regular data communication and read-out of the SIR at the same time.

Like all the other functions using the Host Interface, the reference supply uV_{IO} needs to be operational to read out the SIR.

The SIR readout is possible in all non-low power modes and in BD_Standby mode (see **Table 8**).

Table 8 Readout mechanism and modes of operation

Modes of Operation	Active / Not Active
BD_Normal	active
BD_ReceiveOnly	active
BD_GoToSleep Command	not active
BD_Standby	active
BD_Sleep	not active

Note: The SIR readout depends on the current operating mode selected and not on the host command applied. In case of undervoltage events, the host command could be BD_Normal mode, but the operating mode is BD_Sleep mode. In BD_Sleep mode, no SIR read-out is possible.

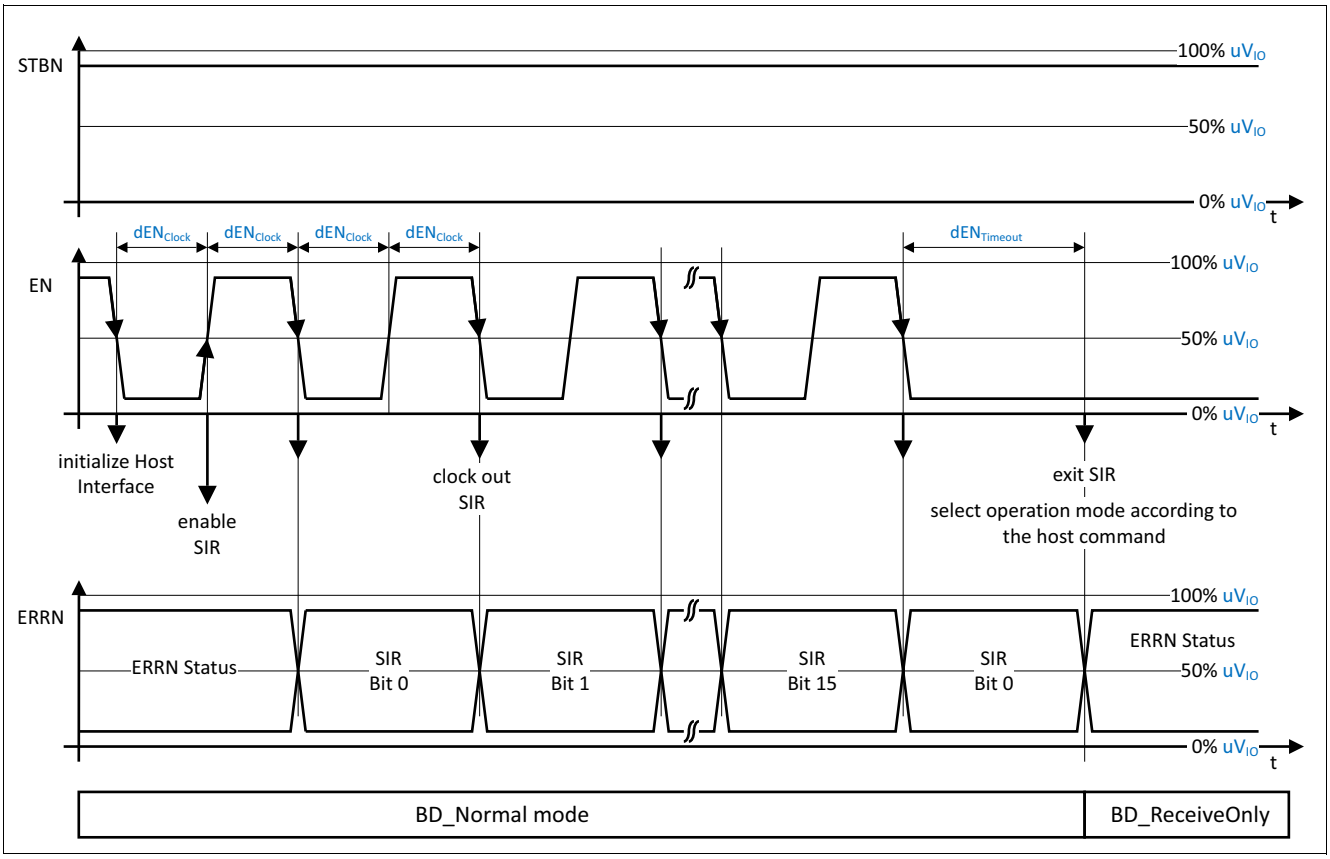


Figure 5 Timing diagram for the SIR readout in BD_Normal mode

During the SIR readout, the EN input acts as the clock and the ERRN output pin acts as the serial “data_out”. Irrespective of the digital signal at the STBN input, the SIR readout is always initialized by a signal change at the EN input pin. When the host command BD_Normal is applied to the Host Interface, the SIR read-out starts with the falling edge at the EN input (see **Figure 5**). For the host commands BD_Standby and BD_ReceiveOnly the read-out starts with the rising edge at the EN pin (see **Figure 6**).

After initialization, the internal timer starts and the TLE9221SX awaits the next signal change within the timing window $dEN_{CLOCK}(min) < t < dEN_{CLOCK}(max)$. The next rising edge[1)] enables the SIR and the bits can be clocked out.

If no signal change occurs after the initialization within the time frame t < $dEN_{Timeout}$, the TLE9221SX exits the SIR readout procedure and changes the operating mode according to the host command applied.

When the SIR is enabled, every falling edge at the EN input serially shifts out the SIR information at the ERRN output pin. With the first falling edge of the clock at the EN input, the least significant bit, bit 0, is clocked out to the ERRN output successively followed by bit 1, bit 2, etc, with every successive falling edge of the clock at the EN input.The SIR bits are “low” active, meaning that the ERRN signal = “low” when the SIR bit is set.

Note: The STBN input pin has no function when the SIR readout is enabled and the readout procedure is running. Nevertheless, it is recommended to keep the STBN pin stable (“high” or “low”) during the SIR readout procedure.

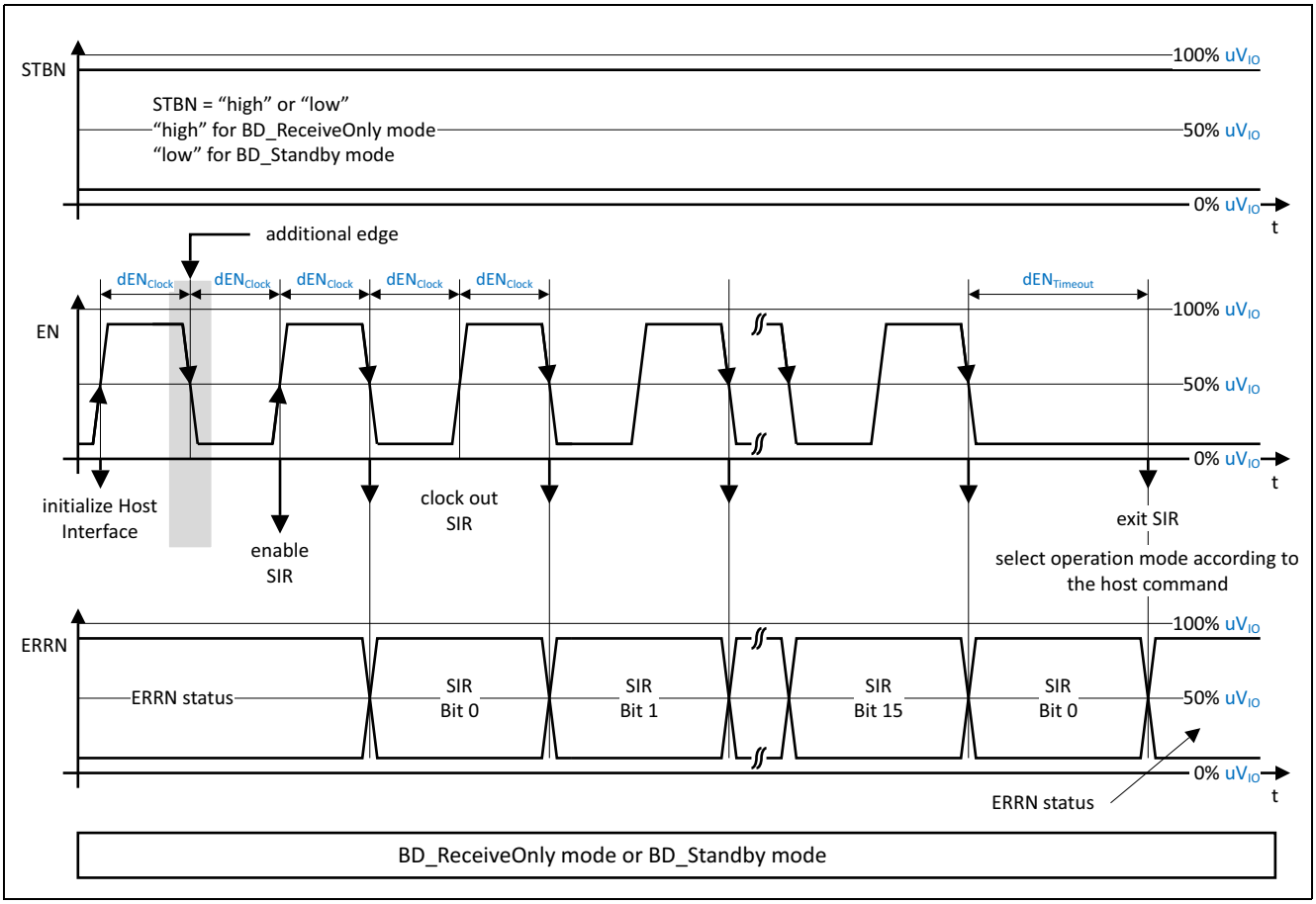


Figure 6 SIR readout in BD_ReceiveOnly or BD_Standby mode

The SIR readout procedure can be terminated at any time by stopping the clock at the EN input pin. While the signal at the EN pin is stable for the time t > $dEN_{Timeout}$, the TLE9221SX exits the SIR and changes to the operating mode according to the host command applied.

Note: It is recommended to leave the SIR read out procedure with the same EN signal that was present when the read out procedure was started. When time t = $dEN_{Timeout}$ expires, the mode change is triggered immediately.

1) While the TLE9221SX is in BD_Normal mode, the rising edge is the first signal change after initialization and enables the SIR readout. For the BD_ReceiveOnly and the BD_Standby mode, there is an additional falling edge between initialization and the SIR being enabled (compare with **Figure 5** and **Figure 6**).

6.2.3 Clearing Sequence of SIR

Failure and status information is latched in the SIR and the bits need to be cleared by a host command. In order to avoid any status bit from being cleared, while the root cause of the bit entry is still present, the TLE9221SX is equipped with a dedicated sequence to clear the bits of the Status Information Register. Before clearing any bits, the TLE9221SX checks, if the root cause of the bit entry is resolved. Only if the root cause of the bit entry has disappeared, the bit will be cleared.

The sequence to clear the bits of the SIR is started by:

- Entering BD_Normal mode via a host command.
- A complete readout of all 16 bits in the SIR.

In case the readout of the SIR is incomplete, for instance, due to a microcontroller interrupt during the readout procedure, the bits in the SIR remain set.

In case the SIR readout continues after the last bit (bit 15) has been clocked out, the TLE9221SX continues and clocks out the first bit (bit 0) again. On the second readout the bits in the SIR have been cleared. The bits will only be cleared if the root cause of setting them has been resolved.

*Note: Applying TLE9221SX the host command BD_Normal does not necessarily clear the SIR, since entering BD_Normal mode can be prevented by an undervoltage event (see **Table 13**).*

6.3 Status Information at the ERRN Output Pin

The ERRN output pin functions as a serial “data-out” during the SIR readout procedure. In any other case, the ERRN output pin indicates the status information. The ERRN pin indicates failure, wake-up events and the wake-up source.

The host command applied determines the incident that is signed at the ERRN output pin. The ERRN output pin is active “low” (details see **Table 9**).

Table 9 Signaling at ERRN

STBN	EN	Host Command	Error Bit[1)]	Wake-up Flag[1)]	ERRN	Condition
Error Indication						
“high”	“high”	BD_Normal	“high”	X[2)]	“high”	–
“high”	“high”	BD_Normal	“low”	X	“low”	–
“high”	“low”	BD_ReceiveOnly	“high”	“high”	“high”	–
“high”	“low”	BD_ReceiveOnly	“low”	“high”	“low”	–
Wake-up Source Indication						
“high”	“low”	BD_ReceiveOnly	X	“low”	“high”	wake-up source bit = “high”
“high”	“low”	BD_ReceiveOnly	X	“low”	“low”	wake-up source bit = “low”
Wake-up Indication						
“low”	“high”	BD_GoToSleep command	X	“high”	“high”	automatically transferred to BD_Sleep
“low”	“high”	BD_GoToSleep command	X	“low”	“low”	automatically transferred to BD_Sleep
“low”	“low”	BD_Standby	X	“high”	“high”	–
“low”	“low”	BD_Standby	X	“low”	“low”	–