



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



TLE9222

TLE9222PX

FlexRay Transceiver

Data Sheet

Rev. 1.0, 2015-07-02

Automotive Power

Table of Contents

1	Overview	4
2	Block Diagram	6
3	Pin Configuration	7
3.1	Pin Assignment	7
3.2	Pin Definitions and Functions	7
4	Functional Description	9
4.1	Operation Modes	9
4.1.1	BD_Normal Mode	10
4.1.2	BD_Standby Mode	10
4.1.3	BD_Off Condition	10
4.2	Communication Controller Interface	11
4.3	Bus Guardian Interface	12
4.4	Host Interface	12
4.5	Power Supply Interface	14
4.5.1	V _{CC} Undervoltage Detection	14
4.5.2	V _{IO} Undervoltage Detection	14
4.5.3	Power-up and Power-down	15
4.6	Remote Wake-up	17
4.6.1	Bus Wake-up Patterns	17
4.6.2	Wake-up by Payload	18
4.7	Fail Safe Functions and Flags	19
4.7.1	Overtemperature detection	19
4.7.2	Bus Error Detector	19
4.7.2.1	RxD-TxD Compare	20
4.7.2.2	Bus Overcurrent	20
4.7.3	Transmitter Time-Out	20
4.7.4	V _{IO} Undervoltage-flag	20
4.7.5	SPI-error flag	20
4.7.6	Error flag	20
4.7.7	Mode Flags	20
4.8	SPI Interface and Status Register	21
4.8.1	Read-out procedure	22
5	General Product Characteristics	23
5.1	Absolute Maximum Ratings	23
5.2	Functional Range	24
5.3	Thermal Resistance	24
6	Electrical Characteristics	25
6.1	Functional Device Characteristics	25
6.2	Diagrams	34
7	Application Information	37
7.1	ESD Robustness according to IEC61000-4-2	37
7.2	Bus Interface Simulation Model Parameter	37
7.3	Application Example	38



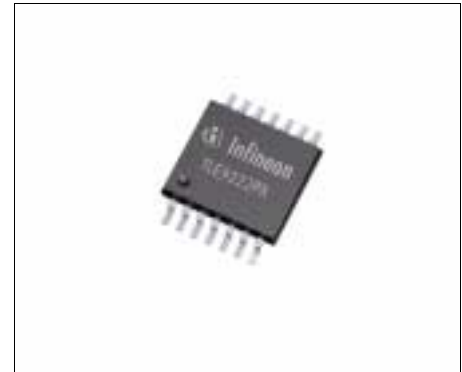
7.4	Implementation of ECU Functional Safety concepts	39
7.5	Minimizing ECU current consumption through BD_Standby mode	40
7.6	Further Application Information	40
8	Package Outlines	41
9	Revision History	42



1 Overview

Features

- Compliant with the FlexRay Electrical Physical Layer Specification version 3.0.1 and ISO 17458-4
- Optimized for time triggered in-vehicle networks with data transmission rates from 1 Mbit/s up to 10 Mbit/s
- Supports minimum bit times down to 60 ns
- Automatic voltage adaptation on the digital interface pins
- Bus failure protection and error detection
- Very high ESD robustness; ± 8 kV according to IEC61000-4-2
- Optimized for high Electromagnetic Compatibility (EMC); Very low emission and high immunity to interference
- Green Product (RoHS compliant)
- AEC Qualified



PG-TSSOP-14

Modes of Operation and Wake-up Features

- Low power standby operation mode with very low quiescent current consumption
- Remote wake-up detection via wake-up patterns and a dedicated wake-up frame

Protection and Diagnostic

- Short-circuit protection on the bus pins
- Overtemperature protection
- Undervoltage monitoring of the V_{CC} power supply and the V_{IO} logic voltage level reference
- Error and wake-up indication on the ERRN output
- Status register for detailed diagnostic information through a simplified SPI interface
- Integrated Bus Guardian interface with enhanced safety feedback path
- Bus pins high impedance when device unpowered

Description

The TLE9222 FlexRay transceiver is designed for data transmission rates from 1 Mbit/s up to 10 Mbit/s according to the FlexRay Electrical Physical Layer Specification 3.0.1. The Bus Driver (BD) realizes the physical interface between a FlexRay node and the communication channel. It provides differential transmit and receive capability to the bus, allowing the node bidirectional time-multiplexed binary data stream transfer. In

Type	Package	Marking
TLE9222PX	PG-TSSOP-14	9222

Overview

In addition to transmit and receive functions, the TLE9222 provides low power standby operation, supply voltage monitoring (undervoltage detection) as well as bus failure detection and represents an ESD-protection barrier between the bus and the ECU.

The TLE9222 supports the following FlexRay functional classes:

- Functional class “Bus driver - bus guardian interface”
- Functional class “Bus driver logic level adaptation”
- Functional class “Bus driver remote wakeup”
- Functional class “Bus driver increased voltage amplitude transmitter”

In BD_Standby mode the quiescent current is decreased to a minimal level while still being able to detect wake-up requests on the bus.

Fail Safe features, like failure detection and the power supply monitoring, combined with an easy accessible status register support requirements for safety related applications with extended diagnostic features.

The TLE9222 is internally protected against transients on the bus pins, BP and BM. This makes it possible to use the TLE9222 for implementing ECUs without additional external bus protection circuitry while fulfilling ESD and ISO pulse requirements of car manufacturers. With its excellent EMC performance the TLE9222 provides a very high immunity against RF disturbances over a broad frequency range and transmits only a minimal level of electromagnetic emission onto the bus.

The TLE9222 is integrated in a RoHS compliant PG-TSSOP-14 package. Using the latest Infineon Smart Power Technology it is especially tailored to withstand the harsh conditions of the automotive environment and qualification according to the AEC-Q100 standard.

Block Diagram

2 Block Diagram

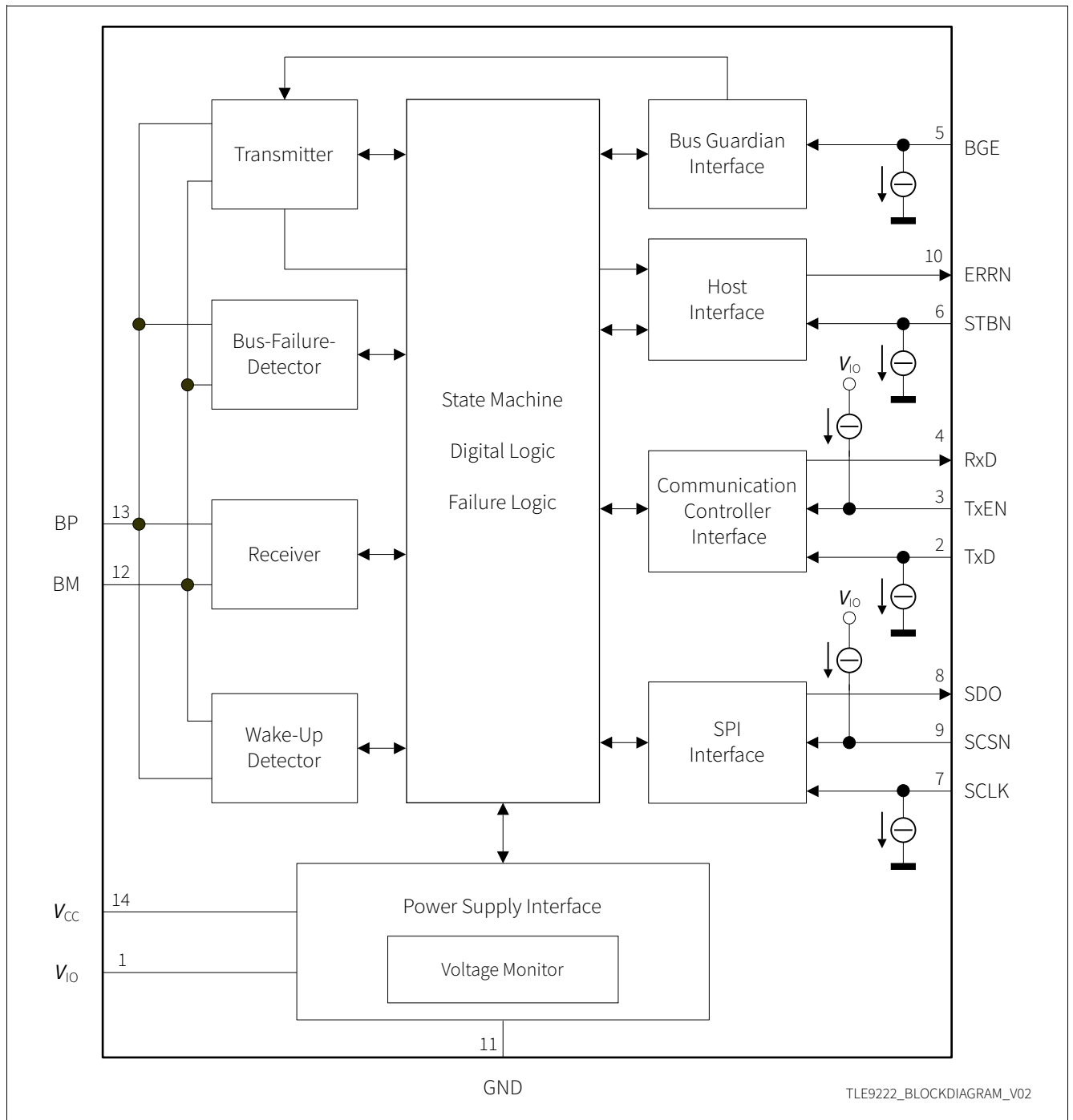


Figure 1 Block diagram

Pin Configuration

3 Pin Configuration

3.1 Pin Assignment

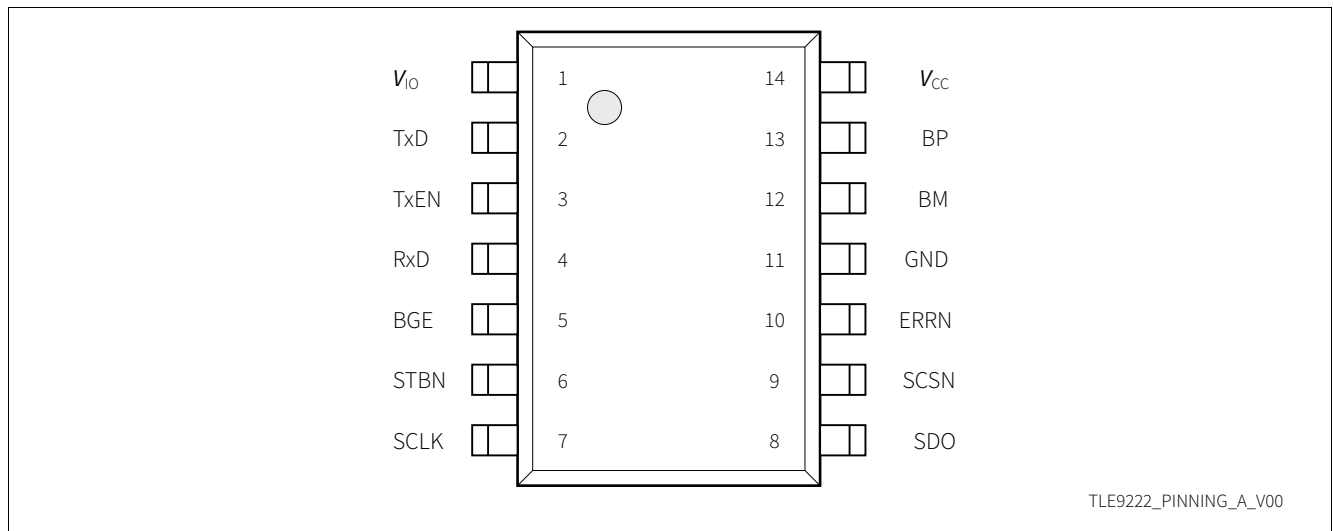


Figure 2 Pin configuration

3.2 Pin Definitions and Functions

Pin	Symbol	Function
1	V_{IO}	Digital Reference Voltage; Digital reference voltage supply for the logic input and output pins, 100 nF decoupling capacitor to GND recommended.
2	TxD	Transmit Data Input; Integrated pull-down to GND.
3	TxEN	Transmitter Enable Not Input; Logical “low” to enable the transmitter output stage, Integrated pull-up to V_{IO} .
4	RxD	Receive Data Output; Output voltage level adapted to the voltage level of V_{IO} .
5	BGE	Bus Guardian Enable Input; Logical “high” to enable the transceiver output stage, Integrated pull-down to GND.
6	STBN	Standby Not Mode Control Input; Digital input for mode selection, logical “high” for BD_Normal mode, Integrated pull-down to GND.
7	SCLK	SPI Clock Input; Integrated pull-down to GND.

Pin Configuration

Pin	Symbol	Function
8	SDO	SPI Data Output;
9	SCSN	SPI Chip Select Not Input; Integrated pull-up to V_{IO} .
10	ERRN	Error Not Diagnosis Output; Logical "low" in failure cases or when wake-up pattern detected.
11	GND	Ground;
12	BM	Bus Line Minus; Negative input / output terminal of the FlexRay bus.
13	BP	Bus Line Plus; Positive input / output terminal of the FlexRay bus.
14	V_{CC}	Supply Voltage; Transceiver 5V supply voltage, 100 nF decoupling capacitors to GND recommended.

Functional Description

4 Functional Description

The TLE9222 realizes the physical interface between the FlexRay node and the communication channel. Differential transmit and receive capability to the FlexRay bus is provided, allowing the node bidirectional time multiplexed binary data stream transfer.

The differential bus voltage is measured between two signal lines, denoted BP (Bus Plus) and BM (Bus Minus), defined as $u_{BUS} = u_{BP} - u_{BM}$. Three different bus states are defined for the FlexRay bus; Idle, Data_0 and Data_1. For the Idle state no differential voltage is driven to BP or to BM. The common mode bus biasing level will depend on the operation mode of all nodes on the bus. For the Data_1 state a positive differential voltage is driven between BP and BM, whereas for the Data_0 state a negative differential voltage is driven between BP and BM.

4.1 Operation Modes

The TLE9222 supports two functional operation modes, BD_Normal mode and BD_Standby mode. In addition, the BD_Off condition describes the behavior of the TLE9222 when unpowered.

Mode transitions of the TLE9222 are triggered by host commands, undervoltage events and during power-up / -down, see [Figure 3](#) and [Table 1](#).

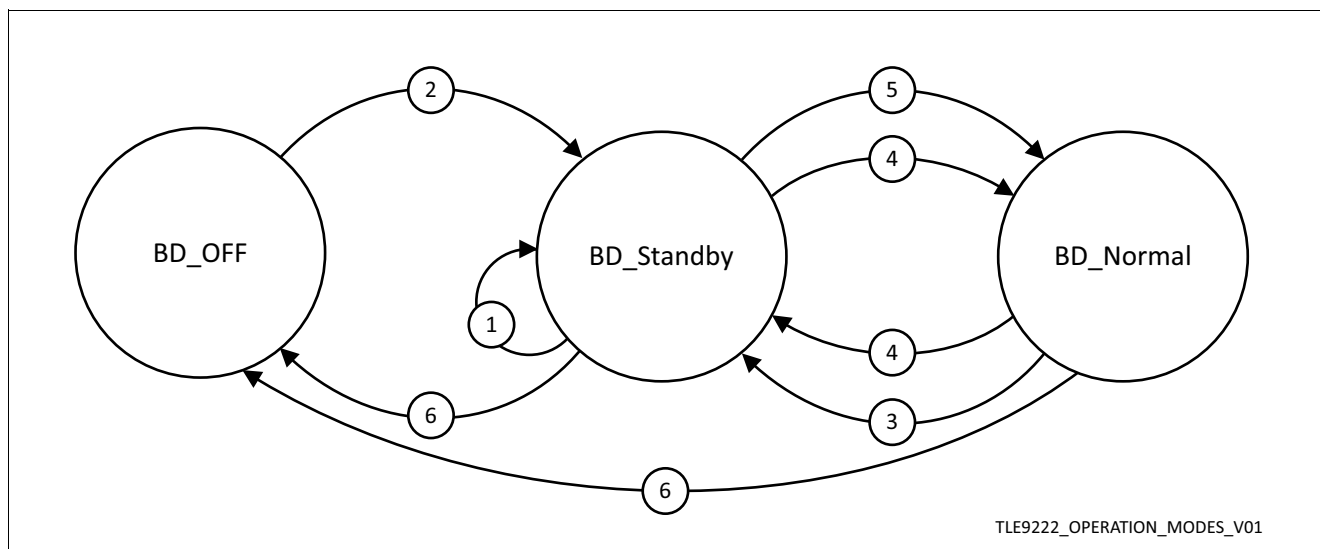


Figure 3 Operation mode state diagram

Table 1 Operation mode transitions

Nr	Reason for transition	Comment
1	Wake-up detection	–
2	Power-on detection	Supply voltage sufficiently supplied via V_{CC} after being unpowered.
3	Undervoltage detection	After V_{CC} and / or V_{IO} undervoltage detection, BD_Standby mode is forced.
4	Host command	Triggered by host command.
5	Undervoltage recovery	Undervoltage recovery while host command requests BD_Normal mode.
6	Power-off	Supply voltage falls below the power-on threshold.

Functional Description

4.1.1 BD_Normal Mode

In BD_Normal mode all interfaces and functions of the TLE9222 are in operating condition. The communication controller interface is fully active; the RxD output reflects the data on the bus pins, the TxD drives the data to the transmitter and the TxEN input enables or disables the transmitter. When the transmitter is activated, fail safe functionality like the transmitter time-out, overtemperature detection and bus error detection are also enabled. The bus biasing is connected to $V_{CC} / 2$ via the internal common mode resistors. With the RxEN flag in the status register the bus states idle or active can be read out through the SPI interface.

The host interface is active and fully functional, as well as status register read-out on the SPI interface. Through the bus guardian interface, the transmitter can be activated or disabled.

The wake-up detector is active, but received wake-up information is not flagged while in BD_Normal mode.

The power supply interface including voltage monitor on both V_{CC} and V_{IO} is active. Undervoltage events are signalled on the ERRN output and in the status register, and trigger a mode transition to BD_Standby mode. BD_Normal mode can only be entered with a valid host command while both power supplies are within their operational range.

4.1.2 BD_Standby Mode

After power-up the TLE9222 automatically enters BD_Standby, an idle mode with optimized low power consumption. In BD_Standby mode neither sending nor receiving data is possible, both the transmitter and the receiver are disabled. The bus biasing is connected to GND through the internal common mode resistors.

The communication controller interface is inactive. The TxD and the TxEN inputs are not functional. The RxD output is used for signalling wake-up or error information, depending on the host command. The host interface is active and fully functional, as well as status register read-out on the SPI interface.

The bus guardian interface is inactive and detection of bus transmission through the RxEN flag in the status register is not possible. The bus failure detector is not active, no bus failure can be detected.

The wake-up detector is active and signals wake-up requests on the ERRN and RxD outputs while the host command is BD_Standby mode.

The power supply interface with voltage monitoring on both V_{CC} and V_{IO} is active. If the TLE9222 is forced to BD_Standby mode because of undervoltage events while the host command is BD_Normal mode, this is signalled on the ERRN output. Additionally, the information is stored in the status register.

4.1.3 BD_Off Condition

The TLE9222 enters the BD_Off condition when the V_{CC} power supply drops below the $uBDP DV_{CC}$ power-on-reset threshold. In this state the transmitter and the receiver are turned off, the wake-up function is not operational, the RxD and ERRN outputs are “low” and the SDO output is in high impedance state. If the V_{IO} reference supply is available, the logical inputs are set to their default states as given in [Table 2](#).

Table 2 Logic inputs when unconnected / default states

Input Signal	Default State
TxD	Low
TxEN	High
STBN	Low
BGE	Low

Functional Description

Table 2 Logic inputs when unconnected / default states

Input Signal	Default State
SCSN	High
SCLK	Low

4.2 Communication Controller Interface

The communication controller interface is the link between the TLE9222 and the FlexRay communication controller, comprising three digital signals:

- TxEN (Transmit Data Enable Not) input
- TxD (Transmit Data) input
- RxD (Receive Data) output

The logical I/O levels of all three digital pins are adapted to the V_{IO} digital reference voltage supply.

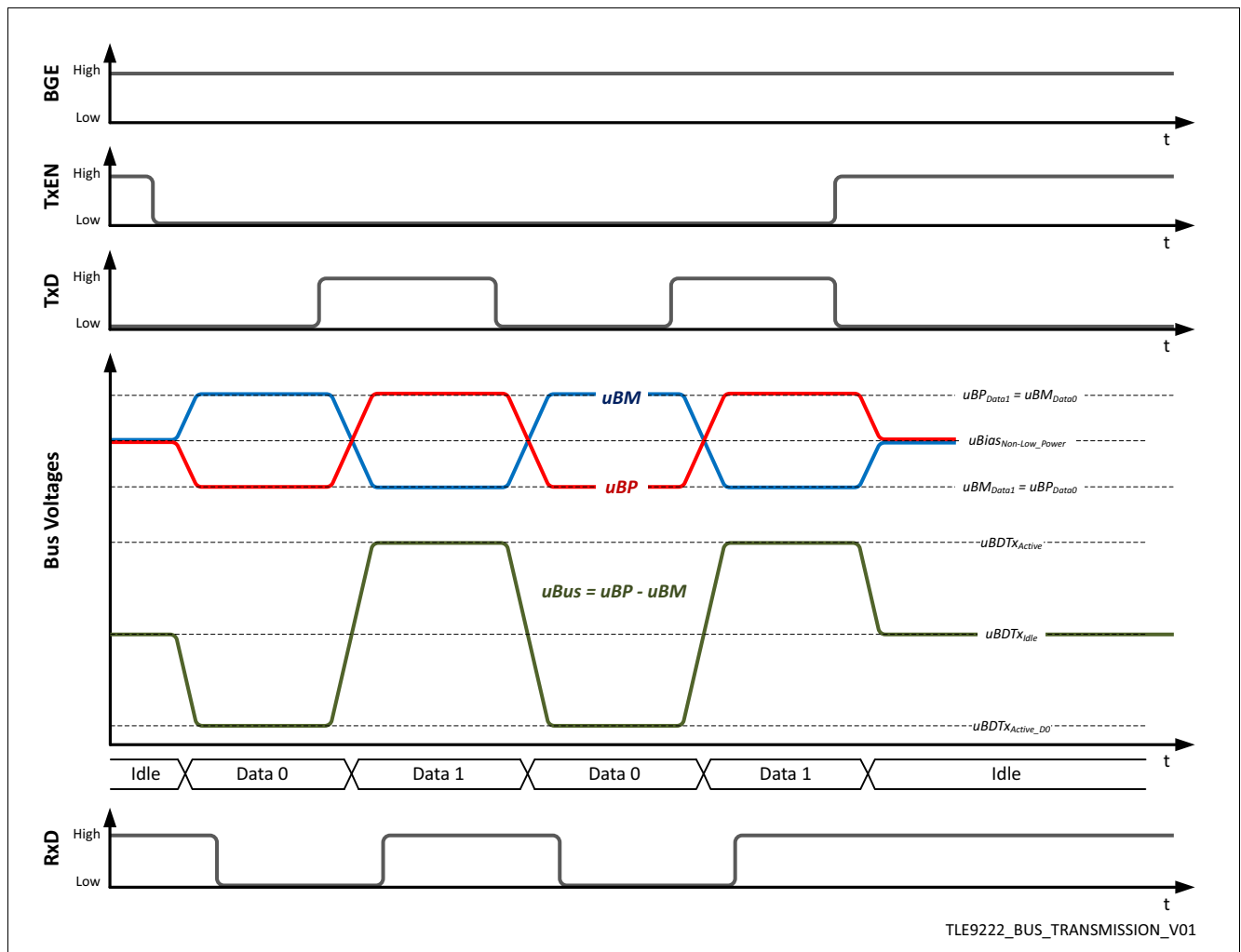


Figure 4 FlexRay physical layer bus signals

The communication controller interface drives the serial digital data stream available on the TxD input to the FlexRay bus via the transmitter. Simultaneously the receiver of the TLE9222 monitors the data on the FlexRay bus and transfers the data to a serial digital data stream back to the RxD output. A logical “low” signal on the

Functional Description

TxD input drives a Data_0 signal on the FlexRay bus; a Data_0 signal on the FlexRay bus results in a logical “low” signal on the RxD output. Vice versa a logical “high” on TxD drives a Data_1 signal on the FlexRay bus and results in a logical “high” signal on the RxD output. The RxD output is also used to signal wake-up events while the transceiver is in BD_Standby mode.

The TxEN input is only functional in BD_Normal mode and requires a transition from “high” to “low” for initiating bus transmissions. After TxEN has been set “low” while the BGE input is “high”, a “low” level on the TxD input enables the transmitter.

For avoiding unintentional blocking of the FlexRay bus in case of failures, the transmitter is protected with a time-out function. In case a time-out occurs, the transmitter will automatically be disabled and the error will be signalled by the ERRN output and in the status register. A more detailed description of this fail safe function is given in [Chapter 4.7.3](#).

4.3 Bus Guardian Interface

The bus guardian interface allows an external supervision device to immediately interrupt any bus transmission of the TLE9222. A logical “low” signal on the BGE input disables the transmitter of the TLE9222 while operating in BD_Normal mode, regardless of the signals on the TxD and TxEN inputs.

For increasing the ECU system safety level, an enhanced redundant feedback path has been implemented for the bus guardian interface. A monitoring circuit directly at the transmitter output stages provides reliable feedback by setting the ERRN output “low” and indication with the BGE flag in the status register after the transmitter has been disabled through the Bus Guardian interface.

The logical I/O level of the BGE input is adapted to the digital reference voltage level uV_{IO} . Together with the TxEN input, the BGE input is monitored for the transmitter time-out function (see [Chapter 4.7.3](#)).

Additionally, the status register includes the RxEN (Receive Enable NOT) flag that indicates activity (Data_0 or Data_1) on the FlexRay bus. This detection is only active in BD_Normal Mode. The RxEN bit can be read out with the SPI Interface as described in [Chapter 4.8](#).

4.4 Host Interface

The host interface enables the host to control the operation mode of the TLE9222 and to flag status information. The host interface is implemented using *hard wired signals, Option A* according to the FlexRay EPL Spec. 3.0.1.

Table 3 Host Command

STBN	Resulting operation mode
High	BD_Normal
Low	BD_Standby

The STBN (Standby Not) input controls the operation mode of the TLE9222. Unless the TLE9222 is being forced to BD_Standby mode because of undervoltage events, the host command will set operation mode as given in [Table 3](#). Mode change by host command is completed within the time $dB_{D_{ModeChange}}$ after the host command is applied. Voltage spikes on the STBN input that are shorter than $dB_{D_{LogicFilter}}$ are filtered out and ignored.

Functional Description

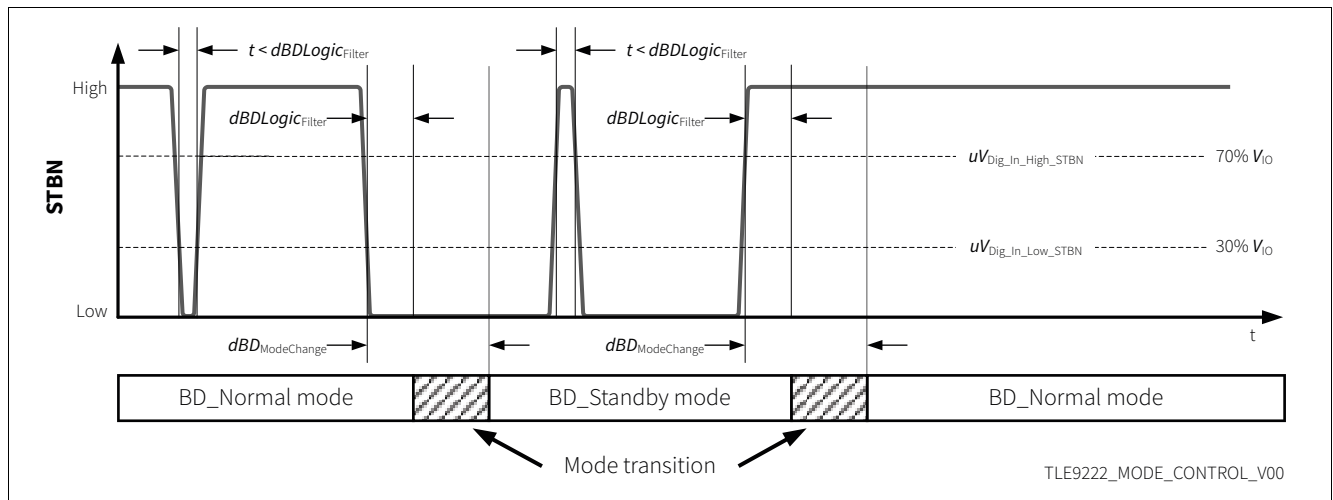


Figure 5 Mode control with the STBN input

The ERRN output is used to signal events detected by the TLE9222 to the host controller. Depending on the provided host command, the ERRN output indicates errors or wake-up events, see [Table 4](#). The TLE9222 reacts on and signals these events on the ERRN output within the time $dReactionTime_{ERRN}$. Detailed information about the detected events as given in [Table 4](#) can be read out from the status register with the SPI interface as described in [Chapter 4.8](#).

Table 4 Signalling on the ERRN and RxD pins

STBN	ERRN	RxD	Cause / Comment	Effect
BD_Normal mode				
High	High	High / Low ¹⁾	Default condition for BD_Normal mode	–
High	Low	High / Low ¹⁾	Bus error detected	–
			Transmitter time-out detected	Transmitter disabled
			Overtemperature event detected	Transmitter disabled
			BGE input “low”	Transmitter disabled
			SPI error detected	–
BD_Standby mode				
Low	High	High	Default condition for BD_Standby mode	–
Low	Low	Low	Bus wake-up detected	–
High	Low	High	V_{CC} undervoltage detected	Forced BD_Standby mode
X ²⁾	Low	Low	V_{IO} undervoltage detected	Forced BD_Standby mode, logic inputs follow default states (see Table 2) SDO “high impedance”
BD_OFF condition				
X ²⁾	Low	Low	uV_{CC} below $uBDPDV_{CC}$	–

1) Depending on bus state; RxD “low” when Data_0 is detected, RxD “high” when Data_1 is detected or when bus is Idle

2) X = “Don’t care”

Functional Description

A “low” output level on the ERRN pin is latched. To reset the ERRN event and the status register either a correct read-out of the status register or a mode change by the host command is required, given that the error condition has been resolved.

4.5 Power Supply Interface

The TLE9222 is powered by the V_{CC} pin which shall be connected to a voltage supply with nominal 5 V. Additionally, the TLE9222 provides the V_{IO} reference voltage pin for all digital inputs and outputs. The voltages at the V_{CC} and V_{IO} pins are monitored for detection of undervoltage events.

4.5.1 V_{CC} Undervoltage Detection

The TLE9222 detects undervoltage events on the V_{CC} pin if the voltage uV_{CC} falls below the undervoltage detection threshold $uBDUVV_{CC}$ for a time $t > dBDUVV_{CC_blk}$. Upon detection the V_{CC} -undervoltage flag and the error flag are set. In case the TLE9222 is in BD_Normal mode, the transmitter will be disabled and the ERRN output will go “low” after the time $dReactionTime_{ERRN}$. After the time $dBDUVV_{CC}$ the TLE9222 will force a transition to BD_Standby, regardless of the host command (see [Figure 6](#)).

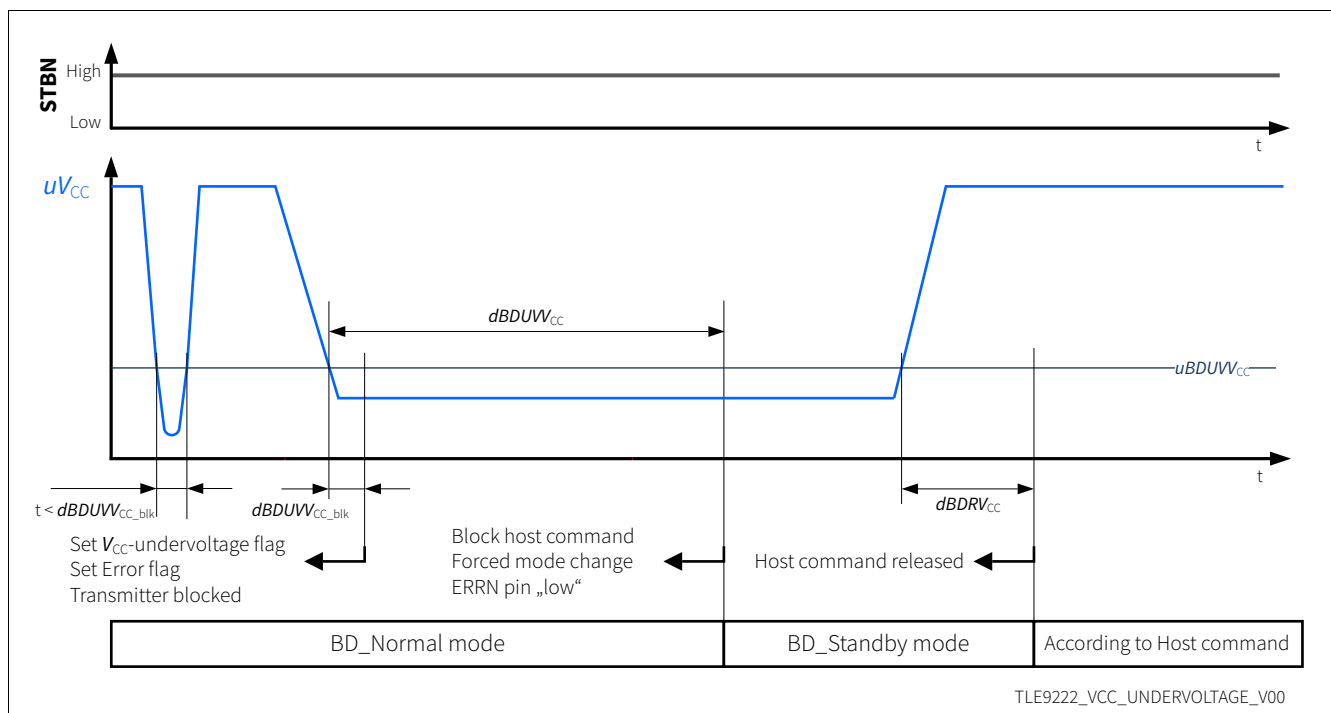


Figure 6 V_{CC} undervoltage detection

The TLE9222 recovers from a V_{CC} undervoltage event after the time $t > dBDRV_{CC}$ following the voltage uV_{CC} rise above the undervoltage detection threshold $uBDUVV_{CC}$. This will release the host command and change operation mode accordingly.

4.5.2 V_{IO} Undervoltage Detection

The V_{IO} undervoltage detection is similar to that on the V_{CC} supply. Undervoltage events on the V_{IO} pin are detected if the voltage uV_{IO} falls below the undervoltage detection threshold uUV_{IO} for a time $t > dBDUVV_{IO_blk}$. Upon detection the V_{IO} -undervoltage flag and the error flag are set. While an undervoltage event is present on the V_{IO} pin, the reference threshold levels of all digital input and output pins are invalid. Therefore, the

Functional Description

TLE9222 blocks the host interface, communication controller interface, SPI interface and the bus guardian interface. The digital outputs RxD and ERRN are set “low” and all digital input pins follow their default levels (see **Table 2**). The SDO output is set to high impedance state. After the time $dBDUV_{I_0}$ the TLE9222 will force a transition to BD_Standby mode.

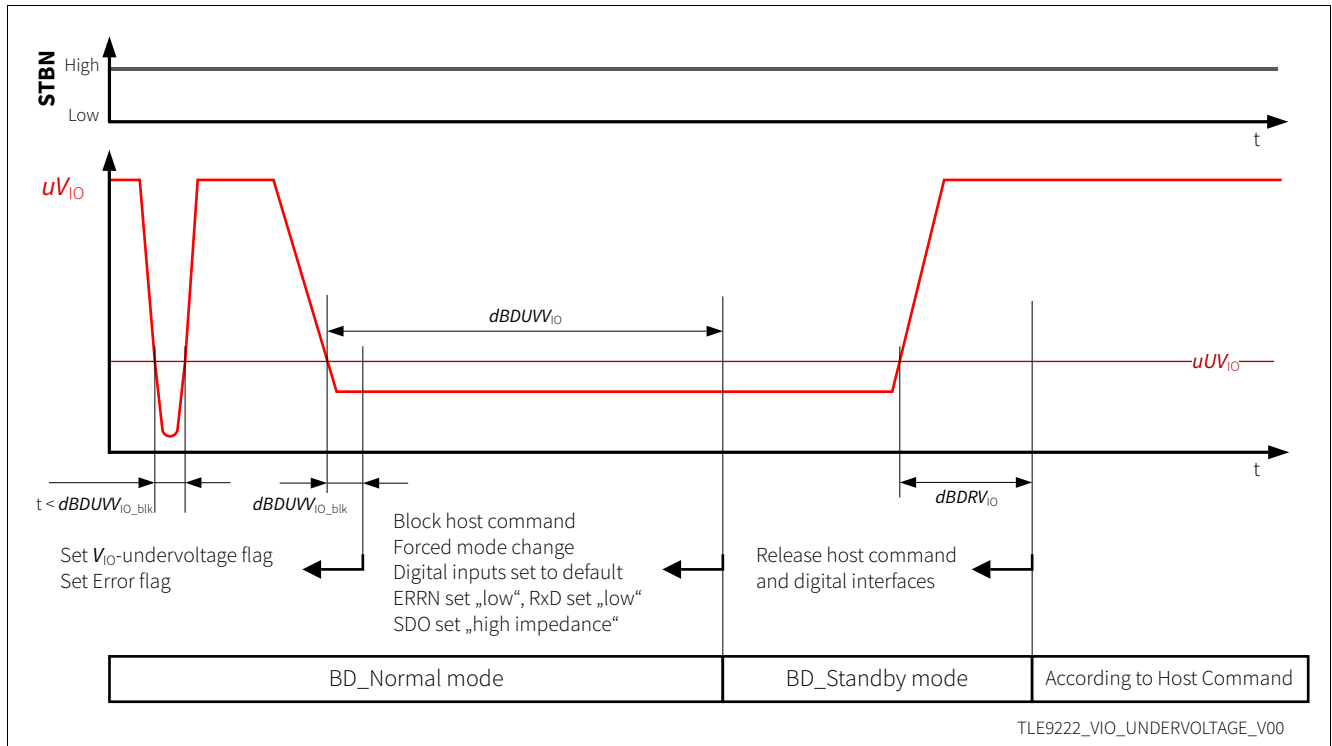


Figure 7 V_{I_0} undervoltage detection

The TLE9222 will recover from a V_{I_0} undervoltage event after the time $t > dBDRV_{I_0}$ following the voltage uV_{I_0} rise above the undervoltage detection threshold uUV_{I_0} . This will release the SPI interface and host command, and change mode accordingly (see **Figure 7**).

4.5.3 Power-up and Power-down

The TLE9222 will remain in BD_Off condition as long as the voltage on the V_{CC} supply pin, uV_{CC} , is below the power-down threshold $uBDPDV_{CC}$. When uV_{CC} is ramped up higher than $uBDPDV_{CC}$ the TLE9222 powers up and begins initialization of the BD_Standby mode within the time dBD_{Power} . After both voltages uV_{CC} and uV_{I_0} have risen above their respective undervoltage detection thresholds ($uBDUV_{CC}$ and uUV_{I_0} , respectively), the digital interfaces will be released and the full functionality of the device will be available. The power-on event can be identified with the corresponding flag in the status register and mode change according to the host command will then be initiated (see **Figure 8**).

Functional Description

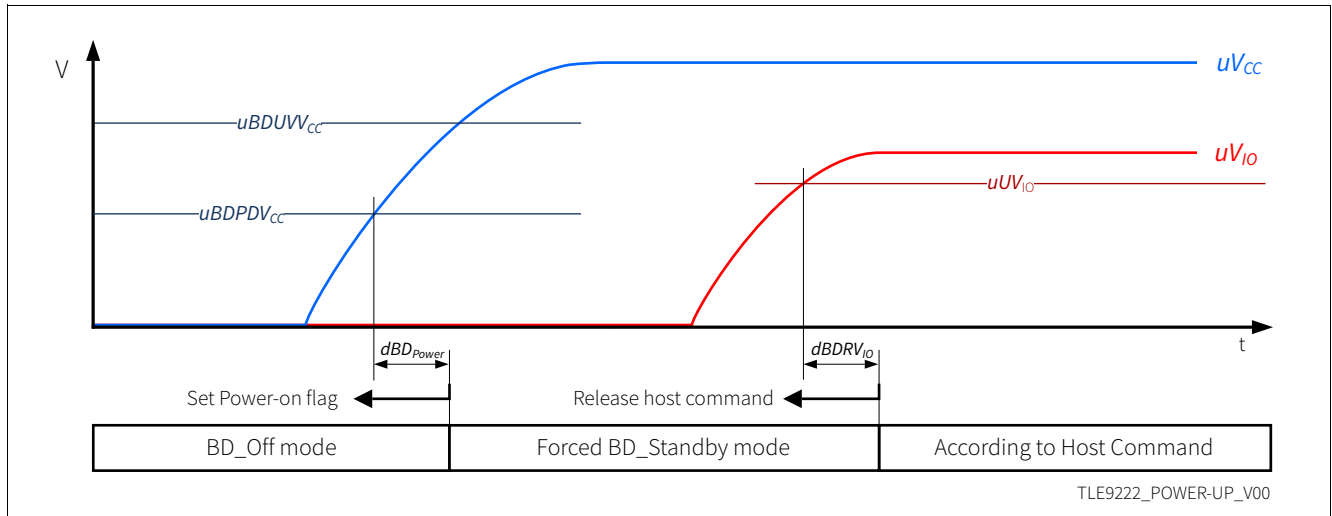


Figure 8 Power-up behavior

The power-down sequence of the TLE9222 is shown in **Figure 9**. As the voltage at the V_{CC} supply pin, uV_{CC} , falls below the undervoltage threshold the V_{CC} -undervoltage flag and the error flag are set. After the detection time for V_{CC} undervoltage $dBDUVCc$ the TLE9222 blocks the host command and automatically enters BD_Standby mode.

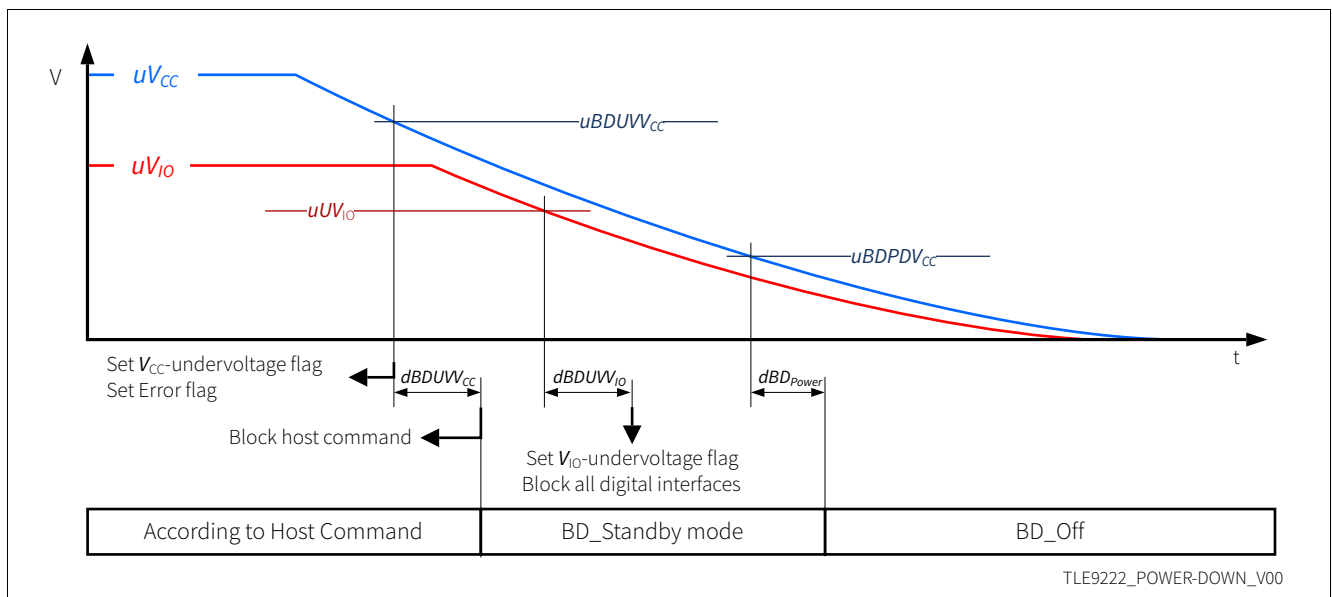


Figure 9 Power-down behavior

While the TLE9222 is being powered down, the behavior on the digital interface level shift reference pin V_{IO} is very similar to the V_{CC} supply pin. As uV_{IO} falls below the undervoltage threshold the undervoltage timer is started and the V_{IO} -undervoltage flag is set. If V_{CC} is not already in undervoltage condition, the error flag is also set. After the detection time for V_{IO} undervoltage, $dBDUVCc$, the TLE9222 blocks the host command (if not already blocked because of V_{CC} undervoltage) and all digital interfaces and enters BD_Standby mode.

When the voltage at the V_{CC} supply pin, uV_{CC} , falls below the power-on threshold $uBDPDCc$ the TLE9222 enters BD_Off condition within the time dBD_{Power} .

Functional Description

4.6 Remote Wake-up

The TLE9222 detects and signals a remote wake-up request after correct reception of a bus wake-up pattern or wake-up payload in a FlexRay data frame while operating in BD_Standby mode. When the valid wake-up pattern or wake-up payload is detected, the TLE9222 signals the request with the remote wake-up flag in the status register and on the RxD and ERRN outputs within the time $dBDWakeupReaction_{Remote}$.

The wake-up detector is also active in BD_Normal mode, but wake-up requests are only flagged when the TLE9222 is in BD_Standby mode.

4.6.1 Bus Wake-up Patterns

A wake-up pattern consists of at least two wake-up symbols. A wake-up symbol on the FlexRay bus is defined as either a phase of Data_0 followed by a phase of Idle, or alternatively as a phase of Data_0 followed by a phase of Data_1. A valid remote wake-up event is detected with the reception of at least two consecutive wake-up symbols on the bus within the time $dWU_{Timeout}$ (see Figure 10 and Figure 11).

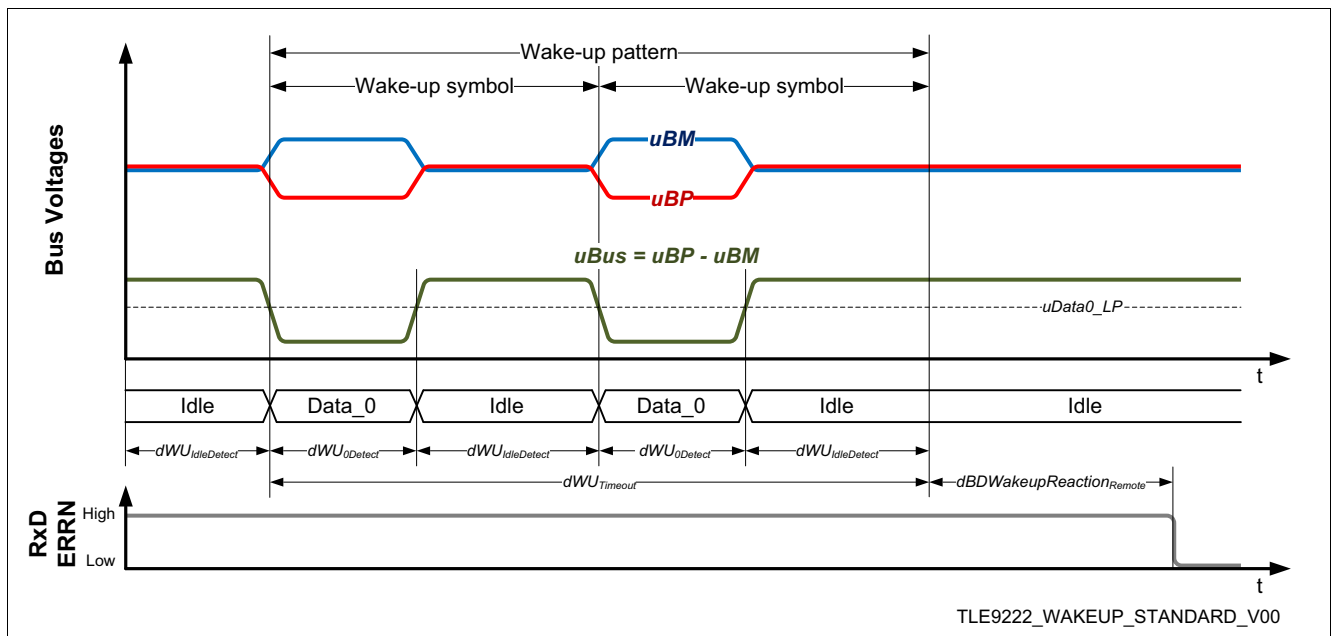


Figure 10 Standard wake-up pattern

The Data_0 phases have to be longer than the time $dWU_{DataDetect}$ while the Idle or Data_1 (alternative wake-up pattern) phases have to be longer than the time $dWU_{IdleDetect}$. The TLE9222 detects and signals both the standard and the alternative wake-up patterns without any behavioral differences.

Functional Description

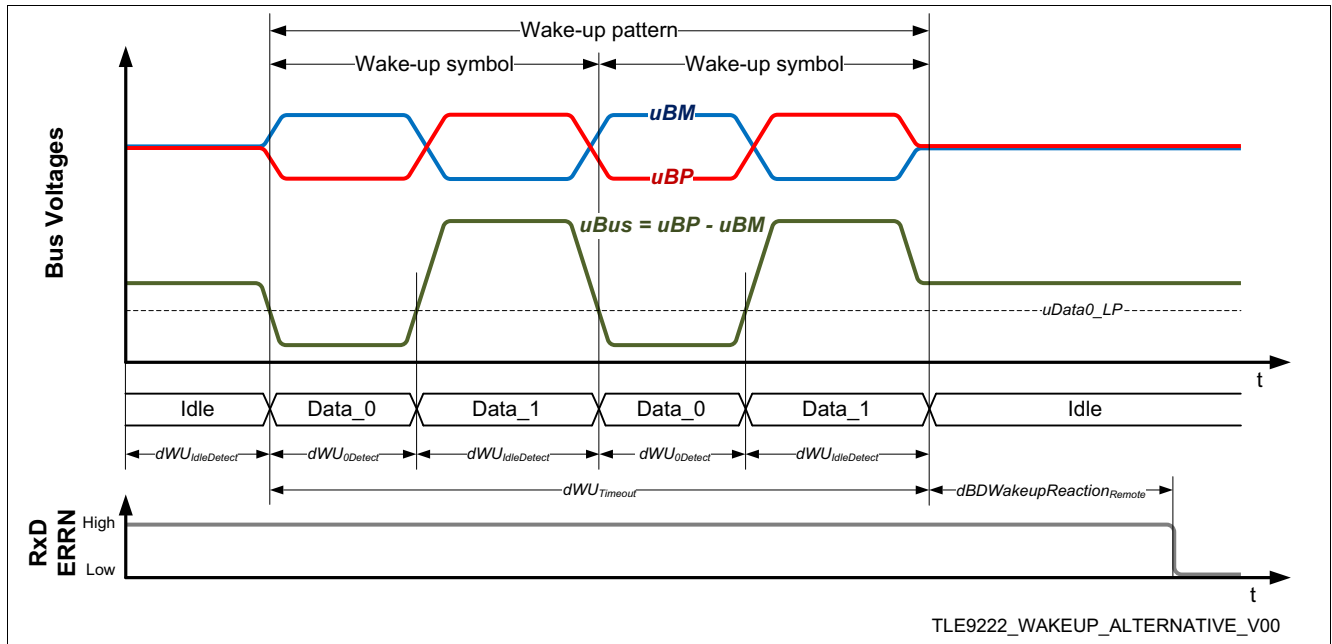


Figure 11 Alternative wake-up pattern

4.6.2 Wake-up by Payload

In addition to wake-up detection by wake-up patterns, the TLE9222 also supports wake-up requests by a specific payload within the data field of a FlexRay communication frame with data transmission rate of 10 Mbit/s.

A dedicated Byte Start Sequence (BSS) is transmitted before each byte of the payload within the FlexRay data frame. The BSS consists of one “high” bit followed by one “low” bit. For transmitting a “Data_0” byte on the FlexRay bus, the FlexRay controller sends 10 bits, the “high” bit and the “low” bit as part of the BSS followed by the eight “low” data bits (HL= BSS; LLLLLLLL= “Data_0”). For sending a “Data_1” byte the FlexRay controller sends the “high” bit and the “low” bit, followed by the eight consecutive “high” data bits (HL= BSS; HHHHHHHH= “Data_1”) (see Figure 12).

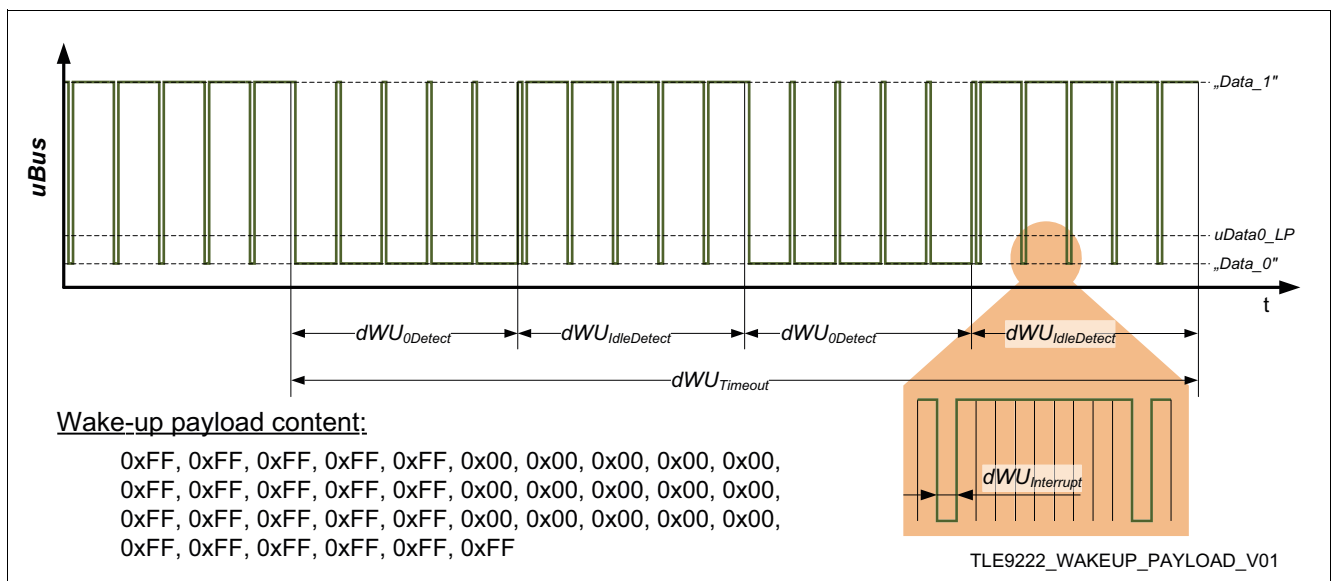


Figure 12 Wake-up by payload

Functional Description

4.7 Fail Safe Functions and Flags

In addition to power supply undervoltage detection, the TLE9222 provides several functions for detection of local or remote failures with corresponding status flags. These errors are signalled with the ERRN output and can be read out from the status register. When local errors are detected, the TLE9222 initiates fail safe procedures for device self protection and prevention of communication channel interruption.

4.7.1 Overtemperature detection

The transmitter of the TLE9222 is protected against overtemperature events when active in BD_Normal mode. If the junction temperature rises above the $T_{J(\text{Warning})}$ threshold the temperature-warning flag in the status register is set. If the junction temperature continues to rise and exceeds the $T_{J(\text{Shut_Down})}$ threshold, the transmitter will be disabled and the overtemperature event will be flagged by the temperature-high flag in the status register and signalled with the ERRN output.

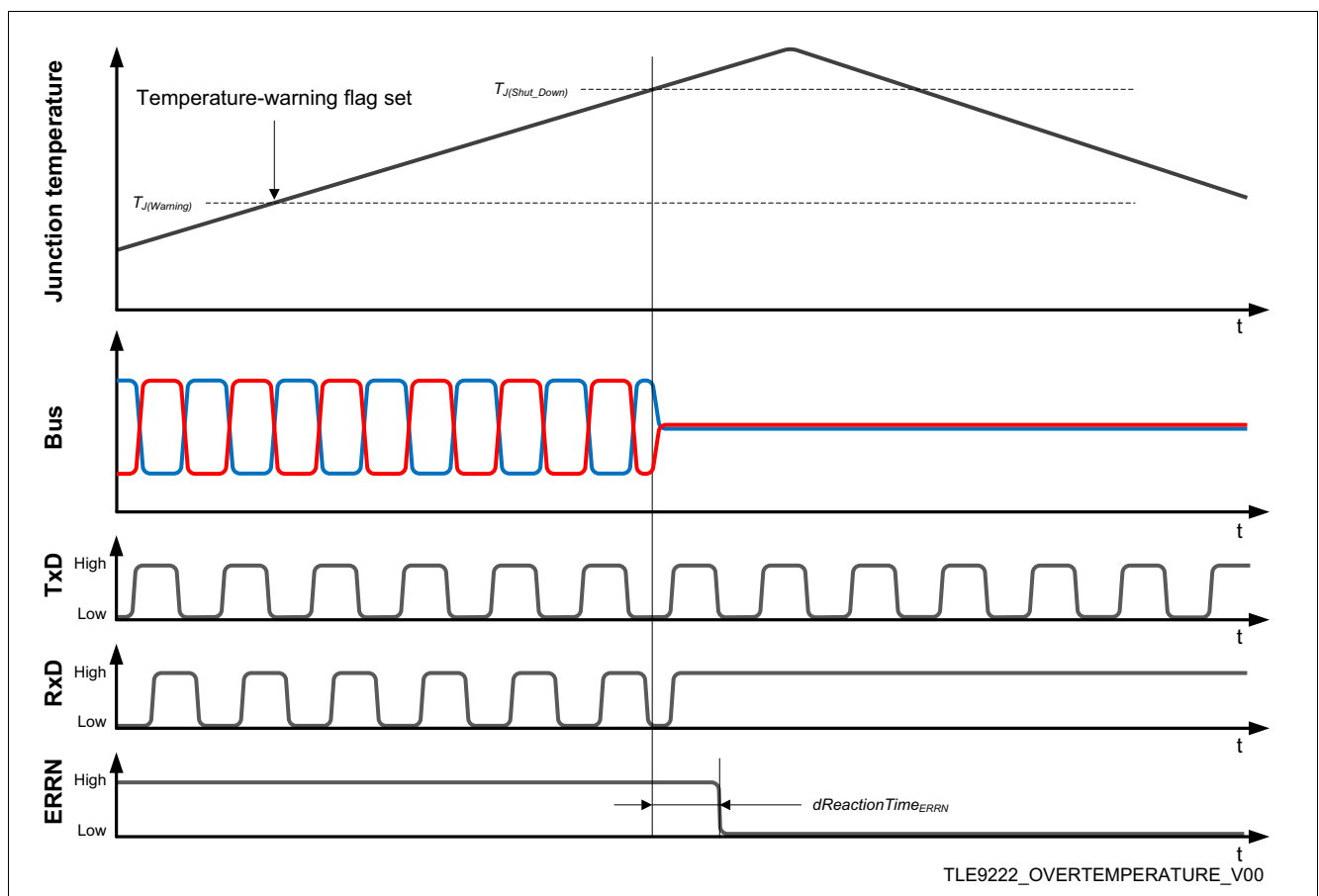


Figure 13 Overtemperature protection

4.7.2 Bus Error Detector

The bus error detector monitors the FlexRay bus for identifying external failures which may lead to corrupt data transmission and reception. With the RxD-TxD compare function and the bus overcurrent monitoring, bus errors are detected and signalled with the bus error flag. The bus error detector is only enabled in BD_Normal mode while the transmitter is active.

Functional Description

4.7.2.1 RxD-TxD Compare

When the TLE9222 transmits data on the bus (TxEN “low” and BGE “high”), the digital input data on TxD is compared with the received data on the RxD output. If the data is not identical, a failure condition is identified. Both the positive and the negative edges on the TxD input signal triggers an internal comparator to compare the TxD signal with the RxD signal. The results are stored in an internal error counter. When the internal error counter exceeds 10 reported comparison failures, the bus error flag will be set. The error counter is reset when the transmitter is deactivated.

4.7.2.2 Bus Overcurrent

The BP and BM bus pins have implemented current sensors for detection of overcurrent conditions in the direction in or out of the pins. Detection of overcurrent is the typical signature of a short circuit of one of the bus lines to the ground or a supply line.

4.7.3 Transmitter Time-Out

For avoiding unintentional blocking of the FlexRay bus in case of e.g. a malfunctioning microcontroller or short circuits on the PCB, the transmitter is protected with a time-out function. When the transmitter is activated for bus transmission while in BD_Normal mode, with a “low” signal on TxEN and “high” on BGE, a timer is started. In case a time-out occurs, the transmitter will automatically be disabled and the failure will be signaled on the ERRN output and in the status register.

The transmitter timer is reset when the transmitter is deactivated with either TxEN or BGE.

4.7.4 V_{IO} Undervoltage-flag

During V_{IO} undervoltage events, the SPI register is blocked and can not be read out. After undervoltage recovery, depending on host command and the status of other register flags, the V_{IO} -undervoltage flag may or may not be set. Please refer to [Chapter 4.7.6](#).

4.7.5 SPI-error flag

The SPI-error flag is used for indication of incorrect SPI read-out procedure, please find detailed description in [Chapter 4.8.1](#).

4.7.6 Error flag

If any local errors or bus errors are detected, the respective bit in the status register is flagged together with the error flag (bit 12). If the error flag is set, but no other error contributing flags in the status register set, then this indicates that a V_{IO} undervoltage event has occurred in the past but recovery has already taken place.

While the error flag is set and the host command on the STBN input is “high”, the ERRN output is “low”.

4.7.7 Mode Flags

The mode flag in the status register indicates the current operating mode of the TLE9222, regardless of the applied host command. If the TLE9222 is in BD_Standby mode, bit 1 will be “low”. If the current operation mode is BD_Normal, bit 1 will be “high”. The mode flag will only toggle during an operation mode change, i.e. not be reset by SPI register read-out. The mode indication can be beneficial for the host when the TLE9222 is forced to a different mode than requested with the host command during V_{CC} undervoltage events.

Functional Description

4.8 SPI Interface and Status Register

The TLE9222 has a 16-bit SPI interface for reading out the internal status register. The bits in the register reflects detailed flags regarding external events such as wake-up and power-on recognition, detection of errors / warnings and operation mode indication, see [Table 5](#).

Table 5 Bit definition of the status register

Bit	Name	Indication	Comment
Bit 0	Remote wake-up flag	“Low”: Remote wake-up detected	–
		“High”: –	–
Bit 1	Mode flag	”Low”: BD_Standby mode	–
		“High”: BD_Normal mode	–
Bit 2	BGE flag	“Low”: Transmitter disabled by Bus Guardian, BGE input “low” in BD_Normal mode	Error, will trigger Bit 12 → “low”
		“High”: –	–
Bit 3	RxEN flag	“Low”: Bus activity ongoing	Not latched
		“High”: Bus idle	–
Bit 4	Power-on flag	“Low”: Power-on detected	–
		“High”: –	–
Bit 5	Bus-error flag	“Low”: Bus error detected	Error, will trigger Bit 12 → “low”
		“High”: –	–
Bit 6	Temperature-high flag	“Low”: Overtemperature detected	Error, will trigger Bit 12 → “low”
		“High”: –	–
Bit 7	Transmitter time-out flag	“Low”: Transmitter activation time-out	Error, will trigger Bit 12 → “low”
		“High”: –	–
Bit 8	V _{CC} -undervoltage flag	“Low”: V _{CC} Undervoltage detected	Error, will trigger Bit 12 → “low”
		“High”: –	–
Bit 9	V _{IO} -undervoltage flag	“Low”: V _{IO} Undervoltage detected	Error, will trigger Bit 12 → “low”
		“High”: –	–
Bit 10	SPI-error flag	“Low”: SPI error detected	Error, will trigger Bit 12 → “low”
		“High”: –	–
Bit 11	Temperature-warning flag	“Low”: High temperature warning	–
		“High”: –	–
Bit 12	Error flag	“Low”: Error(s) detected	Error, will trigger ERRN output “low” if signal on STBN is “high”
		“High”: No errors detected	–
Bit 13	Reserved	Always ”High”	–
Bit 14	Reserved	Always “Low”	–
Bit 15	Even parity bit	“Low”: Odd parity of Bit 0 to Bit 14	–
		“High”: Even parity of Bit 0 to Bit 14	–

Functional Description

All the flags in the status register are “active low”, the default level is “high”.

The RxEN flag indicates ongoing bus transmission. As soon as the bus state returns to idle, this flag is set “high”.

The wake-up, power-on and error flags and their corresponding status register bits are latched “low”. A mode change by host command or a correct SPI status bit register read-out will reset these flags, given that the error condition has been resolved.

4.8.1 Read-out procedure

The SPI interface of the TLE9222 is enabled by the SCSN (SPI Chip Select Not) input. While SCSN is “high”, the SDO (SPI Data Output) output is in a high impedance state and clock signals on the SCLK input are ignored. The read-out procedure is initiated with a “low” signal on SCSN, which will cause the SDO output to be set “low” (see [Figure 13](#)). After the time $dSPI_{Lead}$ the status register data can be shifted out on the SDO output synchronized with the rising edge of a clock signal on the SCLK input. With a clock signal period of $dSPI_{Clk}$, the TLE9222 supports SPI data rates in the range 10 kbit/s to 4 Mbit/s. If a transition on SCSN from “high” to “low” is detected while SCLK is “high”, this would be identified as a SPI error.

Within the SCSN period, the time $dSPI_{SCSN_Low}$ while the signal on SCSN is “low”, exactly 16 clock cycles are expected for a correct read-out procedure. Incorrect SPI access, with more or less than 16 SCLK cycles or wrong timing, is protected by the SPI timer. If the read-out time $dSPI_{SCSN_Low}$ expires, the SDO output is set to “high impedance” within the time $dSPI_{SDOZ}$. Additionally the error flag and SPI-error flag in the status register will be set, while the state of all other latched bits are left unchanged.

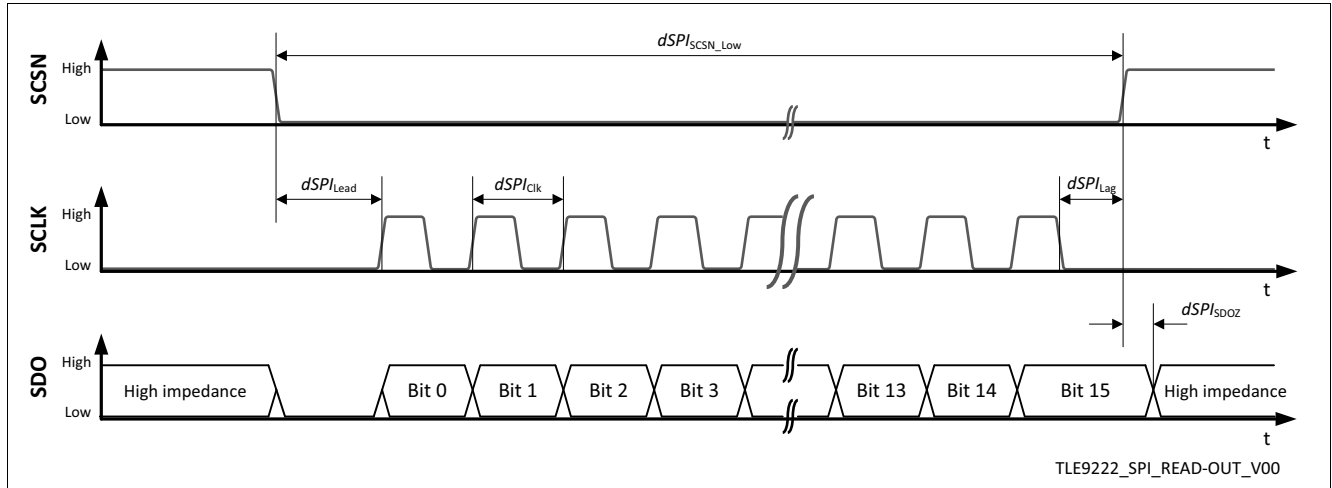


Figure 14 SPI read-out

After a correct SPI read-out process, the information on the ERRN output and the flags in the status register are refreshed. Next SPI read-out can be initiated after SCSN is set “high” for the time $dSPI_{Interframe}$.

The SPI interface is available in both BD_Normal mode and BD_Standby mode, but SPI readout should not occur at the same time as a mode change with the host interface, the time $dBd_{ModeChange}$ must be respected. The SPI register is also blocked during undervoltage conditions on V_{IO} .

While the TLE9222 is set in BD_Standby with host command (pin STBN = “low”) and no wake-up or errors have been detected, the SPI interface requires an enable time of $dSPI_{LeadStbOK}$ from SCSN goes “low” until the first rising edge on the clock signal on the SCLK input can be applied.

General Product Characteristics

5 General Product Characteristics

5.1 Absolute Maximum Ratings

Table 6 Absolute Maximum Ratings ¹⁾

All voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Voltages							
Supply Voltage V_{CC}	uV_{CC}	-0.3	–	6.0	V	–	P_5.1.1
Digital Reference Voltage V_{IO}	uV_{IO}	-0.3	–	6.0	V	–	P_5.1.2
DC voltage on pin BP	uBP	-40	–	40	V	–	P_5.1.3
DC voltage on pin BM	uBM	-40	–	40	V	–	P_5.1.4
DC voltage on logic input pins TxD, TxEN, BGE, STBN, SCSN, SCLK	uV_{Logic_in}	-0.3	–	6.0	V	–	P_5.1.5
DC voltage on logic output pins RxD, ERRN, SDO	uV_{Logic_out}	-0.3	–	$uV_{IO} + 0.3$	V	–	P_5.1.6
Currents							
Output Current on pin RxD	$iRxD$	-40	–	40	mA	–	P_5.1.7
Output Current on pin ERRN	$iERRN$	-40	–	40	mA	–	P_5.1.8
Output Current on pin SDO	$iSDO$	-40	–	40	mA	–	P_5.1.9
Temperature							
Junction Temperature	T_j	-40	–	150	°C	–	P_5.1.10
Storage Temperature	T_{stg}	-55	–	150	°C	–	P_5.1.11
ESD Susceptibility							
ESD Susceptibility to GND on BP and BM	$uESD_{Ext}$	-8	–	8	kV	HBM ²⁾	P_5.1.12
ESD Susceptibility to GND all other pins	$uESD_{Int}$	-2	–	2	kV	HBM ²⁾	P_5.1.13
ESD Susceptibility to GND all pins	$uESD_{CDM}$	-750	–	750	V	CDM ³⁾	P_5.1.14

1) Not subject to production test, specified by design.

2) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS001 (1.5k Ω , 100 pF).

3) ESD susceptibility, Charged Device Model "CDM" ESDA STM5.3.1 or ANSI/ESD S.5.3.1.

Notes

1. Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

General Product Characteristics

5.2 Functional Range

Table 7 Operating Range

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Supply Voltage V_{CC}	uV_{CC}	4.75	–	5.25	V	–	P_5.2.1
Digital Reference Voltage V_{IO}	uV_{IO}	3.0	–	5.25	V	–	P_5.2.2
Junction Temperature	T_J	-40	–	150	°C	–	P_5.2.3

Note: Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the Electrical Characteristics table.

5.3 Thermal Resistance

Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to www.jedec.org.

Table 8 Thermal Resistance ¹⁾

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Thermal Resistance							
Junction to Ambient	R_{thJA}	–	120	–	K/W	²⁾	P_5.3.1
Thermal Shutdown Junction Temperature							
Thermal warning temp.	$T_{J(warning)}$	150	160	170	°C	–	P_5.3.2
Thermal shut-down temp.	$T_{J(Shut_Down)}$	170	180	190	°C	–	P_5.3.3
Thermal shutdown hysteresis	ΔT	–	6	–	K	–	P_5.3.4

1) Not subject to production test, specified by design.

2) Specified R_{thJA} value is according to Jedec JESD51-2,-7 at natural convection on FR4 2s2p board; The TLE9222 (PG-TSSOP-14) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70µm Cu, 2 x 35µm Cu).

Electrical Characteristics

6 Electrical Characteristics

6.1 Functional Device Characteristics

Table 9 Electrical Characteristics

$uV_{CC} = 4.75\text{ V to }5.25\text{ V}$; $uV_{IO} = 3.0\text{ V to }5.25\text{ V}$; $R_{DCLoad} = 45\text{ Ohm}$; $C_{DCLoad} = 100\text{ pF}$; $T_j = -40^\circ\text{C to }+150^\circ\text{C}$
 All voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max			
Current Consumption V_{CC} Power Supply							
Current Consumption in BD_Normal mode	iV_{CC}	–	33	40	mA	Transmitter active	P_6.1.1
Current Consumption in BD_Normal mode	iV_{CC_idle}	–	6	15	mA	Transmitter idle;	P_6.1.2
Current Consumption in BD_Standby mode	$iV_{CC_Stb_150}$	–	30	40	μA	$T_j \leq 150^\circ\text{C}$; No bus activity or local errors detected; Logic inputs in default states; ERRN = “high”	P_6.1.3
Current Consumption in BD_Standby mode	$iV_{CC_Stb_85}$	–	17	25	μA	$T_j \leq 85^\circ\text{C}$; No bus activity or local errors detected; Logic inputs in default states; ERRN = “high”	P_6.1.4
Current Consumption in BD_Off condition	iV_{CC_off}	–	–	35	μA	Logic inputs in default states;	P_6.1.5
Current Consumption V_{IO} Reference							
Current Consumption in BD_Normal mode	iV_{IO}	–	0.15	0.5	mA	–	P_6.1.6
Current Consumption in BD_Standby mode	iV_{IO_Stb}	–	1	5	μA	No bus activity or local errors detected; Logic inputs in default states; ERRN = “high”	P_6.1.7
Current Consumption in BD_Off condition	iV_{IO_off}	–	–	5	μA	Logic inputs in default states	P_6.1.8
Undervoltage Detection V_{CC} Power Supply							
Undervoltage detection threshold on V_{CC}	$uBDUV_{CC}$	4.0	4.25	4.75	V	–	P_6.1.9
Undervoltage detection hysteresis on V_{CC}	$uBDUV_{CC_Hys}$	–	100	–	mV	–	P_6.1.10