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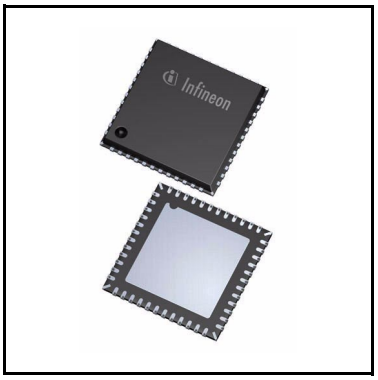
TLE9261BQXV33
System Basis Chip

Mid-Range+ System Basis Chip Family

Quality Requirement Category: Automotive



Features

- Two integrated Low-Drop Voltage Regulators: Main regulator (5 V or 3.3 V up to 250 mA) and auxiliary regulator (5 V up to 100 mA) with off-board usage protection
- Voltage regulator (5 V, 3.3 V or 1.8 V) with external PNP transistor configurable for off-board usage or for load sharing
- 1 high-speed CAN transceiver supporting FD communication up to 5 Mbit/s featuring CAN Partial Networking & CAN FD tolerant mode according to ISO 11898-2:2016 & SAE J2284
- 4 high-side outputs 7 Ω typ., 2 HV GPIOs, 3 HV wake inputs
- Integrated fail-safe and supervision functions, e.g. fail-safe, watchdog, interrupt- and reset outputs
- 16-bit SPI for configuration and diagnostics

Applications

- Body Control Modules (BMC), Passive keyless entry and start modules, Gateway applications
- Heating, ventilation and air conditioning (HVAC)
- Seat, roof, tailgate, trailer, door and other closure modules
- Light control modules
- Gear shifters and selectors

Description

Body System IC with Integrated Voltage Regulators, Power Management Functions, HS-CAN Transceiver supporting CAN FD .
Featuring Multiple High-Side Switches and High-Voltage Wake Inputs.

Type	Package	Marking
TLE9261BQXV33	PG-VQFN-48-31	TLE9261BQXV33

Table of Contents

1 Overview

Scalable System Basis Chip Family

- Product family with various products for complete scalable application coverage.
- Dedicated Data Sheets are available for the different product variants
- Complete compatibility (hardware and software) across the family
- TLE9263 with 2 LIN transceivers, 3 voltage regulators
- TLE9262 with 1 LIN transceiver, 3 voltage regulators
- TLE9261 without LIN transceivers, 3 voltage regulators
- Product variants for 5V (TLE926xQX) and 3.3V (TLE926xQXV33) output voltage for main voltage regulator
- CAN Partial Networking variants for 5V (TLE926x-3QX) and 3.3V (TLE926x-3QXV33) output voltage

Device Description

The TLE9261BQXV33 is a monolithic integrated circuit in an exposed pad VQFN-48 (7mm x 7mm) power package with Lead Tip Inspection (LTI) feature to support Automatic Optical Inspection (AOI).
The device is designed for various CAN automotive applications as main supply for the microcontroller and as interface for a CAN bus network.

To support these applications, the System Basis Chip (SBC) provides the main functions, such as a 3.3V low-dropout voltage regulator (LDO) for e.g. a microcontroller supply, another 5V low-dropout voltage regulator with off-board protection for e.g. sensor supply, another 3.3V/1.8V regulator to drive an external PNP transistor, which can be used as an independent supply for off-board usage or in load sharing configuration with the main regulator VCC1, a HS-CAN transceiver supporting CAN FD for data transmission, high-side switches with embedded protective functions and a 16-bit Serial Peripheral Interface (SPI) to control and monitor the device. Also implemented are a configurable timeout / window watchdog circuit with a reset feature, three Fail Outputs and an undervoltage reset feature.

The device offers low-power modes in order to minimize current consumption on applications that are connected permanently to the battery. A wake-up from the low-power mode is possible via a message on the buses, via the bi-level sensitive monitoring/wake-up inputs as well as via cyclic wake.

The device is designed to withstand the severe conditions of automotive applications.

Overview

Product Features

- Very low quiescent current consumption in Stop- and Sleep Mode
- Periodic Cyclic Wake in SBC Normal- and Stop Mode
- Periodic Cyclic Sense in SBC Normal-, Stop- and Sleep Mode
- Low-Drop Voltage Regulator 3.3V, 250mA
- Low-Drop Voltage Regulator 5V, 100mA, protected features for off-board usage
- Low-Drop Voltage Regulator, driving an external PNP transistor - 3.3V in load sharing configuration or 3.3V/1.8V in stand-alone configuration, protected features for off-board usage. Current limitation by shunt resistor (up to 350mA with 470mΩ external shunt resistor) in stand-alone configuration
- High-Speed CAN Transceiver:
  - fully compliant to HS-CAN standard ISO 11898-2:2016
  - supporting CAN FD communication up to 5 Mbps
- Fully compliant to “Hardware Requirements for LIN, CAN and FlexRay Interfaces in Automotive Applications” Revision 1.3, 2012-05-04
- Four High-Side Outputs 7Ω typ.
- Dedicated supply pin for High-Side Outputs
- Two General Purpose High-Voltage In- and Outputs (GPIOs) configurable as add. Fail Outputs, Wake Inputs, Low-Side switches or High-Side switches
- Three universal High-Voltage Wake Inputs for voltage level monitoring
- Alternate High-Voltage Measurement Function, e.g. for battery voltage sensing
- Configurable wake-up sources
- Reset Output
- Configurable timeout and window watchdog
- Up to three Fail Outputs (depending on configuration)
- Overtemperature and short circuit protection feature
- Wide supply input voltage and temperature range
- Software compatible to all SBC families TLE926x and TLE927x
- Green Product (RoHS compliant) & AEC Qualified
- PG-VQFN-48 leadless exposed-pad power package with Lead Tip Inspection (LTI) feature to support Automatic Optical Inspection (AOI)

2 Block Diagram

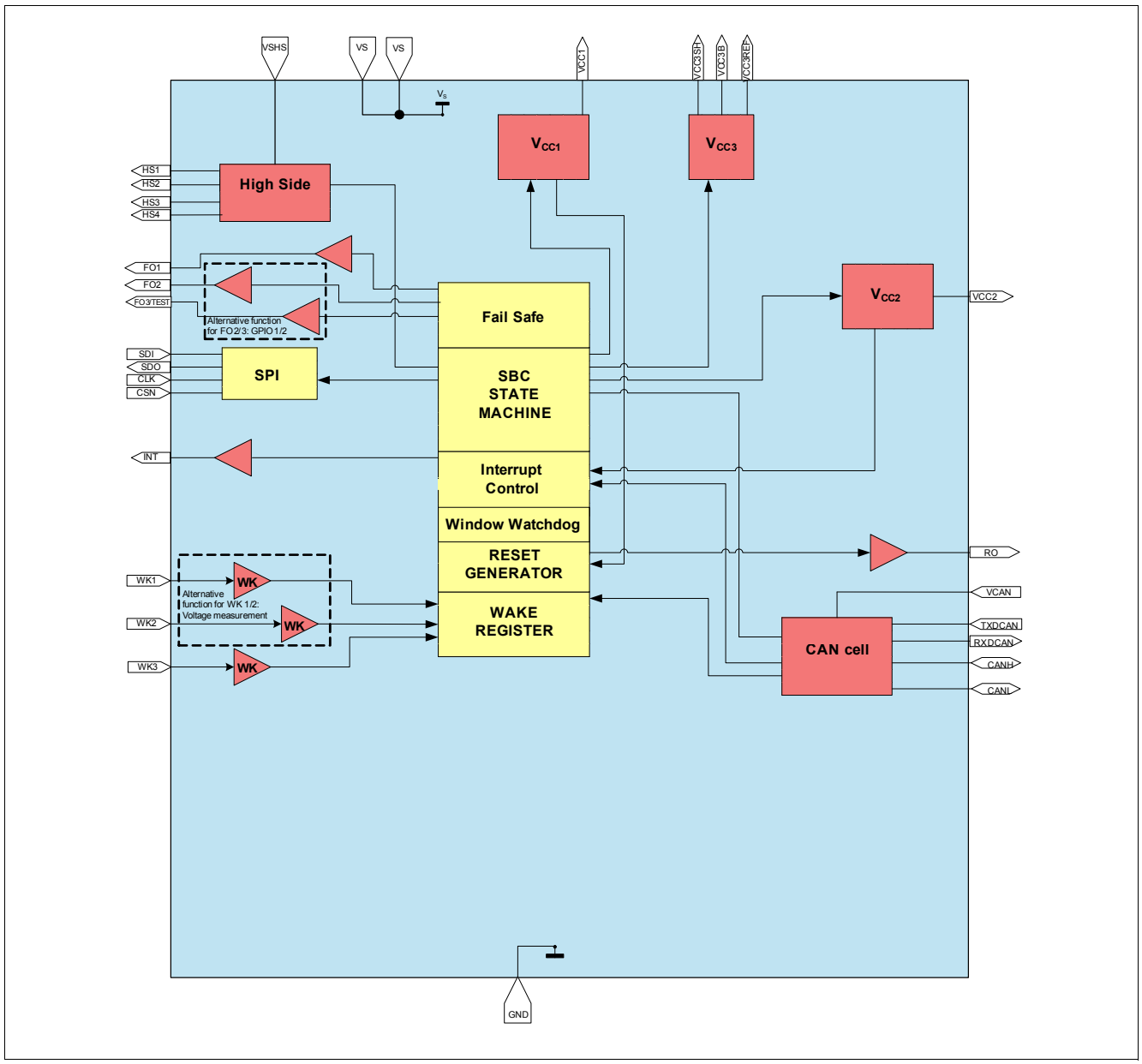


Figure 1 Block Diagram

3 Pin Configuration

3.1 Pin Assignment

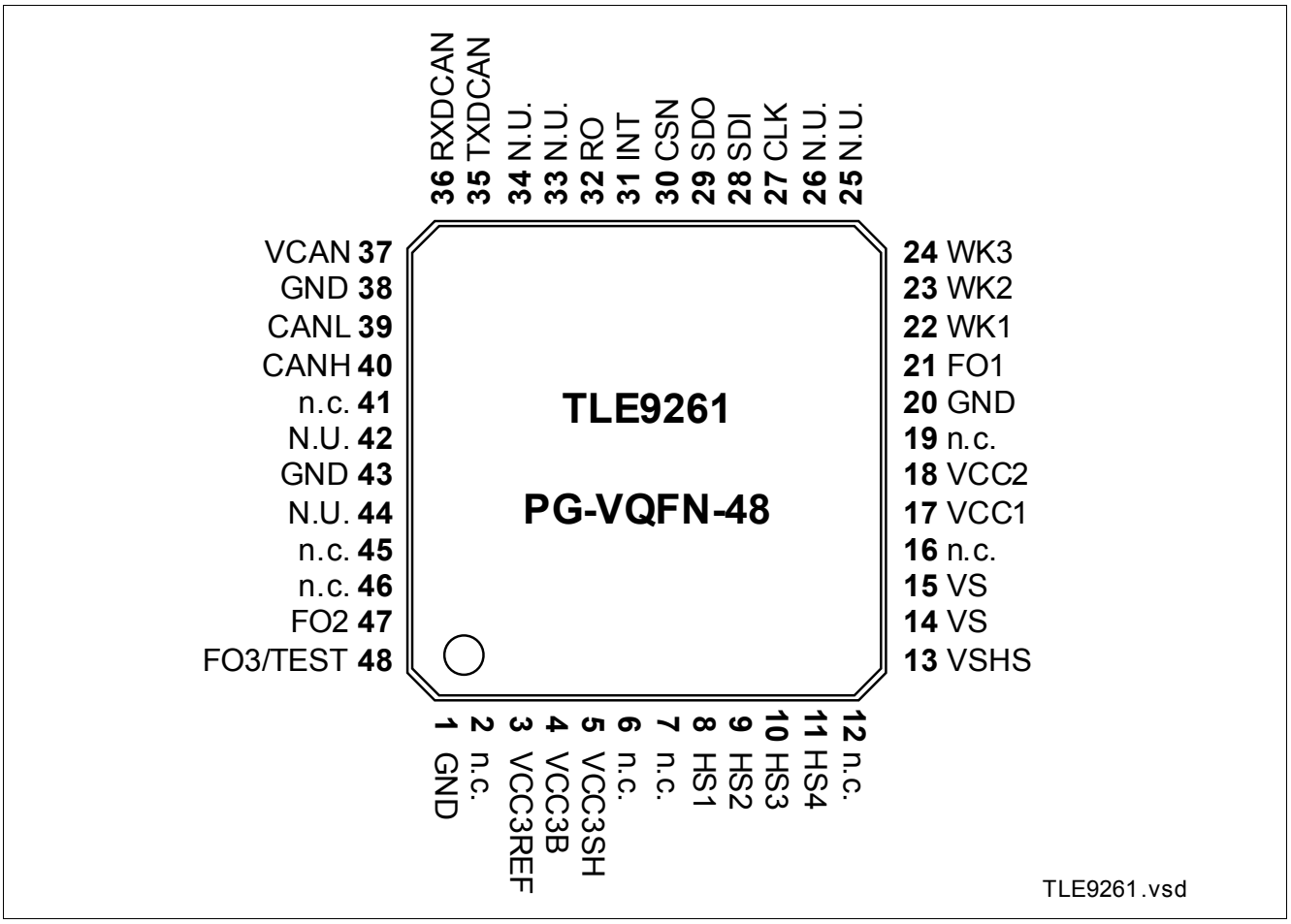


Figure 2 Pin Configuration

3.2 Pin Definitions and Functions

Pin	Symbol	Function
1	GND	**Ground**
2	n.c.	**not connected;** internally not bonded.
3	VCC3REF	**VCC3REF;** Collector connection for external PNP, reference input
4	VCC3B	**VCC3B;** Base connection for external PNP
5	VCC3SH	**VCC3SH;** Emitter connection for external PNP, shunt connection
6	n.c.	**not connected;** internally not bonded.
7	n.c.	**not connected;** internally not bonded.
8	HS1	**High Side Output 1;** typ. 7Ω
9	HS2	**High Side Output 2;** typ. 7Ω
10	HS3	**High Side Output 3;** typ. 7Ω
11	HS4	**High Side Output 4;** typ. 7Ω
12	n.c	**not connected;** internally not bonded.
13	VSHS	**Supply Voltage HS and GPIO1/2 in HS configuration; Supply voltage for High-Side Switches modules and respective UV-/OV supervision; Connected to battery voltage with reverse protection diode and filter against EMC**; connect to VS if separate supply is not needed
14	VS	**Supply Voltage; Supply voltage for chip internal supply and voltage regulators; Connected to Battery Voltage with external reverse protection Diode and Filter against EMC**
15	VS	**Supply Voltage; Supply voltage for chip internal supply and voltage regulators; Connected to Battery Voltage with external reverse protection Diode and Filter against EMC**
16	n.c.	**not connected;** internally not bonded.
17	VCC1	**Voltage Regulator Output 1**
18	VCC2	**Voltage Regulator Output 2**
19	n.c.	**not connected;** internally not bonded.
20	GND	**GND**
21	FO1	**Fail Output 1**
22	WK1	**Wake Input 1;** Alternative function: HV-measurement function input pin (only in combination with WK2, see **Chapter 11.2.2**)
23	WK2	**Wake Input 2;** Alternative function: HV-measurement function output pin (only in combination with WK1, see **Chapter 11.2.2**)
24	WK3	**Wake Input 3**
25	N.U.	**Not Used;** Used for internal testing purpose. Do not connect, leave open
26	N.U.	**Not Used;** Used for internal testing purpose. Do not connect, leave open
27	CLK	**SPI Clock Input**
28	SDI	**SPI Data Input; into SBC (=MOSI)**
29	SDO	**SPI Data Output;** out of SBC (=MISO)

Pin Configuration

Pin	Symbol	Function
30	CSN	**SPI Chip Select Not Input**
31	INT	**Interrupt Output**; used as wake-up flag for microcontroller in SBC Stop or Normal Mode and for indicating failures. Active low. During start-up used to set the SBC configuration. External pull-up sets config 1/3, no external pull-up sets config 2/4.
32	RO	**Reset Output**
33	N.U.	**Not Used;** Used for internal testing purpose. Do not connect, leave open
34	N.U.	**Not Used;** Used for internal testing purpose. Do not connect, leave open
35	TXDCAN	**Transmit CAN**
36	RXDCAN	**Receive CAN**
37	VCAN	**Supply Input; for internal HS-CAN cell**
38	GND	**GND**
39	CANL	**CAN Low Bus Pin**
40	CANH	**CAN High Bus Pin**
41	n.c.	**not connected;** internally not bonded.
42	N.U.	**Not Used;** Used for internal testing purpose. Do not connect, leave open
43	GND	**Ground**
44	N.U.	**Not Used;** Used for internal testing purpose. Do not connect, leave open
45	n.c.	**not connected;** internally not bonded.
46	n.c.	**not connected;** internally not bonded.
47	FO2	**Fail Output 2** - Side Indicator; Side indicators 1.25Hz 50% duty cycle output; Open drain. Active LOW. **Alternative Function: GPIO1**; configurable pin as WK, or LS, or HS supplied by VSHS (default is FO2, see also **Chapter 13.1.1**)
48	FO3/TEST	**Fail Output 3** - Pulsed Light Output; Break/rear light 100Hz 20% duty cycle output; Open drain. Active LOW **TEST**; Connect to GND to activate SBC Development Mode; Integrated pull-up resistor. Connect to VS with pull-up resistor or leave open for normal operation. **Alternative Function: GPIO2**; configurable pin as WK, or LS, or HS supplied by VSHS (default is FO3, see also **Chapter 13.1.1**)
Cooling Tab	GND	Cooling Tab - Exposed Die Pad; For cooling purposes only, do not use as an electrical ground.[1)]

1) The exposed die pad at the bottom of the package allows better power dissipation of heat from the SBC via the PCB. The exposed die pad is not connected to any active part of the IC an can be left floating or it can be connected to GND (recommended) for the best EMC performance.

*Note: all VS Pins must be connected to battery potential or insert a reverse polarity diodes where required; all GND pins as well as the Cooling Tab must be connected to one common GND potential; note that the tie bars at each package corner are connected to the cooling tab (see also **Chapter 17**)*

3.3 Hints for Unused Pins

It must be ensured that the correct configurations are also selected, i.e. in case functions are not used that they are disabled via SPI:

- WK1/2/3: connect to GND and disable WK inputs via SPI
- HSx: leave open
- CANH/L, RXDCAN, TXDCAN: leave all pins open
- RO / FOx: leave open
- INT: leave open
- TEST: connect to GND during power-up to activate SBC Development Mode;
  connect to VS or leave open for normal user mode operation
- VCC2: leave open and keep disabled
- VCC3: See **Chapter 8.5**
- VCAN: connect to VCC1
- n.c.: not connected; internally not bonded; connect to GND
- **N.U.**: Not Used; Used for internal testing purposes only. Do not connect, leave open, i.e. not connected to any potential on the board. In case N.U. pins are connected on the board an open bridge has to be foreseen to avoid external disturbances. The bridge can be shorted by a 0 Ω resistance if signal is needed.

3.4 Hints for Alternate Pin Functions

In case of alternate pin functions, selectable via SPI, it must be ensured that the correct configurations are also selected via SPI, in case it is not done automatically. Please consult the respective chapter. In addition, following topics shall be considered:

- WK1..2: The pins can be either used as HV wake / voltage monitoring inputs or for a voltage measurement function (via bit **WK_MEAS**). In the second case, the WK1..2 pins shall not be used / assigned for any wake detection nor cyclic sense functionality, i.e. WK1 and WK2 must be disabled in the register **WK_CTRL_2** and the level information is to be ignored in the register **WK_LVL_STAT**.
- FO2..3: The pins can also be configured as GPIOs in the **GPIO_CTRL** register. In this case, the pins shall not be used for any fail output functionality. The default function after Power on Reset (POR) is FOx.

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Table 1 Absolute Maximum Ratings[1)]

T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Voltages							
Supply Voltage (VS, VSHS)	$VS_{x,\,max}$	-0.3	–	28	V	–	P_4.1.1
Supply Voltage (VS, VSHS)	$VS_{x,\,max}$	-0.3	–	40	V	Load Dump, max. 400 ms	P_4.1.2
Voltage Regulator 1	$V_{CC1,\,max}$	-0.3	–	5.5	V	–	P_4.1.3
Voltage Regulator 2	$V_{CC2,\,max}$	-0.3	–	28	V	V_{CC2} = 40V for Load Dump, max. 400 ms;	P_4.1.4
Voltage Regulator 3 (VCC3REF)	$V_{CC3REF,max}$	-0.3	–	28	V	V_{CC3REF} = 40V for Load Dump, max. 400 ms;	P_4.1.5
Voltage Regulator 3 (VCC3B)	$V_{CC3B,max}$	-0.3	–	V_S + 10	V	V_{CC3B} = 40V for Load Dump, max. 400 ms;	P_4.1.25
Voltage Regulator 3 (VCC3SH)	$V_{CC3SH,max}$	V_S - 0.30	–	V_S + 0.30	V	–	P_4.1.26
Wake Inputs WK1..3	$V_{WK,\,max}$	-0.3	–	40	V	–	P_4.1.6
Fail Pin FO1	$V_{FO1,\,max}$	-0.3	–	40	V	–	P_4.1.7
Fail Pins FO2, FO3/TEST	$V_{FO2\_3,\,max}$	-0.3	–	V_S + 0.3	V	–	P_4.1.23
CANH, CANL	$V_{BUS,\,max}$	-27	–	40	V	–	P_4.1.8
Maximum Differential CAN Bus Voltage	$V_{CAN\_Diff,\,max}$	-5	–	10	V	–	P_4.1.27
Logic Input Pins (CSN, CLK, SDI, TXDCAN)	$V_{I,\,max}$	-0.3	–	V_{CC1} + 0.3	V	–	P_4.1.9
Logic Output Pins (SDO, RO, INT, RXDCAN)	$V_{O,\,max}$	-0.3	–	V_{CC1} + 0.3	V	–	P_4.1.10
VCAN Input Voltage	$V_{VCAN,\,max}$	-0.3	–	5.5	V	–	P_4.1.11
High Side 1...4	$V_{HS,\,max}$	-0.3	–	V_{SHS} + 0.3	V	–	P_4.1.12
Currents							
Wake input WK1	$I_{WK1,max}$	0	–	500	µA	[2)]	P_4.1.13
Wake input WK2	$I_{WK2,max}$	-500	–	0	µA	[2)]	P_4.1.14

Table 1 Absolute Maximum Ratings[1)] (cont'd)

T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Temperatures							
Junction Temperature	T_j	-40	–	150	°C	–	P_4.1.15
Storage Temperature	T_{stg}	-55	–	150	°C	–	P_4.1.16
ESD Susceptibility							
ESD Resistivity	$V_{ESD,11}$	-2	–	2	kV	HBM[3)]	P_4.1.17
ESD Resistivity to GND, HSx	$V_{ESD,12}$	-2	–	2	kV	HBM[3)]	P_4.1.18
ESD Resistivity to GND, CANH, CANL	$V_{ESD,13}$	-8	–	8	kV	HBM[4)3)]	P_4.1.19
ESD Resistivity to GND	$V_{ESD,21}$	-500	–	500	V	CDM[5)]	P_4.1.20
ESD Resistivity Pin 1, 12,13,24,25,36,37,48 (corner pins) to GND	$V_{ESD,22}$	-750	–	750	V	CDM[5)]	P_4.1.21

1) Not subject to production test, specified by design.

2) Applies only if WK1 and WK2 are configured as alternative HV-measurement function

3) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS-001 (1.5 kΩ, 100 pF)

4) For ESD "GUN" Resistivity 6KV (according to IEC61000-4-2 "gun test" (150pF, 330Ω)), will be shown in Application Information and test report will be provided from IBEE

5) ESD susceptibility, Charged Device Model "CDM" EIA/JESD22-C101 or ESDA STM5.3.1

Notes

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.*

4.2 Functional Range

Table 2 Functional Range

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Supply Voltage	$V_{S,func}$	V_{POR}	–	28	V	1) V_{POR} see section **Chapter 14.10**	P_4.2.1
CAN Supply Voltage	$V_{CAN,func}$	4.75	–	5.25	V	–	P_4.2.3
SPI frequency	f_{SPI}	–	–	4	MHz	see **Chapter 15.7** for $f_{SPI,max}$	P_4.2.4
Junction Temperature	T_j	-40	–	150	°C	–	P_4.2.5

1) Including Power-On Reset, Over- and Undervoltage Protection

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

Device Behavior Outside of Specified Functional Range:

- 28V < $V_{S,func}$ < 40V: Device will still be functional including the state machine; the specified electrical characteristics might not be ensured anymore. The regulators VCC1/2/3 are working properly, however, a thermal shutdown might occur due to high power dissipation. HSx switches might be turned OFF depending on VSHS_OV configurations. The specified SPI communication speed is ensured; the absolute maximum ratings are not violated, however the device is not intended for continuous operation of VS >28V. The device operation at high junction temperatures for long periods might reduce the operating life time;
- V_{CAN} < 4.75V: The undervoltage bit **VCAN_UV** will be set in the SPI register **BUS_STAT_1** and the transmitter will be disabled as long as the UV condition is present;
- 5.25V < V_{CAN} < 5.50V: CAN transceiver still functional. However, the communication might fail due to out-of-spec operation;
- $V_{POR,f}$ < VS < 5.5V: Device will still be functional; the specified electrical characteristics might not be ensured anymore.
  - The voltage regulators will enter the low-drop operation mode (applies for VCC3 only if bit **VCC3_VS_ UV_OFF** is set),
  - A VCC1_UV reset could be triggered depending on the Vrtx settings,
  - HSx switch behavior will depend on the respective configuration:
    - **HS_UV_SD_EN** = ‘0’ (default): HSx will be turned OFF for VSHS < VSHS_UV and will stay OFF;
    - **HS_UV_SD_EN** = ‘1’: HSx stays on as long as possible. An unwanted overcurrent shut down may occur. OC shut down bit set and the respective HSx switch will stay OFF;
  - FOx outputs will remain ON if they were enabled before VS > 5.5V,
  - The specified SPI communication speed is ensured.

4.3 Thermal Resistance

Table 3 Thermal Resistance[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Junction to Soldering Point	R_{thJSP}	–	6	–	K/W	Exposed Pad	P_4.3.1
Junction to Ambient	R_{thJA}	–	33	–	K/W	2)	P_4.3.2

1) Not subject to production test, specified by design.

2) According to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board for 1.5W. Board: 76.2x114.3x1.5mm³ with 2 inner copper layers (35µm thick), with thermal via array under the exposed pad contacting the first inner copper layer and 300mm2 cooling area on the bottom layer (70µm).

4.4 Current Consumption

Table 4 Current Consumption

Current consumption values are specified at Tj = 25°C, VS = 13.5V, all outputs open (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
SBC Normal Mode							
Normal Mode current consumption	I_{Normal}	–	3.5	6.5	mA	V_S = 5.5 V to 28 V; T_j = -40 °C to +150 °C; VCC2, CAN, VCC3, HSx = OFF	P_4.4.1
SBC Stop Mode							
Stop Mode current consumption	$I_{Stop\_1,25}$	–	44	60	µA	1)VCC2/3, HSx = OFF; CAN, WKx not wake capable; Watchdog = OFF; no load on VCC1; I_PEAK_TH = ‘0’	P_4.4.2
Stop Mode current consumption	$I_{Stop\_1,85}$	–	50	70	µA	1)2)T_j = 85°C; VCC2/3, HSx = OFF; CAN, WKx not wake capable; Watchdog = OFF; no load on VCC1; I_PEAK_TH = ‘0’	P_4.4.3
Stop Mode current consumption (high active peak threshold)	$I_{Stop\_2,25}$	–	64	90	µA	1)VCC2/3, HSx = OFF; CAN, WKx not wake capable; Watchdog = OFF; no load on VCC1; I_PEAK_TH = ‘1’	P_4.4.35
Stop Mode current consumption (high active peak threshold)	$I_{Stop\_2,85}$	–	70	100	µA	1)2)Tj = 85°C; VCC2/3, HSx = OFF; CAN, WKx not wake capable; Watchdog = OFF; no load on VCC1; I_PEAK_TH = ‘1’	P_4.4.36
SBC Sleep Mode							
Sleep Mode current consumption	$I_{Sleep,25}$	–	15	25	µA	VCC2/3, HSx = OFF; CAN, WKx not wake capable	P_4.4.5
Sleep Mode current consumption	$I_{Sleep,85}$	–	25	35	µA	2)T_j = 85°C; VCC2/3, HSx = OFF; CAN, WKx not wake capable	P_4.4.6

Table 4 Current Consumption (cont'd)

Current consumption values are specified at Tj = 25°C, VS = 13.5V, all outputs open (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Feature Incremental Current Consumption							
Current consumption for CAN module, recessive state	$I_{CAN,rec}$	–	2	3	mA	SBC Normal/Stop Mode; CAN Normal Mode; VCC1 connected to VCAN; VTXDCAN = VCC1; no RL on CAN	P_4.4.7
Current consumption for CAN module, dominant state	$I_{CAN,dom}$	–	3	4.5	mA	2)SBC Normal/Stop Mode; CAN Normal Mode; VCC1 connected to VCAN; VTXDCAN = GND; no RL on CAN	P_4.4.8
Current consumption for CAN module, Receive Only Mode	$I_{CAN,RcvOnly}$	–	0.9	1.2	mA	2)SBC Normal/Stop Mode; CAN Receive Only Mode; VCC1 connected to VCAN; VTXDCAN = VCC1; no RL on CAN	P_4.4.9
Current consumption for WK1..3 wake capability (all wake inputs)	$I_{Wake,WKx,25}$	–	0.2	2	µA	3)4)5) SBC Sleep Mode; WK1..3 wake capable (all WKx enabled); CAN = OFF	P_4.4.13
Current consumption for WK1..3 wake capability (all wake inputs)	$I_{Wake,WKx,85}$	–	0.5	3	µA	2)3)4)5)SBC Sleep Mode; T_j = 85°C; WK1..3 wake capable; (all WKx enabled); CAN = OFF	P_4.4.14
Current consumption for CAN wake capability	$I_{Wake,CAN,25}$	–	4.5	6	µA	3)SBC Sleep Mode; CAN wake capable; WK1..3	P_4.4.17
Current consumption for CAN wake capability	$I_{Wake,CAN,85}$	–	5.5	7	µA	2)3)SBC Sleep Mode; T_j = 85°C; CAN wake capable; WK1..3	P_4.4.18
VCC2 Normal Mode current consumption	$I_{Normal,VCC2}$	–	2.5	3.5	mA	V_S = 5.5 V to 28 V; T_j = -40 °C to +150 °C; VCC2 = ON (no load)	P_4.4.32
Current consumption for VCC2 in SBC Sleep Mode	$I_{Sleep,VCC2,25}$	–	25	35	µA	1)3)SBC Sleep Mode; VCC2 = ON (no load); CAN, WK1..3 = OFF	P_4.4.19

Table 4 Current Consumption (cont'd)

Current consumption values are specified at Tj = 25°C, VS = 13.5V, all outputs open (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Current consumption for VCC2 in SBC Sleep Mode	$I_{Sleep,VCC2,85}$	–	30	40	µA	[1)2)3)]SBC Sleep Mode; T_j = 85°C; VCC2 = ON (no load); CAN, WK1..3 = OFF	P_4.4.20
Current consumption for VCC3 in SBC Sleep Mode in stand-alone configuration	$I_{Sleep,VCC3,25}$	–	40	60	µA	[1)3)]SBC Sleep Mode; VCC3 = ON (no load, stand-along config.); CAN, WK1..3 = OFF	P_4.4.21
Current consumption for VCC3 in SBC Sleep Mode in stand-alone configuration	$I_{Sleep,VCC3,85}$	–	50	70	µA	[1)2)3)]SBC Sleep Mode; T_j = 85°C; VCC3 = ON (no load, stand-along config.); CAN, WK1..3 = OFF	P_4.4.22
Current consumption for HSx in SBC Stop Mode	$I_{Stop,HSx,25}$	–	550	675	µA	[3)6)]SBC Stop Mode; Cyclic Sense & HSx= ON (no load); CAN, WK1..3 = OFF	P_4.4.33
Current consumption for HSx in SBC Stop Mode	$I_{Stop,HSx,85}$	–	575	700	µA	[2)3)6)]SBC Stop Mode; T_j = 85°C; Cyclic Sense & HSx = ON (no load); CAN, WK1..3 = OFF	P_4.4.34
Current consumption for cyclic sense function	$I_{Stop,CS25}$	–	20	28	µA	[3)7)8)]SBC Stop Mode; WD = OFF	P_4.4.23
Current consumption for cyclic sense function	$I_{Stop,CS85}$	–	24	35	µA	[2)3)7)8)]SBC Stop Mode; T_j = 85°C; WD = OFF	P_4.4.27
Current consumption for watchdog active in Stop Mode	$I_{Stop,WD25}$	–	20	28	µA	[2)]SBC Stop Mode; Watchdog running	P_4.4.30
Current consumption for watchdog active in Stop Mode	$I_{Stop,WD85}$	–	24	35	µA	[2)]SBC Stop Mode; T_j = 85°C; Watchdog running	P_4.4.31
Current consumption for active fail outputs (FO1..3)	$I_{Stop,FOx}$	–	1.0	2.0	mA	[2)]all SBC Modes; T_j = 25°C; FOx = ON (no load);	P_4.4.24

1) If the load current on VCC1 will exceed the configured VCC1 active peak threshold $I_{VCC1,Ipeak1,r}$ or $I_{VCC1,Ipeak2,r}$, the current consumption will increase by typ. 2.9mA to ensure optimum dynamic load behavior. Same applies to VCC2. For VCC3 the current consumption will increase by typ. 1.4mA. See also **Chapter 6**, **Chapter 7**, **Chapter 8**.

2) Not subject to production test, specified by design.

3) Current consumption adders of features defined for SBC Sleep Mode also apply for SBC Stop Mode and vice versa (unless otherwise specified).

4) No pull-up or pull-down configuration selected.
5) The specified WKx current consumption adder for wake capability applies regardless how many WK inputs are activated.
6) A typ. 75µA / max 125µA (T_j = 85°C) adder applies for every additionally activated HSx switch in SBC Stop Mode;
   In SBC Normal Mode every HSx switch consumes the typ. 75µA / max 125µA (T_j = 85°C) without the initial adder because the biasing is already enabled.
7) HS1 used for cyclic sense, Timer 2, 20ms period, 0.1ms on-time, no load on HS1.

   In general the current consumption adder for cyclic sense in SBC Stop Mode can be calculated with below equation:
   IStop,CS = 18µA + (525µA *tON/TPer)

8) Also applies to Cyclic Wake

Note: There is no additional current consumption contribution due to PWM generators.

5 System Features

This chapter describes the system features and behavior of the TLE9261BQXV33:

- State machine
- SBC mode control
- Device configuration
- State of supply and peripherals
- System functions such as cyclic sense or cyclic wake
- Supervision and diagnosis functions

The System Basis Chip (SBC) offers six operating modes:

- SBC Init Mode: Power-up of the device and after a soft reset,
- SBC Normal Mode: The main operating mode of the device,
- SBC Stop Mode: The first-level power saving mode with the main voltage regulator VCC1 enabled,
- SBC Sleep Mode: The second-level power saving mode with VCC1 disabled,
- SBC Restart Mode: An intermediate mode after a wake event from SBC Sleep or Fail-Safe Mode or after a failure (e.g. WD failure, VCC1 undervoltage reset) to bring the microcontroller into a defined state via a reset. Once the failure condition is not present anymore the device will automatically change to SBC Normal Mode after a delay time (t_{RD1}).
- SBC Fail-Safe Mode: A safe-state mode after critical failures (e.g. WD failure, VCC1 undervoltage reset) to bring the system into a safe state and to ensure a proper restart of the system. VCC1 is disabled. It is a permanent state until either a wake event (via CAN or WKx) occurs or the overtemperature condition is not present anymore.

A special mode, called SBC Development Mode, is available during software development or debugging of the system. All above mentioned operating modes can be accessed in this mode. However, the watchdog counter is stopped and does not need to be triggered. This mode can be accessed by setting the TEST pin to GND during SBC Init Mode.

The device can be configured via hardware (external component) to determine the device behavior after a watchdog trigger failure. See **Chapter 5.1.1** for further information.

The System Basis Chip is controlled via a 16-bit SPI interface. A detailed description can be found in **Chapter 15**.The configuration as well as the diagnosis is handled via the SPI. The SPI mapping of the TLE9261BQXV33 is compatible to other devices of the TLE926x and TLE927x families.

5.1 Block Description of State Machine

The different SBC Modes are selected via SPI by setting the respective SBC **MODE** bits in the register **M_S_CTRL**. The SBC **MODE** bits are cleared when going through SBC Restart Mode and thus always show the current SBC mode.

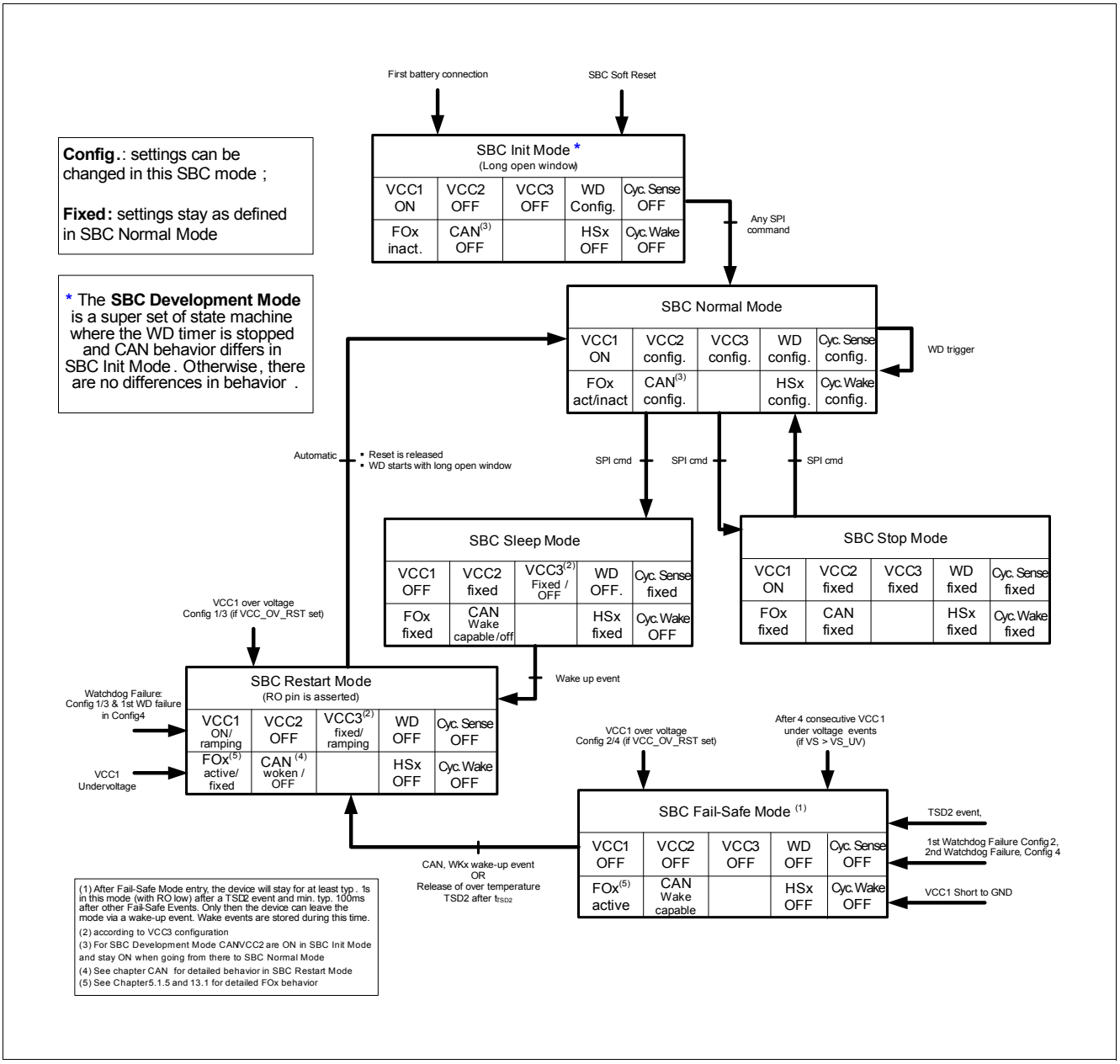


Figure 3 State Diagram showing the SBC Operating Modes

5.1.1 Device Configuration and SBC Init Mode

The SBC starts up in SBC Init Mode after crossing the power-on reset $V_{POR,r}$ threshold (see also **Chapter 14.3**) and the watchdog will start with a long open window (t_{LW}).
During this power-on phase following configurations are stored in the device:

- The device behavior regarding a watchdog trigger failure and a VCC1 overvoltage condition is determined by the external circuitry on the INT pin (see below)
- The selection of the normal device operation or the SBC Development Mode (watchdog disabled for debugging purposes) will be set depending on the voltage level of the FO3/TEST pin (see also **Chapter 5.1.7**).

5.1.1.1 Device Configuration

The configuration selection is intended to select the SBC behavior regarding a watchdog trigger failure. Depending on the requirements of the application, the VCC1 output shall be switched OFF and the device shall go to SBC Fail-Safe Mode in case of a watchdog failure (1 or 2 fails). To set this configuration (Config 2/4), the INT pin does not need an external pull-up resistor. In case VCC1 should not be switched OFF (Config 1/3), the INT pin needs to have an external pull-up resistor connected to VCC1 (see application diagram in **Chapter 16.1**).
Figure 5 shows the timing diagram of the hardware configuration selection. The hardware configuration is defined during SBC Init Mode. The INT pin is internally pulled LOW with a weak pull-down resistor during the reset delay time t_{RD1}, i.e.after VCC1 crosses the reset threshold VRT1 and before the RO pin goes HIGH. The INT pin is monitored during this time (with a continuos filter time of t_{CFG_F}) and the configuration (depending on the voltage level at INT) is stored at the rising edge of RO.

*Note: If the **POR** bit is not cleared then the internal pull-down resistor will be reactivated every time RO is pulled LOW the configuration will be updated at the rising edge of RO. Therefore it is recommended to clear the **POR** bit right after initialization. In case there is no stable signal at INT, then the default value '0' will taken as the config select value = SBC Fail-Safe Mode.*

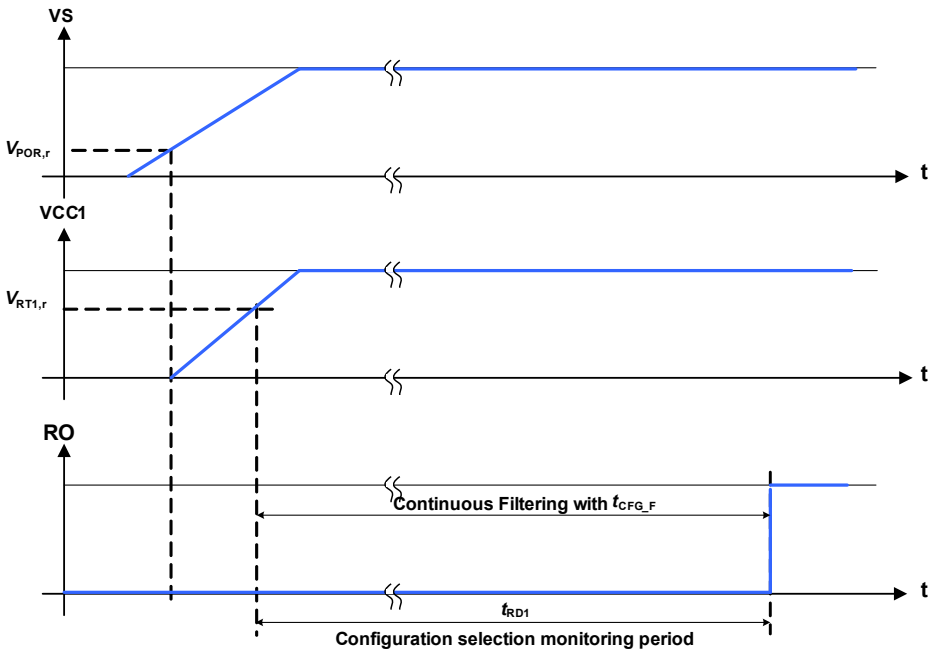


Figure 4 Hardware Configuration Selection Timing Diagram

There are four different device configurations (**Table 5**) available defining the watchdog failure and the VCC1 overvoltage behavior. The configurations can be selected via the external connection on the INT pin and the SPI bit **CFG** in the **HW_CTRL** register (see also **Chapter 15.4**):

- **CFGP** = '1': Config 1 and Config 3:
  - A watchdog trigger failure leads to SBC Restart Mode and depending on **CFG** the Fail Outputs (FOx) are activated after the 1st (Config 1) or 2nd (Config 3) watchdog trigger failure;
  - A VCC1 overvoltage detection will lead to SBC Restart Mode if **VCC1_OV_RST** is set. **VCC1_ OV** will be set and the Fail Outputs are activated;
- **CFGP** = '0': Config 2 and Config 4:
  - A watchdog trigger failure leads to SBC Fail-Safe Mode and depending on **CFG** the Fail Outputs (FOx) are activated after the 1st (Config 2) or 2nd (Config 4) watchdog trigger failure. The first watchdog trigger failure in Config 4 will lead to SBC Restart Mode;
  - A VCC1 overvoltage detection will lead to SBC Fail-Safe Mode if **VCC1_OV_RST** is set. **VCC1_ OV** will be set and the Fail Outputs are activated;

The respective device configuration can be identified by reading the SPI bit **CFG** in the **HW_CTRL** register and the **CFGP** bit in the **WK_LVL_STAT** register.

Table 5 shows the configurations and the device behavior in case of a watchdog trigger failure:

Table 5 Watchdog Trigger Failure Configuration

Config	INT Pin (CFGP)	SPI Bit CFG	Event	FOx Activation	SBC Mode Entry
1	External pull-up	1	1 x Watchdog Failure	after 1st WD Failure	SBC Restart Mode
2	No ext. pull-up	1	1 x Watchdog Failure	after 1st WD Failure	SBC Fail-Safe Mode
3	External pull-up	0	2 x Watchdog Failure	after 2nd WD Failure	SBC Restart Mode
4	No ext. pull-up	0	2 x Watchdog Failure	after 2nd WD Failure	SBC Fail-Safe Mode

Table 6 shows the configurations and the device behavior in case of a VCC1 overvoltage detection when VCC1_OV_RST is set:

Table 6 Device Behavior in Case of VCC1 Overvoltage Detection

Config	INT Pin (CFGP)	CFG Bit	VCC1_OV_RST	Event	VCC1_OV	FOx Activation	SBC Mode Entry
1-4	any value	x	0	1 x VCC1 OV	1	no FOx activation	unchanged
1	External pull-up	1	1	1 x VCC1 OV	1	after 1st VCC1 OV	SBC Restart Mode
2	No ext. pull-up	1	1	1 x VCC1 OV	1	after 1st VCC1 OV	SBC Fail-Safe Mode
3	External pull-up	0	1	1 x VCC1 OV	1	after 1st VCC1 OV	SBC Restart Mode
4	No ext. pull-up	0	1	1 x VCC1 OV	1	after 1st VCC1 OV	SBC Fail-Safe Mode

The respective configuration will be stored for all conditions and can only be changed by powering down the device (VS < $V_{POR,f}$).

5.1.1.2 SBC Init Mode

In SBC Init Mode, the device waits for the microcontroller to finish its startup and initialization sequence. In the SBC Init Mode any valid SPI command will bring the SBC to SBC Normal Mode. During the long open window the watchdog has to be triggered. Thereby the watchdog will be automatically configured.

A missing watchdog trigger during the long open window will cause a watchdog failure and the device will enter SBC Restart Mode.

Wake events are ignored during SBC Init Mode and will therefore be lost.

*Note: Any SPI command will bring the SBC to SBC Normal Mode even if it is a illegal SPI command (see **Chapter 15.2**).*

*Note: For a safe start-up, it is recommended to use the first SPI command to trigger and to configure the watchdog (see **Chapter 14.2**).*

*Note: At power up no **VCC1_UV** will be issued nor will FOx be triggered as long as VCC1 is below the $V_{RT,x}$ threshold and if VS is below the VCC1 short circuit detection threshold **$V_{S,UV}$**. The RO pin will be kept low as long as VCC1 is below the selected $V_{RT,x}$ threshold.*