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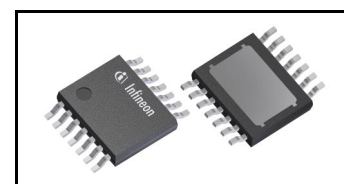


TLE94104EP



Features

- Four half bridge power outputs
- Very low power consumption in sleep mode
- 3.3V / 5V compatible inputs with hysteresis
- All outputs with overload and short circuit protection
- Independently diagnosable outputs (overcurrent, open load)
- Open load diagnostics in ON-state for all high-side and low-side
- 16-bit Standard SPI interface with daisy chain and in-frame response capability for control and diagnosis
- Fast diagnosis with the global error flag
- Overtemperature pre-warning and protection
- Over- and Undervoltage lockout
- Cross-current protection



Potential applications

- HVAC Flap DC motors
- Monostable and bistable relays
- Side mirror x-y adjustment
- Voltage controlled bipolar stepper motors

Product validation

Qualified for Automotive Applications. Product Validation according to AEC-Q100

Description

The TLE94104EP is a protected quad half-bridge driver designed especially for automotive motion control applications such as Heating, Ventilation and Air Conditioning (HVAC) flap DC motor control. It is part of a larger family offering half-bridge drivers from three outputs to twelve outputs with direct interface or SPI interface.

The half bridge drivers are designed to drive DC motor loads in sequential or parallel operation. Operation modes forward (cw), reverse (ccw), brake and high impedance are controlled from a 16-bit SPI interface. It offers diagnosis features such as short circuit, open load, power supply failure and overtemperature detection. In combination with its low quiescent current, this device is attractive among others for automotive applications. The small fine pitch exposed pad package, PG-TSDSO-14, provides good thermal performance and reduces PCB-board space and costs.

Type	Package	Marking
TLE94104EP	PG-TSDSO-14	TLE94104

Table 1 Product Summary

Operating Voltage	V_S	5.5 ... 20 V
Logic Supply Voltage	V_{DD}	3.0 ... 5.5 V
Maximum Supply Voltage for Load Dump Protection	$V_{S(LD)}$	40 V
Minimum Overcurrent Threshold	I_{SD}	0.9 A
Maximum On-State Path Resistance at $T_j = 150^\circ\text{C}$	$R_{DSON(total)_HSx+LSy}$	1.8 + 1.8 Ω
Typical Quiescent Current at $T_j = 85^\circ\text{C}$	I_{SQ}	0.1 μA
Maximum SPI Access Frequency	f_{SCLK}	5 MHz

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Pin Configuration

1 Pin Configuration

1.1 Pin Assignment

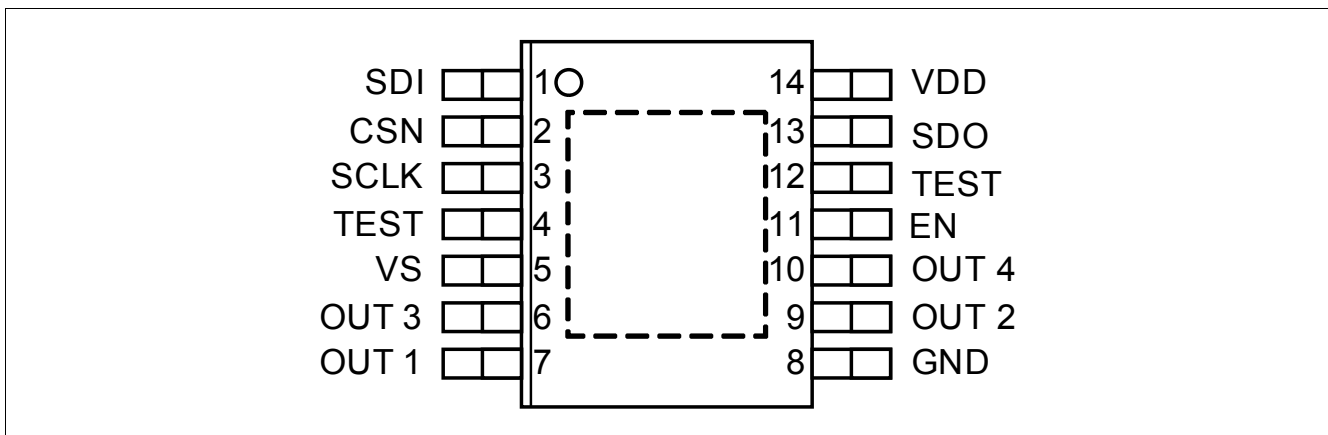


Figure 1 Pin Configuration TLE94104EP with SPI interface

1.2 Pin Definitions and Functions

Pin	Symbol	Function
1	SDI	Serial data input with internal pull down
2	CSN	Chip select Not input with internal pull up
3	SCLK	Serial clock input with internal pull down
4	TEST	Test pin. This pin can be left open or be terminated to ground.
5	VS	Main supply voltage for power half bridges.
6	OUT 3	Power half-bridge 3
7	OUT 1	Power half-bridge 1
8	GND	Ground
9	OUT 2	Power half-bridge 2
10	OUT 4	Power half-bridge 4
11	EN	Enable with internal pull-down; Places device in standby mode by pulling the EN line Low
12	TEST	Test pin. This pin must be terminated to ground
13	SDO	Serial data output
14	VDD	Logic supply voltage
EDP	-	Exposed Die Pad; For cooling and EMC purposes only - not usable as electrical ground. Electrical ground must be provided by pins 8. ¹⁾

1) The exposed die pad at the bottom of the package allows better heat dissipation from the device via the PCB. The exposed pad (EP) must be either left open or connected to GND. It is recommended to connect EP to GND for best EMC and thermal performance.

Block Diagram

2 Block Diagram

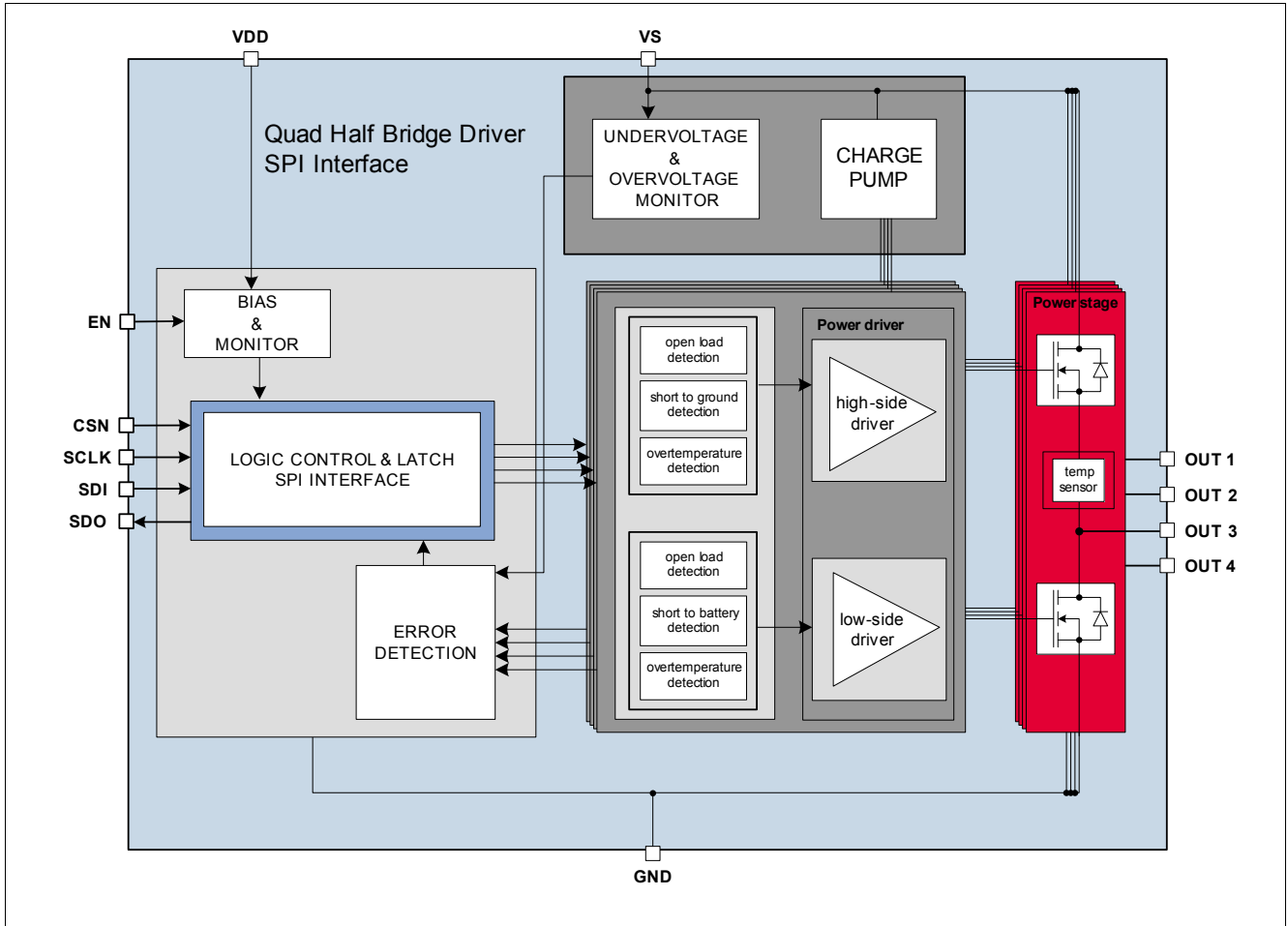


Figure 2 Block Diagram TLE94104EP (SPI Interface)

Block Diagram

2.1 Voltage and current definition

Figure 3 shows terms used in this datasheet, with associated convention for positive values.

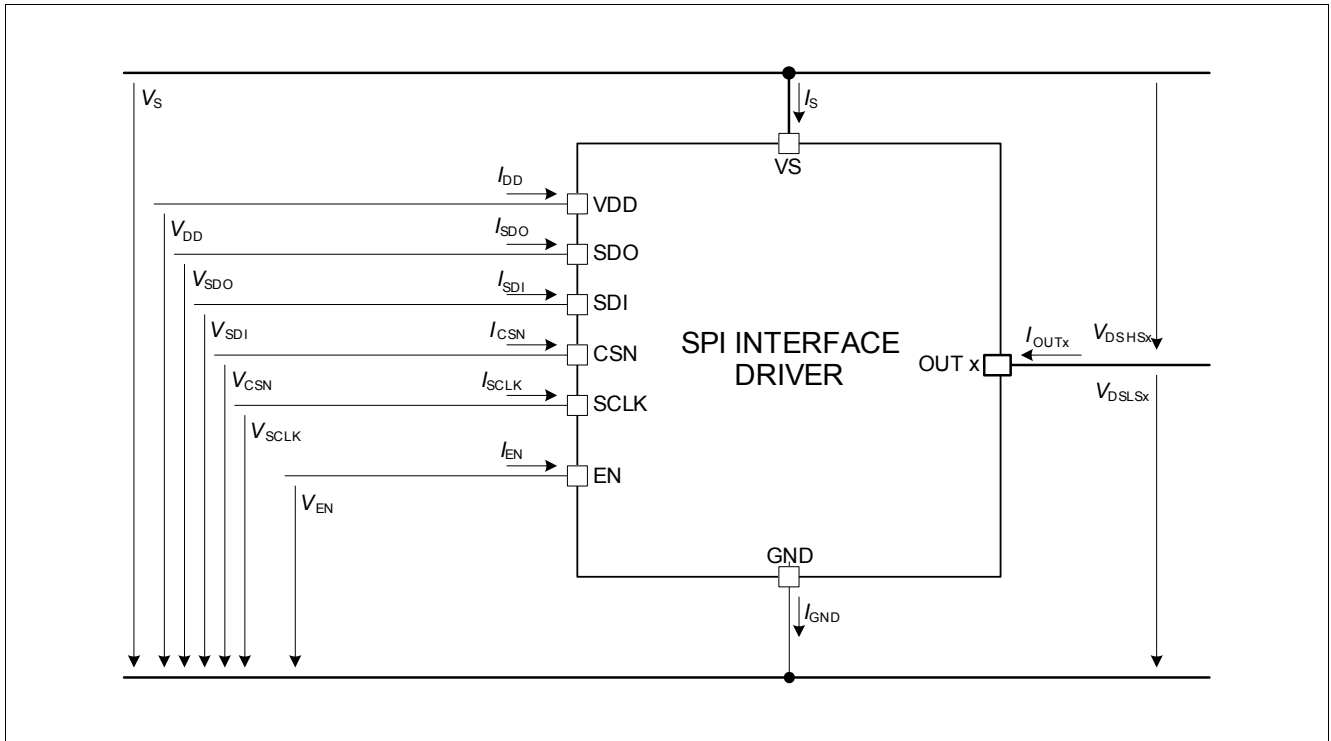


Figure 3 Voltage and Current Definition

General Product Characteristics

3 General Product Characteristics

3.1 Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings¹⁾ $T_j = -40^\circ\text{C}$ to $+150^\circ\text{C}$

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Voltages							
Supply voltage	V_S	-0.3	–	40	V		P_4.1.1
Supply Voltage Slew Rate	$ dV_S/dt $	–	–	10	V/ μs	V_S increasing and decreasing ¹⁾	P_4.2.2
Power half-bridge output voltage	V_{OUT}	-0.3	–	40	V	$0\text{ V} < V_{\text{OUT}} < V_S$	P_4.1.2
Logic supply voltage	V_{DD}	-0.3	–	5.5	V	$0\text{ V} < V_S < 40\text{ V}$	P_4.1.3
Logic input voltages (SDI, SCLK, CSN, EN)	$V_{\text{SDI}}, V_{\text{SCLK}}, V_{\text{CSN}}, V_{\text{EN}}$	-0.3	–	VDD	V	$0\text{ V} < V_S < 40\text{ V}$ $0\text{ V} < V_{\text{DD}} < 5.5\text{ V}$	P_4.1.4
Logic output voltage (SDO)	V_{SDO}	-0.3	–	VDD	V	$0\text{ V} < V_S < 40\text{ V}$ $0\text{ V} < V_{\text{DD}} < 5.5\text{ V}$	P_4.1.5
Test pins	V_{TEST}	-0.3	–	VDD	V	$0\text{ V} < V_S < 40\text{ V}$ $0\text{ V} < V_{\text{DD}} < 5.5\text{ V}$	P_4.1.19
Currents							
Continuous Supply Current for V_S	I_S	0	–	2.0	A	–	P_4.1.20
Current per GND pin	I_{GND}	0	–	2.0	A	–	P_4.1.14
Output Currents	I_{OUT}	-2.0	–	2.0	A	–	P_4.1.15
Temperatures							
Junction temperature	T_j	-40	–	150	$^\circ\text{C}$	–	P_4.1.8
Storage temperature	T_{stg}	-50	–	150	$^\circ\text{C}$	–	P_4.1.9
ESD Susceptibility							
ESD susceptibility OUTn and VS pins versus GND. All other pins grounded.	V_{ESD}	-4	–	4	kV	JEDEC HBM ¹⁾²⁾	P_4.1.10
ESD susceptibility all pins	V_{ESD}	-2	–	2	kV	JEDEC HBM ¹⁾²⁾	P_4.1.11
ESD susceptibility all pins	V_{ESD}	-500	–	500	V	CDM ¹⁾³⁾	P_4.1.12
ESD susceptibility corner pins	V_{ESD}	-750	–	750	V	CDM ¹⁾³⁾	P_4.1.13

1) Not subject to production test, specified by design

2) ESD susceptibility, "JEDEC HBM" according to ANSI/ ESDA/ JEDEC JS001 (1.5 k Ω , 100pF)

3) ESD susceptibility, Charged Device Model "CDM" according JEDEC JESD22-C101

General Product Characteristics**Notes**

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.*

General Product Characteristics
3.2 Functional Range
Table 3 Functional Range

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Supply voltage range for normal operation	$V_{S(nor)}$	5.5	–	20	V	–	P_4.2.1
Logic supply voltage range for normal operation	V_{DD}	3.0	–	5.5	V	–	P_4.2.3
Logic input voltages (SDI, SCLK, CSN, EN)	V_{SDI} , V_{SCLK} , V_{CSN} , V_{EN}	-0.3	–	5.5	V	–	P_4.2.4
Junction temperature	T_j	-40	–	150	°C		P_4.2.5

Note: Within the normal functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

General Product Characteristics

3.3 Thermal Resistance

Table 4 Thermal Resistance TLE94104EP

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction to Case, $T_A = -40^\circ\text{C}$	R_{thjC_cold}	–	14	–	K/W	1)	
Junction to Case, $T_A = 85^\circ\text{C}$	R_{thjC_hot}	–	17	–	K/W	1)	
Junction to ambient, $T_A = -40^\circ\text{C}$ (1s0p, minimal footprint)	$R_{thjA_cold_min}$	–	126	–	K/W	1) 2)	
Junction to ambient, $T_A = 85^\circ\text{C}$ (1s0p, minimal footprint)	$R_{thjA_hot_min}$	–	134	–	K/W	1) 2)	
Junction to ambient, $T_A = -40^\circ\text{C}$ (1s0p, 300mm ² Cu)	$R_{thjA_cold_300}$	–	69	–	K/W	1) 3)	
Junction to ambient, $T_A = 85^\circ\text{C}$ (1s0p, 300mm ² Cu)	$R_{thjA_hot_300}$	–	81	–	K/W	1) 3)	
Junction to ambient, $T_A = -40^\circ\text{C}$ (1s0p, 600mm ² Cu)	$R_{thjA_cold_600}$	–	67	–	K/W	1) 4)	
Junction to ambient, $T_A = 85^\circ\text{C}$ (1s0p, 600mm ² Cu)	$R_{thjA_hot_600}$	–	79	–	K/W	1) 4)	
Junction to ambient, $T_A = -40^\circ\text{C}$ (2s2p)	$R_{thjA_cold_2s2p}$	–	53	–	K/W	1) 5)	
Junction to ambient, $T_A = 85^\circ\text{C}$ (2s2p)	$R_{thjA_hot_2s2p}$	–	67	–	K/W	1) 5)	

1) Not subject to production test, specified by design.

2) Specified R_{thjA} value is according to JEDEC JESD51-2, -3 at natural convection on FR4 1s0p board; The product (chip + package) was simulated on a 76.2 x 114.3 x 1.5mm board with minimal footprint copper area and 35µm thickness. $T_a = -40^\circ\text{C}$, each channel dissipates 0.2W. $T_a = 85^\circ\text{C}$, each channel dissipates 0.135W.

3) Specified R_{thjA} value is according to JEDEC JESD51-2, -3 at natural convection on FR4 1s0p board; The product (chip + package) was simulated on a 76.2 x 114.3 x 1.5mm board with additional cooling of 300mm² copper area and 35µm thickness. $T_a = -40^\circ\text{C}$, each channel dissipates 0.2W. $T_a = 85^\circ\text{C}$, each channel dissipates 0.135W.

4) Specified R_{thjA} value is according to JEDEC JESD51-2, -3 at natural convection on FR4 1s0p board; The product (chip + package) was simulated on a 76.2 x 114.3 x 1.5mm board with additional cooling of 600mm² copper area and 35µm thickness. $T_a = -40^\circ\text{C}$, each channel dissipates 0.2W. $T_a = 85^\circ\text{C}$, each channel dissipates 0.135W.

5) Specified R_{thjA} value is according to JEDEC JESD51-2, -3 at natural convection on FR4 2s2p board; The product (chip + package) was simulated on a 76.2 x 114.3 x 1.5mm board with two inner copper layers (4 x 35µm Cu). $T_a = -40^\circ\text{C}$, each channel dissipates 0.2W. $T_a = 85^\circ\text{C}$, each channel dissipates 0.135W.

General Product Characteristics

3.4 Electrical Characteristics

Table 5 Electrical Characteristics, $V_S=5.5\text{ V to }20\text{ V}$, $V_{DD} = 3.0\text{ V to }5.5\text{ V}$, $T_j = -40^\circ\text{C to }+150^\circ\text{C}$, EN= HIGH, $I_{OUTn} = 0\text{ A}$; Typical values refer to $V_{DD} = 5.0\text{ V}$, $V_S = 13.5\text{ V}$ and $T_j = 25^\circ\text{C}$ unless otherwise specified; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Current Consumption, EN = GND							
Supply Quiescent current	I_{SQ}	–	0.1	2	μA	$-40^\circ\text{C} \leq T_j \leq 85^\circ\text{C}$	P_4.4.1
Logic supply quiescent current	I_{DD_Q}	–	0.1	1	μA	$-40^\circ\text{C} \leq T_j \leq 85^\circ\text{C}$	P_4.4.2
Total quiescent current	$I_{SQ} + I_{DD_Q}$	–	0.6	3	μA	$-40^\circ\text{C} \leq T_j \leq 85^\circ\text{C}$	P_4.4.3
Current Consumption, EN=HIGH							
Supply current	I_S	–	0.13	0.5	mA	Power drivers and power stages are off	P_4.4.4
Supply current	I_{S_HSON}	–	1.5	3	mA	All high-sides ON ¹⁾²⁾	P_4.4.101
Logic supply current	I_{DD}	–	0.6	2.5	mA	SPI not active	P_4.4.5
Logic supply current	I_{DD_RUN}	–	2.5	–	mA	SPI 5MHz ²⁾	P_4.4.6
Total supply current	$I_S + I_{DD_RUN}$	–	2.7	–	mA	SPI 5MHz ²⁾	P_4.4.7
Over- and Undervoltage Lockout							
Undervoltage Switch ON voltage threshold	V_{UV_ON}	4.4	4.90	5.3	V	V_S increasing	P_4.4.8
Undervoltage Switch OFF voltage threshold	V_{UV_OFF}	4	4.50	4.9	V	V_S decreasing	P_4.4.9
Undervoltage Switch ON/OFF hysteresis	V_{UV_HY}	–	0.40	–	V	$V_{UV_ON} - V_{UV_OFF}$ ²⁾	P_4.4.10
Oversvoltage Switch OFF voltage threshold	V_{OV_OFF}	21	23	25	V	V_S increasing	P_4.4.11
Oversvoltage Switch ON voltage threshold	V_{OV_ON}	20	22	24	V	V_S decreasing	P_4.4.12
Oversvoltage Switch ON/OFF hysteresis	V_{OV_HY}	–	1	–	V	$V_{OV_OFF} - V_{OV_ON}$ ²⁾	P_4.4.13
V_{DD} Power-On-Reset	V_{DD_POR}	2.40	2.63	2.90	V	V_{DD} increasing	P_4.4.14
V_{DD} Power-Off-Reset	V_{DD_POFFR}	2.35	2.57	2.85	V	V_{DD} decreasing	P_4.4.15
V_{DD} Power ON/OFF hysteresis	$V_{DD_POR_HY}$	–	0.06	–	V	$V_{DD_POR} - V_{DD_POFFR}$ ²⁾	P_4.4.98
Static Drain-source ON-Resistance (High-Side or Low-Side)							
High-Side or Low-Side R_{DSON} (all outputs)	$R_{DSON_HB_25C}$	–	825	1200	m Ω	$I_{OUT} = \pm 0.5\text{ A}$; $T_j = 25^\circ\text{C}$	P_4.4.16
High-Side or Low-Side R_{DSON} (all outputs)	$R_{DSON_HB_150C}$	–	1350	1800	m Ω	$I_{OUT} = \pm 0.5\text{ A}$; $T_j = 150^\circ\text{C}$	P_4.4.17

General Product Characteristics

Table 5 Electrical Characteristics, $V_S = 5.5\text{ V to }20\text{ V}$, $V_{DD} = 3.0\text{ V to }5.5\text{ V}$, $T_j = -40^\circ\text{C to }+150^\circ\text{C}$, $EN = \text{HIGH}$, $I_{OUTn} = 0\text{ A}$; Typical values refer to $V_{DD} = 5.0\text{ V}$, $V_S = 13.5\text{ V}$ and $T_j = 25^\circ\text{C}$ unless otherwise specified; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified) (cont'd)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output Protection and Diagnosis of high-side (HS) channels of half-bridge output							
HS Overcurrent Shutdown Threshold	I_{SD_HS}	-1.5	-1.2	-0.9	A	See Figure 5	P_4.4.20
Difference between shutdown and limit current	$I_{LIM_HS} - I_{SD_HS}$	-1.2	-0.6	0	A	²⁾ $ I_{LIM_HS} \geq I_{SD_HS} $ See Figure 5	P_4.4.21
Overcurrent Shutdown filter time	t_{dSD_HS}	15	19	23	μs	²⁾	P_4.4.22
Open Load Detection Current	I_{OLD1_HS}	-15	-8	-3	mA	-	P_4.4.23
Open Load Detection filter time	t_{OLD1_HS}	2000	3000	4000	μs	²⁾	P_4.4.24
Output Protection and Diagnosis of low-side (LS) channels of half-bridge output							
LS Overcurrent Shutdown Threshold	I_{SD_LS}	0.9	1.2	1.5	A	See Figure 6	P_4.4.27
Difference between shutdown and limit current	$I_{LIM_LS} - I_{SD_LS}$	0	0.6	1.2	A	²⁾ $I_{LIM_LS} \geq I_{SD_LS}$ Figure 6	P_4.4.28
Overcurrent Shutdown filter time	t_{dSD_LS}	15	19	23	μs	²⁾	P_4.4.29
Open Load Detection Current	I_{OLD_LS}	3	8	15	mA	-	P_4.4.30
Open Load Detection filter time	t_{OLD_LS}	2000	3000	4000	μs	²⁾	P_4.4.31
Outputs OUT(1...n) leakage current							
HS leakage current in off state	I_{QLHn_NOR}	-2	-0.5	-	μA	$V_{OUTn} = 0\text{ V}$; $EN = \text{High}$	P_4.4.32
HS leakage current in off state	I_{QLHn_SLE}	-2	-0.5	-	μA	$V_{OUTn} = 0\text{ V}$; $EN = \text{GND}$	P_4.4.33
LS Leakage current in off state	I_{QLLn_NOR}	-	0.5	2	μA	$V_{OUTn} = V_S$; $EN = \text{High}$	P_4.4.34
LS Leakage current in off state	I_{QLLn_SLE}	-	0.5	2	μA	$V_{OUTn} = V_S$; $EN = \text{GND}$	P_4.4.35
Output Switching Times. See Figure 7 and Figure 8.							
Slew rate of high-side and low-side outputs	d_{VOUT}/dt	0.1	0.45	0.75	$\text{V}/\mu\text{s}$	Resistive load = 100Ω ; $V_S = 13.5\text{ V}$ ³⁾	P_4.4.36
Output delay time high side driver on	t_{dONH}	5	20	35	μs	Resistive load = 100Ω to GND	P_4.4.37
Output delay time high side driver off	t_{dOFFH}	15	45	75	μs	Resistive load = 100Ω to GND	P_4.4.38
Output delay time low side driver on	t_{dONL}	5	20	35	μs	Resistive load = 100Ω to VS	P_4.4.39
Output delay time low side driver off	t_{dOFFL}	15	45	75	μs	Resistive load = 100Ω to VS	P_4.4.40
Cross current protection time, high to low	t_{DHL}	100	130	160	μs	Resistive load = 100Ω ²⁾	P_4.4.41

General Product Characteristics

Table 5 Electrical Characteristics, $V_S = 5.5\text{ V to }20\text{ V}$, $V_{DD} = 3.0\text{ V to }5.5\text{ V}$, $T_j = -40^\circ\text{C to }+150^\circ\text{C}$, $EN = \text{HIGH}$, $I_{OUTn} = 0\text{ A}$; Typical values refer to $V_{DD} = 5.0\text{ V}$, $V_S = 13.5\text{ V}$ and $T_j = 25^\circ\text{C}$ unless otherwise specified; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified) (cont'd)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Cross current protection time, low to high	t_{DLH}	100	130	160	μs	Resistive load = $100\Omega^2$	P_4.4.42
Input Interface: Logic Input EN							
High-input voltage	V_{ENH}	$0.7 \cdot V_{DD}^*$	–	V_{DD}	V	–	P_4.4.43
Low-input voltage	V_{ENL}	0	–	$0.3 \cdot V_{DD}^*$	V	–	P_4.4.44
Hysteresis of input voltage	V_{ENHY}	–	500	–	mV	²⁾	P_4.4.45
Pull down resistor	R_{PD_EN}	20	40	70	k Ω	$V_{EN} = 0.2 \times V_{DD}$	P_4.4.46
SPI frequency							
Maximum SPI frequency	$f_{SPI,max}$	–	–	5.0	MHz	^{2) 4)}	P_4.4.47
SPI INTERFACE: Delay Time from EN rising edge to first Data in							
Setup time	t_{set}	–	–	150	μs	²⁾ See Figure 12	P_4.4.48
SPI INTERFACE: Input Interface, Logic Inputs SDI, SCLK, CSN							
H-input voltage threshold	V_{IH}	$0.7 \cdot V_{DD}^*$	–	V_{DD}	V	–	P_4.4.50
L-input voltage threshold	V_{IL}	0	–	$0.3 \cdot V_{DD}^*$	V	–	P_4.4.51
Hysteresis of input voltage	V_{IHY}	–	500	–	mV	²⁾	P_4.4.52
Pull up resistor at pin CSN	R_{PU_CSN}	20	40	70	k Ω	$V_{CSN} = 0.7 \times V_{DD}$	P_4.4.53
Pull down resistor at pin SDI, SCLK	R_{PD_SDI} , R_{PD_SCLK}	20	40	70	k Ω	$V_{SDI}, V_{SCLK} = 0.2 \times V_{DD}$	P_4.4.54
Input capacitance at pin CSN, SDI or SCLK	C_I	–	10	15	pF	$0\text{V} < V_{DD} < 5.25\text{V}^2$	P_4.4.55
Input Interface, Logic Output SDO							
H-output voltage level	V_{SDOH}	$V_{DD} - 0.4$	$V_{DD} - 0.2$	V_{DD}	V	$I_{SDOH} = -1.6\text{ mA}$	P_4.4.56
L-output voltage level	V_{SDOL}	0	0.2	0.4	V	$I_{SDOL} = 1.6\text{ mA}$	P_4.4.57
Tri-state Leakage Current	I_{SDOLK}	-1	–	1	μA	$V_{CSN} = V_{DD}$; $0\text{V} < V_{SDO} < V_{DD}$	P_4.4.58
Tri-state input capacitance	C_{SDO}	–	10	15	pF	²⁾	P_4.4.59
Data Input Timing. See Figure 13 and Figure 15.							
SCLK Period	t_{pCLK}	200	–	–	ns	²⁾	P_4.4.60
SCLK High Time	t_{SCLKH}	$0.45 \cdot t_{pCLK}^*$	–	$0.55 \cdot t_{pCLK}^*$	ns	²⁾	P_4.4.61
SCLK Low Time	t_{SCLKL}	$0.45 \cdot t_{pCLK}^*$	–	$0.55 \cdot t_{pCLK}^*$	ns	²⁾	P_4.4.62

General Product Characteristics

Table 5 Electrical Characteristics, $V_S = 5.5\text{ V to }20\text{ V}$, $V_{DD} = 3.0\text{ V to }5.5\text{ V}$, $T_j = -40^\circ\text{C to }+150^\circ\text{C}$, $EN = \text{HIGH}$, $I_{OUTn} = 0\text{ A}$; Typical values refer to $V_{DD} = 5.0\text{ V}$, $V_S = 13.5\text{ V}$ and $T_j = 25^\circ\text{C}$ unless otherwise specified; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified) (cont'd)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
SCLK Low before CSN Low	t_{BEF}	125	–	–	ns	2)	P_4.4.63
CSN Setup Time	t_{lead}	250	–	–	ns	2)	P_4.4.64
SCLK Setup Time	t_{lag}	250	–	–	ns	2)	P_4.4.65
SCLK Low after CSN High	t_{BEH}	125	–	–	ns	2)	P_4.4.66
SDI Setup Time	t_{SDI_setup}	30	–	–	ns	2)	P_4.4.67
SDI Hold Time	t_{SDI_hold}	30	–	–	ns	2)	P_4.4.68
Input Signal Rise Time at pin SDI, SCLK, CSN	t_{rIN}	–	–	50	ns	2)	P_4.4.69
Input Signal Fall Time at pin SDI, SCLK, CSN	t_{fIN}	–	–	50	ns	2)	P_4.4.70
Delay time from EN falling edge to standby mode	t_{DMODE}	–	–	8	μs	2)	P_4.4.71
Minimum CSN High Time	t_{CSNH}	5	–	–	μs	2)	P_4.4.72

Data Output Timing. See Figure 13.

SDO Rise Time	t_{rSDO}	–	30	80	ns	$C_{load} = 40\text{pF}^{2)}$	P_4.4.73
SDO Fall Time	t_{fSDO}	–	30	80	ns	$C_{load} = 40\text{pF}^{2)}$	P_4.4.74
SDO Enable Time after CSN falling edge	t_{ENSDO}	–	–	75	ns	Low Impedance ²⁾	P_4.4.75
SDO Disable Time after CSN rising edge	t_{DISSDO}	–	–	75	ns	High Impedance ²⁾	P_4.4.76
Duty cycle of incoming clock at SCLK	$duty_{SCLK}$	45	–	55	%	2)	P_4.4.77
SDO Valid Time for $V_{DD} = 3.3\text{ V}$	t_{VASDO3}	–	70	95	ns	$V_{SDO} < 0.2 \times V_{DD}$ $V_{SDO} > 0.8 \times V_{DD}$ $C_{load} = 40\text{pF}^{2)}$	P_4.4.78
SDO Valid Time for $V_{DD} = 5\text{ V}$	t_{VASDO5}	–	50	65	ns	$V_{SDO} < 0.2 \times V_{DD}$ $V_{SDO} > 0.8 \times V_{DD}$ $C_{load} = 40\text{pF}^{2)}$	P_4.4.79

Thermal warning & Shutdown

Thermal warning junction temperature	T_{jW}	120	135	150	$^\circ\text{C}$	See Figure 9 ²⁾	P_4.4.80
Thermal shutdown junction temperature	T_{jSD}	160	175	190	$^\circ\text{C}$	See Figure 9 ²⁾	P_4.4.81
Thermal comparator hysteresis	T_{jHYS}	–	4	–	$^\circ\text{C}$	2)	P_4.4.82
Difference between $T_{jSD} - T_{jW}$	$T_{jSD} - T_{jW}$	–	40	–	$^\circ\text{C}$	2)	P_4.4.120

1) I_{S_HSON} does not include the load current

2) Not subject to production test, specified by design

General Product Characteristics

- 3) Measured for 20% - 80% of V_S .
- 4) Not applicable in daisy chain configuration

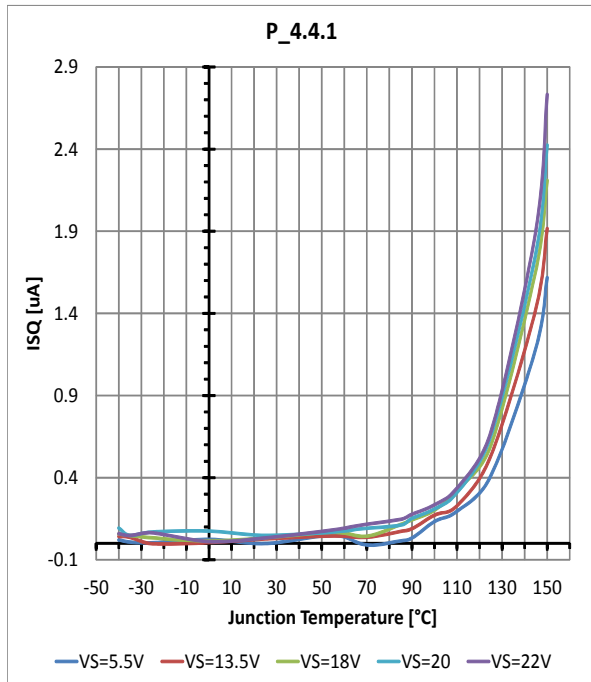
Characterization results

4 Characterization results

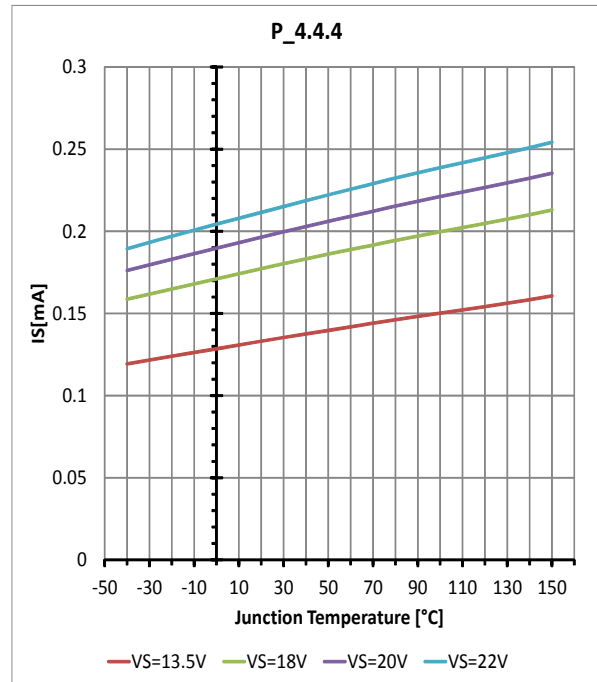
Performed on 5 devices, over operating temperature and nominal/extended supply range.

Typical performance characteristics

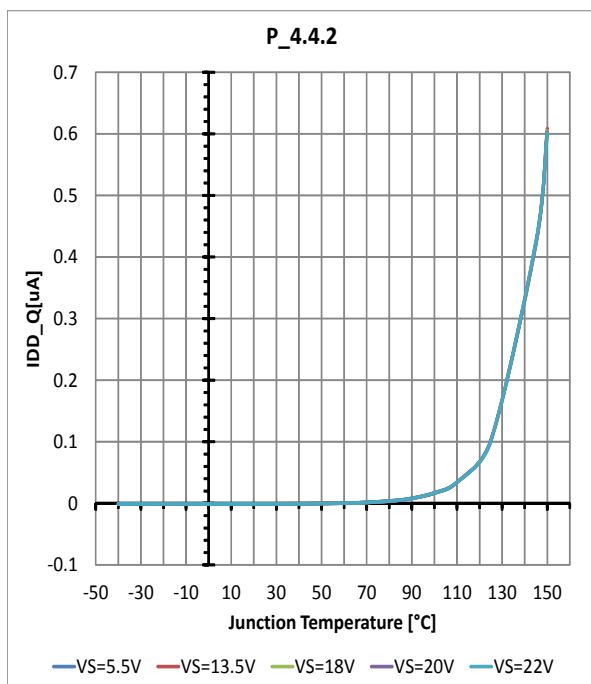
Supply quiescent current



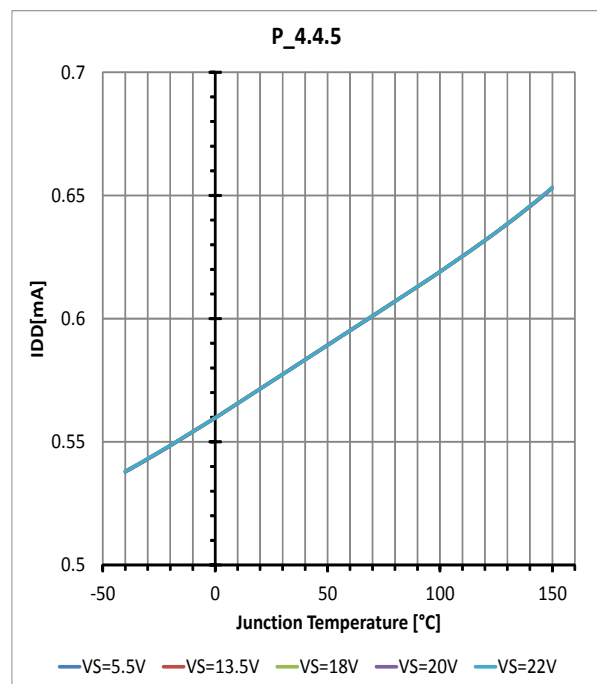
Supply current



Logic supply quiescent current

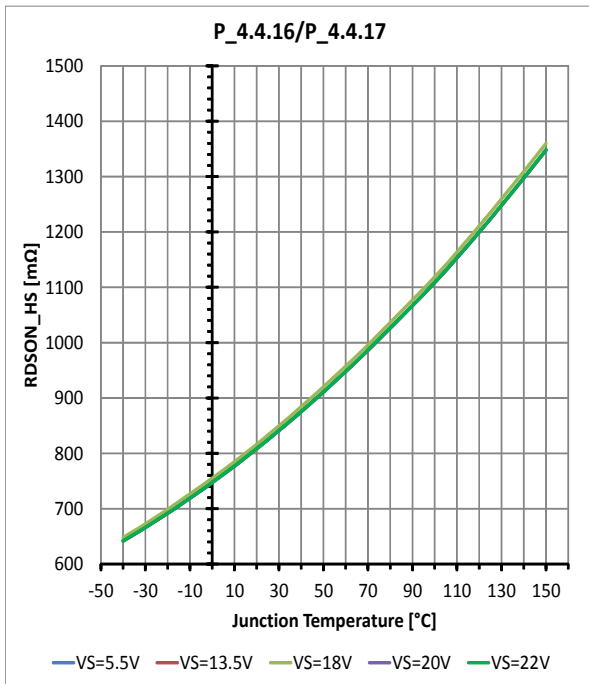


Logic supply current

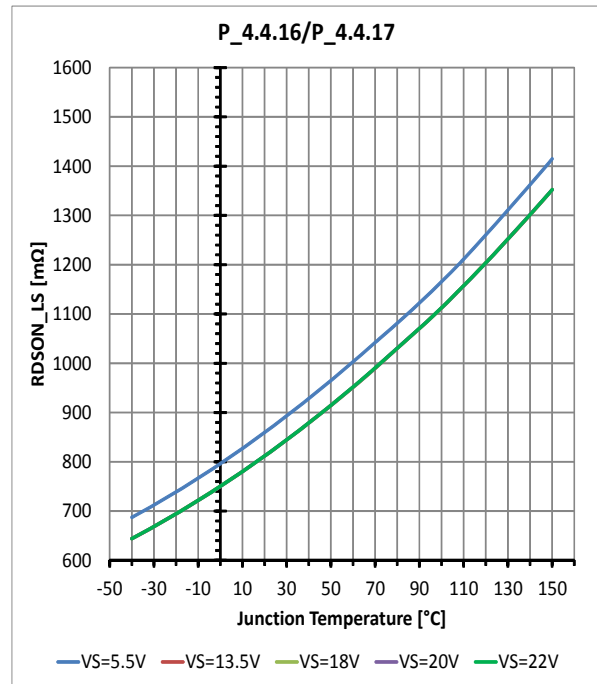


Characterization results

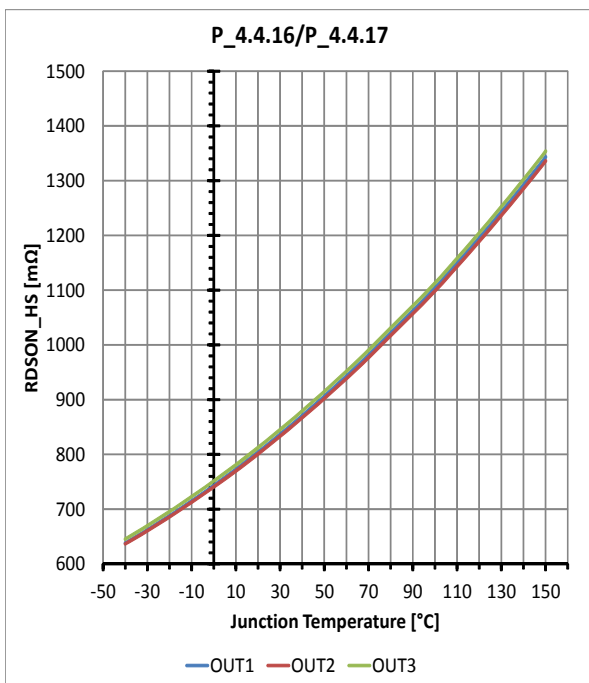
HS static Drain-source ON-resistance



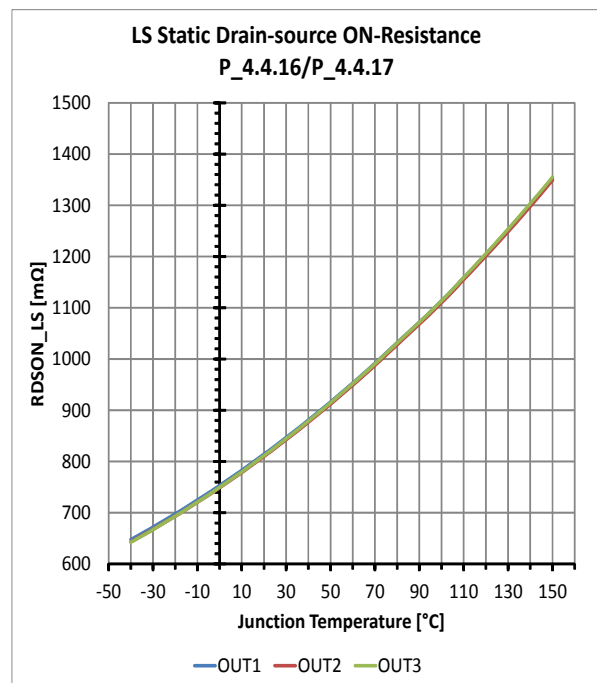
LS static Drain-source ON-resistance



HS static drain-source ON-resistance
VS = 13.5V and VDD = 5V

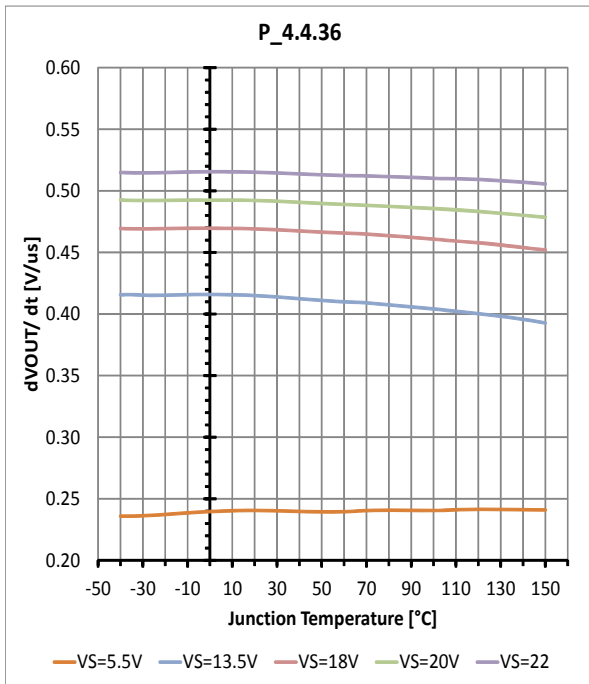


LS static drain-source ON-resistance
VS = 13.5V and VDD = 5V

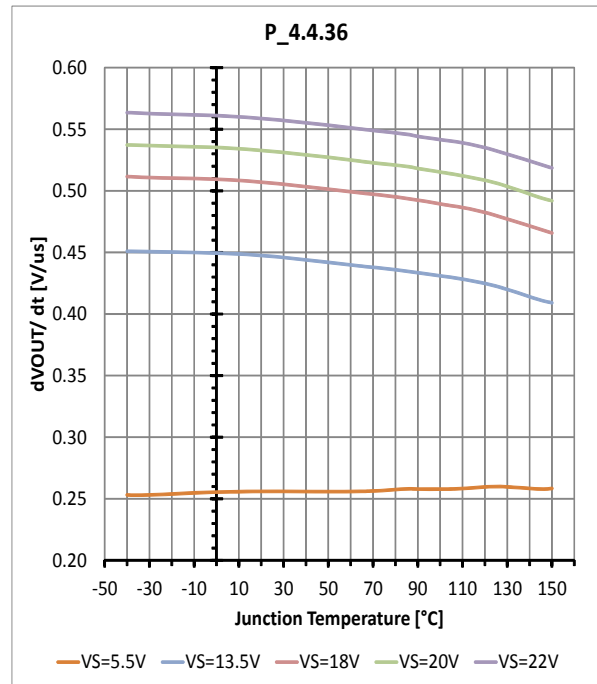


Characterization results

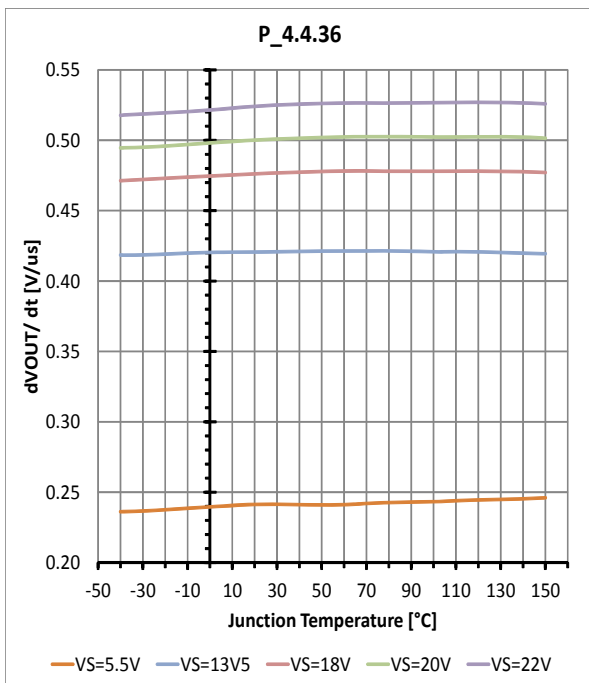
Slew rate ON of high-side outputs



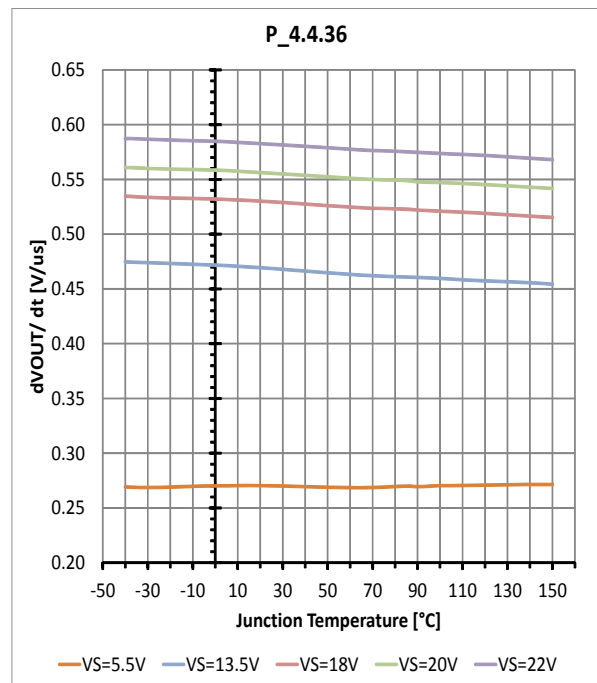
Slew rate ON of low-side outputs



Slew rate OFF of high-side outputs

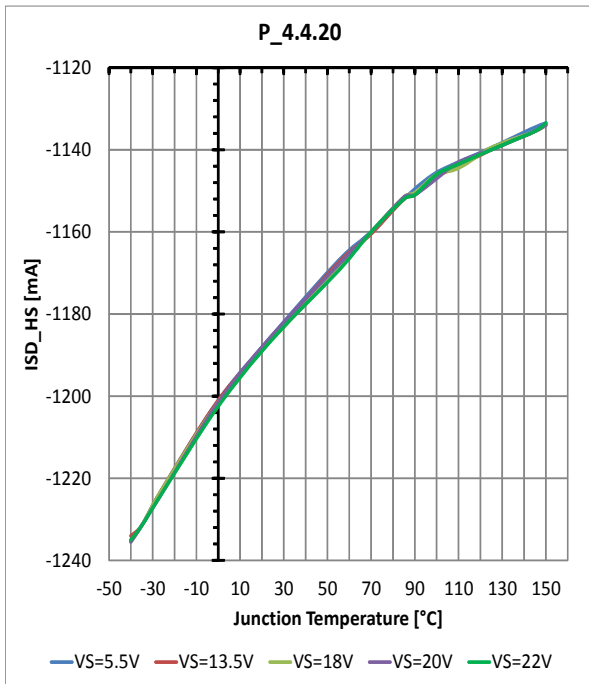


Slew rate OFF of low-side outputs

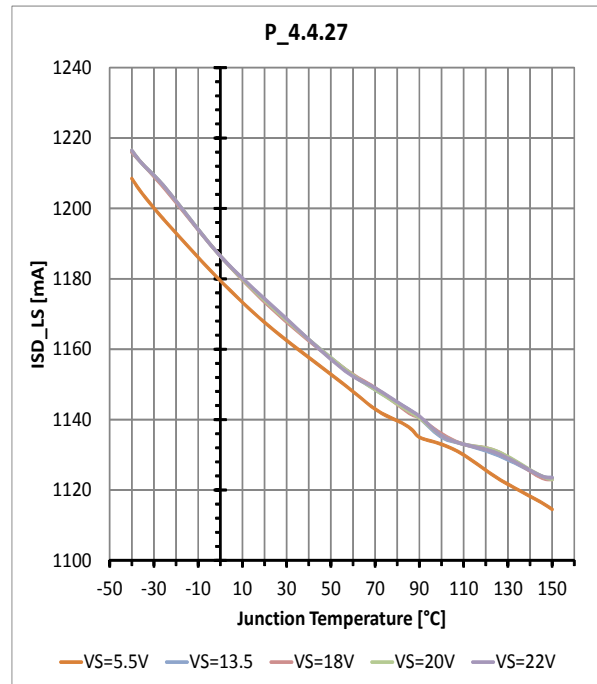


Characterization results

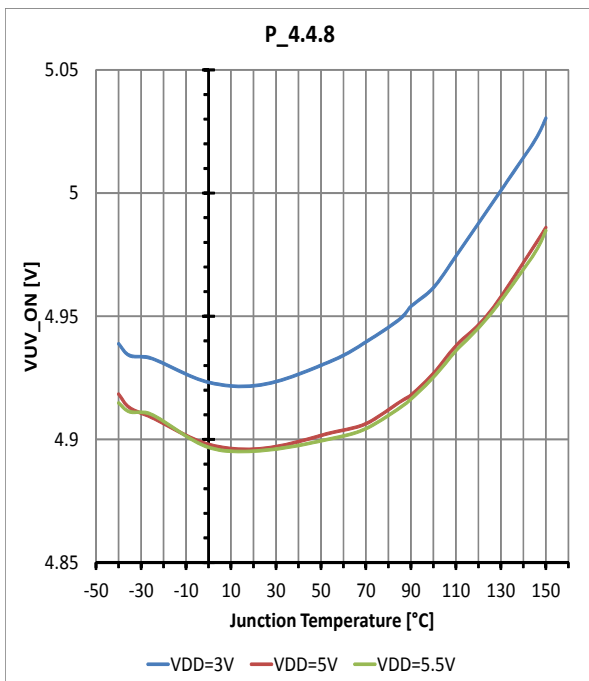
HS overcurrent shutdown threshold



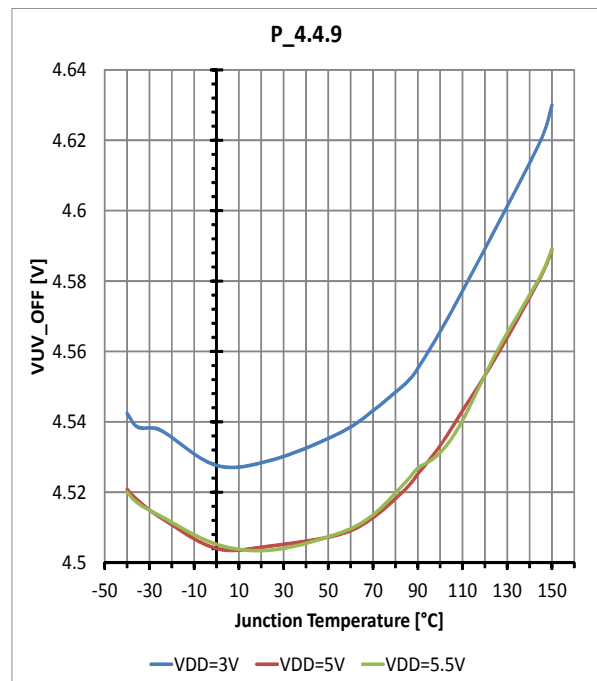
LS overcurrent shutdown threshold



Undervoltage switch ON voltage threshold

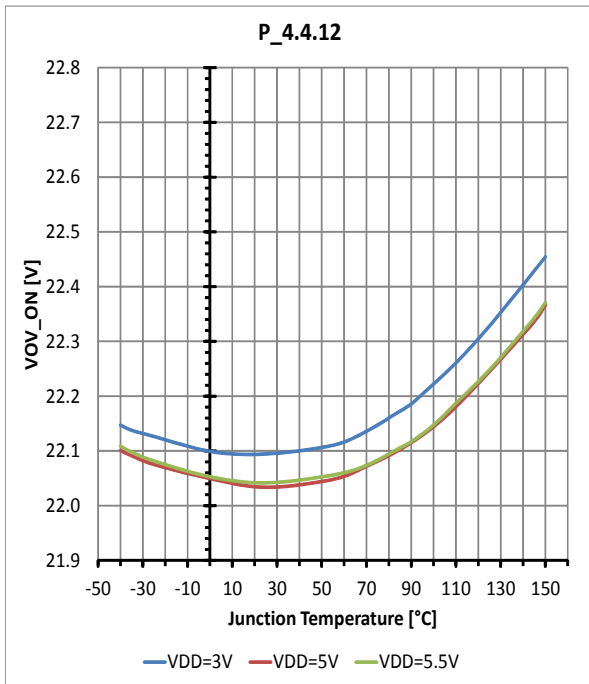


Undervoltage switch OFF voltage threshold

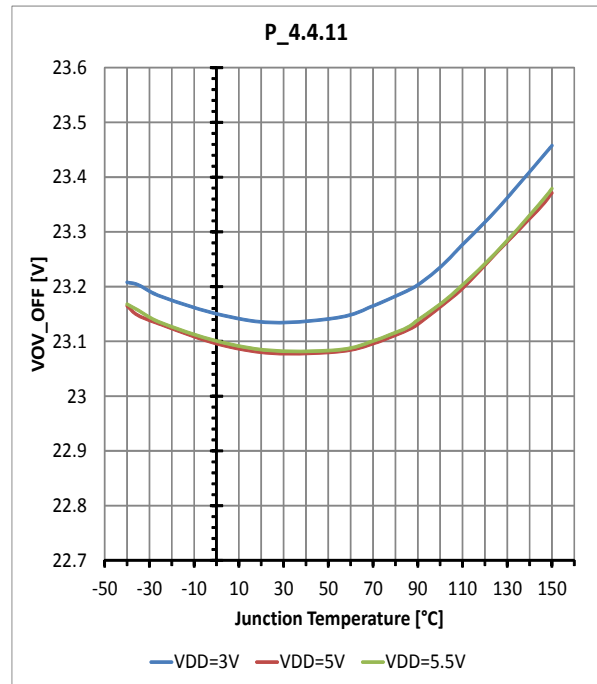


Characterization results

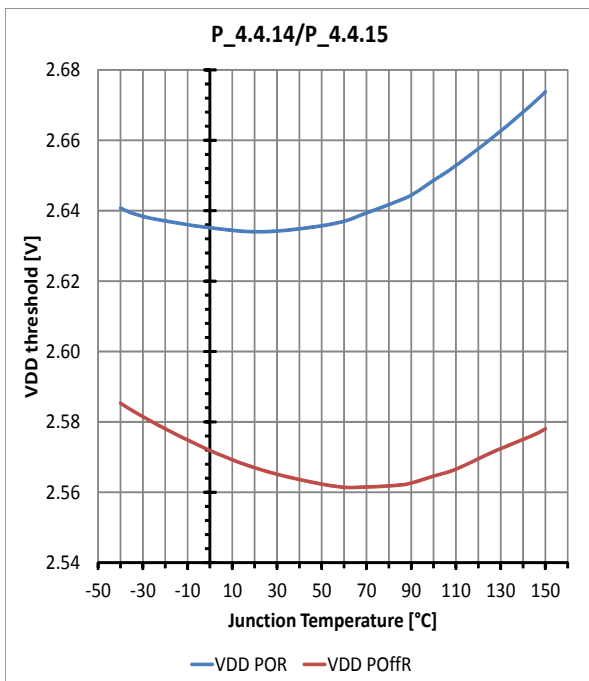
Overvoltage switch ON voltage threshold



Overvoltage switch OFF voltage threshold



VDD Power-on-reset and VDD Power-off-reset



General Description

5 General Description

5.1 Power Supply

The TLE94104EP has two power supply inputs, V_S and V_{DD} . The half bridge outputs are supplied by V_S , which is connected to the 12V automotive supply rail. V_{DD} is used to supply the I/O buffers and internal voltage regulator of the device.

V_S and V_{DD} supplies are separated so that information stored in the logic block remains intact in the event of voltage drop outs or disturbances on V_S . The system can therefore continue to operate once V_S has recovered, without having to resend commands to the device.

A rising edge on V_{DD} crossing V_{DD_POR} triggers an internal Power-On Reset (POR) to initialize the IC at power-on. All data stored internally is deleted, and the outputs are switched off (high impedance).

An electrolytic and 100nF ceramic capacitors are recommended to be placed as close as possible to the V_S supply pin of the device for improved EMC performance in the high and low frequency band. The electrolytic capacitor must be dimensioned to prevent the V_S voltage from exceeding the absolute maximum rating. In addition, decoupling capacitors are recommended on the V_{DD} supply pin.

5.2 Operation modes

5.2.1 Normal mode

The TLE94104EP enters normal mode by setting the EN input High. In normal mode, the charge pump is active and all output transistors can be configured via SPI.

5.2.2 Sleep mode

The TLE94104EP enters sleep mode by setting the EN input Low. The EN input has an internal pull-down resistor.

In sleep mode, all output transistors are turned off and the SPI register banks are reset. The current consumption is reduced to $I_{SQ} + I_{DD_Q}$.

5.3 Reset Behaviour

The following reset triggers have been implemented in the TLE94104EP:

V_{DD} Undervoltage Reset:

The SPI Interface shall not function if V_{DD} is below the undervoltage threshold, V_{DD_POFFR} . The digital block will be deactivated, the logic contents cleared and the output stages are switched off. The digital block is initialized once V_{DD} voltage levels is above the undervoltage threshold, V_{DD_POR} . Then the NPOR bit is reset (NPOR = 0 in **SYS_DIAG1** and Global Status Register).

Reset on EN pin:

If the EN pin is pulled Low, the logic content is reset and the device enters sleep mode.

The reset event is reported by the NPOR bit (NPOR = 0) once the TLE94104EP is in normal mode (EN = High; $V_{DD} > V_{DD_POR}$).

General Description

5.4 Reverse Polarity Protection

The TLE94104EP requires an external reverse polarity protection. During reverse polarity, the free-wheeling diodes across the half bridge output will begin to conduct, causing an undesired current flow (I_{RB}) from ground potential to battery and excessive power dissipation across the diodes. As such, a reverse polarity protection diode is recommended (see [Figure 4](#)).

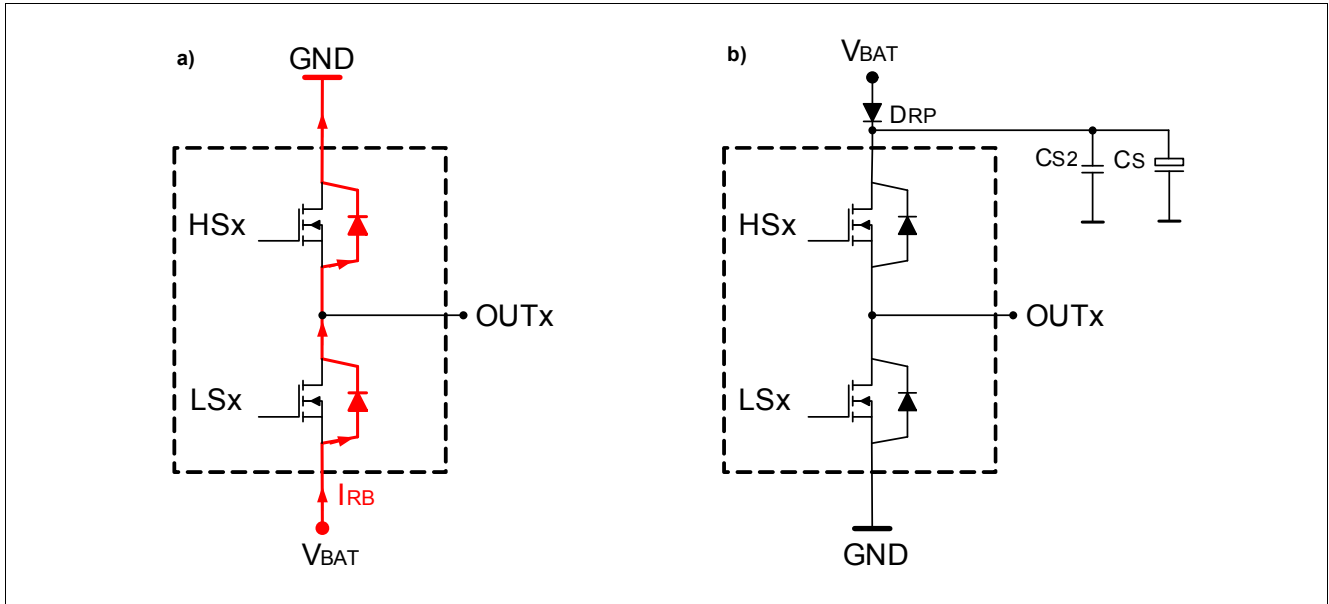


Figure 4 Reverse Polarity Protection

6 Half-Bridge Outputs

6.1 Functional Description

The half-bridge outputs of the TLE94104EP are intended to drive motor loads.

If the outputs are driven continuously via SPI, for example HS1 and LS2 used to drive a motor, then the following suggested SPI commands shall be sent:

- Activate HS1: Bit HB1_HS_EN in HB_ACT_1_CTRL register
- Activate LS2: Bit HB2_LS_EN in HB_ACT_1_CTRL register

Half-Bridge Outputs

6.2 Protection & Diagnosis

The TLE94104EP is equipped with an SPI interface to control and diagnose the state of the half-bridge drivers. This device has embedded protective functions which are designed to prevent IC destruction under fault conditions described in the following sections. Fault conditions are treated as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

The following table provides a summary of fault conditions, protection mechanisms and recovery states embedded in the TLE94104EP device.

Table 6 Summary of diagnosis and monitoring of outputs

Fault condition	Error Flag (EF) behaviour	Error bit: Status Register	Output Protection mechanism	Output error state	Output and error flag (EF) recovery
Overcurrent	Latch	1. Load Error bit, LE (bit 6) in SYS_DIAG 1: Global Status 1 Register 2. Localized error for each HS and LS channel of half-bridge, HBn_HS_OC and HBn_LS_OC bits in SYS_DIAG_2 status register.	Error output shutdown and latched	High-Z	Half-bridge control bits remain set despite error, however the output stage is shutdown. Clear EF to reactivate output stage.
Open load	Latch	1. Load Error bit, LE (bit 6) in SYS_DIAG 1: Global Status 1 Register 2. Localized error for each HS and LS channel of half-bridge, HBn_HS_OL and HBn_LS_OL bits in SYS_DIAG3 status register.	None	No state change	An open load detection does not change the state of the output. EF to be cleared.
Temperature pre-warning	Latch	Global error bit 1, TPW in SYS_DIAG_1: Global Status 1 register	None	No state change	Not applicable
Temperature shutdown	Latch	Global error bit 2, TSD in SYS_DIAG_1: Global Status 1 register	All outputs shutdown and latched.	High-Z	Half-bridge control bits remain set despite error, however the output stage is shutdown. Clear EF to reactivate output stage.