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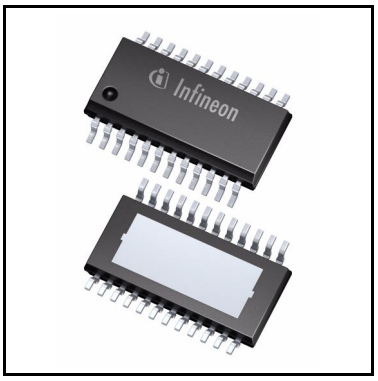
TLE94112EL



Features

- Twelve half bridge power outputs
- Very low power consumption in sleep mode
- 3.3V / 5V compatible inputs with hysteresis
- All outputs with overload and short circuit protection
- Independently diagnosable outputs (overcurrent, open load)
- Open load diagnostics in ON-state for all high-side and low-side
- Outputs with selectable open load thresholds (HS1, HS2)
- 16-bit Standard SPI interface with daisy chain and in-frame response capability for control and diagnosis
- Fast diagnosis with the global error flag
- PWM capable outputs for frequencies 80Hz, 100Hz and 200Hz with 8-bit duty cycle resolution
- Overtemperature pre-warning and protection
- Over- and Undervoltage lockout
- Cross-current protection

Applications

- HVAC Flap DC motors
- Monostable and bistable Relays
- Side mirror x-y adjustment and mirror fold
- LEDs

Description

The TLE94112EL is a protected twelve-fold half-bridge driver designed especially for automotive motion control applications such as Heating, Ventilation and Air Conditioning (HVAC) flap DC motor control. It is part of a larger family offering half-bridge drivers from three outputs to twelve outputs with direct interface or SPI interface.

The half bridge drivers are designed to drive DC motor loads in sequential or parallel operation. Operation modes forward (cw), reverse (ccw), brake and high impedance are controlled from a 16-bit SPI interface. It offers diagnosis features such as short circuit, open load, power supply failure and overtemperature detection. In combination with its low quiescent current, this device is attractive among others for automotive applications. The small fine pitch exposed pad package, PG-SSOP-24, provides good thermal performance and reduces PCB-board space and costs.

Type	Package	Marking
TLE94112EL	PG-SSOP-24	TLE94112EL

Table 1 Product Summary

Normal Operating Voltage	V_S	5.5 ... 18 V
Extended Operating Voltage	V_S	18 ... 20 V
Logic Supply Voltage	V_{DD}	3.0 ... 5.5 V
Maximum Supply Voltage for Load Dump Protection	$V_{S(LD)}$	40 V
Minimum Overcurrent Threshold	I_{SD}	0.9 A
Maximum On-State Path Resistance at T_j = 150°C	$R_{DSON(total)\_HSx+LSy}$	1.8 + 1.8 Ω
Typical Quiescent Current at T_j = 85°C	I_{SQ}	0.1 µA
Maximum SPI Access Frequency	f_{SCLK}	5 MHz

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1 Pin Configuration

1.1 Pin Assignment

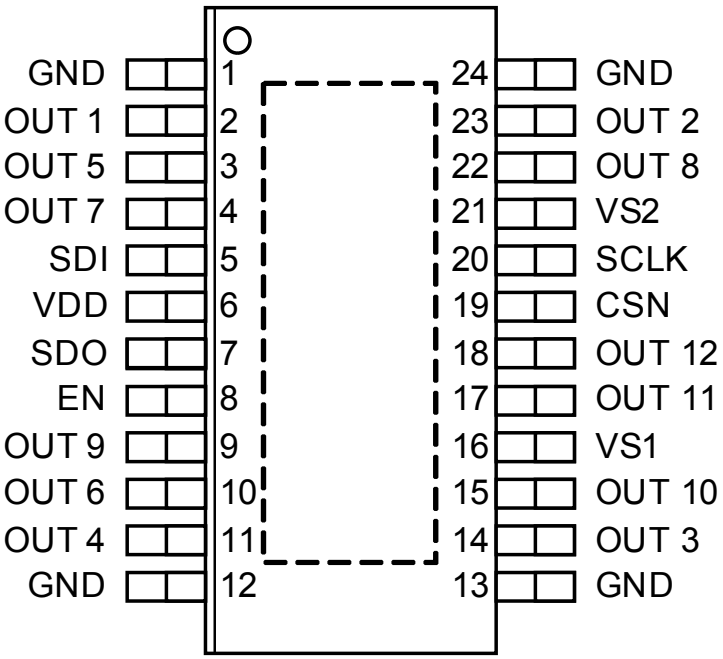


Figure 1 Pin Configuration TLE94112EL

1.2 Pin Definitions and Functions

Pin	Symbol	Function
1	GND	Ground. All ground pins should be externally connected together.
2	OUT 1	Power half-bridge 1
3	OUT 5	Power half-bridge 5
4	OUT 7	Power half-bridge 7
5	SDI	Serial data input with internal pull down
6	VDD	Logic supply voltage
7	SDO	Serial data output
8	EN	Enable with internal pull-down; Places device in standby mode by pulling the EN line Low
9	OUT 9	Power half-bridge 9
10	OUT 6	Power half-bridge 6
11	OUT 4	Power half-bridge 4
12	GND	Ground. All ground pins should be externally connected together.

Pin Configuration

Pin	Symbol	Function
13	GND	Ground. All ground pins should be externally connected together.
14	OUT 3	Power half-bridge 3
15	OUT 10	Power half-bridge 10
16	VS1	Main supply voltage for power half bridges. VS1 should be externally connected to VS2.
17	OUT 11	Power half-bridge 11
18	OUT 12	Power half-bridge 12
19	CSN	Chip select Not input with internal pull up
20	SCLK	Serial clock input with internal pull down
21	VS2	Main supply voltage for power half bridges. VS1 should be externally connected to VS2.
22	OUT 8	Power half-bridge 8
23	OUT 2	Power half-bridge 2
24	GND	Ground. All ground pins should be externally connected together.
EDP	-	Exposed Die Pad; For cooling and EMC purposes only - not usable as electrical ground. Electrical ground must be provided by pins 1,12,13,24. [1)]

1) The exposed die pad at the bottom of the package allows better heat dissipation from the device via the PCB. The exposed pad (EP) must be either left open or connected to GND. It is recommended to connect EP to GND for best EMC and thermal performance.

2 Block Diagram

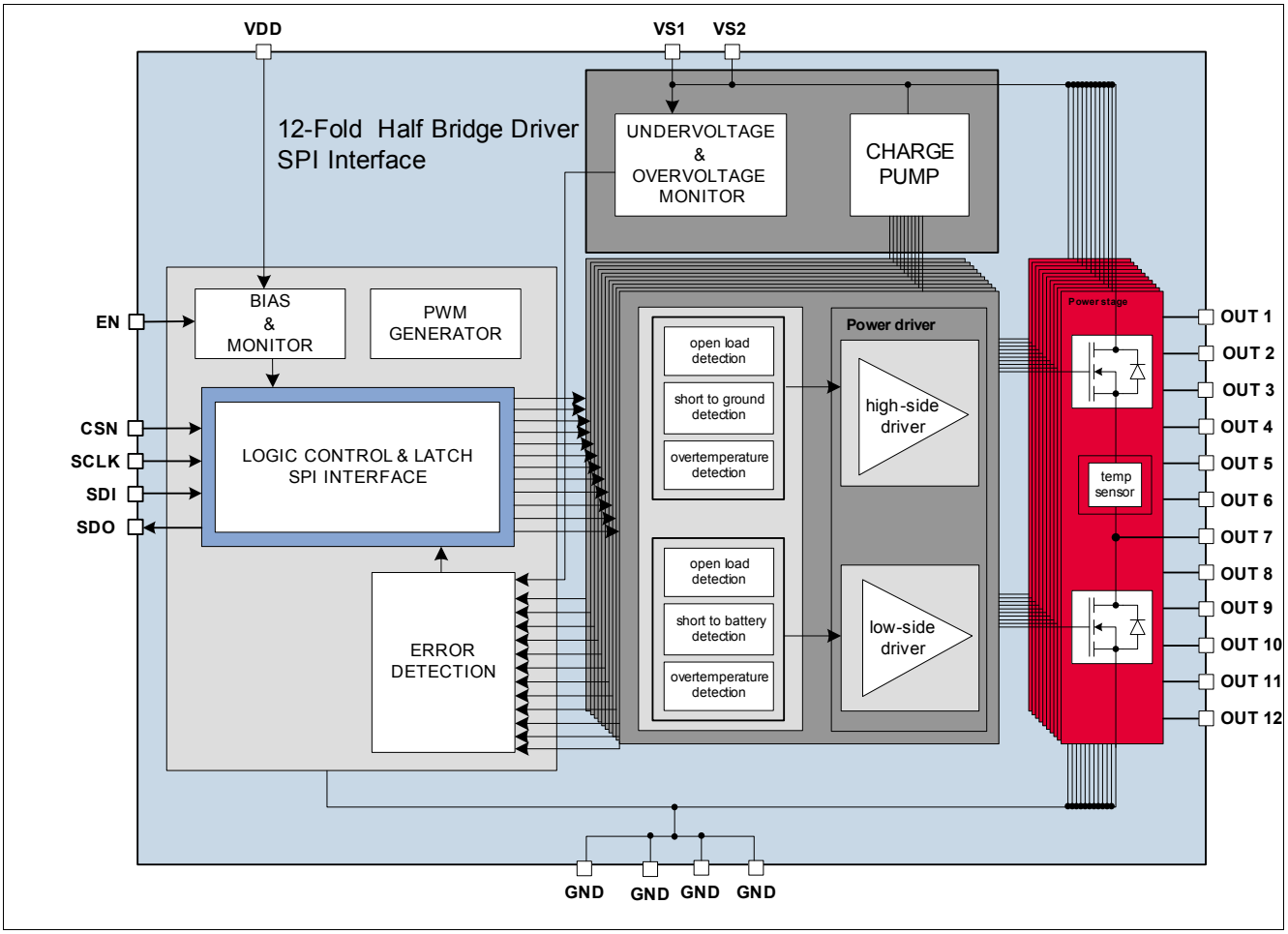


Figure 2 Block Diagram TLE94112EL (SPI Interface)

2.1 Voltage and current definition

Figure 3 shows terms used in this datasheet, with associated convention for positive values.

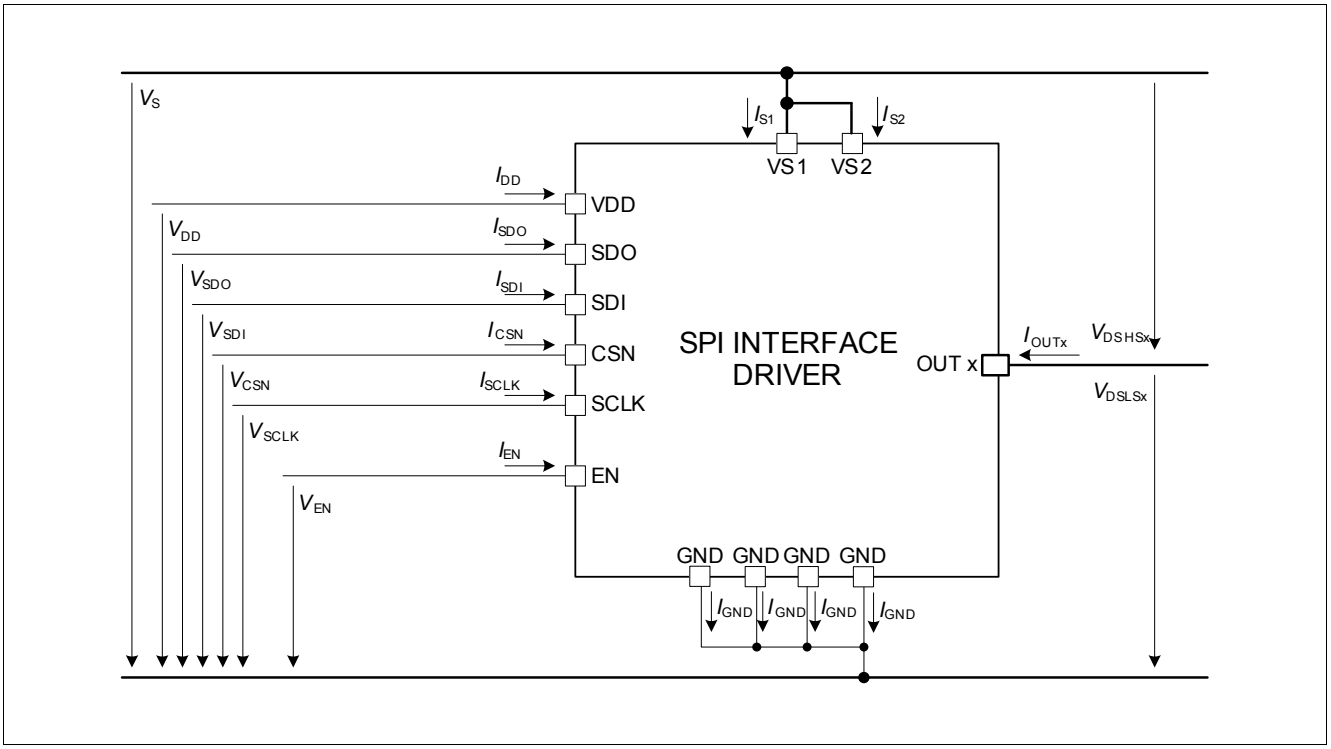


Figure 3 Voltage and Current Definition

3 General Product Characteristics

3.1 Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings[1] T_j = -40°C to +150°C

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Voltages							
Supply voltage	V_S	-0.3	–	40	V	$V_S = V_{S1} = V_{S2}$	P_4.1.1
Supply Voltage Slew Rate	$\lvert dV_S/dt \rvert$	–	–	10	V/µs	V_S increasing and decreasing [1]	P_4.2.2
Power half-bridge output voltage	V_{OUT}	-0.3	–	40	V	$0\ V < V_{OUT} < V_S$	P_4.1.2
Logic supply voltage	V_{DD}	-0.3	–	5.5	V	$0\ V < V_S < 40\ V$	P_4.1.3
Logic input voltages (SDI, SCLK, CSN, EN)	V_{SDI}, V_{SCLK}, V_{CSN}, V_{EN}	-0.3	–	VDD	V	$0\ V < V_S < 40\ V$ $0\ V < V_{DD} < 5.5V$	P_4.1.4
Logic output voltage (SDO)	V_{SDO}	-0.3	–	VDD	V	$0\ V < V_S < 40\ V$ $0\ V < V_{DD} < 5.5V$	P_4.1.5
Currents							
Continuous Supply Current for V_{S1}	I_{S1}	0	–	3.0	A	–	P_4.1.6
Continuous Supply Current for V_{S2}	I_{S2}	0	–	3.0	A	–	P_4.1.7
Current per GND pin	I_{GND}	0	–	2.0	A	–	P_4.1.14
Output Currents	I_{OUT}	-2.0	–	2.0	A	–	P_4.1.15
Temperatures							
Junction temperature	T_j	-40	–	150	°C	–	P_4.1.8
Storage temperature	T_{stg}	-50	–	150	°C	–	P_4.1.9
ESD Susceptibility							
ESD susceptibility OUTn and VSx pins versus GND. All other pins grounded.	V_{ESD}	-8	–	8	kV	JEDEC HBM[1)2)]	P_4.1.10
ESD susceptibility all pins	V_{ESD}	-2	–	2	kV	JEDEC HBM[1)2)]	P_4.1.11
ESD susceptibility all pins	V_{ESD}	-500	–	500	V	CDM[1)3)]	P_4.1.12
ESD susceptibility corner pins	V_{ESD}	-750	–	750	V	CDM[1)3)]	P_4.1.13

1) Not subject to production test, specified by design

2) ESD susceptibility, “JEDEC HBM” according to ANSI/ ESDA/ JEDEC JS001 (1.5 kΩ, 100pF)

3) ESD susceptibility, Charged Device Model “CDM” according JEDEC JESD22-C101

Notes

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.*

3.2 Functional Range

Table 3 Functional Range

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Supply voltage range for normal operation	$V_{S(nor)}$	5.5	–	18	V	–	P_4.2.1
Extended supply voltage range	$V_{S(ext)}$	18	–	20	V	1)2)	P_4.2.7
Logic supply voltage range for normal operation	V_{DD}	3.0	–	5.5	V	–	P_4.2.3
Logic input voltages (SDI, SCLK, CSN, EN)	V_{SDI}, V_{SCLK}, V_{CSN}, V_{EN}	-0.3	–	5.5	V	–	P_4.2.4
Junction temperature	T_j	-40	–	150	°C		P_4.2.5

1) Not subject to production test, specified by design.

2) In the extended supply range, the device is still functional. However, deviations of the specified electrical characteristics are possible.

Note: Within the normal functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

3.3 Thermal Resistance

Table 4 Thermal Resistance TLE94112EL

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction to Case, T_A = -40°C	R_{thjC_cold}	–	5	–	K/W	1)	
Junction to Case, T_A = 85°C	R_{thjC_hot}	–	6	–	K/W	1)	
Junction to ambient, T_A = -40°C (1s0p, minimal footprint)	$R_{thjA\_cold\_min}$	–	69	–	K/W	1) 2)	
Junction to ambient, T_A = 85°C (1s0p, minimal footprint)	$R_{thjA\_hot\_min}$	–	70	–	K/W	1) 2)	
Junction to ambient, T_A = -40°C (1s0p, 300mm2 Cu)	$R_{thjA\_cold\_300}$	–	41	–	K/W	1) 3)	
Junction to ambient, T_A = 85°C (1s0p, 300mm2 Cu)	$R_{thjA\_hot\_300}$	–	44	–	K/W	1) 3)	
Junction to ambient, T_A = -40°C (1s0p, 600mm2 Cu)	$R_{thjA\_cold\_600}$	–	40	–	K/W	1) 4)	
Junction to ambient, T_A = 85°C (1s0p, 600mm2 Cu)	$R_{thjA\_hot\_600}$	–	43	–	K/W	1) 4)	
Junction to ambient, T_A = -40°C (2s2p)	$R_{thjA\_cold\_2s2p}$	–	24	–	K/W	1) 5)	
Junction to ambient, T_A = 85°C (2s2p)	$R_{thjA\_hot\_2s2p}$	–	29	–	K/W	1) 5)	

1) Not subject to production test, specified by design.

2) Specified R_{thJA} value is according to JEDEC JESD51-2, -3 at natural convection on FR4 1s0p board; The product (chip + package) was simulated on a 76.2 x 114.3 x 1.5mm board with minimal footprint copper area and 35µm thickness. Ta = -40°C, each channel dissipates 0.2W. Ta = 85°C, each channel dissipates 0.135W.

3) Specified R_{thJA} value is according to JEDEC JESD51-2, -3 at natural convection on FR4 1s0p board; The product (chip + package) was simulated on a 76.2 x 114.3 x 1.5mm board with additional cooling of 300mm2 copper area and 35µm thickness. Ta = -40°C, each channel dissipates 0.2W. Ta = 85°C, each channel dissipates 0.135W.

4) Specified R_{thJA} value is according to JEDEC JESD51-2, -3 at natural convection on FR4 1s0p board; The product (chip + package) was simulated on a 76.2 x 114.3 x 1.5mm board with additional cooling of 600mm2 copper area and 35µm thickness. Ta = -40°C, each channel dissipates 0.2W. Ta = 85°C, each channel dissipates 0.135W.

5) Specified R_{thJA} value is according to JEDEC JESD51-2, -3 at natural convection on FR4 2s2p board; The product (chip + package) was simulated on a 76.2 x 114.3 x 1.5mm board with two inner copper layers (4 x 35µm Cu). Ta = -40°C, each channel dissipates 0.2W. Ta = 85°C, each channel dissipates 0.135W.

3.4 Electrical Characteristics

Table 5 Electrical Characteristics, V_S =5.5 V to 18 V, V_{DD} = 3.0V to 5.5V, T_j = -40°C to +150°C, EN= HIGH, I_{OUTn}= 0 A; Typical values refer to V_{DD} = 5.0 V, V_S = 13.5 V and T_J = 25 °C unless otherwise specified; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Current Consumption, EN = GND							
Supply Quiescent current	I_{SQ}	–	0.5	2	µA	-40°C ≤ T_j ≤ 85°C	P_4.4.1
Logic supply quiescent current	I_{DD_Q}	–	0.1	1	µA	-40°C ≤ T_j ≤ 85°C	P_4.4.2
Total quiescent current	I_{SQ} + I_{DD_Q}	–	0.6	3	µA	-40°C ≤ T_j ≤ 85°C	P_4.4.3
Current Consumption, EN=HIGH							
Supply current	I_S	–	0.5	1	mA	Power drivers and power stages are off	P_4.4.4
Supply current	I_{S_HSON}	–	4.5	9	mA	All high-sides ON[1)]	P_4.4.101
Logic supply current	I_{DD}	–	1.5	3	mA	SPI not active	P_4.4.5
Logic supply current	I_{DD_RUN}	–	5	–	mA	SPI 5MHz [3)]	P_4.4.6
Total supply current	I_S + I_{DD_RUN}	–	5.5	–	mA	SPI 5MHz [3)]	P_4.4.7
Over- and Undervoltage Lockout							
Undervoltage Switch ON voltage threshold	$V_{UV\ ON}$	4.25	–	5.25	V	V_S increasing	P_4.4.8
Undervoltage Switch OFF voltage threshold	$V_{UV\ OFF}$	4	–	5.0	V	V_S decreasing	P_4.4.9
Undervoltage Switch ON/OFF hysteresis	$V_{UV\ HY}$	–	0.25	–	V	$V_{UV\ ON}$ - $V_{UV\ OFF}$ [3)]	P_4.4.10
Overvoltage Switch OFF voltage threshold	$V_{OV\ OFF}$	21	–	25	V	V_S increasing	P_4.4.11
Overvoltage Switch ON voltage threshold	$V_{OV\ ON}$	20	–	24	V	V_S decreasing	P_4.4.12
Overvoltage Switch ON/OFF hysteresis	$V_{OV\ HY}$	–	1	–	V	$V_{OV\ OFF}$ - $V_{OV\ ON}$ [3)]	P_4.4.13
V_{DD} Power-On-Reset	$V_{DD\ POR}$	2.40	2.70	2.90	V	V_{DD} increasing	P_4.4.14
V_{DD} Power-Off-Reset	$V_{DD\ POffR}$	2.35	2.65	2.85	V	V_{DD} decreasing	P_4.4.15
V_{DD} Power ON/OFF hysteresis	$V_{DD\ POR\ HY}$	–	0.05	–	V	$V_{DD\ POR}$ - $V_{DD\ POffR}$ [3)]	P_4.4.98
Static Drain-source ON-Resistance (High-Side or Low-Side)							
High-Side or Low-Side R_{DSON} (all outputs)	$R_{DSON\_HB\_25C}$	–	850	1200	mΩ	I_{OUT} = ±0.5 A; T_j = 25 °C	P_4.4.16
High-Side or Low-Side R_{DSON} (all outputs)	$R_{DSON\_HB\_150C}$	–	1400	1800	mΩ	I_{OUT} = ±0.5 A; T_j = 150 °C	P_4.4.17

Table 5 Electrical Characteristics, V_S =5.5 V to 18 V, V_{DD} = 3.0V to 5.5V, T_j = -40°C to +150°C, EN= HIGH, I_{OUTn}= 0 A; Typical values refer to V_{DD} = 5.0 V, V_S = 13.5 V and T_J = 25 °C unless otherwise specified; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified) (cont'd)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
High-Side R_{DSON} (HS1 and HS2 in LED mode)	$R_{DSON\_HI\_HB\_25C}$	–	950	1300	mΩ	2) I_{OUT} = ±0.1 A; T_j = 25 °C	P_4.4.18
High-Side R_{DSON} (HS1 and HS2 in LED mode)	$R_{DSON\_HI\_HB\_150C}$	–	1500	2000	mΩ	2) I_{OUT} = ±0.1 A; T_j = 150 °C	P_4.4.19
Output Protection and Diagnosis of high-side (HS) channels of half-bridge output							
HS Overcurrent Shutdown Threshold	I_{SD_HS}	-1.4	-1.1	-0.9	A	See **Figure 7**	P_4.4.89
Difference between shutdown and limit current	I_{LIM_HS} - I_{SD_HS}	-1.2	-0.6	0	A	3) $\|I_{LIM\_HS}\| \geq \|I_{SD\_HS}\|$ See **Figure 7**	P_4.4.21
Overcurrent Shutdown filter time	t_{dSD_HS}	15	19	23	µs	3)	P_4.4.22
Open Load Detection Current	I_{OLD1_HS}	-15	-8	-3	mA	-	P_4.4.23
Open Load Detection filter time	t_{OLD1_HS}	2000	3000	4000	µs	3)	P_4.4.24
Open Load Detection Current for LED mode (HS1 & HS2)	$I_{OLD2\_HS1,2}$	-3.2	-2	-0.5	mA	Bit OL_SEL_HS1 = 1, OL_SEL_HS2 = 1	P_4.4.25
Open Load Detection filter time for LED mode (HS1 & HS2)	$t_{OLD2\_HS1,2}$	100	200	300	µs	Bit OL_SEL_HS1 = 1, OL_SEL_HS2 = 1; 3)	P_4.4.26
Output Protection and Diagnosis of low-side (LS) channels of half-bridge output							
LS Overcurrent Shutdown Threshold	I_{SD_LS}	0.9	1.1	1.4	A	**Figure 8**	P_4.4.104
Difference between shutdown and limit current	I_{LIM_LS} - I_{SD_LS}	0	0.6	1.2	A	3) $I_{LIM\_LS} \geq I_{SD\_LS}$ **Figure 8**	P_4.4.28
Overcurrent Shutdown filter time	t_{dSD_LS}	15	19	23	µs	3)	P_4.4.29
Open Load Detection Current	I_{OLD_LS}	3	8	15	mA	-	P_4.4.30
Open Load Detection filter time	t_{OLD_LS}	2000	3000	4000	µs	3)	P_4.4.31
Outputs OUT(1...n) leakage current							
HS leakage current in off state	I_{QLHn_NOR}	-2	-0.5	–	µA	V_{OUTn} = 0V ; EN=High	P_4.4.32
HS leakage current in off state	I_{QLHn_SLE}	-2	-0.5	–	µA	V_{OUTn} = 0V; EN=GND	P_4.4.33
LS Leakage current in off state	I_{QLLn_NOR}	–	0.5	2	µA	V_{OUTn} = V_S ; EN=High	P_4.4.34
LS Leakage current in off state	I_{QLLn_SLE}	–	0.5	2	µA	V_{OUTn} = V_S ; EN=GND	P_4.4.35
Output Switching Times. See Figure 9 and Figure 10.							
Slew rate of high-side and low-side outputs	d_{VOUT}/dt	0.1	0.45	0.75	V/µs	Resistive load = 100Ω; V_S=13.5V 4)	P_4.4.36

Table 5 Electrical Characteristics, V_S =5.5 V to 18 V, V_{DD} = 3.0V to 5.5V, T_j = -40°C to +150°C, EN= HIGH, I_{OUTn}= 0 A; Typical values refer to V_{DD} = 5.0 V, V_S = 13.5 V and T_J = 25 °C unless otherwise specified; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified) (cont'd)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output delay time high side driver on	t_{dONH}	5	20	35	µs	Resistive load = 100Ω to GND	P_4.4.37
Output delay time high side driver off	t_{dOFFH}	15	45	75	µs	Resistive load = 100Ω to GND	P_4.4.38
Output delay time low side driver on	t_{dONL}	5	20	35	µs	Resistive load = 100Ω to VS	P_4.4.39
Output delay time low side driver off	t_{dOFFL}	15	45	75	µs	Resistive load = 100Ω to VS	P_4.4.40
Cross current protection time, high to low	t_{DHL}	100	130	160	µs	Resistive load = 100Ω[3]	P_4.4.41
Cross current protection time, low to high	t_{DLH}	100	130	160	µs	Resistive load = 100Ω[3]	P_4.4.42
Input Interface: Logic Input EN							
High-input voltage	V_{ENH}	0.7 * V_{DD}	–	–	V	–	P_4.4.43
Low-input voltage	V_{ENL}	–	–	0.3 * V_{DD}	V	–	P_4.4.44
Hysteresis of input voltage	V_{ENHY}	–	500	–	mV	[3]	P_4.4.45
Pull down resistor	R_{PD_EN}	20	40	70	kΩ	V_{EN} = 0.2 x V_{DD}	P_4.4.46
SPI frequency							
Maximum SPI frequency	$f_{SPI,max}$	–	–	5.0	MHz	[3] [5]	P_4.4.47
SPI INTERFACE: Delay Time from EN rising edge to first Data in							
Setup time	t_{set}	–	–	150	µs	[3] See **Figure 14**	P_4.4.48
SPI INTERFACE: Input Interface, Logic Inputs SDI, SCLK, CSN							
H-input voltage threshold	V_{IH}	0.7 * V_{DD}	–	–	V	–	P_4.4.50
L-input voltage threshold	V_{IL}	–	–	0.3 * V_{DD}	V	–	P_4.4.51
Hysteresis of input voltage	V_{IHY}	–	500	–	mV	[3]	P_4.4.52
Pull up resistor at pin CSN	R_{PU_CSN}	30	50	80	kΩ	V_{CSN} = 0.7 x V_{DD}	P_4.4.53
Pull down resistor at pin SDI, SCLK	R_{PD_SDI}, R_{PD_SCLK}	20	40	70	kΩ	V_{SDI}, V_{SCLK} = 0.2 x V_{DD}	P_4.4.54
Input capacitance at pin CSN, SDI or SCLK	C_I	–	10	15	pF	0V < V_{DD} < 5.25V [3]	P_4.4.55
Input Interface, Logic Output SDO							
H-output voltage level	V_{SDOH}	V_{DD} - 0.4	V_{DD} - 0.2	–	V	I_{SDOH} = -1.6 mA	P_4.4.56

Table 5 Electrical Characteristics, V_S =5.5 V to 18 V, V_{DD} = 3.0V to 5.5V, T_j = -40°C to +150°C, EN= HIGH, I_{OUTn}= 0 A; Typical values refer to V_{DD} = 5.0 V, V_S = 13.5 V and T_J = 25 °C unless otherwise specified; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified) (cont'd)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
L-output voltage level	V_{SDOL}	–	0.2	0.4	V	I_{SDOL} = 1.6 mA	P_4.4.57
Tri-state Leakage Current	I_{SDOLK}	-1	–	1	µA	$V_{CSN} = V_{DD}$; 0V < V_{SDO} < V_{DD}	P_4.4.58
Tri-state input capacitance	C_{SDO}	–	10	15	pF	3)	P_4.4.59
Data Input Timing. See Figure 15 and Figure 17.							
SCLK Period	t_{pCLK}	200	–	–	ns	3)	P_4.4.60
SCLK High Time	t_{SCLKH}	0.45 * t_{pCLK}	–	0.55 * t_{pCLK}	ns	3)	P_4.4.61
SCLK Low Time	t_{SCLKL}	0.45 * t_{pCLK}	–	0.55 * t_{pCLK}	ns	3)	P_4.4.62
SCLK Low before CSN Low	t_{BEF}	125	–	–	ns	3)	P_4.4.63
CSN Setup Time	t_{lead}	250	–	–	ns	3)	P_4.4.64
SCLK Setup Time	t_{lag}	250	–	–	ns	3)	P_4.4.65
SCLK Low after CSN High	t_{BEH}	125	–	–	ns	3)	P_4.4.66
SDI Setup Time	t_{SDI_setup}	30	–	–	ns	3)	P_4.4.67
SDI Hold Time	t_{SDI_hold}	30	–	–	ns	3)	P_4.4.68
Input Signal Rise Time at pin SDI, SCLK, CSN	t_{rIN}	–	–	50	ns	3)	P_4.4.69
Input Signal Fall Time at pin SDI, SCLK, CSN	t_{fIN}	–	–	50	ns	3)	P_4.4.70
Delay time from EN falling edge to standby mode	t_{DMODE}	–	–	8	µs	3)	P_4.4.71
Minimum CSN High Time	t_{CSNH}	5	–	–	µs	3)	P_4.4.72
Data Output Timing. See Figure 15.							
SDO Rise Time	t_{rSDO}	–	30	80	ns	C_{load} = 40pF 3)	P_4.4.73
SDO Fall Time	t_{fSDO}	–	30	80	ns	C_{load} = 40pF 3)	P_4.4.74
SDO Enable Time after CSN falling edge	t_{ENSDO}	–	–	75	ns	Low Impedance 3)	P_4.4.75
SDO Disable Time after CSN rising edge	t_{DISSDO}	–	–	75	ns	High Impedance 3)	P_4.4.76
Duty cycle of incoming clock at SCLK	$duty_{SCLK}$	45	–	55	%	3)	P_4.4.77
SDO Valid Time for V_{DD} = 3.3V	t_{VASDO3}	–	70	95	ns	V_{SDO} < 0.2 x V_{DD} V_{SDO} > 0.8 x V_{DD} C_{load} = 40pF 3)	P_4.4.78

Table 5 Electrical Characteristics, V_S =5.5 V to 18 V, V_{DD} = 3.0V to 5.5V, T_j = -40°C to +150°C, EN= HIGH, I_{OUTn}= 0 A; Typical values refer to V_{DD} = 5.0 V, V_S = 13.5 V and T_J = 25 °C unless otherwise specified; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified) (cont'd)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
SDO Valid Time for V_{DD} = 5V	t_{VASDO5}	–	50	65	ns	V_{SDO} < 0.2 x V_{DD} V_{SDO} > 0.8 V_{DD} C_{load} = 40pF 3)	P_4.4.79
Thermal warning & Shutdown							
Thermal warning junction temperature	T_{jW}	120	140	170	°C	See **Figure 11** 3)	P_4.4.80
Thermal shutdown junction temperature	T_{jSD}	150	175	200	°C	See **Figure 11** 3)	P_4.4.81
Thermal comparator hysteresis	T_{jHYS}	–	5	–	°C	3)	P_4.4.82
Ratio of SD to W temperature	T_{jSD} / T_{jW}	1.05	1.20	–	–	3)	P_4.4.83

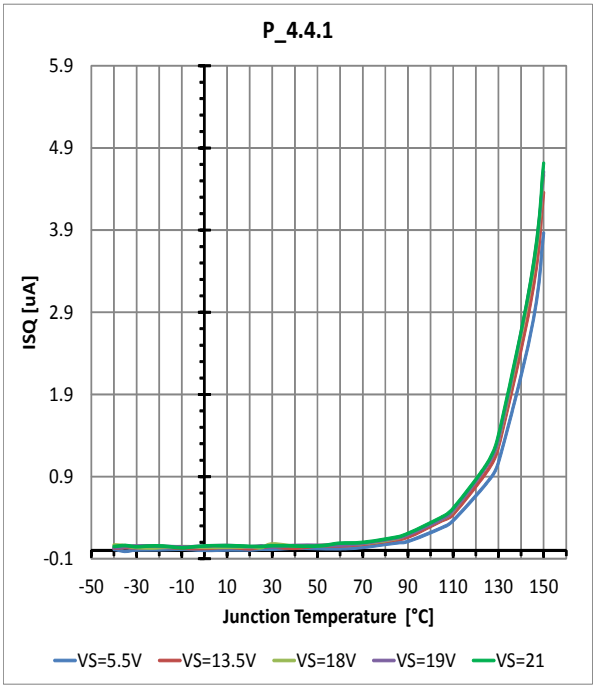
1) I_{S_HSON} does not include the load current
2) HS1, respectively HS2, is set to LED mode by setting OL_SEL_HS1 bit to 1, respectively OL_SEL_HS2 bit to 1
3) Not subject to production test, specified by design
4) Measured for 20% - 80% of V_S.
5) Not applicable in daisy chain configuration

4 Characterization results

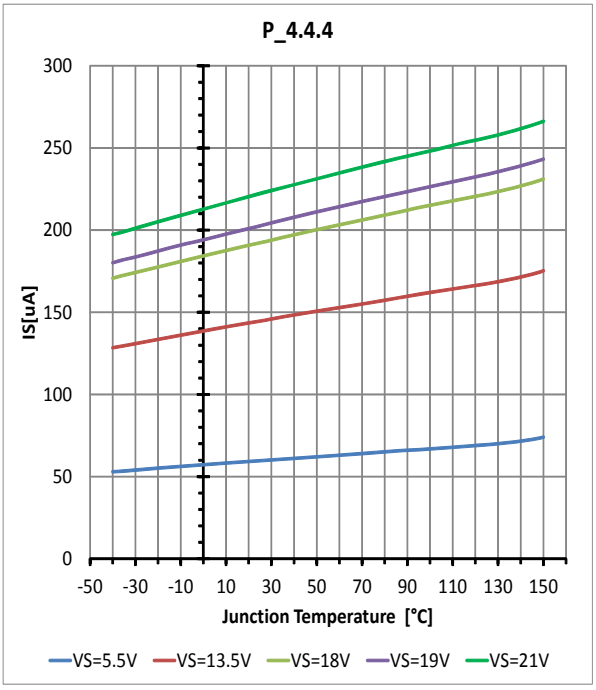
Performed on 7 devices from 2 lots, over operating temperature and nominal/extended supply range.

Typical performance characteristics

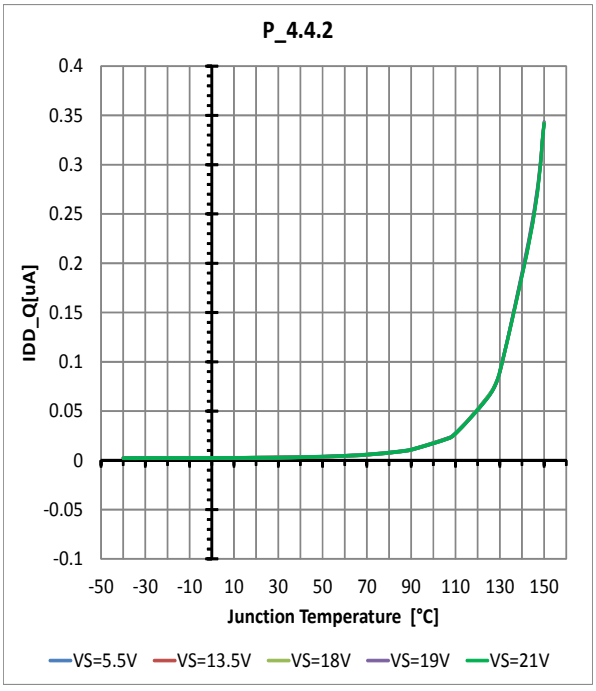
Supply quiescent current



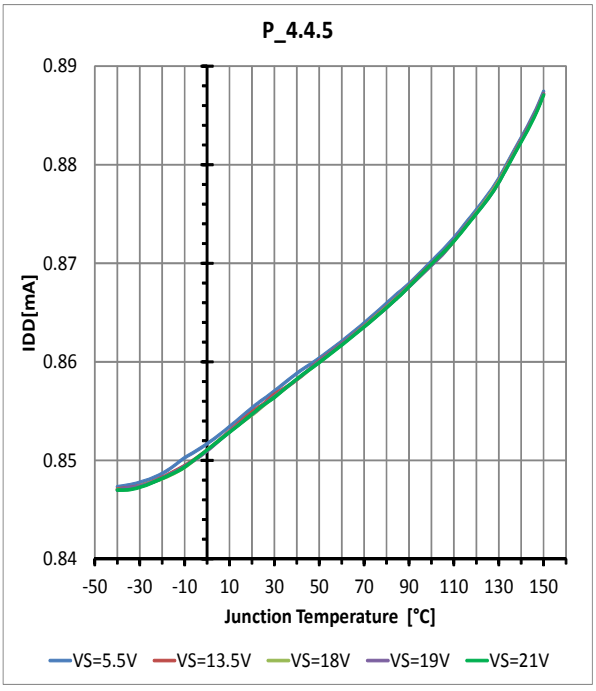
Supply current



Logic supply quiescent current

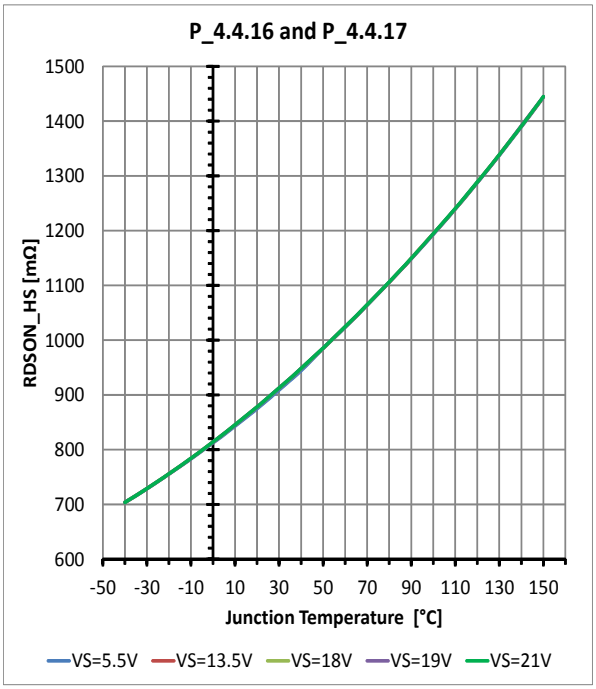


Logic supply current

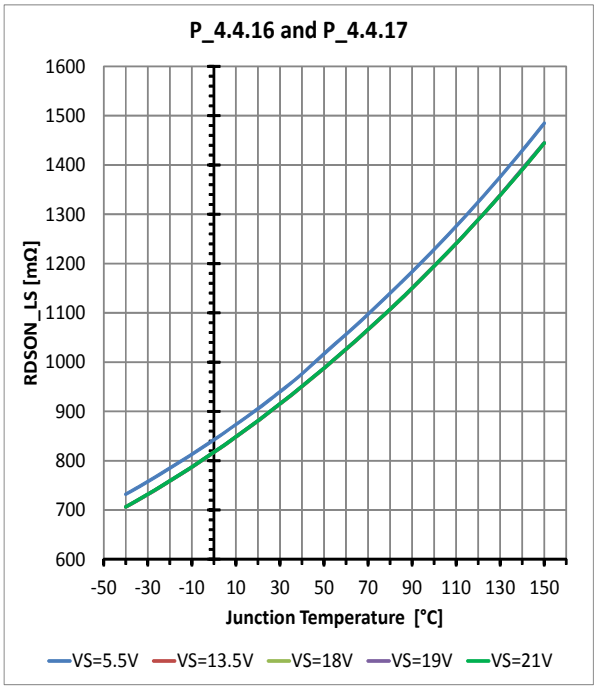


Characterization results

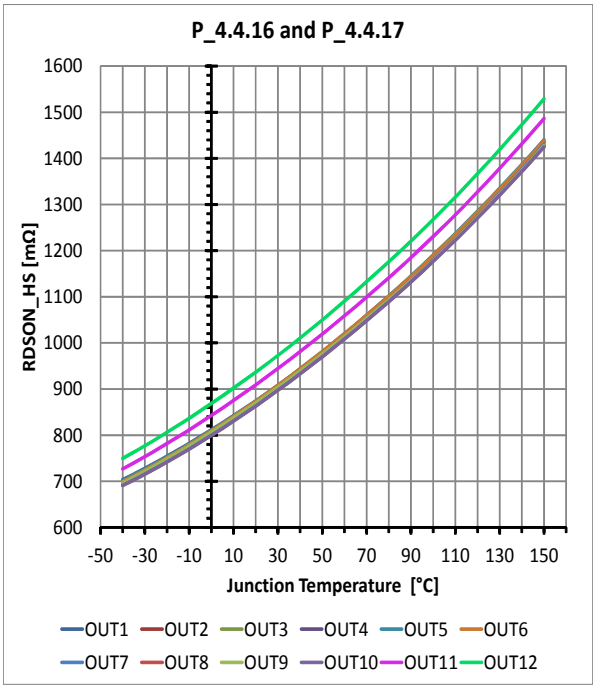
HS static Drain-source ON-resistance



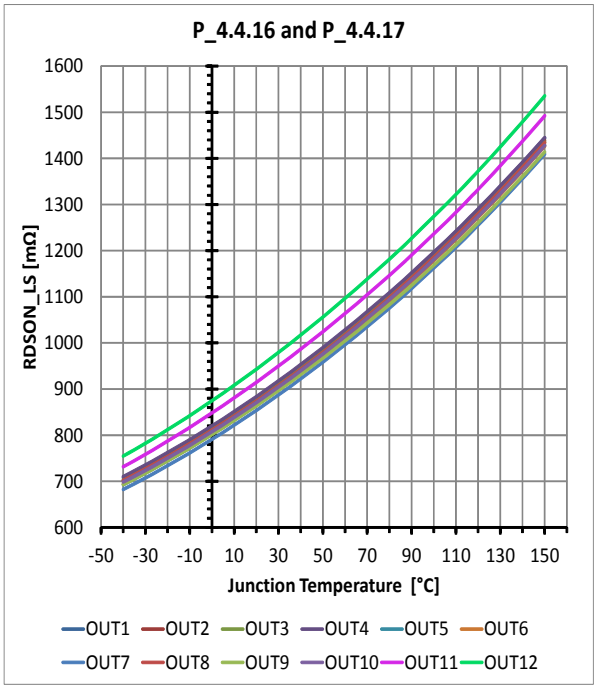
LS static Drain-source ON-resistance



HS static drain-source ON-resistance VS = 13.5V and VDD = 5V

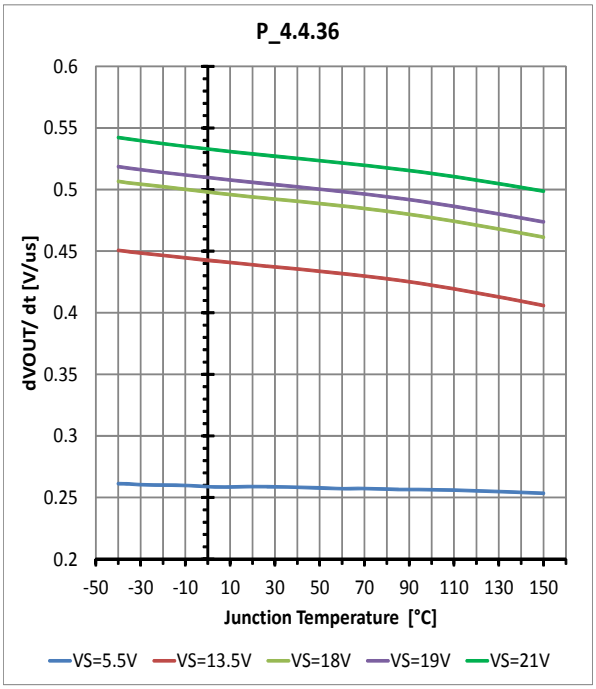


LS static drain-source ON-resistance VS = 13.5V and VDD = 5V

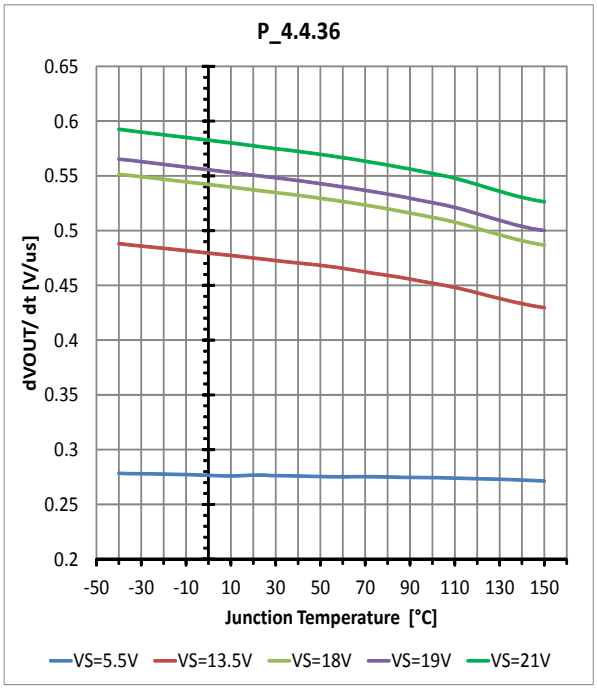


Characterization results

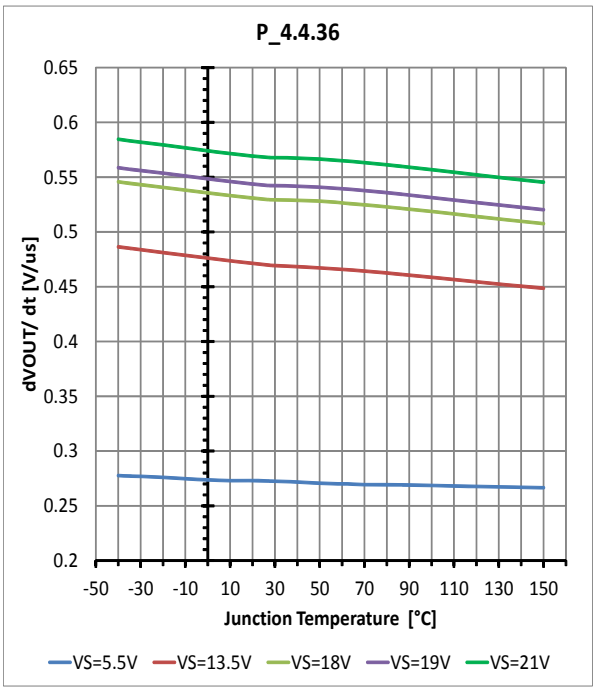
Slew rate ON of high-side outputs



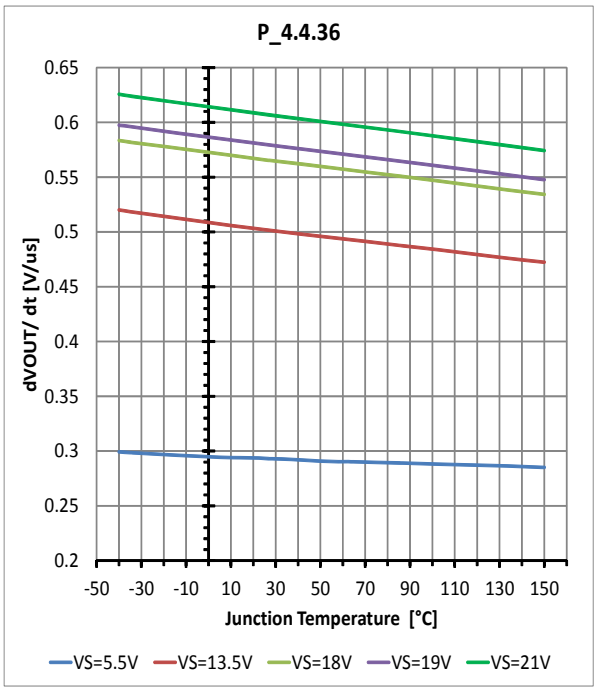
Slew rate ON of low-side outputs



Slew rate OFF of high-side outputs

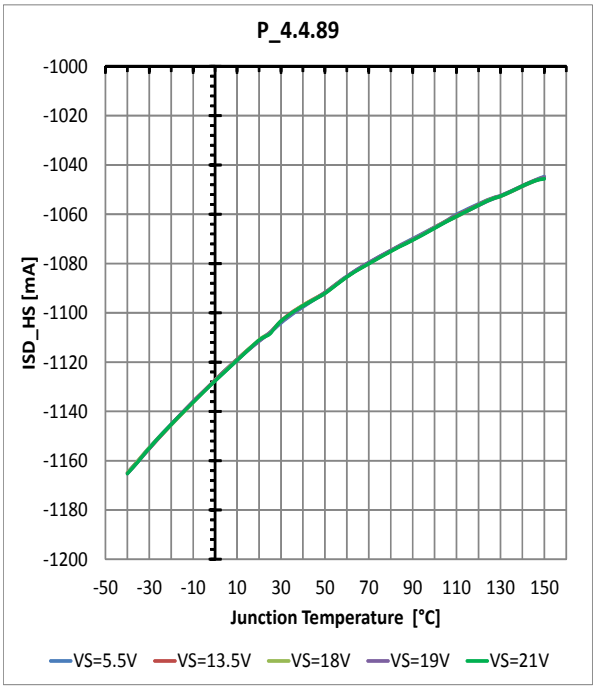


Slew rate OFF of low-side outputs

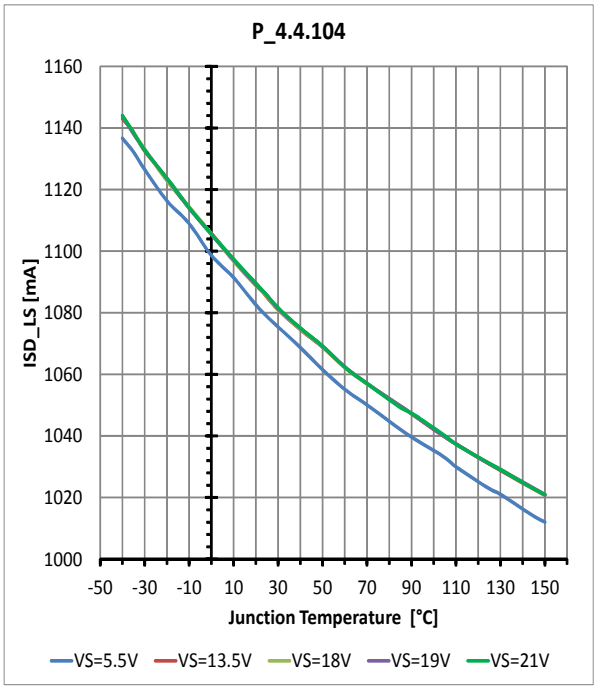


Characterization results

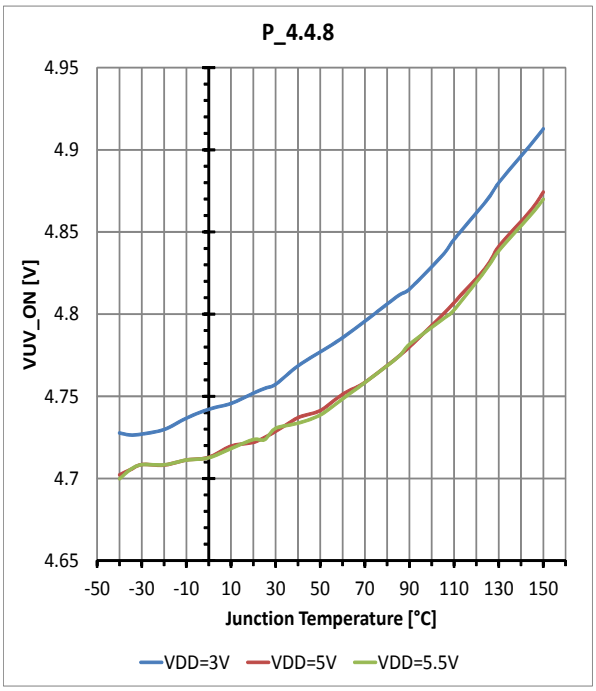
HS overcurrent shutdown threshold



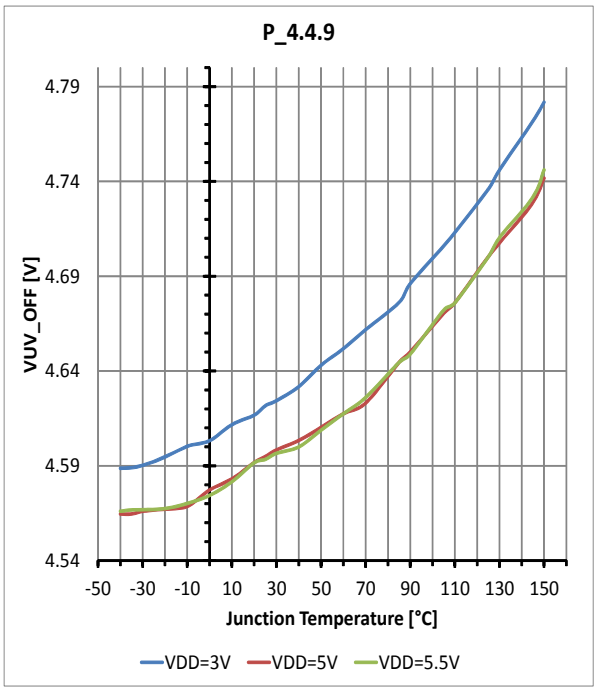
LS overcurrent shutdown threshold



Undervoltage switch ON voltage threshold

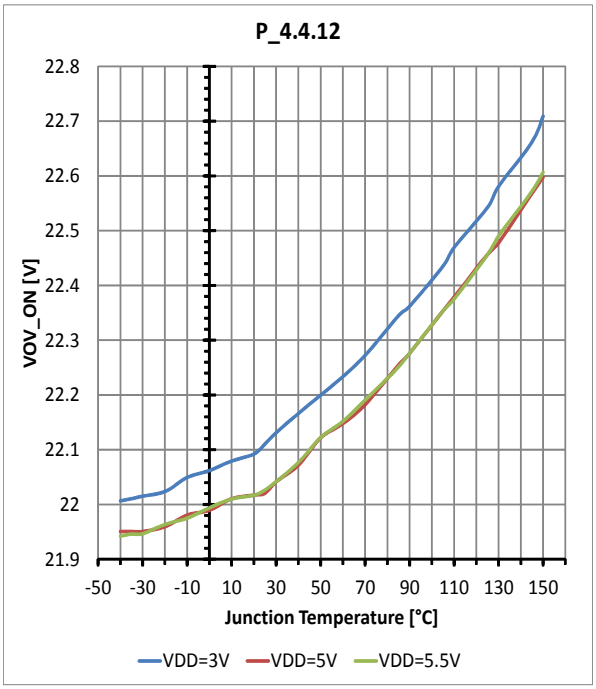


Undervoltage switch OFF voltage threshold

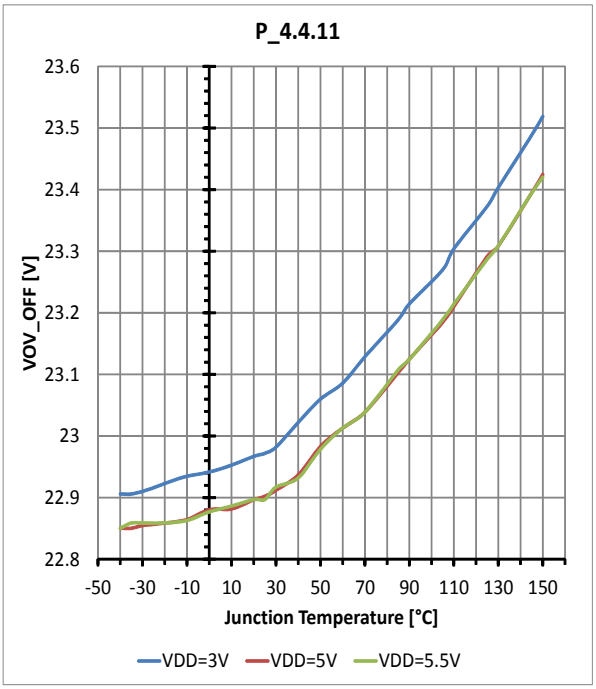


Characterization results

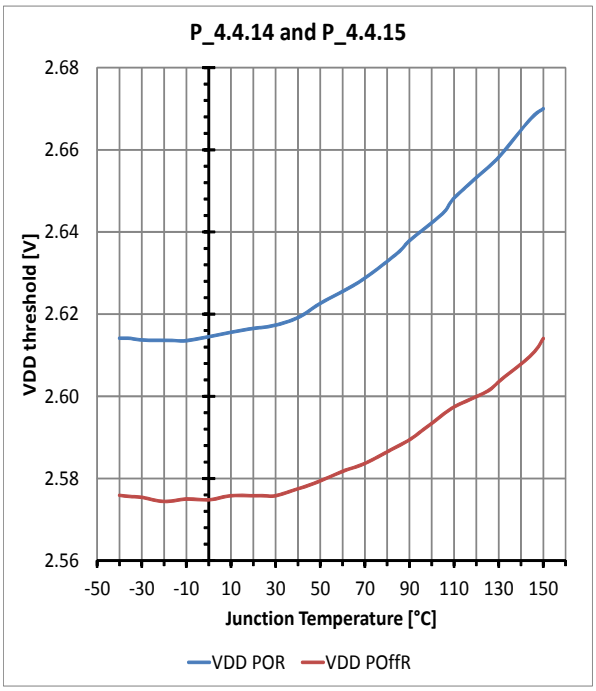
Overvoltage switch ON voltage threshold



Overvoltage switch OFF voltage threshold



VDD Power-on-reset and VDD Power-off-reset



5 General Description

5.1 Power Supply

The TLE94112EL has two power supply inputs, V_S and V_{DD}. The half bridge outputs are supplied by V_S, which is connected to the 12V automotive supply rail. V_{DD} is used to supply the I/O buffers and internal voltage regulator of the device.

V_S and V_{DD} supplies are separated so that information stored in the logic block remains intact in the event of voltage drop outs or disturbances on V_S. The system can therefore continue to operate once V_S has recovered, without having to resend commands to the device.

A rising edge on V_{DD} crossing $V_{DD\ POR}$ triggers an internal Power-On Reset (POR) to initialize the IC at power-on. All data stored internally is deleted, and the outputs are switched off (high impedance).

An electrolytic and 100nF ceramic capacitors are recommended to be placed as close as possible to the V_S supply pin of the device for improved EMC performance in the high and low frequency band. The electrolytic capacitor must be dimensioned to prevent the VS voltage from exceeding the absolute maximum rating. In addition, decoupling capacitors are recommended on the V_{DD} supply pin.

5.2 Operation modes

5.2.1 Normal mode

The TLE94112EL enters normal mode by setting the EN input High. In normal mode, the charge pump is active and all output transistors can be configured via SPI.

5.2.2 Sleep mode

The TLE94112EL enters sleep mode by setting the EN input Low. The EN input has an internal pull-down resistor.

In sleep mode, all output transistors are turned off and the SPI register banks are reset. The current consumption is reduced to $I_{SQ} + I_{DD\_Q}$.

5.3 Reset Behaviour

The following reset triggers have been implemented in the TLE94112EL:

V_{DD} Undervoltage Reset:

The SPI Interface shall not function if V_{DD} is below the undervoltage threshold, $V_{DD\ POffR}$. The digital block will be deactivated, the logic contents cleared and the output stages are switched off . The digital block is initialized once V_{DD} voltage levels is above the undervoltage threshold, $V_{DD\ POR}$. Then the NPOR bit is reset (NPOR = 0 in **SYS_DIAG1** and Global Status Register).

Reset on EN pin:

If the EN pin is pulled Low, the logic content is reset and the device enters sleep mode.

The reset event is reported by the NPOR bit (NPOR = 0) once the TLE94112EL is in normal mode (EN = High; VDD > $V_{DD\ POR}$).

5.4 Reverse Polarity Protection

The TLE94112EL requires an external reverse polarity protection. During reverse polarity, the free-wheeling diodes across the half bridge output will begin to conduct, causing an undesired current flow (I_{RB}) from ground potential to battery and excessive power dissipation across the diodes. As such, a reverse polarity protection diode is recommended (see **Figure 4**).

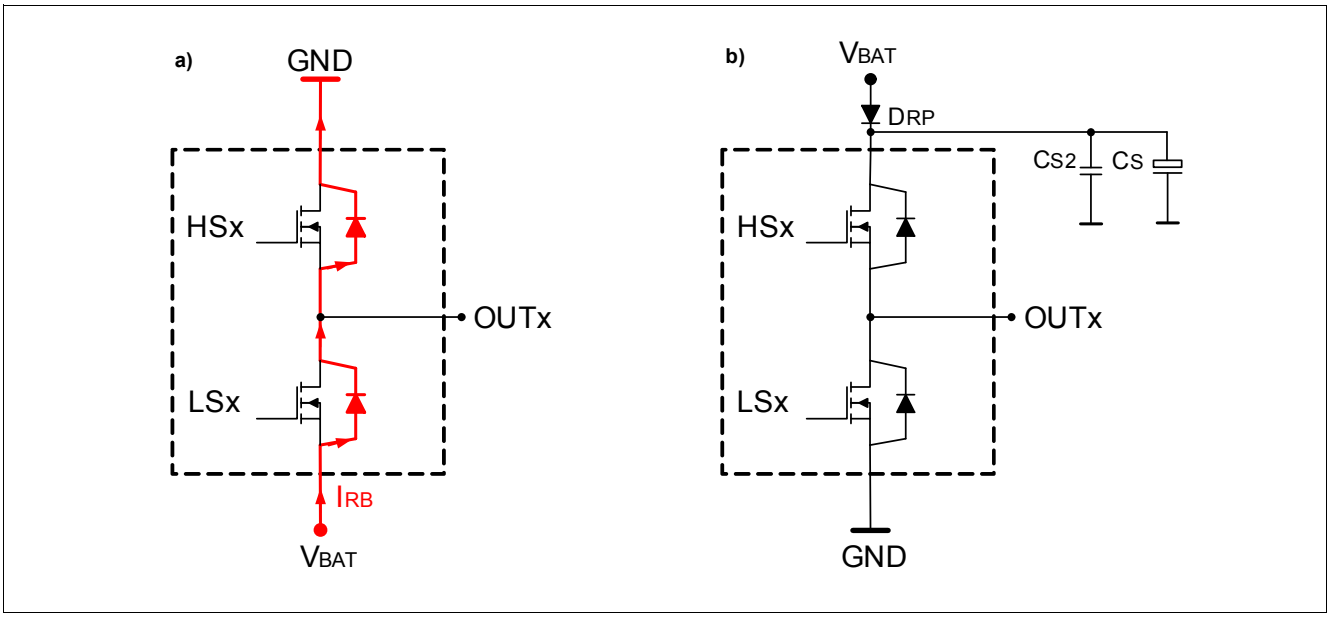


Figure 4 Reverse Polarity Protection

6 Half-Bridge Outputs

6.1 Functional Description

The half-bridge outputs of the TLE94112EL are intended to drive motor loads. These outputs can either be driven continuously or PWM enabled via SPI.

If the outputs are driven continuously via SPI, for example HS1 and LS2 used to drive a motor, then the following suggested SPI commands shall be sent:

- Activate HS1: Bit HB1_HS_EN in HB_ACT_1_CTRL register
- Activate LS2: Bit HB2_LS_EN in HB_ACT_1_CTRL register

6.1.1 Half-bridge operation with PWM enabled

All half-bridge outputs of the TLE94112EL are capable of PWM operation. They can either be used to drive an inductive load (e.g. DC brush motor) or optionally a resistive load (e.g. LED). Each half-bridge output has been allocated a maximum of three PWM channels with individual duty cycle settings with 8-bit resolution. Each channel is further mapped to a maximum of three PWM frequency options, i.e. 80Hz,100Hz and 200Hz. This feature enables a highly flexible PWM operation while driving loads with varying control profiles.

PWM frequency and duty cycle can be changed on demand during PWM operation of the desired half-bridge output. Glitches on the PWM output waveform, which may arise as a result of on-demand changes in PWM operation, will be prevented by the internal logic circuitry.

When operating with motor loads, active or passive free-wheeling configuration is available via SPI to select the speed at which the inductive current can decay over the full-bridge circuit. The default setting is passive free-wheeling.

Note: Active free-wheeling is effectively applied if the selected duty cycle corresponds to turn-on times of the HS and the LS, which are longer than the sum of the cross conduction times tDHL + tDLH.

Table 6 PWM capability and frequency selection per half-bridge output

Control Register: HBx_MODEn (n=0,1)	PWM Frequency 80Hz (Control Register: PWM_CH_FREQ_CTRL)	PWM Frequency 100Hz (Control Register: PWM_CH_FREQ_CTRL)	PWM Frequency 200Hz (Control Register: PWM_CH_FREQ_CTRL)
PWM Channel 1	PWM_CH1_FREQ_n (n=0,1) Bit ‘01_B’	PWM_CH1_FREQ_n (n=0,1) Bit ‘10_B’	PWM_CH1_FREQ_n (n=0,1) Bit ‘11_B’
PWM Channel 2	PWM_CH2_FREQ_n (n=0,1) Bit ‘01_B’	PWM_CH2_FREQ_n (n=0,1) Bit ‘10_B’	PWM_CH2_FREQ_n (n=0,1) Bit ‘11_B’
PWM Channel 3	PWM_CH3_FREQ_n (n=0,1) Bit ‘01_B’	PWM_CH3_FREQ_n (n=0,1) Bit ‘10_B’	PWM_CH3_FREQ_n (n=0,1) Bit ‘11_B’