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# TLE9832

Microcontroller with LIN and Power Switches for Automotive Applications

## Data Sheet

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# 1 Summary of Features

- High performance XC800 core
  - compatible to standard 8051 core
  - up to 40 MHz clock frequency
  - two clocks per machine cycle architecture
  - two data pointers
- On-chip memory
  - 32 kByte + 4 kByte Flash for program code and data (4 kByte EEPROM emulation built-in)
  - 512 Byte One Time Programmable Memory (OTP)
  - 512 Byte 100 Time Programmable Memory (100TP)
  - 256 Byte RAM, 3 kByte XRAM
  - BootROM for startup firmware and Flash routines
- Core logic supply at 1.5 V
- On-chip OSC and PLL for clock generation
  - Loss of clock detection with fail safe mode for power switches
- Watchdog timer (WDT) with programmable window feature for refresh operation and warning prior to overflow
- General-purpose I/O Port (GPIO) with wake-up capability
- Multiplication/division unit (MDU) for arithmetic calculation
- Software libraries to support floating point and MDU calculations
- Five 16-Bit timers - Timer 0, Timer 1, Timer 2, Timer 21 and Timer 3
- Capture/compare unit for PWM signal generation (CCU6) with Timer 12 and Timer 13
- Full duplex serial interface (UART) with LIN support
- Synchronous serial channel (SSC)
- On-chip debug support via 2-wire Device Access Port (DAP)
- LIN Bootstrap loader (LIN BSL)
- LIN transceiver compliant to LIN 1.3, LIN 2.0 and LIN 2.1
- 2 x Low Side Switches with clamping capability incl. PWM functionality, e.g. as relay driver
- 1x High Side Switch with cyclic sense option and PWM functionality, e.g. for LED or powering of switches
- 5 x High Voltage Monitor Input pins for wake-up and with cyclic sense and analog measurement option
- Measurement unit with 10 channels, 8-Bit A/D Converter (ADC2) and data post processing
- 8 channels, 10-Bit A/D Converter (including battery voltage and supply voltage measurement) (ADC1)
- Single power supply from 3.0 V to 27 V
- Low-dropout voltage regulators (LDO)
- Dedicated 5 V voltage regulator for external loads (e.g. hall sensor)
- Programmable window watchdog (WDT1) with independent on-chip clock source
- Power saving modes
  - MCU slow-down mode
  - Stop Mode
  - Sleep Mode
  - Cyclic wake-up and cyclic sense during Stop Mode and Sleep Mode
- Power-on and undervoltage/brownout reset generator
- Overtemperature protection
- Overcurrent protection with shutdown
- Supported by a full range of development tools including C compilers, macro assembler packages, emulators, evaluation boards, HLL debugger, programming tools, software packages
- Temperature Range $T_J$: -40 °C up to 150 °C
- Packages TLE9832QV: VQFN-48-22 and TLE9832QX: VQFN-48-29
- Green package (RoHS compliant)

## 1.1 Device Types / Ordering Information

The TLE983x product family features devices with different peripheral modules, configurations and program memory sizes to offer cost-effective solutions for different application requirements. Table 1 describes the TLE9832 device configuration.

**Table 1 Device Configuration**

| Device Name | Max Clock Frequency | High Side Switches | High Voltage Monitor Inputs | Flash Size | Bidirectional Parallel Port I/O´s | Operational Amplifier |
|---|---|---|---|---|---|---|
| TLE9832QV | 40 MHz | 1 | 5 | 36 kByte | 11 | no |
| TLE9832QX | 40 MHz | 1 | 5 | 36 kByte | 11 | no |

## 1.2 Abbreviations

The following acronyms and terms are used within this document. List see in Table 2.

**Table 2 Acronyms**

| Acronyms | Name |
|---|---|
| ALU | Arithmetic Logic Unit |
| CCU6 | Capture Compare Unit 6 |
| CGU | Clock Generation Unit |
| CMU | Cyclic Management Unit |
| DAP | Device Access Port |
| DPP | Data Post Processing |
| ECC | Error Correction Code |
| EEPROM | Electrically Erasable Programmable Read Only Memory |
| GPIO | General Purpose Input Output |
| FSR | Full Scale Range |
| ICU | Interrupt Control Unit |
| IRAM | Internal Random Access Memory - Internal Data Memory |
| LDO | Low DropOut voltage regulator |
| LIN | Local Interconnect Network |
| LSB | Least Significant Bit |
| MCU | Micro Controller Unit |
| MDU | Multiplication Division Unit |
| MMC | Monitor Mode Control |
| MSB | Most Significant Bit |
| NMI | Non Maskable Interrupt |
| OCDS | On Chip Debug Support |
| OTP | One Time Programmable |
| OSC | Oscillator |
| PC | Program Counter |
| PCU | Power Control Unit |
| PD | Pull Down |
| PGU | Power supply Generation Unit |
| PLL | Phase Locked Loop |
| PMU | Power Management Unit |
| PSW | Program Status Word |
| PU | Pull Up |
| PWM | Pulse Width Modulation |
| RAM | Random Access Memory |
| RCU | Reset Control Unit |
| RMU | Reset Management Unit |

**Table 2 Acronyms**

| Acronyms | Name |
|---|---|
| ROM | Read Only Memory |
| SCK | SSC Clock |
| SFR | Special Function Register |
| SOW | Short Open Window (for WDT1) |
| SPI | Serial Peripheral Interface |
| SSC | Synchronous Serial Channel |
| SSU | System Status Unit |
| TMS | Test Mode Select |
| UART | Universal Asynchronous Receiver Transmitter |
| UDIG | Universal Digital Controller for ADC1 |
| VBG | Voltage reference Band Gap |
| WDT | Watchdog timer |
| WMU | Wake-up Management Unit |
| XRAM | On-Chip eXternal Data Memory |
| XSFR | On-Chip eXternal Special Function Register |

# 2 General Device Information

## 2.1 Pin Configuration

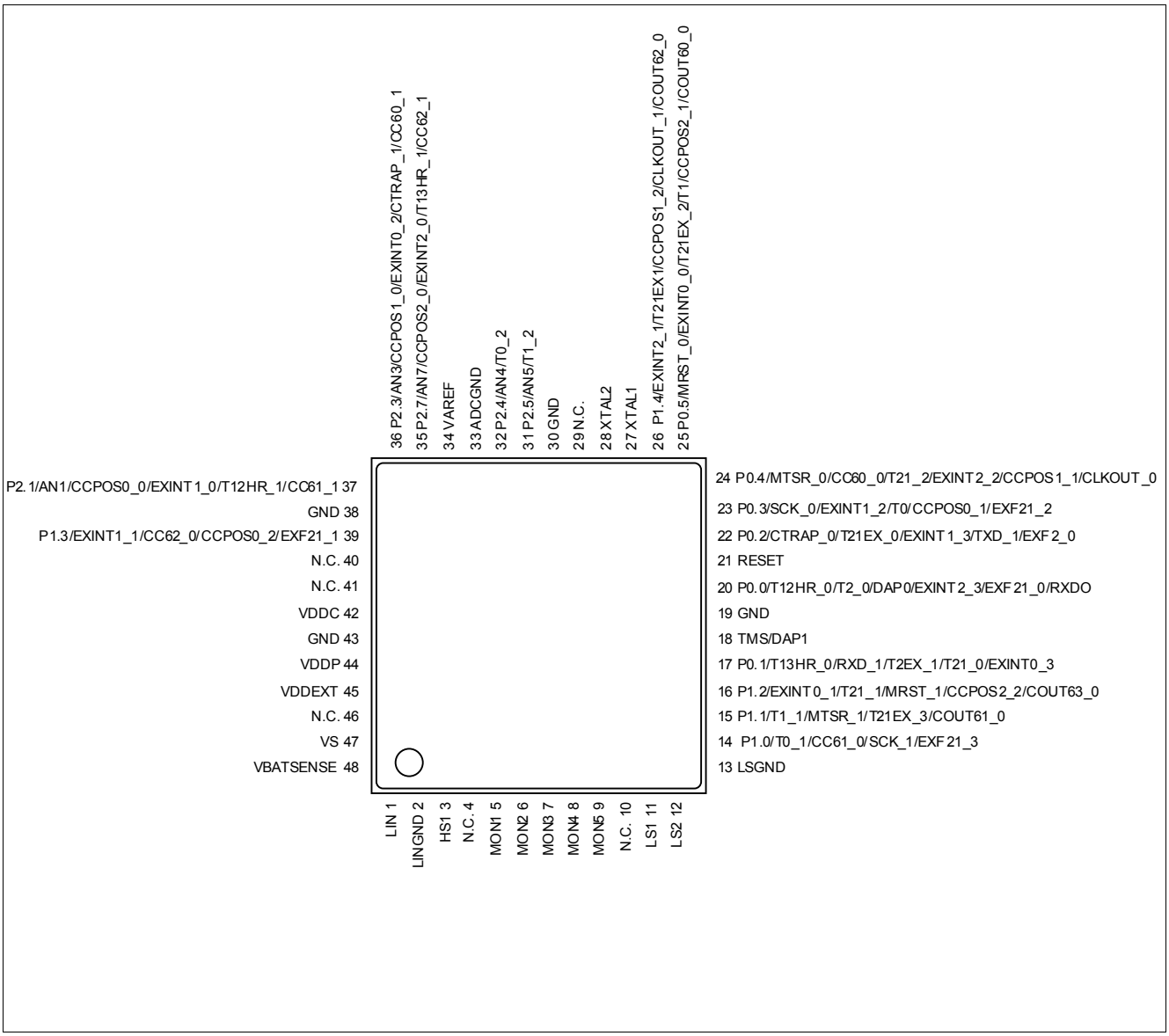


**Figure 1 TLE9832 pin configuration, VQFN-48-22 and VQFN-48-29 package (top view)**

## 2.2 Pin Definitions and Functions

After reset, all pins are configured as input (except supply and LIN pins) with one of the following settings:

- Pull-up device enabled only (PU)
- Pull-down device enabled only (PD)
- Input with both pull-up and pull-down devices disabled (I)
- Output with output stage deactivated = high impedance state (Hi-Z)

The functions and default states of the TLE9832 external pins are provided in the following table.

Type: indicates the pin type.

- I/O: Input or output
- I: Input only
- O: Output only
- P: Power supply

**Table 3 Pin Definitions and Functions**

| Symbol | Pin Number | Type | Reset State | Function | |
|---|---|---|---|---|---|
| **P0** | | | | **Port 0**<br>Port 0 is an 6-Bit bidirectional general purpose I/O port. Alternate functions can be assigned as follows: DAP, CCU6, Timer 0, Timer 1, Timer 2, Timer 21, UART, SSC, external interrupt input and clock output. | |
| P0.0 | 20 | I/O | I/PU | T12HR_0<br>T2_0<br>DAP0<br>EXINT2_3<br>EXF21_0<br>RXDO | CCU6 Timer 12 hardware run input<br>Timer 2 input<br>Debug Access Port 0<br>External interrupt input 0<br>Timer 21 external flag output<br>UART transmit data output (synchronous mode) |
| P0.1 | 17 | I/O | I/PU | T13HR_0<br>RXD_1<br>T2EX_1<br>T21_0<br>EXINT0_3 | CCU6 Timer 13 hardware run input<br>UART receive input<br>Timer 2 external trigger input<br>Timer 21 input<br>External interrupt input 0 |
| P0.2 | 22 | I/O | I/PU | $\overline{\text{CTRAP\_0}}$<br>T21EX_0<br>EXINT1_3<br>TXD_1<br>EXF2_0 | CCU6 trap input<br>Timer 21 external trigger input<br>External interrupt input 1<br>UART transmit output<br>Timer 2 external flag output |
| P0.3 | 23 | I/O | I/PU | SCK_0<br>EXINT1_2<br>T0<br>CCPOS0_1<br>EXF21_2 | SSC clock input (for slave) / output (for master)<br>External interrupt input 1<br>Timer 0 input<br>CCU6 hall input 0<br>Timer 21 external flag output |
| P0.4 | 24 | I/O | I/PU | MTSR_0<br>CC60_0<br>T21_2<br>EXINT2_2<br>CCPOS1_1<br>CLKOUT_0 | SSC master transmit output / slave receive input<br>CCU6 capture/compare channel 0 input/output<br>Timer 21 input<br>External interrupt input 2<br>CCU6 hall input 1<br>Clock output |

**Table 3 Pin Definitions and Functions** (cont'd)

| Symbol | Pin Number | Type | Reset State | Function | |
|---|---|---|---|---|---|
| P0.5 | 25 | I/O | I/PU | MRST_0<br>EXINT0_0<br>T21EX_2<br>T1<br>CCPOS2_1<br>COUT60_0 | SSC master receive input / slave transmit output<br>External interrupt input 0<br>Timer 21 external trigger input<br>Timer 1 input<br>CCU6 hall input 2<br>CCU6 capture/compare channel 0 output |
| **P1** | | | | **Port 1**<br>Port 1 is an 5-Bit bidirectional general purpose I/O port.<br>Alternate functions can be assigned as follows:<br>CCU6, Timer 0, Timer 1 Timer 21, SSC, external interrupt input and clock output. | |
| P1.0 | 14 | I/O | I | T0_1<br>CC61_0<br>SCK_1<br>EXF21_3 | Timer 0 input<br>CCU6 capture/compare channel 1 input/output<br>SSC clock input (for slave) / output (for master)<br>Timer 21 external flag output |
| P1.1 | 15 | I/O | I | T1_1<br>MTSR_1<br>T21EX_3<br>COUT61_0 | Timer 1 input<br>SSC master transmit output/slave receive input<br>Timer 21 external trigger input<br>CCU6 capture/compare channel 1 output |
| P1.2 | 16 | I/O | I | EXINT0_1<br>T21_1<br>MRST_1<br>CCPOS2_2<br>COUT63_0 | External interrupt input 0<br>Timer 21 input<br>SSC master receive input/slave transmit output<br>CCU6 hall input 2<br>CCU6 capture/compare channel 3 output |
| P1.3 | 39 | I/O | I | EXINT1_1<br>CC62_0<br>CCPOS0_2<br>EXF21_1 | External interrupt input 1<br>CCU6 capture/compare channel 2 input/output<br>CCU6 hall input 0<br>Timer 21 external flag output |
| P1.4 | 26 | I/O | I | EXINT2_1<br>T21EX_1<br>CCPOS1_2<br>CLKOUT_1<br>COUT62_0 | External interrupt input 2<br>Timer 21 external trigger input<br>CCU6 hall input 1<br>Clock output<br>CCU6 capture/compare channel 2 output |
| **P2** | | | | **Port 2**<br>Port 2 is an 5-Bit general purpose input-only port.<br>Alternate functions can be assigned as follows:<br>CCU6, Timer 0, Timer 1, Timer 21 and external interrupt input<br>It is also used as analog inputs for the 10-Bit ADC (ADC1). | |
| P2.1 | 37 | I | I | AN1<br>CCPOS0_0<br>EXINT1_0<br>T12HR_1<br>CC61_1 | ADC1 analog input channel 1<br>CCU6 hall input 0<br>External interrupt input 1<br>CCU6 Timer 12 hardware run input<br>CCU6 capture/compare channel 1 input |

**Table 3 Pin Definitions and Functions** (cont'd)

| Symbol | Pin Number | Type | Reset State | Function | |
|---|---|---|---|---|---|
| P2.3 | 36 | I | I | AN3<br>CCPOS1_0<br>EXINT0_2<br>CTRAP_1<br>CC60_1 | ADC1 analog input channel 3<br>CCU6 hall input 1<br>External interrupt input 0<br>CCU6 trap input<br>CCU6 capture/compare channel 0 input |
| P2.4 | 32 | I | I | AN4<br>T0_2 | ADC1 analog input channel 4<br>Timer 0 input |
| P2.5 | 31 | I | I | AN5<br>T1_2 | ADC1 analog input channel 5<br>Timer 1 input |
| P2.7 | 35 | I | I | AN7<br>CCPOS2_0<br>EXINT2_0<br>T13HR_1<br>CC62_1 | ADC1 analog input channel 7<br>CCU6 hall input 2<br>External interrupt input 2<br>CCU6 timer 13 hardware run input<br>CCU6 capture/compare channel 2 input |
| **Power Supply** | | | | | |
| VS | 47 | P | – | Battery supply input | |
| VDDP | 44 | P | – | I/O port supply (5.0 V). Do not connect external loads. For buffer and bypass capacitors. | |
| VDDC | 42 | P | – | Core supply (1.5 V during Active Mode, 0.9 V during Stop Mode). Do not connect external loads. For buffer/bypass capacitor. | |
| VDDEXT | 45 | P | – | External voltage supply output (5.0 V, 20 mA) | |
| LSGND | 13 | P | – | Low Side ground LS1, LS2 | |
| GND | 30, 43, 19, 38 | P | – | Core supply ground; analog supply ground | |
| ADCGND | 33 | P | – | Analog supply ground for ADC1 | |
| LINGND | 2 | P | – | LIN ground | |
| **Monitor Inputs** | | | | | |
| MON1 | 5 | I | I | High Voltage Monitor Input 1 | |
| MON2 | 6 | I | I | High Voltage Monitor Input 2 | |
| MON3 | 7 | I | I | High Voltage Monitor Input 3 | |
| MON4 | 8 | I | I | High Voltage Monitor Input 4 | |
| MON5 | 9 | I | I | High Voltage Monitor Input 5 | |
| **High Side Switch / Low Side Switch Outputs** | | | | | |
| LS1 | 11 | O | Hi-Z | Low Side Switch output 1 | |
| LS2 | 12 | O | Hi-Z | Low Side Switch output 2 | |
| HS1 | 3 | O | Hi-Z | High Side Switch output 1 | |
| **LIN Interface** | | | | | |
| LIN | 1 | I/O | PU | LIN bus interface input/output | |
| **Others** | | | | | |

**Table 3 Pin Definitions and Functions** (cont'd)

| Symbol | Pin Number | Type | Reset State | Function |
|---|---|---|---|---|
| VAREF | 34 | I/O | O | 5V ADC1 reference voltage |
| XTAL1 | 27 | I | I | External oscillator input |
| XTAL2 | 28 | O | Hi-Z | External oscillator output |
| TMS | 18 | I | I/PD | TMS test mode select input<br>DAP1 Debug Access Port 1 |
| RESET | 21 | I/O | I/O/PU | Reset input, not available during Sleep Mode |
| VBAT_SENSE | 48 | I | I | Battery supply voltage sense input |
| N.C. | 10, 29, 40, 41, 46 | – | – | Not connected - can be connected to GND |
| N.C. | 4 | – | – | Not connected - leave pin open |

# 3 Functional Description

This highly integrated circuit contains analog and digital functional blocks. For system and interface control an embedded 8-Bit state-of-the-art microcontroller, compatible to the standard 8051 core with On-Chip Debug Support (OCDS), is available. For internal and external power supply purposes, on-chip low drop-out regulators are existent. An internal oscillator provides a cost effective and suitable clock in particular for LIN slave nodes. As communication interface, a LIN transceiver and several High Voltage Monitor Inputs with adjustable threshold and filters are available. Furthermore one High Side Switch (e.g. for driving LEDs or cyclic powering of switches), two Low Side Switches (e.g. for relays) and several general purpose input/outputs (GPIO) with pulse-width modulation (PWM) capabilities are available.

The Micro Controller Unit (MCU) supervision and system protection including reset feature is controlled by a programmable window watchdog. A cyclic wake-up circuit, supply voltage supervision and integrated temperature sensors are available on-chip.

All relevant modules offer power saving modes in order to support terminal 30 connected automotive applications. A wake-up from the power saving mode is possible via a LIN bus message, via the monitoring inputs, via the GPIO ports or repetitive with a programmable time period (cyclic wake-up).

The integrated circuit is available in a VQFN-48-22 and VQFN-48-29 package with 0.5 mm pitch and is designed to withstand the severe conditions of automotive applications.

## Block Diagram

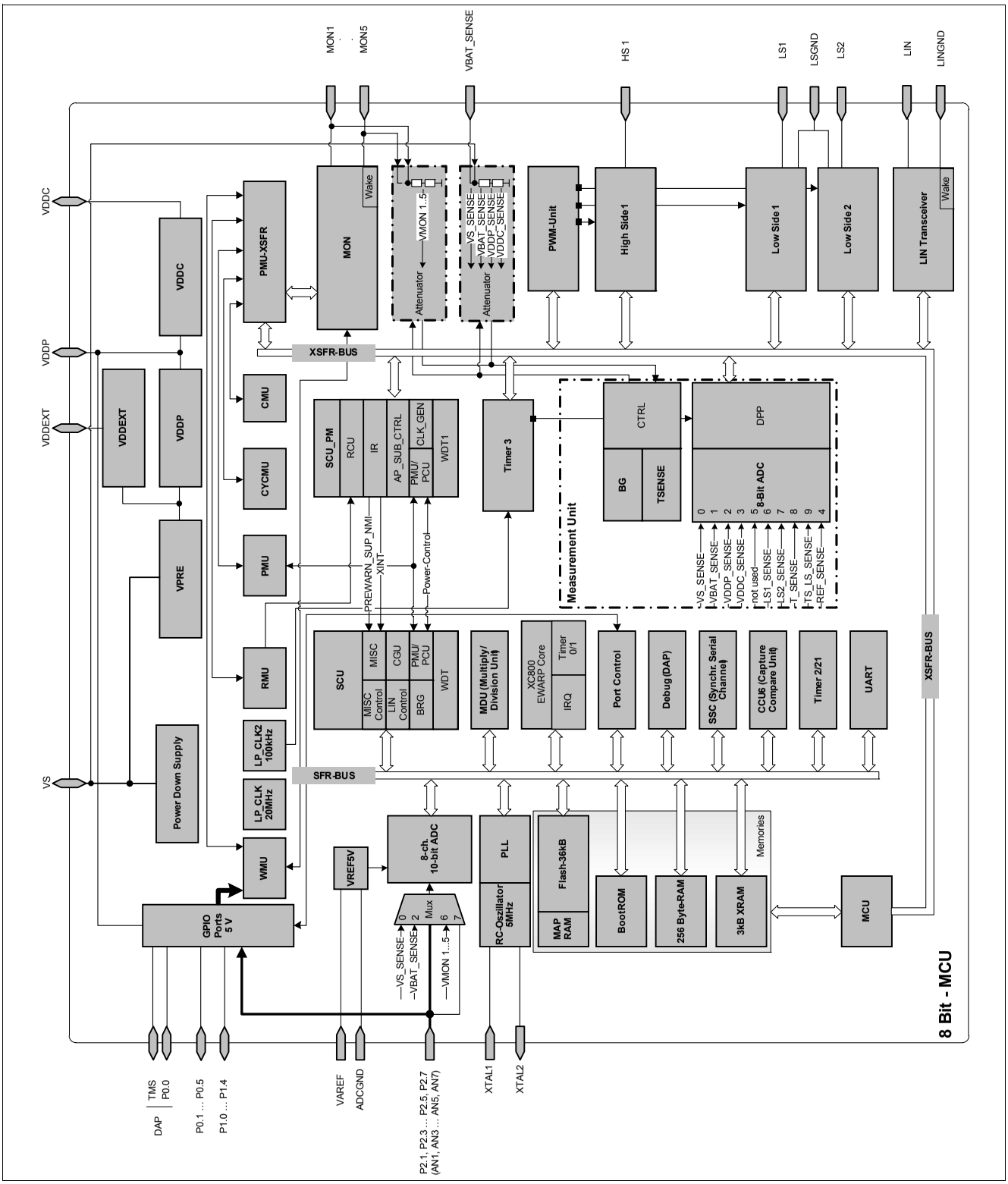


**Figure 2 Block Diagram**

The TLE9832 has several operational modes mainly to support low power consumption requirements. The low power modes and state transitions are depicted in **Figure 3** below.

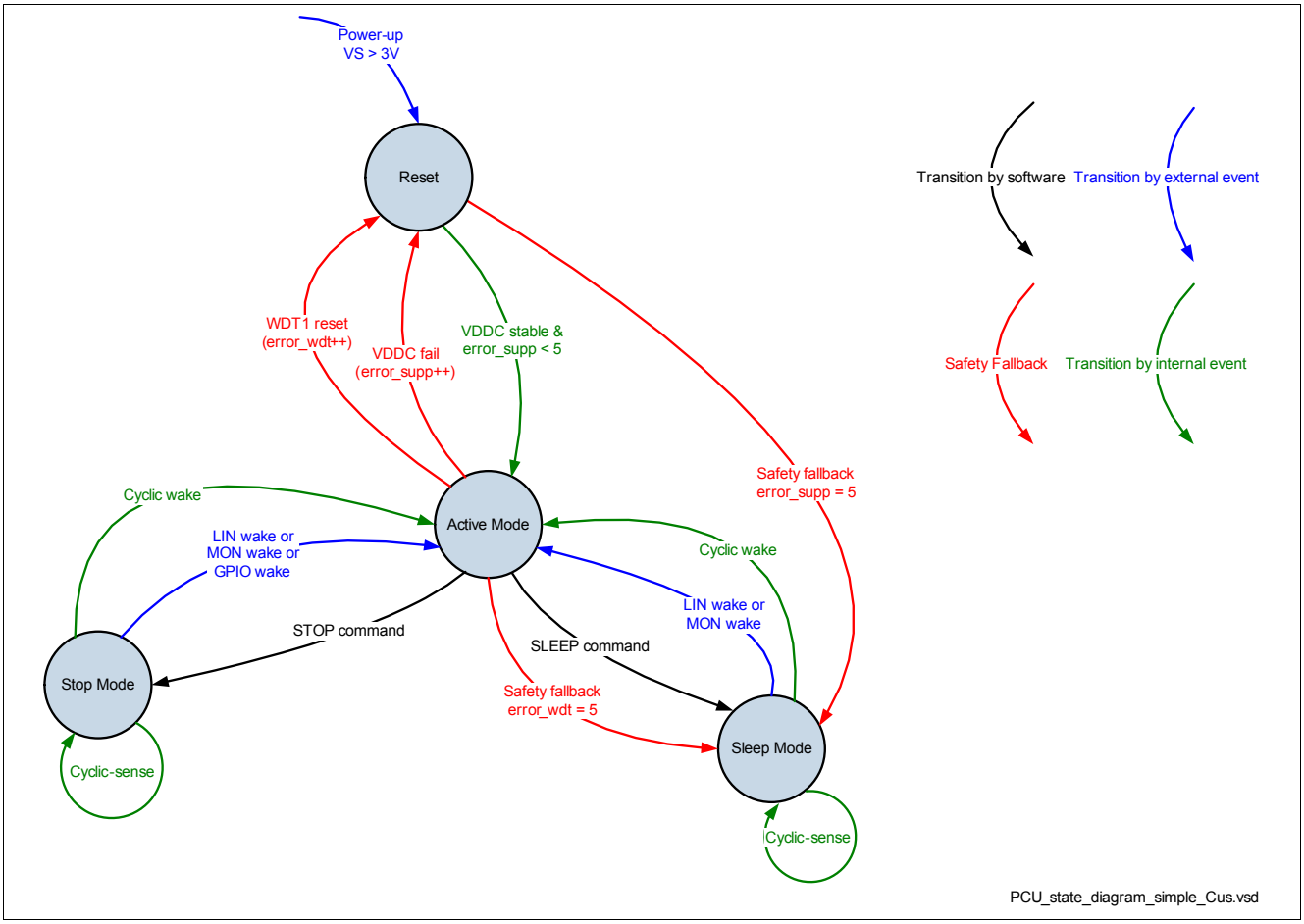


**Figure 3 Power Control State Diagram**

### Reset Mode

The Reset Mode is a transition mode e.g. during power-up of the device after a power-on reset. In this mode the on-chip power supplies are enabled and all other modules are initialized. Once the core supply VDDC is stable, the Active Mode is entered. In case the watchdog timer WDT1 fails for more than four times, a fail-safe transition to the Sleep Mode is done.

### Active Mode

In Active Mode all modules are activated and the TLE9832 is fully operational.

### Stop Mode

The Stop Mode is one out of two low power modes. The transition to the low power modes is done by setting the respective Bits in the mode control register. In Stop Mode the embedded microcontroller is still powered allowing faster wake-up reaction times. A wake-up from this mode is possible by LIN bus activity, the High Voltage Monitor Input pins or the respective 5V GPIOs.

### Sleep Mode

The Sleep Mode is the second low-power mode. The transition to the low-power modes is done by setting the respective Bits in the MCU mode control register. In Sleep Mode the embedded microcontroller power supply is deactivated allowing the lowest system power consumption, but the wake-up time is longer compared to the Stop Mode. A wake-up from this mode is possible by LIN bus activity or the High Voltage Monitor Input pins. A wake-up from Sleep Mode behaves similar to a power-on reset.

### Cyclic Wake-up Mode

The cyclic wake-up mode is a special operating mode of the Sleep Mode and the Stop Mode. The transition to the cyclic wake-up mode is done by first setting the respective Bits in the mode control register followed by the SLEEP or STOP command. Additional to the cyclic wake-up behavior (wake-up after a programmable time period), the wake-up sources of the normal Stop Mode and Sleep Mode are available.

### Cyclic Sense Mode

The cyclic sense mode is a special operating mode of the Sleep Mode and the Stop Mode. The transition to the cyclic sense mode is done by first setting the respective Bits in the mode control register followed by the STOP or SLEEP command. In cyclic sense mode the High Side Switch can be switched on periodically for biasing some switches for example. The wake-up condition is configurable, when the sense result of defined monitor inputs at a window of interest changed compared to the previous wake-up period or reached a defined state respectively. In this case the Active Mode is entered immediately. For cyclic sense in Stop Mode VDDEXT can be switched on periodically. Furthermore cyclic sense allows to sense dedicated GPIO port states and transitions when in Stop Mode.

The following table shows the possible power mode configurations of each major module or function respectively.

**Table 4 Power mode configurations**

| Module/function | Active Mode | Stop Mode | Sleep Mode | Comment |
|---|---|---|---|---|
| VDD1V5PD | ON | ON | ON | Power Down Supply |
| VPRE, VDDP, VDDC | ON | ON (no dynamic load) | OFF | – |
| VDDEXT | ON/OFF | ON (no dynamic load)/OFF cyclic ON/OFF | OFF | – |
| HS | ON/OFF | cyclic ON/OFF | cyclic ON/OFF | cyclic sense |
| LSx | ON/OFF | OFF | OFF | – |
| PWM GEN. | ON/OFF | OFF | OFF | – |
| LIN TRx | ON/OFF | wake-up only/ OFF | wake-up only/ OFF | – |
| MON1 - MON5 (wake-up) | n.a. | disabled/static/cyclic | disabled/static/ cyclic | cyclic: combined with HS=on |
| MON1 - MON5 (measurement) | ON/OFF | OFF | OFF | available on four channels |
| VS sense | ON/OFF brownout detection | brownout detection | brownout detection | brownout detection done in PCU |
| VBAT_SENSE | ON/OFF | OFF | OFF | – |
| GPIO 5V (wake-up) | n.a. | disabled/static/cyclic | OFF | – |
| GPIO 5V (active) | ON | ON | OFF | – |
| WDT1 | ON | OFF | OFF | – |

**Table 4 Power mode configurations**

| Module/function | Active Mode | Stop Mode | Sleep Mode | Comment |
|---|---|---|---|---|
| CYCLIC Modes | n.a. | cyclic wake-up/ cyclic sense/OFF | cyclic wake-up/ cyclic sense/OFF | cyclic sense with HS, VDDEXT; wake-up from cyclic wake needs MC for entering Sleep Mode / Stop Mode again |
| Measurement Unit | ON[1)] | OFF | OFF | – |
| MCU | ON/slow-down/HALT | STOP[2)] | OFF | – |
| CLOCK GEN (MC) | ON | OFF | OFF | – |
| LP_CLK (20 MHz) | ON | OFF | OFF | WDT1 |
| LP_CLK2 (100 kHz) | ON | ON | ON | for cyclic wake-up |

1) Cannot not be switched off due to safety reasons

2) MC PLL clock disabled, MC supply reduced to 0.9 V

### Wake-up Source Prioritization

All wake-up sources have the same priority. In order to handle the asynchronous nature of the wake-up sources, the first wake-up signal will initiate the wake-up sequence. Nevertheless all wake-up sources are latched in order to provide all wake-up events to the application software. The software can clear the wake-up source flags. It is ensured, that no wake-up event is lost.

As default wake-up sources, the LIN and MON inputs are activated after power-on reset only. GPIO ports as wake-up sources are disabled by default after power-on reset. The application software can reconfigure the wake-up sources according to the application needs.

### Wake-up Levels and Transitions

The wake-up can be triggered by rising, falling or both signal edges for each monitor and GPIO input individually.

## 3.1 Power Management Unit (PMU)

The purpose of the power management unit is to ensure the fail safe behavior of embedded automotive systems. Therefore the power management unit controls all system modes including the corresponding transitions. The power management unit is responsible for generating all required voltage supplies for the embedded MCU (VDDC, VDDP) and the external sensor supply (VDDEXT). Additionally, the PMU provides well defined sequences for the system mode transitions and generates hierarchical reset priorities. The reset priorities control the reset behavior of all system functionalities, especially the reset behavior of the embedded MCU, including the test hardware. All these functions are controlled by finite state machines. The system master functionality of the PMU forces the generation of an independent logic supply (Power Down Supply) and system clock (LP_CLK). Therefore the PMU needs a module internal logic supply and system clock which works independently of the MCU clock.

The following state diagram shows the available modes of the device.

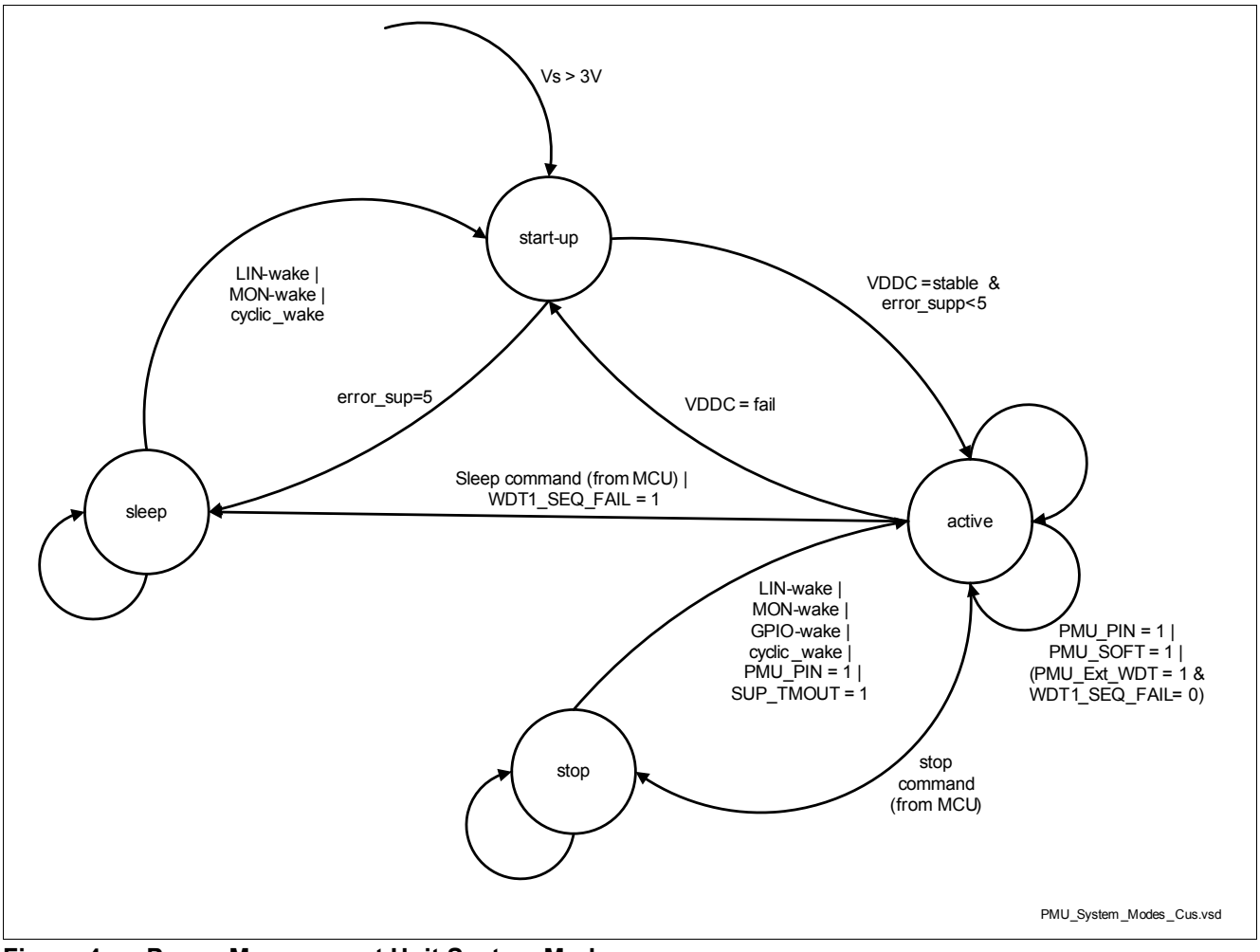


**Figure 4 Power Management Unit System Modes**

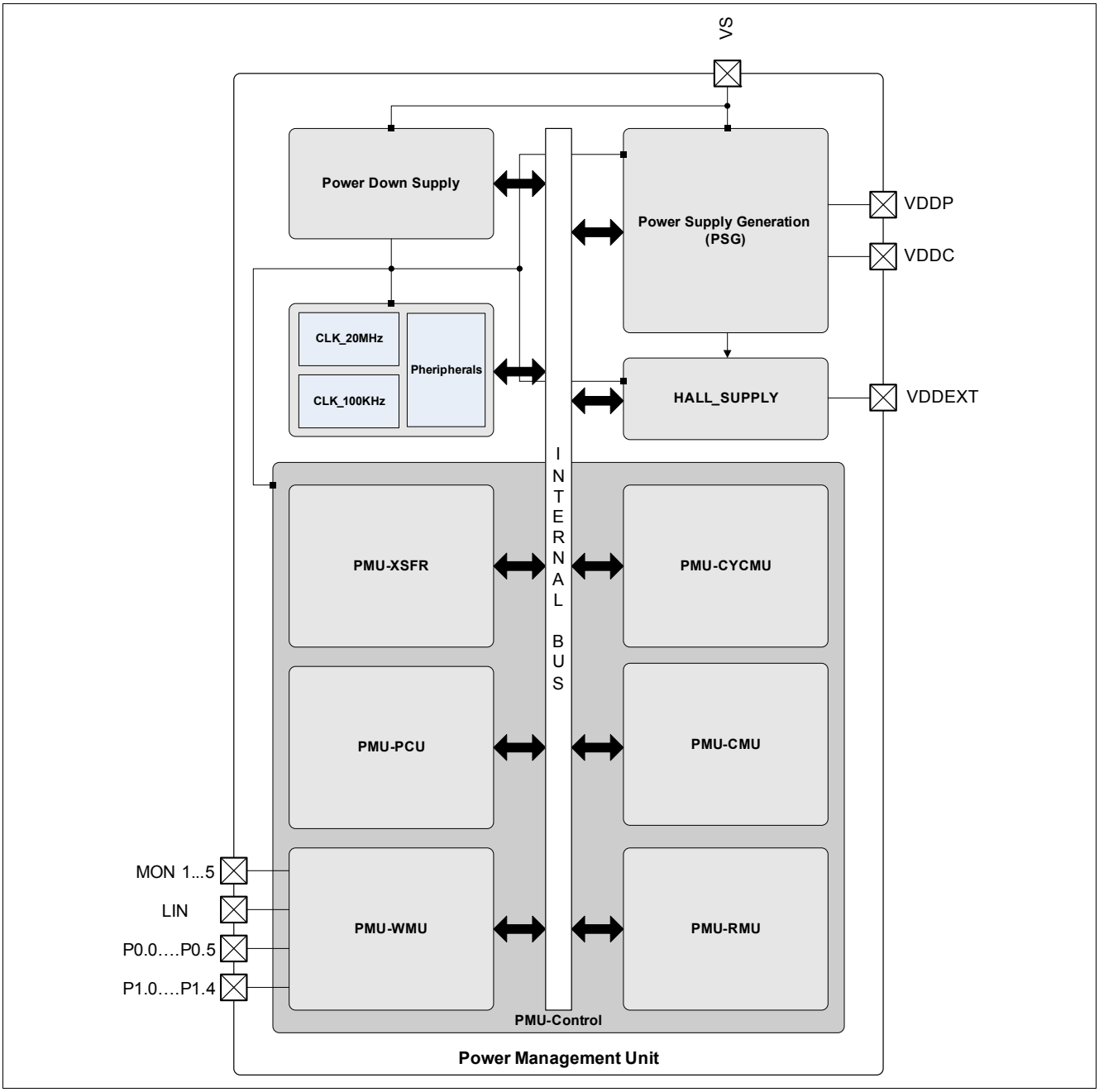


**Figure 5 Power Management Unit Block Diagram**

**Table 5 Description of PMU Submodules**

| Mod. Name | Modules | Functions |
|---|---|---|
| Power Down Supply | Independent Supply Voltage Generation for PMU | This supply is only dedicated to the PMU to ensure a independent operation of generated power supplies (VDDP, VDDC). |
| LP_CLK (= 20 MHz) | - Clock Source for all PMU submodules<br>- Backup Clock Source for System<br>- Clock Source for WDT1 | This ultra low power oscillator generates the clock for the PMU.<br>This clock is also used as backup clock for the system in case of PLL clock failure and as independent clock source for WDT1 |
| LP_CLK2 (= 100 kHz) | Clock Source for PMU | This ultra low power oscillator generates the clock for the PMU mainly in Stop Mode and in the cyclic modes. |
| Peripherals | Peripheral blocks of PMU | This blocks includes all relevant peripherals to ensure a stable and fail safe PMU startup and operation |
| Power Supply Generation Unit (PGU) | Voltage regulators for VDDP and VDDC | This block includes the voltage regulators for the pad supply (VDDP) and the core supply (VDDC) including all diagnosis and safety features |
| VDDEXT (Hall Sensor Supply) | Voltage regulator for VDDEXT to supply external modules (e.g. Hall Sensors) | This voltage regulator is a dedicated supply for external modules and can also be used for cyclic sense operations (e.g. with hall sensor) |
| PMU-XSFR | All PMU relevant Extended Special Function Registers | This module contains all PMU relevant registers, which are needed to control and monitor the PMU. |
| PMU-PCU | Power Control Unit of the PMU | This block is responsible for controlling all power related actions within the PGU Module. |
| PMU-WMU | Wake-up Management Unit of the PMU | This block is responsible for controlling all wake-up related actions within the PMU Module. |
| PMU-CYCMU | Cyclic Management Unit of the PMU | This block is responsible for controlling all actions within cyclic mode. |
| PMU-CMU | Clock Management Unit of the PMU | This block is responsible for controlling all clocking actions within the PMU. |
| PMU-RMU | Reset Management Unit of the PMU | This block is responsible for generating all system required resets. |

### 3.1.1 Voltage Regulator 5.0V (VDDP)

This module represents the 5 V voltage regulator, which serves as pad supply for the parallel port pins and other 5 V analog functions.

**Features**

- 5 V low-drop voltage regulator
- Current limitation
- Overcurrent monitoring and shutdown with MCU signalling (Interrupt)
- Overvoltage monitoring with MCU signalling (Interrupt)
- Undervoltage monitoring with MCU signalling (Interrupt)
- Preregulator for VDDC regulator
- GPIO supply
- Pull-down current source at the output for Sleep Mode (100 µA)

The output capacitor $C_{VDDP}$ is mandatory to ensure a proper regulator functionality.

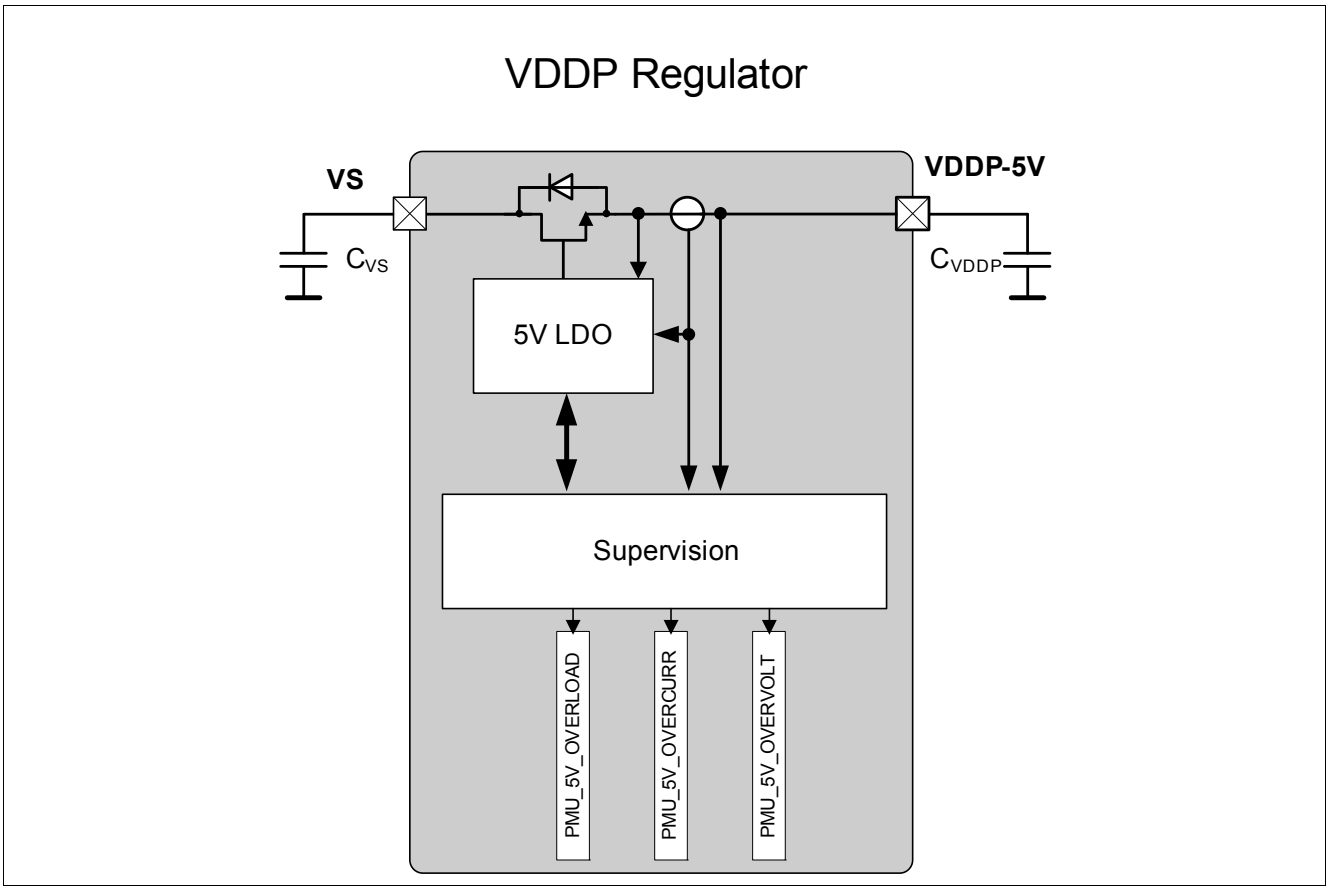


**Figure 6 Module Block Diagram of VDDP Voltage Regulator**

### 3.1.2 Voltage Regulator 1.5V (VDDC)

This module represents the 1.5 V voltage regulator, which serves as core supply for the 8-bit µC and other chip internal analog 1.5 V functions (e.g. 8 Bit ADC). To further reduce the current consumption of the 8-bit MCU during Stop Mode the output voltage is optionally reduced to 0.9 V.

**Features**

- 1.5 V low-drop voltage regulator
- Optional 0.9 V in Stop Mode
- Current limitation
- Overcurrent monitoring and shutdown with MCU signalling (interrupt)
- Overvoltage monitoring with MCU signalling (interrupt)
- Undervoltage monitoring with MCU signalling (interrupt)
- Pull-down current source at the output for Sleep Mode (100 µA)

The output capacitor $C_{VDDC}$ is mandatory to ensure a proper regulator functionality.

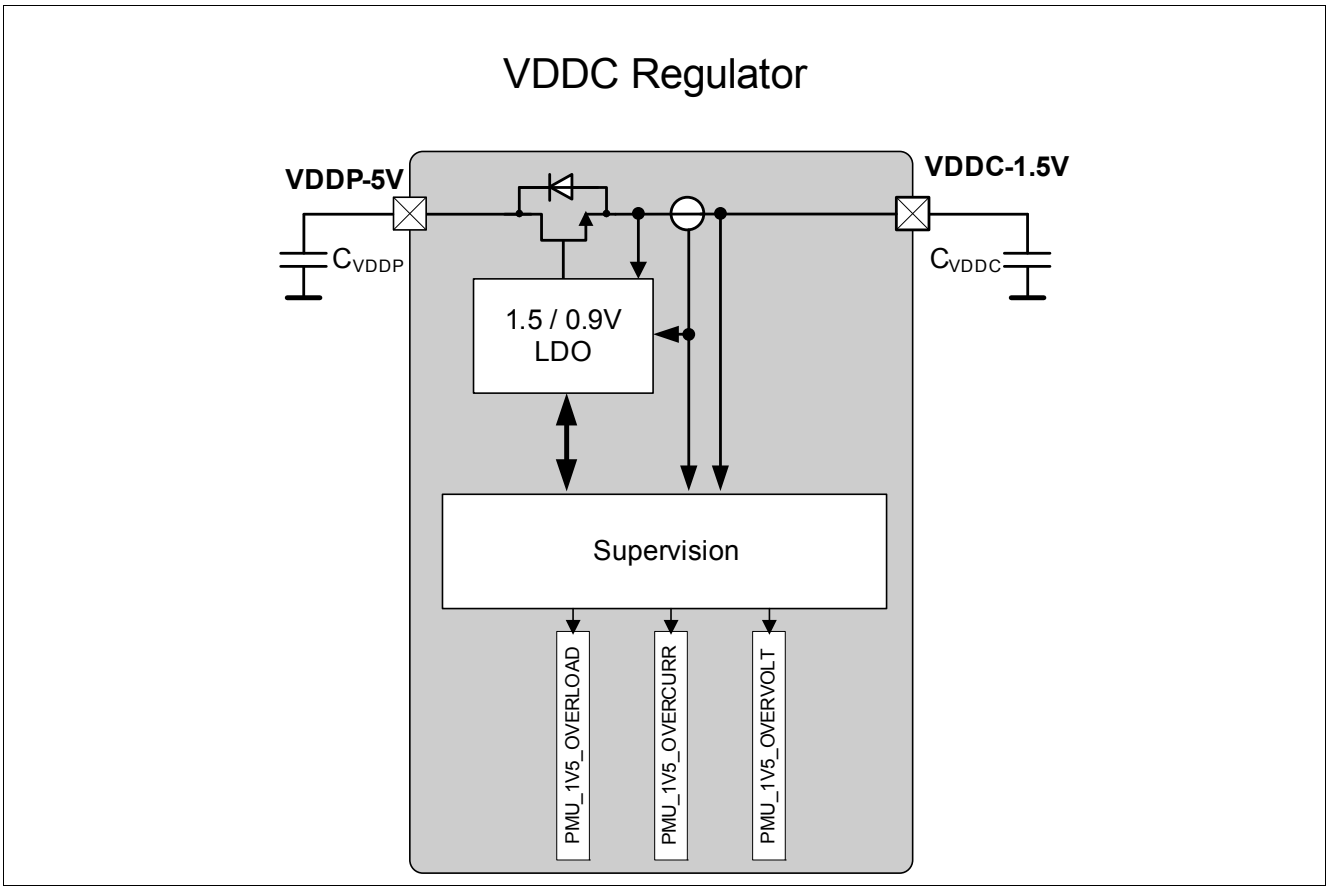


**Figure 7 Module Block Diagram of VDDC Voltage Regulator**

### 3.1.3 External Voltage Regulator 5.0V (VDDEXT)

The external voltage regulator provides 5 V output voltage in order to supply external circuitry like LEDs, hall sensors or potentiometers.

**Features**

- Switchable +5 V, 20 mA low-drop voltage regulator
- Switch-on overcurrent blanking time in order to drive small capacitive loads
- Short circuit robust
- Overvoltage monitoring with MCU interrupt signalling
- Undervoltage monitoring with MCU interrupt signalling
- Selectable switch-on slew-rate 0.95 V/µs max. @10 mA supply current, 10 nF capacitive load
- Pull-down current source at the output for Sleep Mode and off mode (100 µA)
- Cyclic sense option together with GPIOs

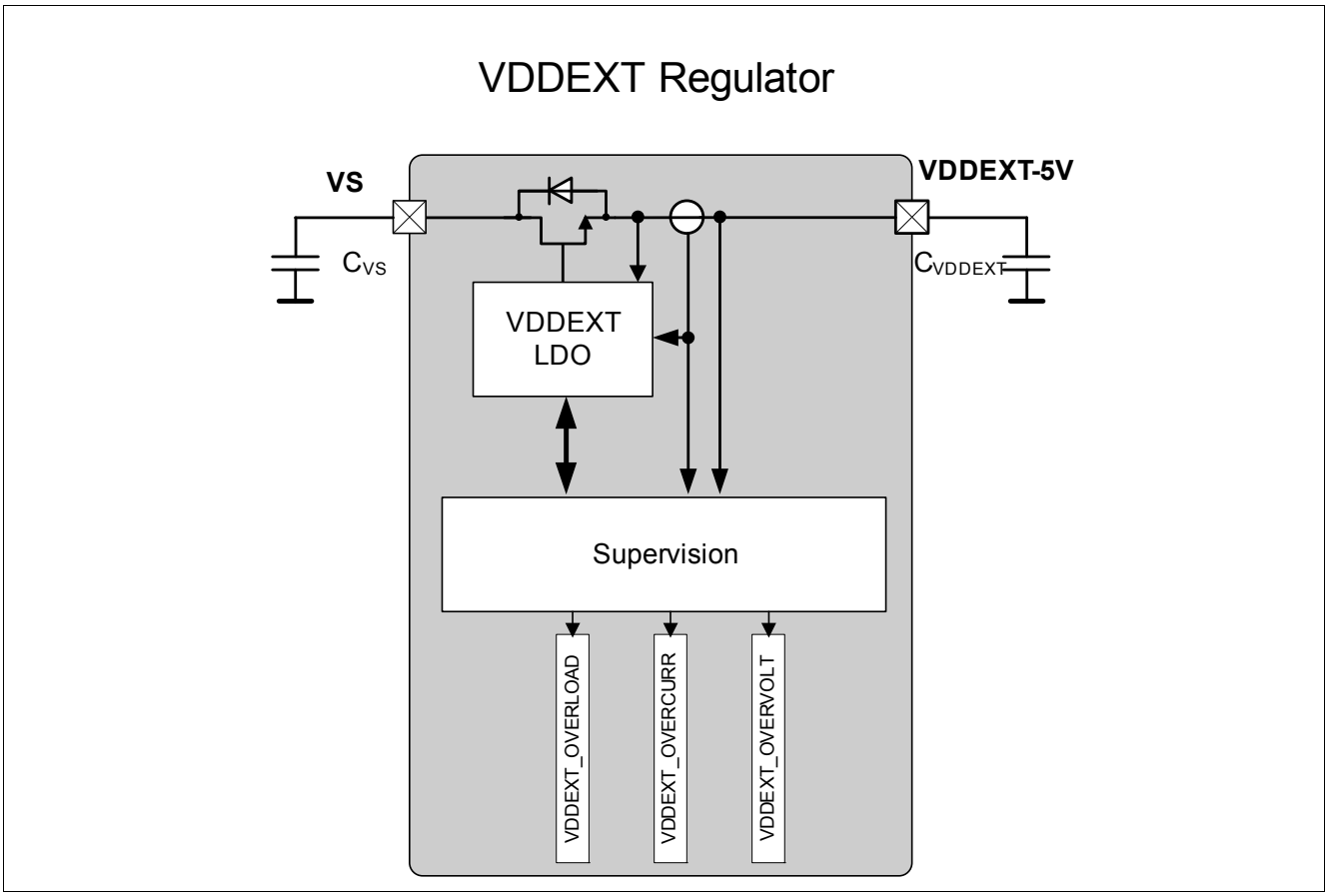


**Figure 8 Module Block Diagram**

## 3.2 System Control Unit

### 3.2.1 System Control Unit - Power Modules

The System Control Unit of the power modules consists of the following sub-modules:

- Reset Control Unit (RCU): generation of all required subsystem resets
- Clock Generation Unit (CGU): providing all required clocks to the analog subsystem
- Interrupt Control Unit (ICU): all system relevant interrupt flags and status flags
- Power Control Unit (PCU): takes over control when device enters and exits Sleep Mode and Stop Mode
- System Status Unit (SSU): controls mode changes due to system failures
- External Watchdog (WDT1): independent system watchdog to monitor system activity

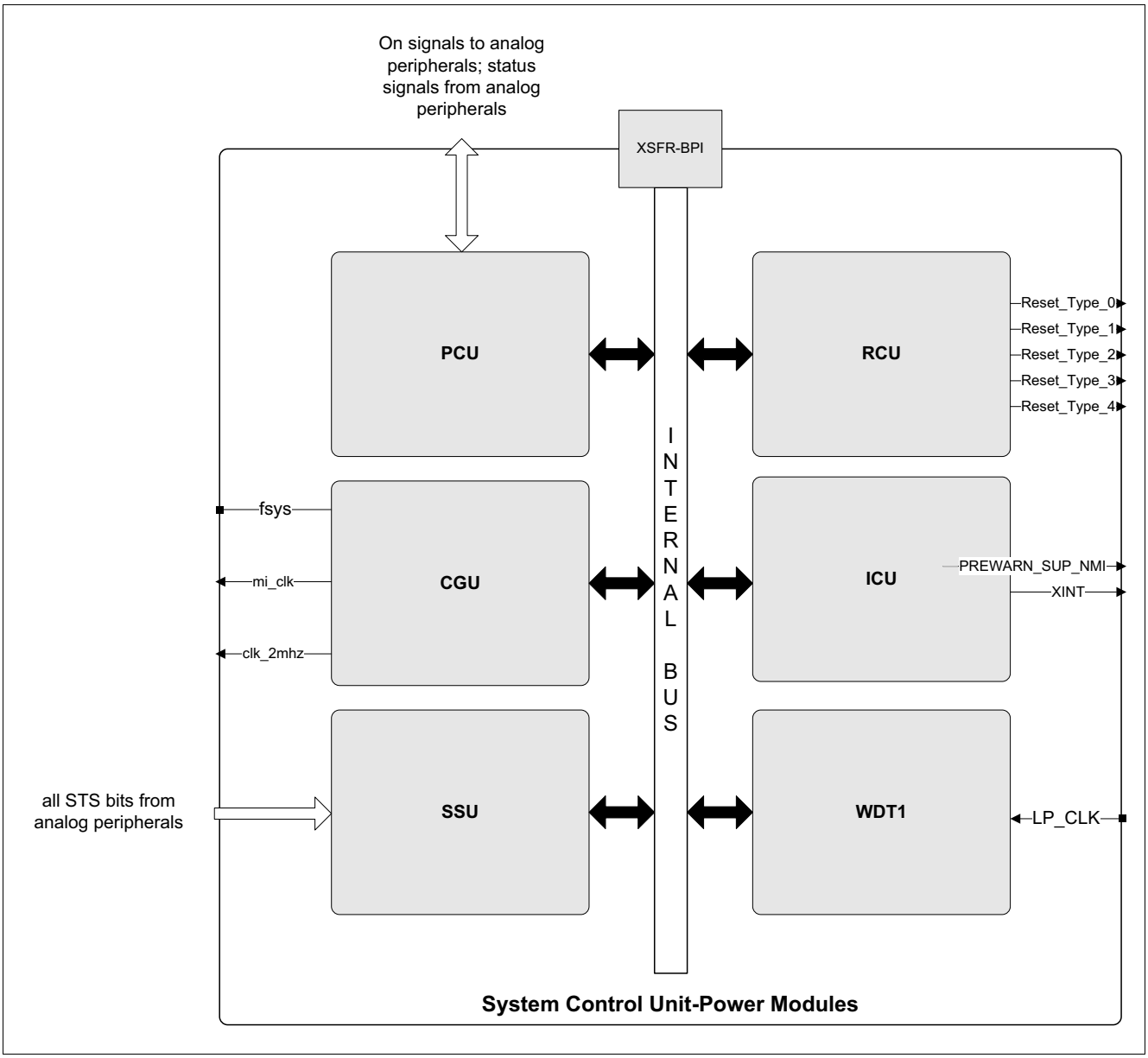


**Figure 9 Block Diagram of System Control Unit - Power Modules**