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TLE9844-2QX

Microcontroller with LIN and Power Switches for Automotive Applications

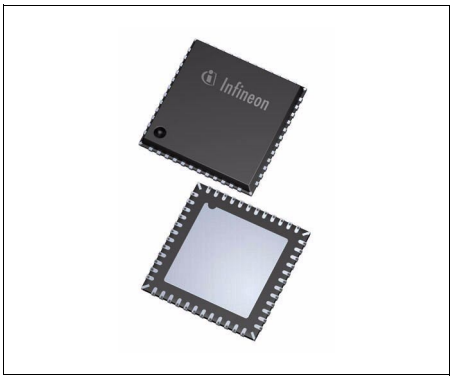
Data Sheet

Rev. 1.0, 2016-05-06

Automotive Power

Table of Contents

1 Overview



VQFN-48-31

Summary of Features

- 32-bit ARM Cortex-M0 Core
  - up to 40 MHz clock frequency
  - one clock per machine cycle architecture
  - single cycle multiplier
- On-chip memory
  - 64 KB Flash (including EEPROM)
  - 4 KB EEPROM (emulated in Flash)
  - 768 bytes 100 Time Programmable Memory (100TP)
  - 4 KB RAM
  - Boot ROM for startup firmware and Flash routines
- On-chip OSC
- 2 Low-Side Switches incl. PWM functionality, can be used e.g. as relay driver
- 2 High-Side Switches with cyclic sense option and PWM functionality, e.g. for supplying LEDs or switch panels (min. 150 mA)
- 5 High Voltage Monitor Input pins for wake-up and with cyclic sense with analog measurement option
- 10 General-purpose I/O Ports (GPIO)
- 6 Analog input Ports
- 10-Bit A/D Converter with 6 analog inputs + VBAT_SENSE + VS + 5 high voltage monitoring inputs
- 8-Bit A/D Converter with 7 inputs for voltage and temperature supervision
- Measurement unit with 12 channels together with the onboard 10-Bit A/D converter and data post processing
- 16-Bit timers - GPT12, Timer 2 and Timer 21
- Capture/compare unit for PWM signal generation (CCU6)
- 2 full duplex serial interfaces (UART1, UART2), UART1 with LIN support
- 2 synchronous serial channels (SSC1, SSC2)
- On-chip debug support via 2-wire SWD
- LIN Bootstrap loader to program the Flash via LIN (LIN BSL)
- 1 LIN 2.2 transceiver
- Single power supply from 3.0 V to 28 V
- Low-dropout voltage regulators (LDO)
- 5 V voltage supply VDDEXT for external loads (e.g. Hall-sensor)
- Core logic supply at 1.5 V
- Programmable window watchdog (WDT1) with independent on-chip clock source
- Power saving modes:
  - Micro Controller Unit slow-down mode

Type	Package	Marking
TLE9844-2QX	VQFN-48-31	TLE9844-2QX

  - Sleep Mode with cyclic sense option
  - Cyclic wake-up during Sleep Mode
  - Stop Mode with cyclic sense option
- Power-on and undervoltage/brownout reset generator
- Overtemperature protection
- Short circuit protection for all voltage regulators and actuators (High Side, Low Side)
- Loss of clock detection with fail safe mode for power switches
- Temperature Range T_J: -40 °C up to 150 °C
- Package VQFN-48-31 with LTI feature
- Green package (RoHS compliant)
- AEC Qualified

1.1 Abbreviations

The following acronyms and terms are used within this document. List see in Table 1.

Table 1 Acronyms

Acronyms	Name
AHB	ARM Advanced High-Performance Bus
CCU6	Capture Compare Unit 6
CGU	Clock Generation Unit
CLKMU	Clock Management Unit
CMU	Cyclic Management Unit
DPP	Data Post Processing
ECC	Error Correction Code
EEPROM	Electrically Erasable Programmable Read Only Memory
GPIO	General Purpose Input Output
HV	High Voltage
ICU	Interrupt Control Unit
LDO	Low DropOut voltage regulator
LIN	Local Interconnect Network
LSB	Least Significant Bit
LTI	Lead Tip Inspection
LV	Low Voltage
MCU	Microcontroller Unit
MF	Measurement Functions
MPU	Memory Protection Unit
MRST	Master Receive / Slave Transmit, corresponds to MISO in SPI
MSB	Most Significant Bit
MTSR	Master Transmit / Slave Receive, corresponds to MOSI in SPI
MU	Measurement Unit
NMI	Non Maskable Interrupt
NVIC	Nested Vector Interrupt Controller
OSC	Oscillator
OTP	One Time Programmable
PBA	Peripheral Bridge
PC	Program Counter
PCU	Power Control Unit
PD	Pull Down
PGU	Power supply Generation Unit
PLL	Phase Locked Loop
PMU	Power Management Unit
PPB	Private Peripheral Bus

Table 1 Acronyms

Acronyms	Name
PSW	Program Status Word
PU	Pull Up
PWM	Pulse Width Modulation
RAM	Random Access Memory
RCU	Reset Control Unit
rfu	reserved for future use
RMU	Reset Management Unit
ROM	Read Only Memory
SCU	System Control Unit
SOW	Short Open Window (for WDT1)
SPI	Serial Peripheral Interface
SSC	Synchronous Serial Channel
SWD	ARM Serial Wire Debug
TCCR	Temperature Compensation Control Register
TMS	Test Mode Select
TSD	Thermal Shut Down
UART	Universal Asynchronous Receiver Transmitter
VBG	Voltage reference Band Gap
VCO	Voltage Controlled Oscillator
WDT1	Watchdog timer in SCU-PM (System Control Unit - Power Modules)
WMU	Wake-up Management Unit
100TP	100 Times Programmable

2 Block Diagram

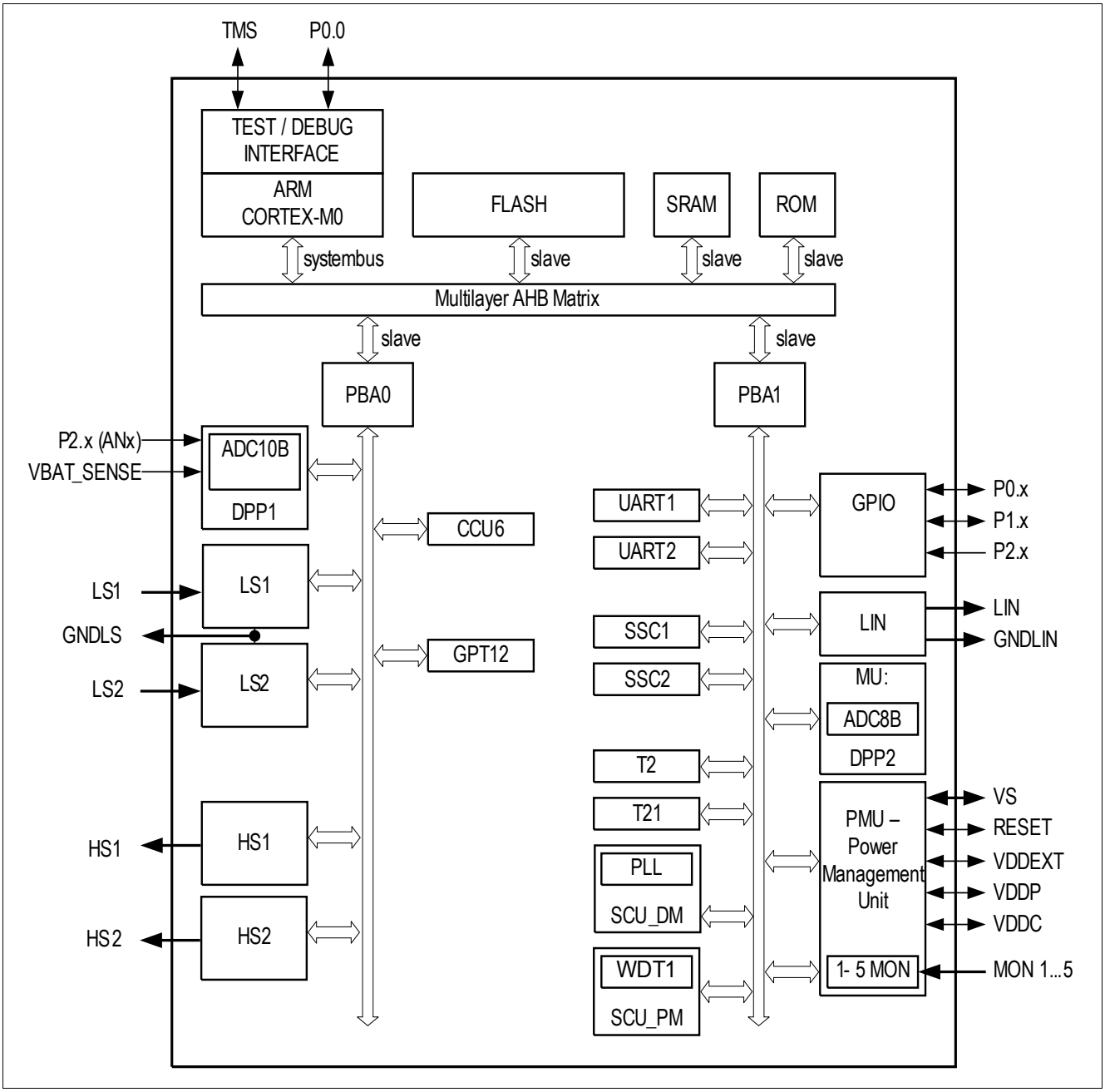


Figure 1 Block Diagram, TLE9844-2QX

3 Device Pinout and Pin Configuration

3.1 Device Pinout

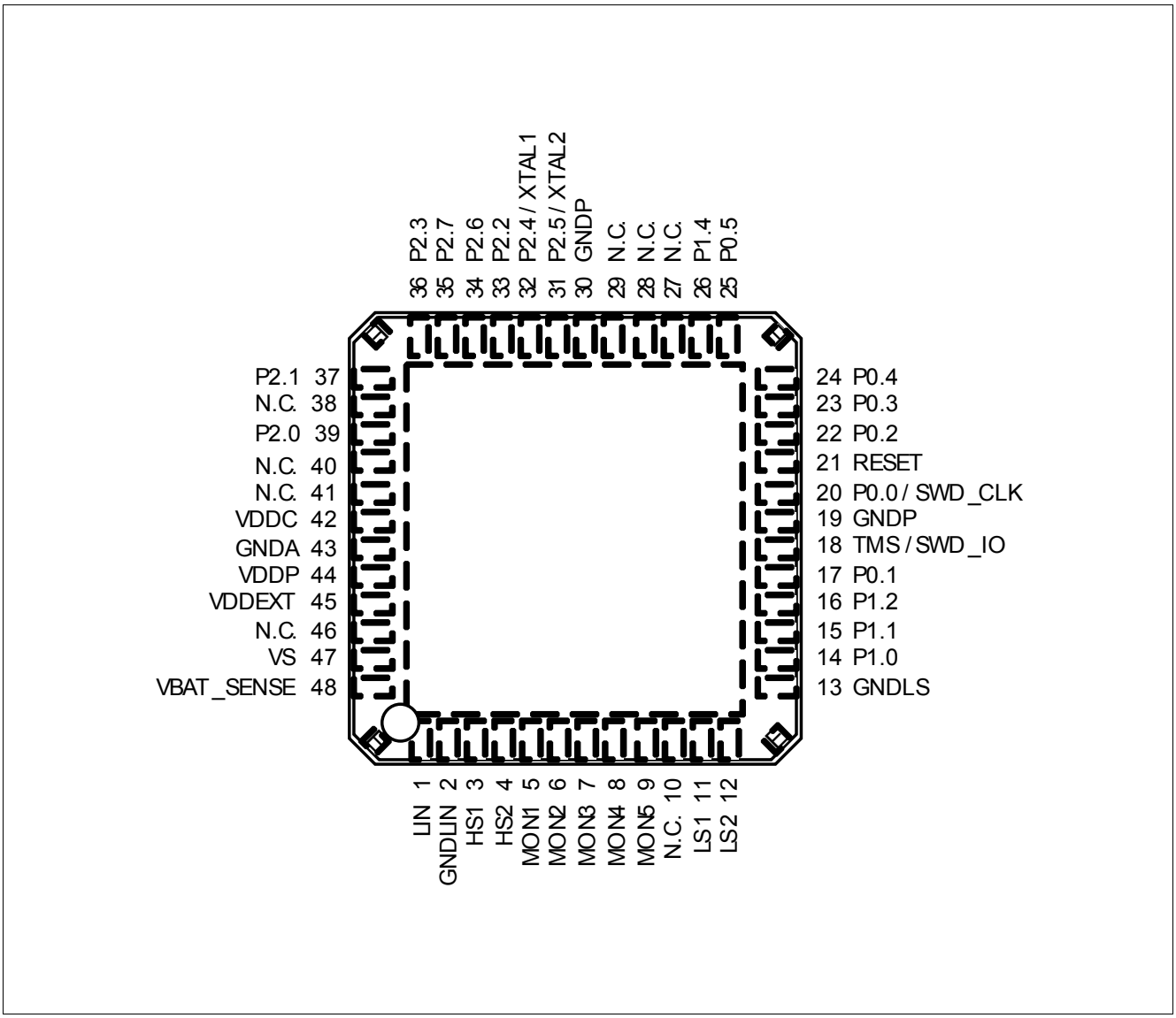


Figure 2 Device Pinout, TLE9844-2QX

3.2 Pin Configuration

After reset, all pins are configured as input (except supply and LIN pins) with one of the following settings:

- Pull-up enabled only (PU)
- Pull-down enabled only (PD)
- Input with both pull-up and pull-down disabled (I)
- Output with output stage deactivated = high impedance state (Hi-Z)

The functions and default states of the TLE9844-2QX external pins are provided in the following table.

Type: indicates the pin type.

- I/O: Input or output
- I: Input only
- O: Output only
- P: Power supply

Not all alternate functions listed, see **Chapter 14**.

Table 2 Pin Definitions and Functions

Symbol	Pin Number	Type	Reset State	Function
P0				**Port 0** Port 0 is an 6-Bit bidirectional general purpose I/O port. Alternate functions can be assigned and are listed in the Port description. Main function is listed below.
P0.0	20	I/O	I/PU	SWD_CLK Serial Wire Debug Clock GPIO General Purpose IO Alternate function mapping see **Table 8**
P0.1	17	I/O	I/PU	GPIO General Purpose IO Alternate function mapping see **Table 8**
P0.2	22	I/O	I/PD	GPIO General Purpose IO Alternate function mapping see **Table 8**
P0.3	23	I/O	I/PU	GPIO General Purpose IO Alternate function mapping see **Table 8**
P0.4	24	I/O	I/PU	GPIO General Purpose IO Alternate function mapping see **Table 8**
P0.5	25	I/O	I/PU	GPIO General Purpose IO Alternate function mapping see **Table 8**
P1				**Port 1** Port 1 is an 4-Bit bidirectional general purpose I/O port. Alternate functions can be assigned and are listed in the Port description. Main function is listed below.
P1.0	14	I/O	I	GPIO General Purpose IO Alternate function mapping see **Table 9**
P1.1	15	I/O	I	GPIO General Purpose IO Alternate function mapping see **Table 9**
P1.2	16	I/O	I	GPIO General Purpose IO Alternate function mapping see **Table 9**
P1.4	26	I/O	I	GPIO General Purpose IO Alternate function mapping see **Table 9**

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Number	Type	Reset State	Function
P2				**Port 2** Port 2 is an 8-Bit general purpose input-only port. Alternate functions can be assigned and are listed in the Port description. Main function is listed below.
P2.0	39	I	I	AN0 ADC1 analog input channel 12 Alternate function mapping see **Table 10**
P2.1	37	I	I	AN1 ADC1 analog input channel 7 Alternate function mapping see **Table 10**
P2.2	33	I	I	AN2 ADC1 analog input channel 8 Alternate function mapping see **Table 10**
P2.3	36	I	I	AN3 ADC1 analog input channel 9 Alternate function mapping see **Table 10**
P2.4	32	I	I	Alternate function mapping see **Table 10** XTAL1[1)] External oscillator input
P2.5	31	I O	I Hi-Z	Alternate function mapping see **Table 10** XTAL2[1)] External oscillator output
P2.6	34	I	I	AN6 ADC1 analog input channel 10 Alternate function mapping see **Table 10**
P2.7	35	I	I	AN7 ADC1 analog input channel 11 Alternate function mapping see **Table 10**
Power Supply				
VS	47	P	–	Battery supply input
VDDP	44	P	–	I/O port supply (5.0 V). Do not connect external loads. For buffer and bypass capacitors.
VDDC	42	P	–	Core supply (1.5 V during Active Mode, 0.9 V during Stop Mode). Do not connect external loads. For buffer/bypass capacitor.
VDDEXT	45	P	–	External voltage supply output (5.0 V, 20 mA)
GNDLS	13	P	–	Low-side ground LS1, LS2
GNDP	19, 30	P	–	Core supply ground
GNDA	43	P	–	Analog supply ground
GNDLIN	2	P	–	LIN ground
Monitor Inputs				
MON1	5	I	I	High Voltage Monitor Input 1
MON2	6	I	I	High Voltage Monitor Input 2
MON3	7	I	I	High Voltage Monitor Input 3
MON4	8	I	I	High Voltage Monitor Input 4
MON5	9	I	I	High Voltage Monitor Input 5
High-Side Switch / Low-Side Switch Outputs				
LS1	11	O	Hi-Z	Low-Side switch output 1

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Number	Type	Reset State	Function
LS2	12	O	Hi-Z	Low-Side Switch output 2
HS1	3	O	Hi-Z	High-Side Switch output 1
HS2	4	O	Hi-Z	High-Side Switch output 2
LIN Interface				
LIN	1	I/O	PU	LIN bus interface input/output
Others				
TMS	18	I	I/PD	TMS test mode select input SWD_IO Serial Wire Debug input/output
RESET	21	I/O	I/O/PU	Reset input/output, not available during Sleep Mode
VBAT_SENSE	48	I	I	Battery supply voltage sense input
N.C.	10, 27, 28, 29, 38, 40, 41, 46	–	–	Not connected, can be connected to GND
EP	–	–	–	Exposed Pad, connect to GND

1) configurable by user

4 Modes of Operation

This highly integrated circuit contains analog and digital functional blocks. For system and interface control an embedded 32-Bit Cortex-M0 microcontroller is included. For internal and external power supply purposes, on-chip low drop-out regulators are existent. An internal oscillator (no external components necessary) provides a cost effective and suitable clock in particular for LIN slave nodes. As communication interface, a LIN transceiver and several High Voltage Monitor Inputs with adjustable threshold and filters are available. Furthermore two High-Sides Switches (e.g. for driving LEDs or powering of switches), two low-side switches (e.g. for relays) and several general purpose input/outputs (GPIO) with pulse-width modulation (PWM) capabilities are available.

The Micro Controller Unit supervision and system protection including reset feature is controlled by a programmable window watchdog. A cyclic wake-up circuit, supply voltage supervision and integrated temperature sensors are available on-chip.

All relevant modules offer power saving modes in order to support terminal 30 connected automotive applications. A wake-up from the power saving mode is possible via a LIN bus message, via the monitoring inputs or repetitive with a programmable time period (cyclic wake-up).

The integrated circuit is available in a package with 0.5 mm pitch and is designed to withstand the challenging conditions of automotive applications.

The TLE9844-2QX has several operational modes mainly to support low power consumption requirements. The low power modes and state transitions are depicted in **Figure 3** below.

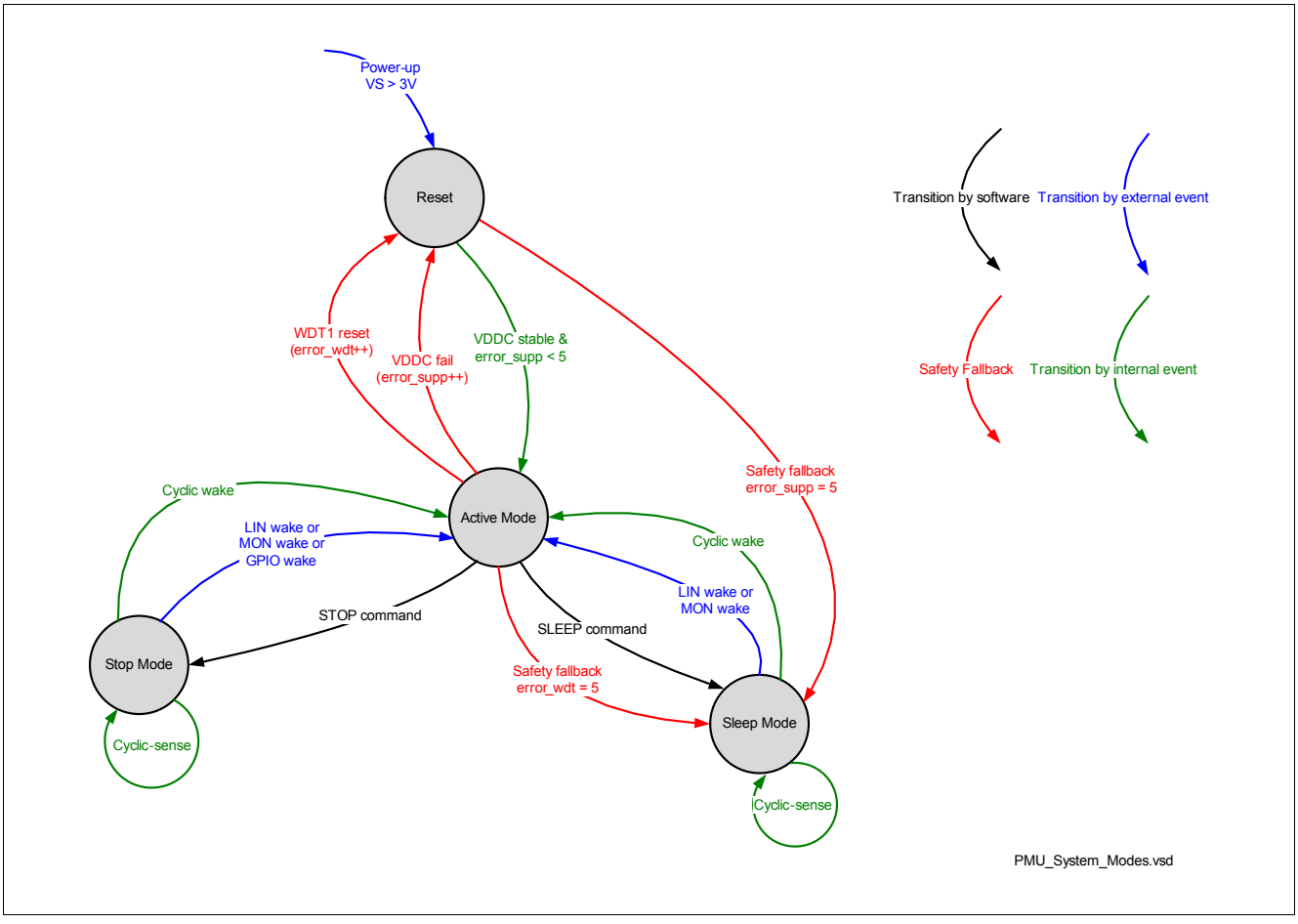


Figure 3 Power Control State Diagram

Reset Mode

The Reset Mode is a transition mode e.g. during power-up of the device after a power-on reset. In this mode the on-chip power supplies are enabled and all other modules are initialized. Once the core supply VDDC is stable, the Active Mode is entered. In case the watchdog timer WDT1 fails for more than four times, a fail-safe transition to the Sleep Mode is done.

Active Mode

In Active Mode all modules are activated and the TLE9844-2QX is fully operational.

Stop Mode

The Stop Mode is one out of two major low power modes. The transition to the low power modes is done by setting the respective Bits in the mode control register. In Stop Mode the embedded microcontroller is still powered allowing faster wake-up reaction times, but not clocked. A wake-up from this mode is possible by LIN bus activity, the High Voltage Monitor Input pins or the respective 5V GPIOs.

Sleep Mode

The Sleep Mode is a major low-power mode. The transition to the low-power modes is done by setting the respective Bits in the Micro Controller Unit mode control register. The sleep time is configurable. In Sleep Mode the embedded microcontroller power supply is deactivated, allowing the lowest system power consumption, but the wake-up time is longer compared to the Stop Mode. In this mode a 64 bit wide buffer for data storage is available. A wake-up from this mode is possible by LIN bus activity or the High Voltage Monitor Input pins and cyclic wake. A wake-up from Sleep Mode behaves similar to a power-on reset. While changing into Sleep Mode, no incoming wake-requests are lost (i.e. no dead-time). It is possible to enter sleep-mode even with LIN dominant.

Cyclic Wake-up Mode

The cyclic wake-up mode is a special operating mode of the Sleep Mode and the Stop Mode. The transition to the cyclic wake-up mode is done by first setting the respective Bits in the mode control register followed by the SLEEP or STOP command. Additional to the cyclic wake-up behavior (wake-up after a programmable time period), the wake-up sources of the normal Stop Mode and Sleep Mode are available.

Cyclic Sense Mode

The cyclic sense mode is a special operating mode of the Sleep Mode and the Stop Mode. The transition to the cyclic sense mode is done by first setting the respective Bits in the mode control register followed by the STOP or SLEEP command. In cyclic sense mode the High-Side Switch can be switched on periodically for biasing some switches for example. The wake-up condition is configurable, when the sense result of defined monitor inputs at a window of interest changed compared to the previous wake-up period or reached a defined state respectively. In this case the Active Mode is entered immediately.

The following table shows the possible power mode configurations of each major module or function respectively.

Table 3 Power Mode Configurations

Module/function	Active Mode	Sleep Mode	Stop Mode	Comment
VPRE, VDDP, VDDC	ON	OFF	ON	–
VDDEXT	ON/OFF	OFF	cyclic ON/OFF	–
HSx	ON/OFF	cyclic ON/OFF	cyclic ON/OFF	cyclic sense
LSx	ON/OFF	OFF	OFF	–
LIN TRx	ON/OFF	wake-up only / OFF	wake-up only/ OFF	–

Table 3 Power Mode Configurations (cont'd)

Module/function	Active Mode	Sleep Mode	Stop Mode	Comment
MONx (wake-up)	n.a.	disabled/static/ cyclic	disabled/static/ cyclic	cyclic: combined with HS=on
MONx (measurement)	ON/OFF	OFF	OFF	available on all channels
VS sense	ON/OFF brownout detection	brownout detection	brownout detection	brownout det. done in PCU
VBAT_SENSE	ON/OFF	OFF	OFF	–
GPIO 5V	ON	OFF	ON	–
WDT1	ON	OFF	OFF	–
CYCLIC WAKE	n.a.	cyclic wake-up/ cyclic sense/OFF	cyclic wake-up/ cyclic sense/OFF	cyclic sense with HS; wake-up needs MC for enter Sleep Mode again
Measurement	ON[1)]	OFF	OFF	–
Micro Controller Unit	ON/slow-down/STOP	OFF	OFF	–
CLOCK GEN (MC)	ON	OFF	OFF	–
LP_CLK (f_{LP_CLK})	ON	OFF	OFF	WDT1
LP_CLK2 (f_{LP_CLK2})	ON	ON	ON	for cyclic wake-up

1) May not be switched off due to safety reasons

Wake-up Source Prioritization

All wake-up sources have the same priority. In order to handle the asynchronous nature of the wake-up sources, the first wake-up signal will initiate the wake-up sequence. Nevertheless all wake-up sources are latched in order to provide all wake-up events to the application software. The software can clear the wake-up source flags. It is ensured, that no wake-up event is lost.

As default wake-up sources, MON inputs and cyclic wake are activated after power-on reset, LIN is disabled as wake-up source by default.

Wake-up Levels and Transitions

The wake-up can be triggered by rising, falling or both signal edges for each monitor input individually.

5 Power Management Unit (PMU)

5.1 Features

- System modes control (startup, sleep, stop and active)
- Power management (cyclic wake)
- Control of system voltage regulators with diagnosis (overload, short, overvoltage)
- Fail safe mode detection and operation in case of system errors (watchdog fail)
- Wake-up sources configuration and management (LIN, MON, GPIOs)
- System error logging

5.2 Introduction

The purpose of the power management unit is to ensure the fail safe behavior of the system IC. Therefore the power management unit controls all system modes including the corresponding transitions. The power management unit is responsible for generating all needed voltage supplies for the embedded MCU (VDDC, VDDP) and the external supply (VDDEXT). Additionally, the PMU provides well defined sequences for the system mode transitions and generates hierarchical reset priorities. The reset priorities control the reset behavior of all system functionalities especially the reset behavior of the embedded MCU. All these functions are controlled by finite state machines. The system master functionality of the PMU requires the generation of an independent logic supply and system clock. Therefore the PMU has a module internal logic supply and system clock which works independently of the MCU clock.

5.2.1 Block Diagram

The following figure shows the structure of the Power Management Unit. **Table 4** describes the submodules more detailed.

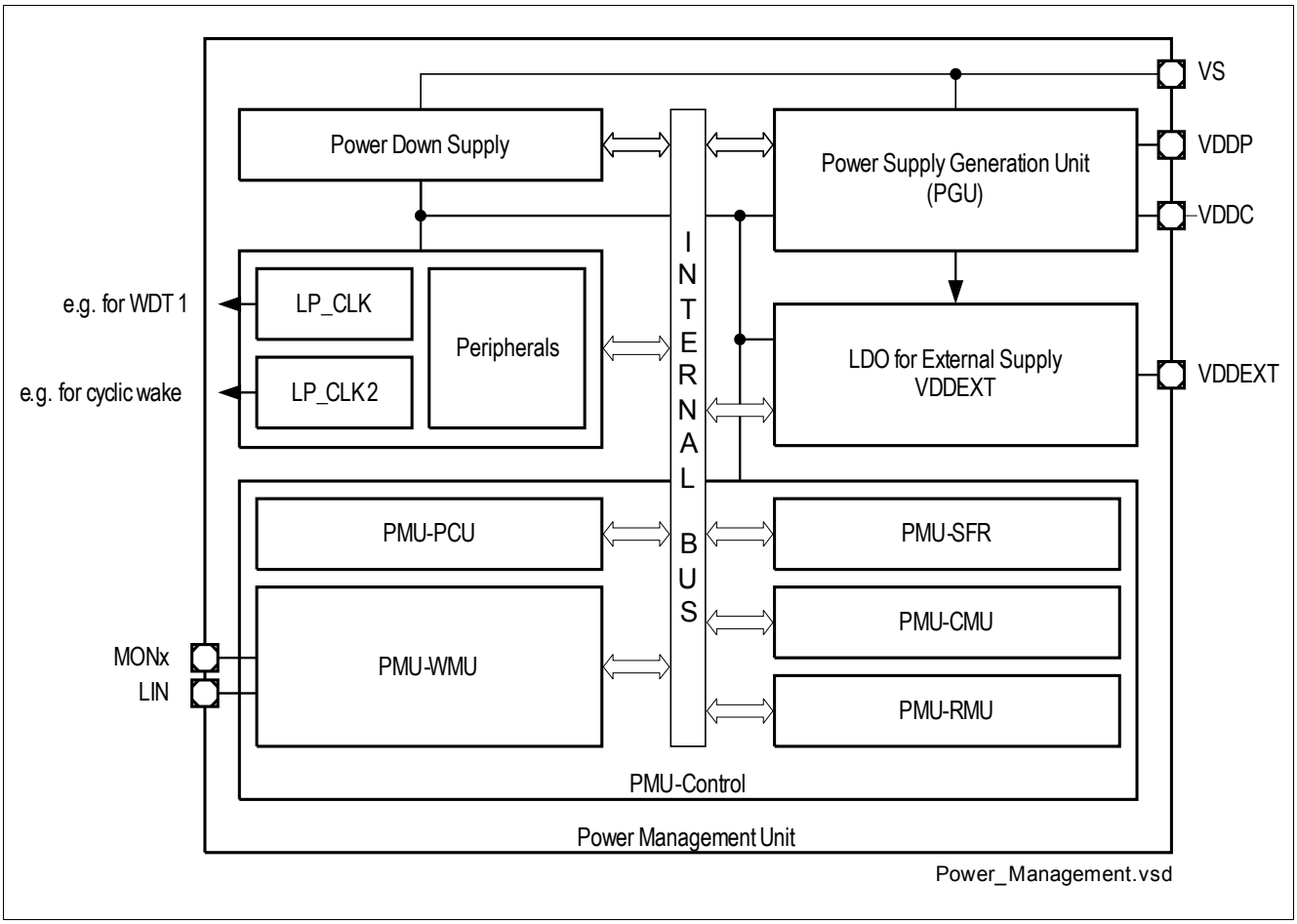


Figure 4 Power Management Unit Block Diagram

Table 4 Description of PMU Submodules

Mod. Name	Modules	Functions
Power Down Supply	Independent Supply Voltage Generation for PMU	This supply is dedicated to the PMU to ensure an independent operation from generated power supplies (VDDP, VDDC).
LP_CLK (=f_{LP_CLK})	- Clock Source for all PMU submodules - Backup Clock Source for System - Clock Source for WDT1	This ultra low power oscillator generates the clock for the PMU. This clock is also used as backup clock for the system in case of PLL Clock failure and as independent clock source for WDT1.
LP_CLK2 (=f_{LP_CLK2})	Clock Source for PMU	This ultra low power oscillator generates the clock for the PMU in Stop Mode and in the cyclic modes.
Peripherals	Peripheral Blocks of PMU	These blocks include the analog peripherals to ensure a stable and fail safe PMU startup and operation (bandgap, bias).

Table 4 Description of PMU Submodules (cont'd)

Mod. Name	Modules	Functions
Power Supply Generation Unit (PGU)	Voltage regulators for VDDP and VDDC	This block includes the voltage regulators for the pad supply (VDDP) and the core supply (VDDC).
VDDEXT	Voltage regulator for VDDEXT to supply external modules (e.g. Sensors)	This voltage regulator is a dedicated supply for external modules.
PMU-SFR	All PMU relevant Extended Special Function Registers	This module contains all PMU relevant registers, which are needed to control and monitor the PMU.
PMU-PCU	Power Control Unit of the PMU	This block is responsible for controlling all power related actions within the PGU Module.It also contains all regulator related diagnosis like under- and overvoltage detection, overcurrent and short circuit diagnoses.
PMU-WMU	Wake-up Management Unit of the PMU	This block is responsible for controlling all Wake-up related actions within the PMU Module.
PMU-CMU	Cyclic Management Unit of the PMU	This block is responsible for controlling all actions within cyclic mode.
PMU-RMU	Reset Management Unit of the PMU	This block generates resets triggered by the PMU like undervoltage or short circuit reset, and passes all resets to the relevant modules and their register. A reset status register with every reset source is available.

5.2.2 PMU Modes Overview

The following state diagram shows the available modes of the device.

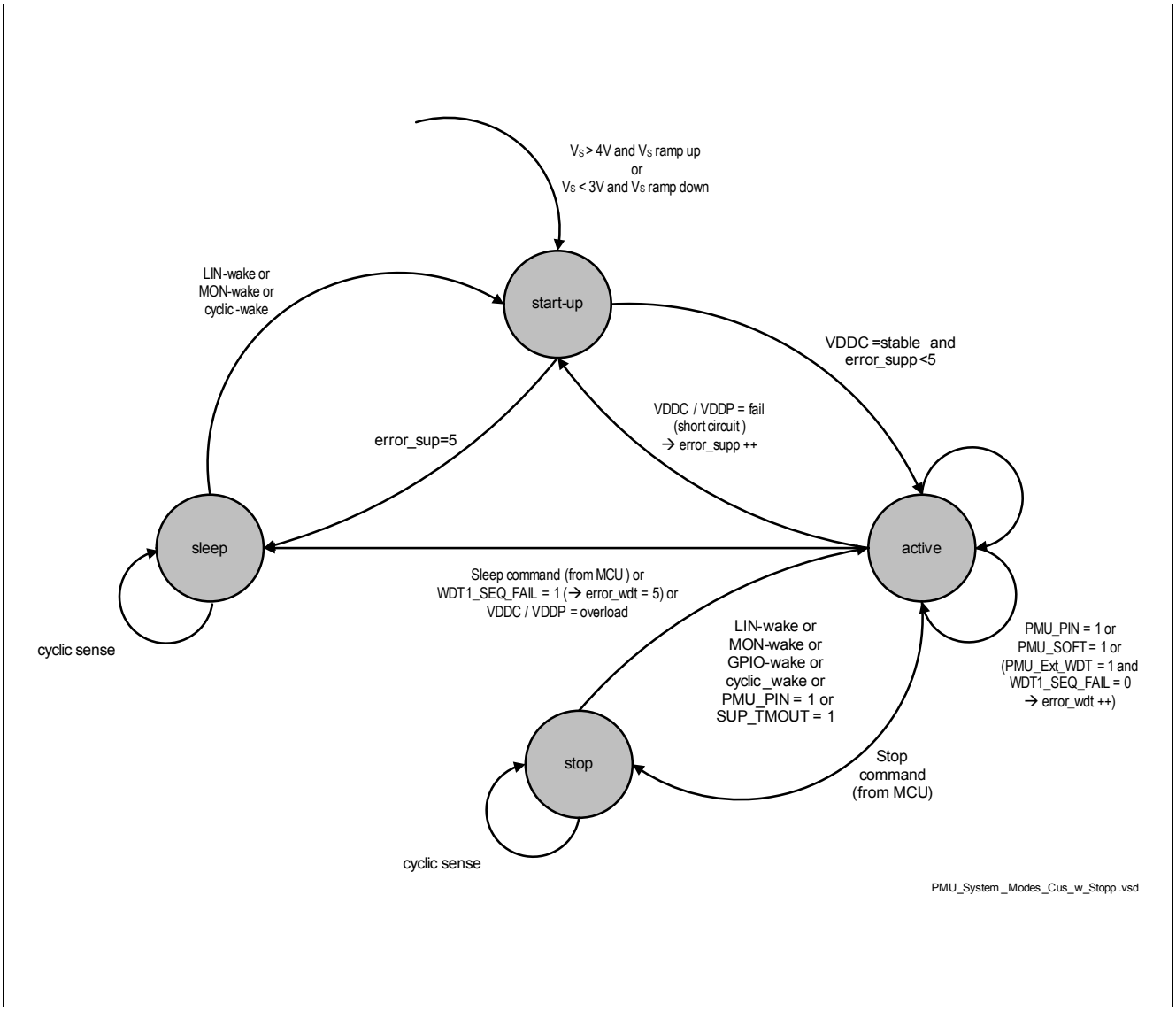


Figure 5 Power Management Unit System Modes

5.3 Power Supply Generation (PGU)

5.3.1 Voltage Regulator 5.0V (VDDP)

This module represents the 5 V voltage regulator, which provides the pad supply for the parallel port pins and other 5 V analog functions (e.g. LIN Transceiver).

Features

- 5 V low-drop voltage regulator
- Overcurrent monitoring and shutdown with MCU signalling (Interrupt)
- Overvoltage monitoring with MCU signalling (Interrupt)
- Undervoltage monitoring with MCU signalling (Interrupt)
- Undervoltage monitoring with Reset (Undervoltage Reset, V_{DDPUV})
- Overtemperature shutdown with MCU signalling (Interrupt)
- Pre-Regulator for VDDC Regulator
- GPIO Supply
- Pull Down Current Source at the output for Sleep Mode only (typ.5 mA)

The output capacitor C_{VDDP} is mandatory to ensure a proper regulator functionality.

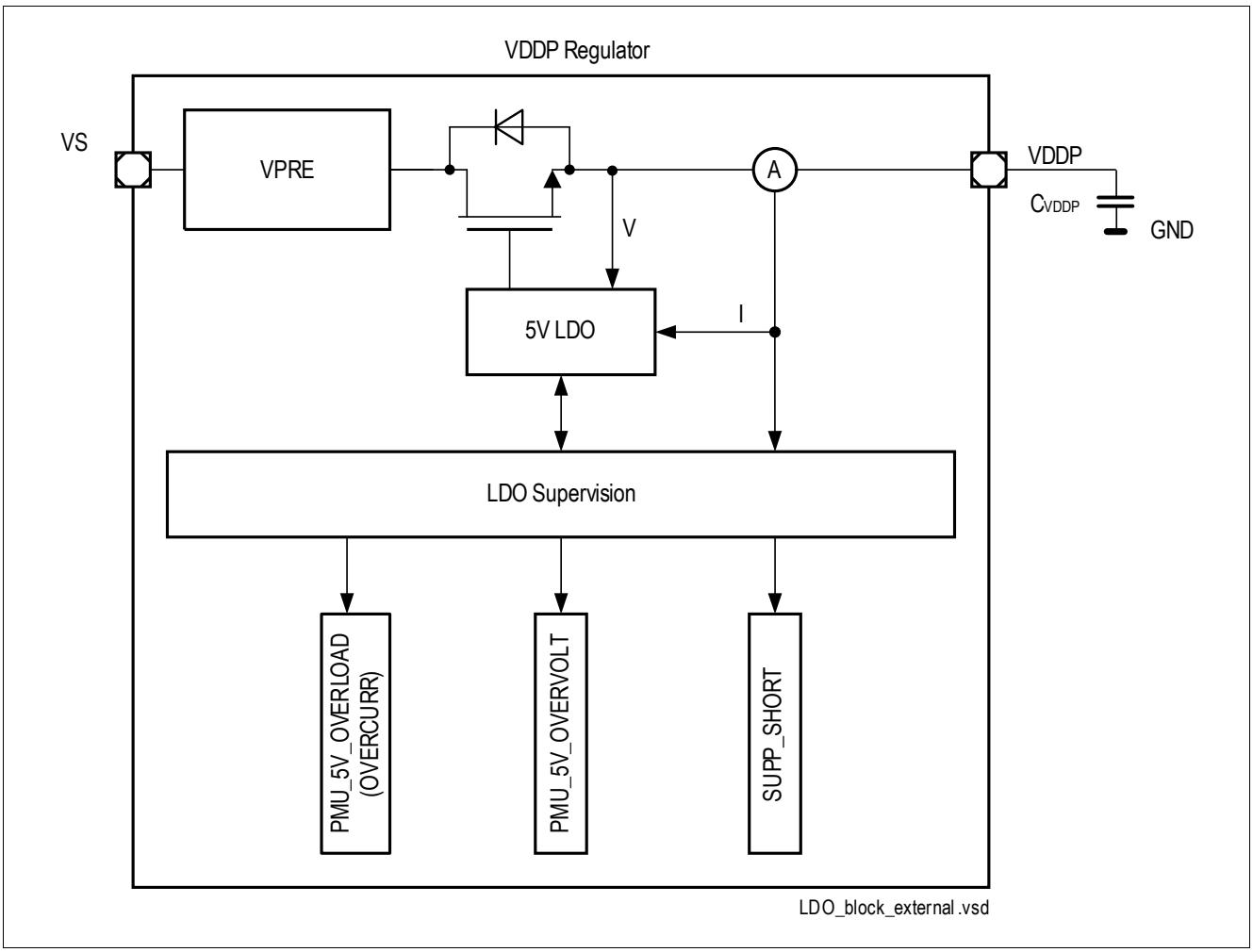


Figure 6 Module Block Diagram of VDDP Voltage Regulator

5.3.2 Voltage Regulator 1.5V (VDDC)

This module represents the 1.5 V voltage regulator, which provides the supply for the microcontroller core, digital peripherals and other chip internal analog 1.5 V functions (e.g. ADC).

Features

- 1.5 V low-drop voltage regulator
- Overcurrent monitoring and Shutdown with MCU signalling (Interrupt)
- Overvoltage monitoring with MCU signalling (Interrupt)
- Undervoltage monitoring with MCU signalling (interrupt)
- Undervoltage monitoring with reset
- Overtemperature Shutdown with MCU signalling (Interrupt)
- Pull Down Current Source at the output for Sleep Mode only (typ. 100 µA)

The output capacitor C_{VDDC} is mandatory to ensure a proper regulator functionality.

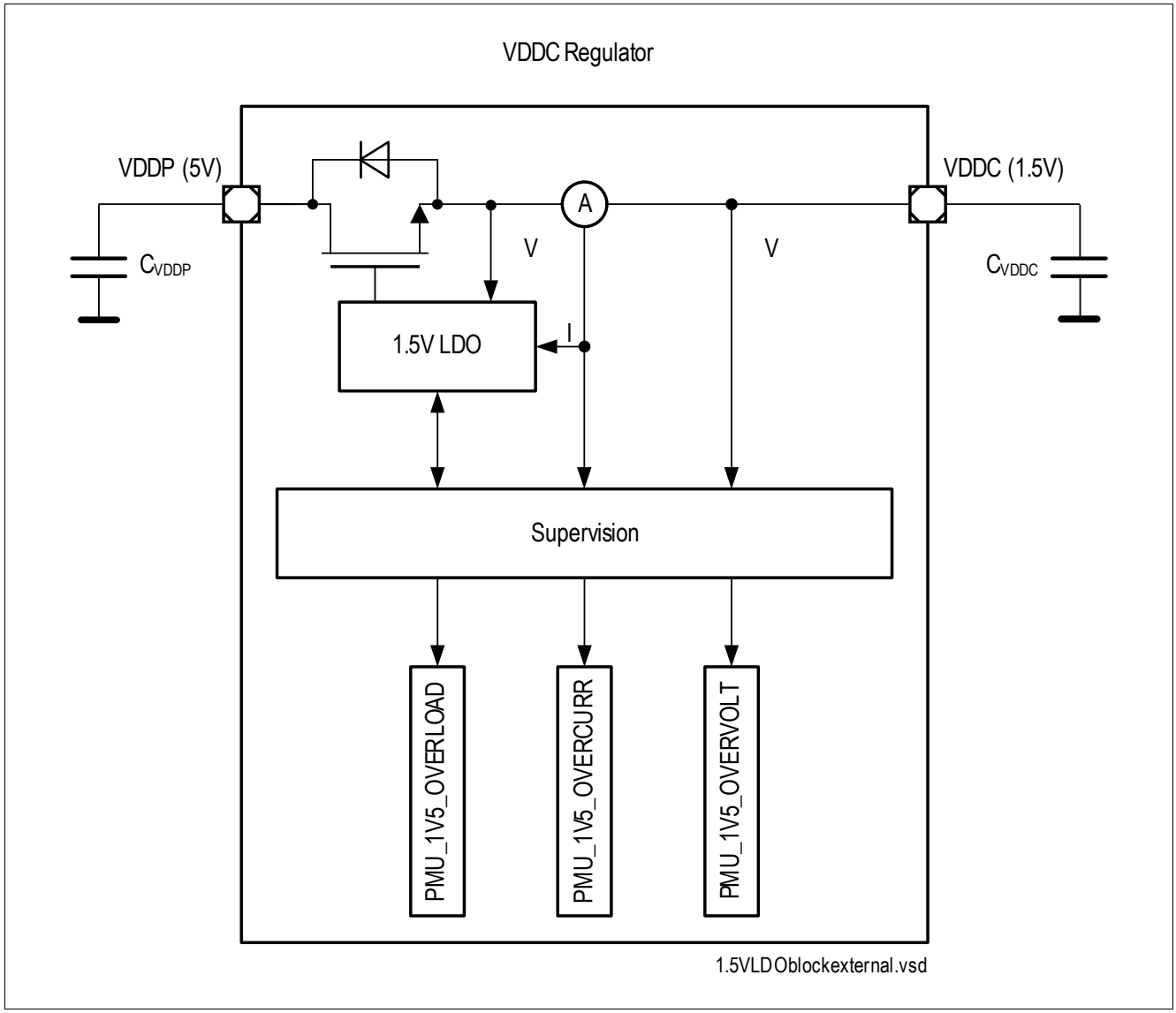


Figure 7 Module Block Diagram of VDDC Voltage Regulator

5.3.3 External Voltage Regulator 5.0V (VDDEXT)

This module represents the 5 V voltage regulator, which serves as a supply for external circuits. It can be used e.g. to supply an external sensor, LEDs or potentiometers.

Features

- Switchable (by software) +5 V, low-drop voltage regulator
- Switch-on undervoltage blanking time in order to drive small capacitive loads
- Intrinsic current limitation
- Undervoltage monitoring and shutdown with MCU signalling (Interrupt)
- Overtemperature Shutdown with MCU signalling (Interrupt)
- Pull Down Current Source at the output for Sleep Mode only (typ. 100 µA)
- Cyclic sense option together with GPIOs
- Low current mode available to ensure reduced stop mode current consumption. In this mode current capability is reduced to I_{VDDEXT_LCM}

The output capacitor C_{VDDEXT} is mandatory to ensure a proper regulator functionality.

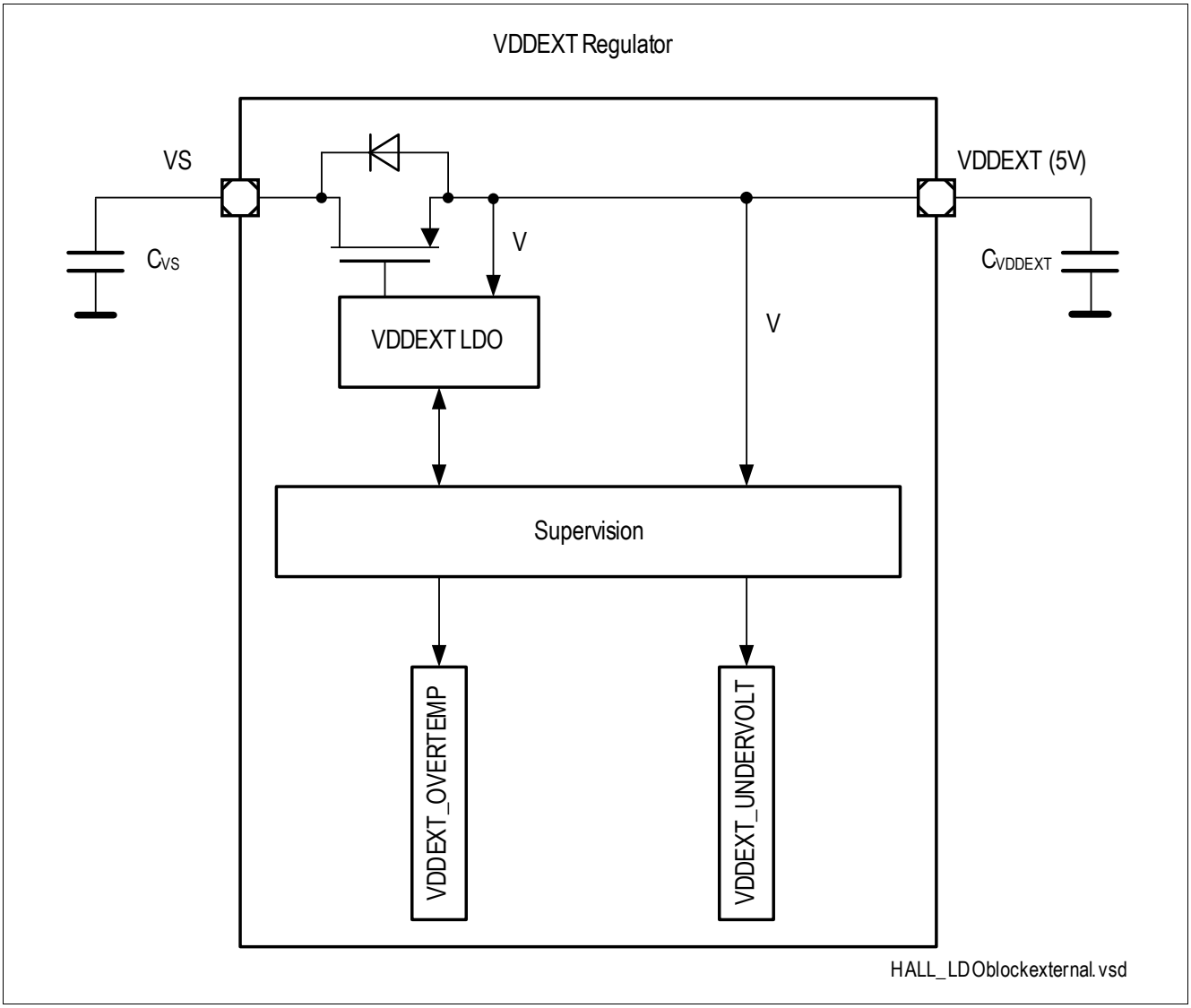


Figure 8 Module Block Diagram

5.3.4 Power-on Reset Concept

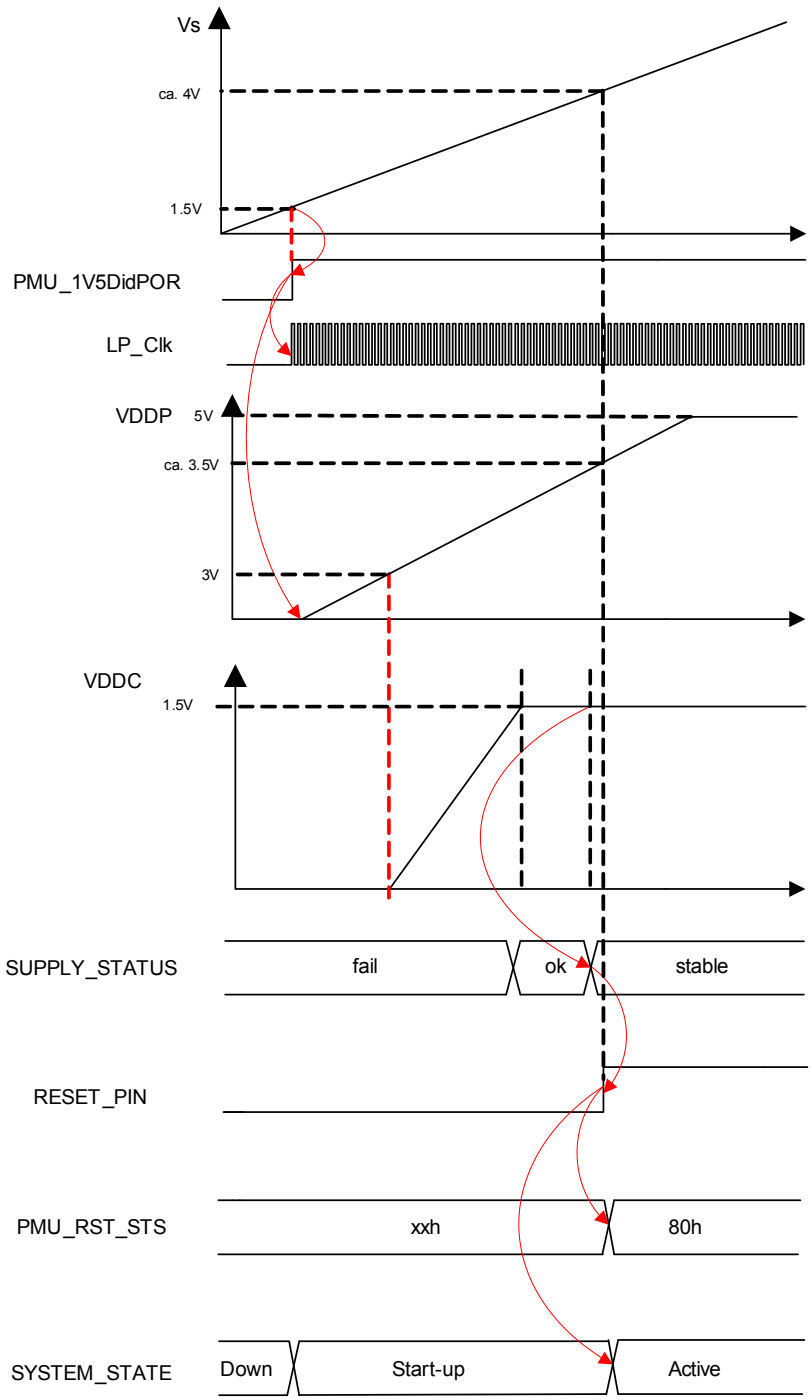


Figure 9 Power-on Reset Concept