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TLE9879QXW40

Microcontroller with LIN and BLDC MOSFET Driver for Automotive Applications

Extended Operating Temperature Range (Grade 0)

BF-Step

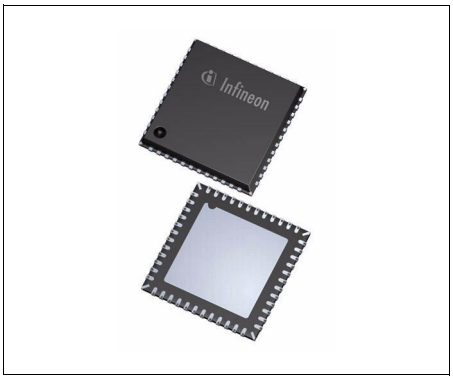
Data Sheet

Rev. 1.1, 2017-03-23

Automotive Power

Table of Contents

1 Overview



VQFN-48-29

Summary of Features

- 32 bit ARM Cortex M3 Core
  - up to 40 MHz clock frequency
  - one clock per machine cycle architecture
- On-chip memory
  - 128 kByte Flash including
  - 4 kByte EEPROM (emulated in Flash)
  - 512 Byte 100 Time Programmable Memory (100TP)
  - 6 kByte RAM
  - Boot ROM for startup firmware and Flash routines
- On-chip OSC and PLL for clock generation
  - PLL loss-of-lock detection
- MOSFET driver including charge pump
- 10 general-purpose I/O Ports (GPIO)
- 5 analog inputs, 10-bit A/D Converter (ADC1)
- 16-bit timers - GPT12, Timer 2, Timer 21 and Timer 3
- Capture/compare unit for PWM signal generation (CCU6)
- 2 full duplex serial interfaces (UART) with LIN support (for UART1 only)
- 2 synchronous serial channels (SSC)
- On-chip debug support via 2-wire SWD
- 1 LIN 2.2 transceiver
- 1 high voltage monitoring input
- Single power supply from 5.5 V to 27 V
- Extended power supply voltage range from 3 V to 28 V
- Low-dropout voltage regulators (LDO)
- High speed operational amplifier for motor current sensing via shunt
- 5 V voltage supply for external loads (e.g. Hall sensor)
- Core logic supply at 1.5 V
- Programmable window watchdog (WDT1) with independent on-chip clock source
- Power saving modes
  - MCU slow-down Mode
  - Sleep Mode
  - Stop Mode
  - Cyclic wake-up Sleep Mode
- Power-on and undervoltage/brownout reset generator

Type	Package	Marking
TLE9879QXW40	VQFN-48-29	

- Overtemperature protection
- Short circuit protection
- Loss of clock detection with fail safe mode entry for low system power consumption
- Temperature Range T_j = -40 °C to +175 °C
- Package VQFN-48 with LTI feature
- Green package (RoHS compliant)
- AEC qualified

1.1 Abbreviations

The following acronyms and terms are used within this document. List see in Table 1.

Table 1 Acronyms

Acronyms	Name
AHB	Advanced High-Performance Bus
APB	Advanced Peripheral Bus
CCU6	Capture Compare Unit 6
CGU	Clock Generation Unit
CMU	Cyclic Management Unit
CP	Charge Pump for MOSFET driver
CSA	Current Sense Amplifier
DPP	Data Post Processing
ECC	Error Correction Code
EEPROM	Electrically Erasable Programmable Read Only Memory
EIM	Exceptional Interrupt Measurement
FSM	Finite State Machine
GPIO	General Purpose Input Output
H-Bridge	Half Bridge
ICU	Interrupt Control Unit
IEN	Interrupt Enable
IIR	Infinite Impulse Response
LDM	Load Instruction
LDO	Low DropOut voltage regulator
LIN	Local Interconnect Network
LSB	Least Significant Bit
LTI	Lead Tip Inspection
MCU	Memory Control Unit
MF	Measurement Functions
MSB	Most Significant Bit
MPU	Memory Protection Unit
MRST	Master Receive Slave Transmit
MTSR	Master Transmit Slave Receive
MU	Measurement Unit
NMI	Non Maskable Interrupt
NVIC	Nested Vector Interrupt Controller
NVM	Non-Volatile Memory
OTP	One Time Programmable
OSC	Oscillator
PBA	Peripheral Bridge

Table 1 Acronyms

Acronyms	Name
PCU	Power Control Unit
PD	Pull Down
PGU	Power supply Generation Unit
PLL	Phase Locked Loop
PPB	Private Peripheral Bus
PU	Pull Up
PWM	Pulse Width Modulation
RAM	Random Access Memory
RCU	Reset Control Unit
RMU	Reset Management Unit
ROM	Read Only Memory
SCU-DM	System Control Unit - Digital Modules
SCU-PM	System Control Unit - Power Modules
SFR	Special Function Register
SOW	Short Open Window (for WDT)
SPI	Serial Peripheral Interface
SSC	Synchronous Serial Channel
STM	Store Instruction
SWD	ARM Serial Wire Debug
TCCR	Temperature Compensation Control Register
TMS	Test Mode Select
TSD	Thermal Shut Down
UART	Universal Asynchronous Receiver Transmitter
VBG	Voltage reference Band Gap
VCO	Voltage Controlled Oscillator
VPRE	Pre Regulator
WDT	Watchdog Timer in SCU-DM
WDT1	Watchdog Timer in SCU-PM
WMU	Wake-up Management Unit
100TP	100 Time Programmable

2 Block Diagram

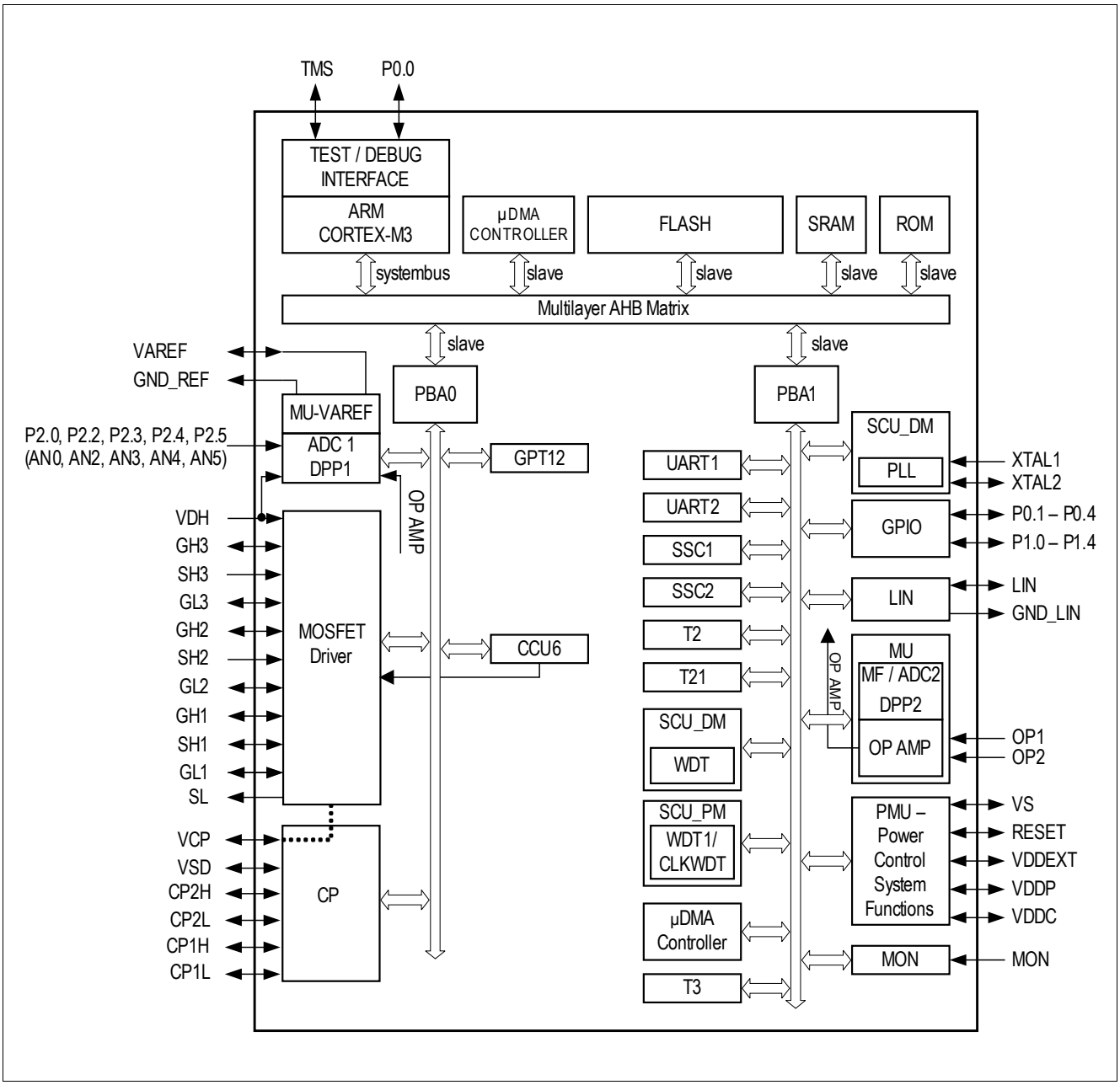


Figure 1 Block Diagram TLE9879QXW40

3 Device Pinout and Pin Configuration

3.1 Device Pinout

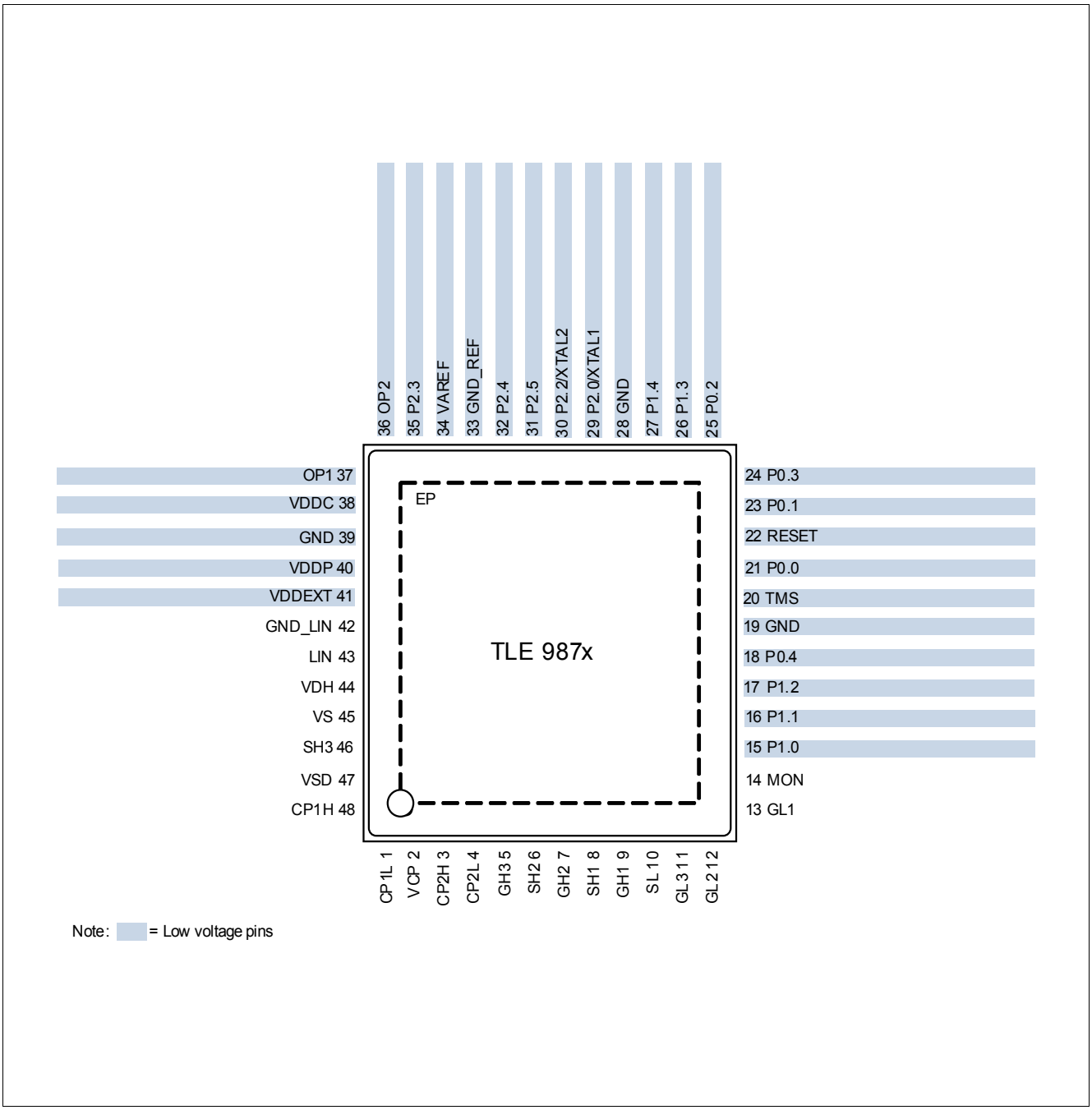


Figure 2 Device Pinout, TLE9879QXW40

3.2 Pin Configuration

After reset, all pins are configured as input (except supply and LIN pins) with one of the following settings:

- Pull-up device enabled only (PU)
- Pull-down device enabled only (PD)
- Input with both pull-up and pull-down devices disabled (I)
- Output with output stage deactivated = high impedance state (Hi-Z)

The functions and default states of the TLE9879QXW40 external pins are provided in the following table.

Type: indicates the pin type.

- I/O: Input or output
- I: Input only
- O: Output only
- P: Power supply

Not all alternate functions listed.

Table 2 Pin Definitions and Functions

Symbol	Pin Number	Type	Reset State[1)]	Function	
P0				**Port 0** Port 0 is a 5-bit bidirectional general purpose I/O port. Alternate functions can be assigned and are listed in the port description. Main function is listed below.	
P0.0	21	I/O	I/PU	SWD	Serial Wire Debug Clock
P0.1	23	I/O	I/PU	GPIO	General Purpose IO Alternate function mapping see **Table 8**
P0.2	25	I/O	I/PD	GPIO	General Purpose IO Alternate function mapping see **Table 8** *Note: For a functional SWD connection this GPIO must be tied to zero!*
P0.3	24	I/O	I/PU	GPIO	General Purpose IO Alternate function mapping see **Table 8**
P0.4	18	I/O	I/PD	GPIO	General Purpose IO Alternate function mapping see **Table 8**
P1				**Port 1** Port 1 is a 5-bit bidirectional general purpose I/O port. Alternate functions can be assigned and are listed in the Port description. The principal functions are listed below.	
P1.0	15	I/O	I	GPIO	General Purpose IO Alternate function mapping see **Table 9**
P1.1	16	I/O	I	GPIO	General Purpose IO Alternate function mapping see **Table 9**
P1.2	17	I/O	I	GPIO	General Purpose IO Alternate function mapping see **Table 9**
P1.3	26	I/O	I	GPIO	General Purpose IO, used for Inrush Transistor Alternate function mapping see **Table 9**
P1.4	27	I/O	I	GPIO	General Purpose IO Alternate function mapping see **Table 9**

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Number	Type	Reset State[1)]	Function
P2				**Port 2** Port 2 is a 5-bit general purpose input-only port. Alternate functions can be assigned and are listed in the Port description. Main function is listed below.
P2.0/XTAL1	29	I/I	I	AN0 ADC analog input 0 Alternate function mapping see **Table 10**
P2.2/XTAL2	30	I/O	I	AN2 ADC analog input 2 Alternate function mapping see **Table 10**
P2.3	35	I	I	AN3 ADC analog input 3 Alternate function mapping see **Table 10**
P2.4	32	I	I	AN4 ADC analog input 4 Alternate function mapping see **Table 10**
P2.5	31	I	I	AN5 ADC analog input 5 Alternate function mapping see **Table 10**
Power Supply				
VS	45	P	–	Battery supply input
VDDP	40	P	–	[2)]I/O port supply (5.0 V). Connect external buffer capacitor.
VDDC	38	P	–	[3)]Core supply (1.5 V during Active Mode). Do not connect external loads, connect external buffer capacitor.
VDDEXT	41	P	–	External voltage supply output (5.0 V, 20 mA)
GND	19	P	–	GND digital
GND	28	P	–	GND digital
GND	39	P	–	GND analog
Monitor Input				
MON	14	I	–	High Voltage Monitor Input
LIN Interface				
LIN	43	I/O	–	LIN bus interface input/output
GND_LIN	42	P	–	LIN ground
Charge Pump				
CP1H	48	P	–	Charge Pump Capacity 1 High, connect external C
CP1L	1	P	–	Charge Pump Capacity 1 Low, connect external C
CP2H	3	P	–	Charge Pump Capacity 2 High, connect external C
CP2L	4	P	–	Charge Pump Capacity 2 Low, connect external C
VCP	2	P	–	Charge Pump Capacity
VSD	47	P	–	Battery supply input for Charge Pump
MOSFET Driver				
VDH	44	P	–	Voltage Drain High Side MOSFET Driver
SH3	46	P	–	Source High Side FET 3
SH2	6	P	–	Source High Side FET 2

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Number	Type	Reset State[1)]	Function
GH2	7	P	–	Gate High Side FET 2
SH1	8	P	–	Source High Side FET 1
GH1	9	P	–	Gate High Side FET 1
SL	10	P	–	Source Low Side FET
GL2	12	P	–	Gate Low Side FET 2
GL1	13	P	–	Gate Low Side FET 1
GH3	5	P	–	Gate High Side FET 3
GL3	11	P	–	Gate Low Side FET 3
Others				
GND_REF	33	P	–	GND for VAREF
VAREF	34	I/O	–	5V ADC1 reference voltage, optional buffer or input
OP1	37	I	–	Negative operational amplifier input
OP2	36	I	–	Positive operational amplifier input
TMS	20	I I/O	I/PD	TMS Test Mode Select input SWD Serial Wire Debug input/output
RESET	22	I/O	–	Reset input, not available during Sleep Mode
EP	–	–	–	Exposed Pad, connect to GND

1) Only valid for digital IOs
2) Also named VDD5V.
3) Also named VDD1V5.

4 Modes of Operation

This highly integrated circuit contains analog and digital functional blocks. An embedded 32-bit microcontroller is available for system and interface control. On-chip, low-dropout regulators are provided for internal and external power supply. An internal oscillator provides a cost effective clock that is particularly well suited for LIN communications. A LIN transceiver is available as a communication interface. Driver stages for a Motor Bridge or BLDC Motor Bridge with external MOSFET are integrated, featuring PWM capability, protection features and a charge pump for operation at low supply voltage. A 10-bit SAR ADC is implemented for high precision sensor measurement. An 8-bit ADC is used for diagnostic measurements.

The Micro Controller Unit supervision and system protection (including a reset feature) is complemented by a programmable window watchdog. A cyclic wake-up circuit, supply voltage supervision and integrated temperature sensors are available on-chip.

All relevant modules offer power saving modes in order to support automotive applications connected to terminal 30. A wake-up from power-save mode is possible via a LIN bus message, via the monitoring input or using a programmable time period (cyclic wake-up).

Featuring LTI, the integrated circuit is available in a VQFN-48-29 package with 0.5 mm pitch, and is designed to withstand the severe conditions of automotive applications.

The TLE9879QXW40 has several operation modes mainly to support low power consumption requirements.

Reset Mode

The Reset Mode is a transition mode used e.g. during power-up of the device after a power-on reset, or after wake-up from Sleep Mode. In this mode, the on-chip power supplies are enabled and all other modules are initialized. Once the core supply VDDC is stable, the device enters Active Mode. If the watchdog timer WDT1 fails more than four times, the device performs a fail-safe transition to Sleep Mode.

Active Mode

In Active Mode, all modules are activated and the TLE9879QXW40 is fully operational.

Stop Mode

Stop Mode is one of two major low power modes. The transition to the low power modes is performed by setting the corresponding bits in the mode control register. In Stop Mode the embedded microcontroller is still powered, allowing faster wake-up response times. Wake-up from this mode is possible through LIN bus activity, by using the high-voltage monitoring pin or the corresponding 5V GPIOs.

Stop Mode with Cyclic Wake-Up

The Cyclic Wake-Up Mode is a special operating mode of the Stop Mode. The transition to the Cyclic Wake-Up Mode is done by first setting the corresponding bits in the mode control register followed by the Stop Mode command. In addition to the cyclic wake-up behavior (wake-up after a programmable time period), asynchronous wake events via the activated sources (LIN and/or MON) are available, as in normal Stop Mode.

Sleep Mode

The Sleep Mode is a low-power mode. The transition to the low-power mode is done by setting the corresponding bits in the MCU mode control register or in case of failure, see below. In Sleep Mode the embedded microcontroller power supply is deactivated allowing the lowest system power consumption. A wake-up from this mode is possible by LIN bus activity, the High Voltage Monitor Input pin or Cyclic Wake-up.

Sleep Mode in Case of Failure

Sleep Mode is activated after 5 consecutive watchdog failures or in case of supply failure (5 times). In this case, MON is enabled as the wake source and Cyclic Wake-Up is activated with 1s of wake time.

Sleep Mode with Cyclic Wake-Up

The Cyclic Wake-Up Mode is a special operating mode of the Sleep Mode. The transition to Cyclic Wake-Up Mode is performed by first setting the corresponding bits in the mode control register followed by the Sleep and Stop Mode command. In addition to the cyclic wake-up behavior (wake-up after a programmable time period), asynchronous wake events via the activated sources (LIN and/or MON) are available, as in normal Sleep Mode.

When using Sleep Mode with cyclic wake-up the voltage regulator is switched off and started again with the wake. A limited number of registers is buffered during sleep, and can be used by SW e.g. for counting sleep/wake cycles.

MCU Slow Down Mode

In MCU Slow Down Mode the MCU frequency is reduced for saving power during operation. LIN communication is still possible. LS MOSFET can be activated.

Wake-Up Source Prioritization

All wake-up sources have the same priority. In order to handle the asynchronous nature of the wake-up sources, the first wake-up signal will initiate the wake-up sequence. Nevertheless all wake-up sources are latched in order to provide all wake-up events to the application software. The software can clear the wake-up source flags. This is to ensure that no wake-up event is lost.

As default wake-up source, the MON input is activated after power-on reset only. Additionally, the device is in Cyclic Wake-Up Mode with the max. configurable dead time setting.

The following table shows the possible power mode configurations including the Stop Mode.

Table 3 Power Mode Configurations

Module/Function	Active Mode	Stop Mode	Sleep Mode	Comment
VDDEXT	ON/OFF	ON (no dynamic load)/OFF	OFF	–
Bridge Driver	ON/OFF	OFF	OFF	
LIN TRx	ON/OFF	wake-up only/ OFF	wake-up only/ OFF	–
VS sense	ON/OFF brownout detection	brownout detection	POR on VS	brownout det. done in PCU
GPIO 5V (wake-up)	n.a.	disabled/static	OFF	–
GPIO 5V (active)	ON	ON	OFF	–
WDT1	ON	OFF	OFF	–
CYCLIC WAKE	n.a.	cyclic wake-up/ cyclic sense/OFF	cyclic wake-up/ OFF	–
Measurement	ON[1)]	OFF	OFF	–
MCU	ON/slow-down/STOP	STOP[2)]	OFF	–
CLOCK GEN (MC)	ON	OFF	OFF	–
LP_CLK (18 MHz)	ON	OFF	OFF	WDT1
LP_CLK2 (100 kHz)	ON/OFF	ON/OFF	ON/OFF	for cyclic wake-up

1) May not be switched off due to safety reasons
2) MC PLL clock disabled, MC supply reduced to 1.1 V

Wake-Up Levels and Transitions

The wake-up can be triggered by rising, falling or both signal edges for the monitor input, by LIN or by cyclic wake-up.

5 Power Management Unit (PMU)

5.1 Features

- System modes control (startup, sleep, stop and active)
- Power management (cyclic wake-up)
- Control of system voltage regulators with diagnosis (overload, short, overvoltage)
- Fail safe mode detection and operation in case of system errors (watchdog fail)
- Wake-up sources configuration and management (LIN, MON, GPIOs)
- System error logging

5.2 Introduction

The power management unit is responsible for generating all required voltage supplies for the embedded MCU (VDDC, VDDP) and the external supply (VDDEXT). The power management unit is designed to ensure fail-safe behavior of the system IC by controlling all system modes including the corresponding transitions. Additionally, the PMU provides well defined sequences for the system mode transitions and generates hierarchical reset priorities. The reset priorities control the reset behavior of all system functionalities especially the reset behavior of the embedded MCU. All these functions are controlled by a state machine. The system master functionality of the PMU make use of an independent logic supply and system clock. For this reason, the PMU has an "Internal logic supply and system clock" module which works independently of the MCU clock.

5.2.1 Block Diagram

The following figure shows the structure of the Power Management Unit. **Table 4** describes the submodules in more detail.

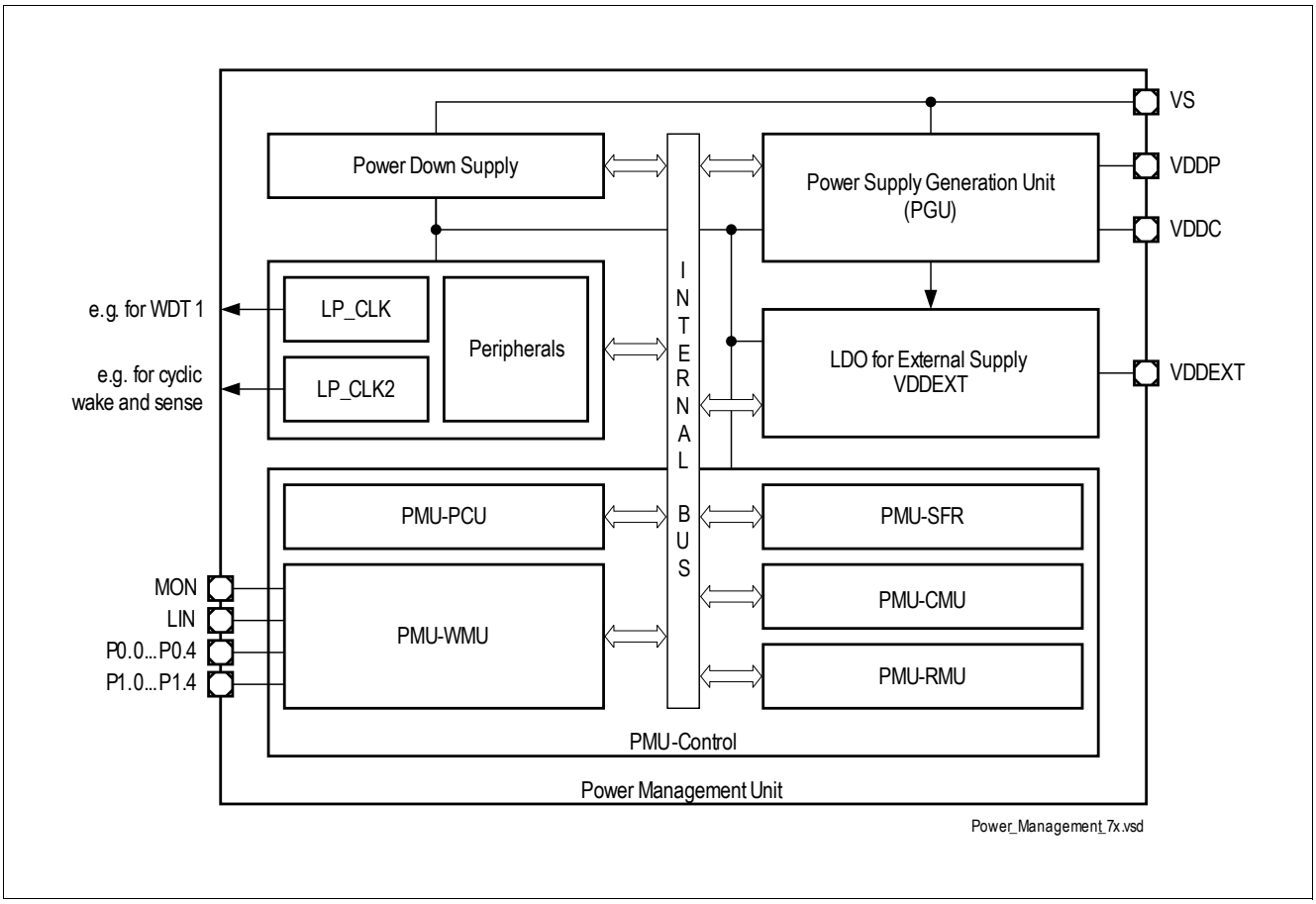


Figure 3 Power Management Unit Block Diagram

Table 4 Description of PMU Submodules

Mod. Name	Modules	Functions
Power Down Supply	Independent supply voltage generation for PMU	This supply is dedicated to the PMU to ensure an independent operation from generated power supplies (VDDP, VDDC).
LP_CLK (= 18 MHz)	- Clock source for all PMU submodules - Backup clock source for System - Clock source for WDT1	This ultra low power oscillator generates the clock for the PMU. This clock is also used as backup clock for the system in case of PLL Clock failure and as an independent clock source for WDT1.
LP_CLK2 (= 100 kHz)	Clock source for PMU	This ultra low power oscillator generates the clock for the PMU in Stop Mode and in the cyclic modes.
Peripherals	Peripheral blocks of PMU	These blocks include the analog peripherals to ensure a stable and fail-safe PMU startup and operation (bandgap, bias).

Table 4 Description of PMU Submodules (cont'd)

Mod. Name	Modules	Functions
Power Supply Generation Unit (PGU)	Voltage regulators for VDDP and VDDC	This block includes the voltage regulators for the pad supply (VDDP) and the core supply (VDDC).
VDDEXT	Voltage regulator for VDDEXT to supply external modules (e.g. sensors)	This voltage regulator is a dedicated supply for external modules and can also be used for cyclic sense operations (e.g. with hall sensor).
PMU-SFR	All Extended Special Function registers that are relevant to the PMU.	This module contains all registers needed to control and monitor the PMU.
PMU-PCU	Power Control Unit of the PMU	This block is responsible for controlling all power related actions within the PGU Module. It also contains all regulator related diagnostics such as undervoltage and overvoltage detection as well as overcurrent and short circuit diagnostics.
PMU-WMU	Wake-Up Management Unit of the PMU	This block is responsible for controlling all wake-up related actions within the PMU Module.
PMU-CMU	Cyclic Management Unit of the PMU	This block is responsible for controlling all actions in cyclic mode.
PMU-RMU	Reset Management Unit of the PMU	This block generates resets triggered by the PMU such as undervoltage or short circuit reset, and passes all resets to the relevant modules and their register.

5.2.2 PMU Modes Overview

The following state diagram shows the available modes of the device.

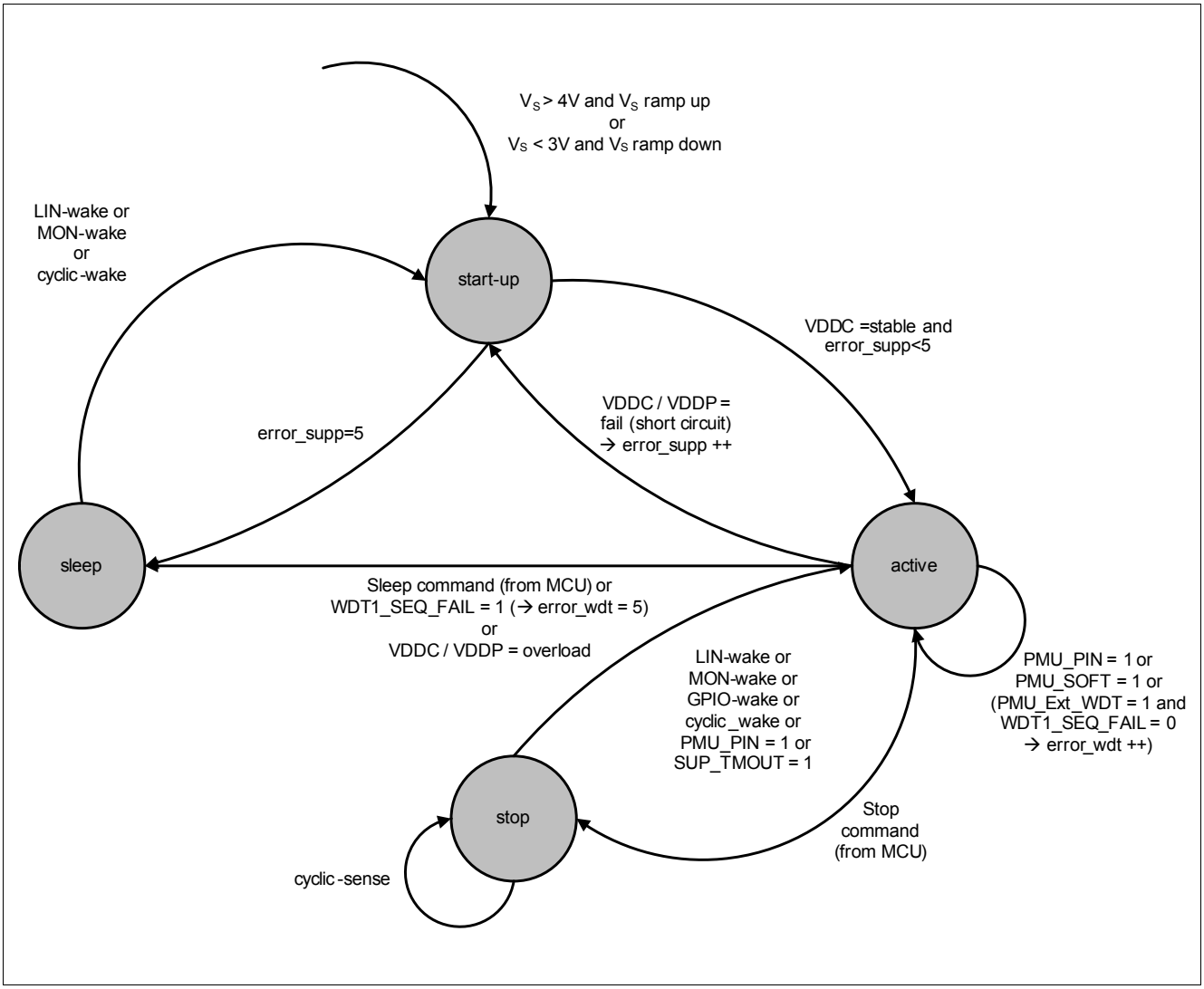


Figure 4 Power Management Unit System Modes

5.3 Power Supply Generation Unit (PGU)

5.3.1 Voltage Regulator 5.0V (VDDP)

This module represents the 5 V voltage regulator, which provides the pad supply for the parallel port pins and other 5 V analog functions (e.g. LIN Transceiver).

Features

- 5 V low-drop voltage regulator
- Overcurrent monitoring and shutdown with MCU signaling (interrupt)
- Overvoltage monitoring with MCU signaling (interrupt)
- Undervoltage monitoring with MCU signaling (interrupt)
- Undervoltage monitoring with reset (Undervoltage Reset, V_{DDPUV})
- Pre-Regulator for VDDC Regulator
- GPIO Supply
- Pull Down Current Source at the output for Sleep Mode only (typ. 5 mA)

The output capacitor C_{VDDP} is mandatory to ensure proper regulator functionality.

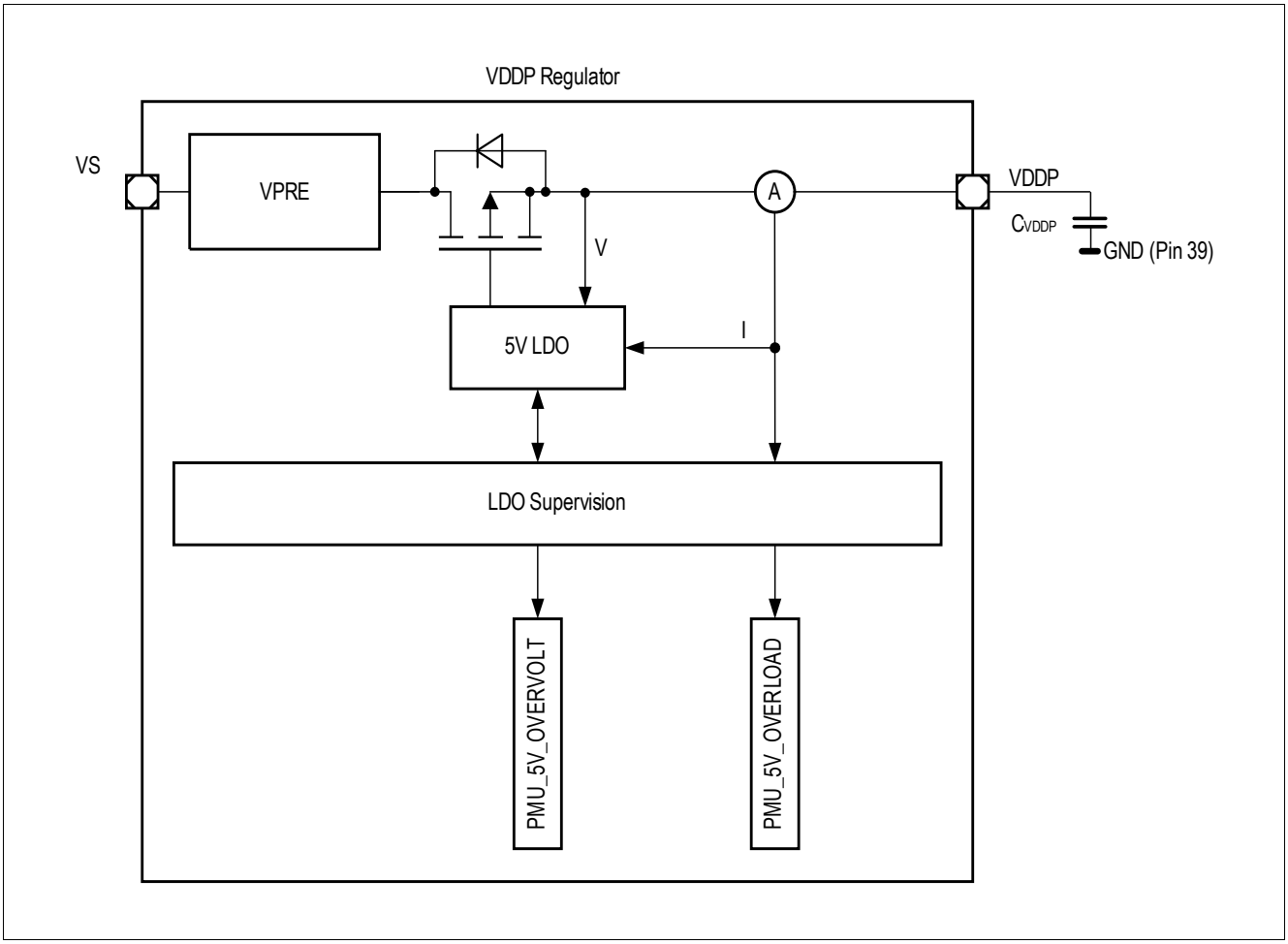


Figure 5 Module Block Diagram of VDDP Voltage Regulator

5.3.2 Voltage Regulator 1.5V (VDDC)

This module represents the 1.5 V voltage regulator, which provides the supply for the microcontroller core, the digital peripherals and other internal analog 1.5 V functions (e.g. ADC2) of the chip. To further reduce the current consumption of the MCU during Stop Mode the output voltage can be lowered to 1.1 V.

Features

- 1.5 V low-drop voltage regulator
- Overcurrent monitoring and shutdown with MCU signaling (interrupt)
- Overvoltage monitoring with MCU signaling (interrupt)
- Undervoltage monitoring with MCU signaling (interrupt)
- Undervoltage monitoring with reset
- Pull Down Current Source at the output for Sleep Mode only (typ. 100 µA)

The output capacitor C_{VDDC} is mandatory to ensure a proper regulator functionality.

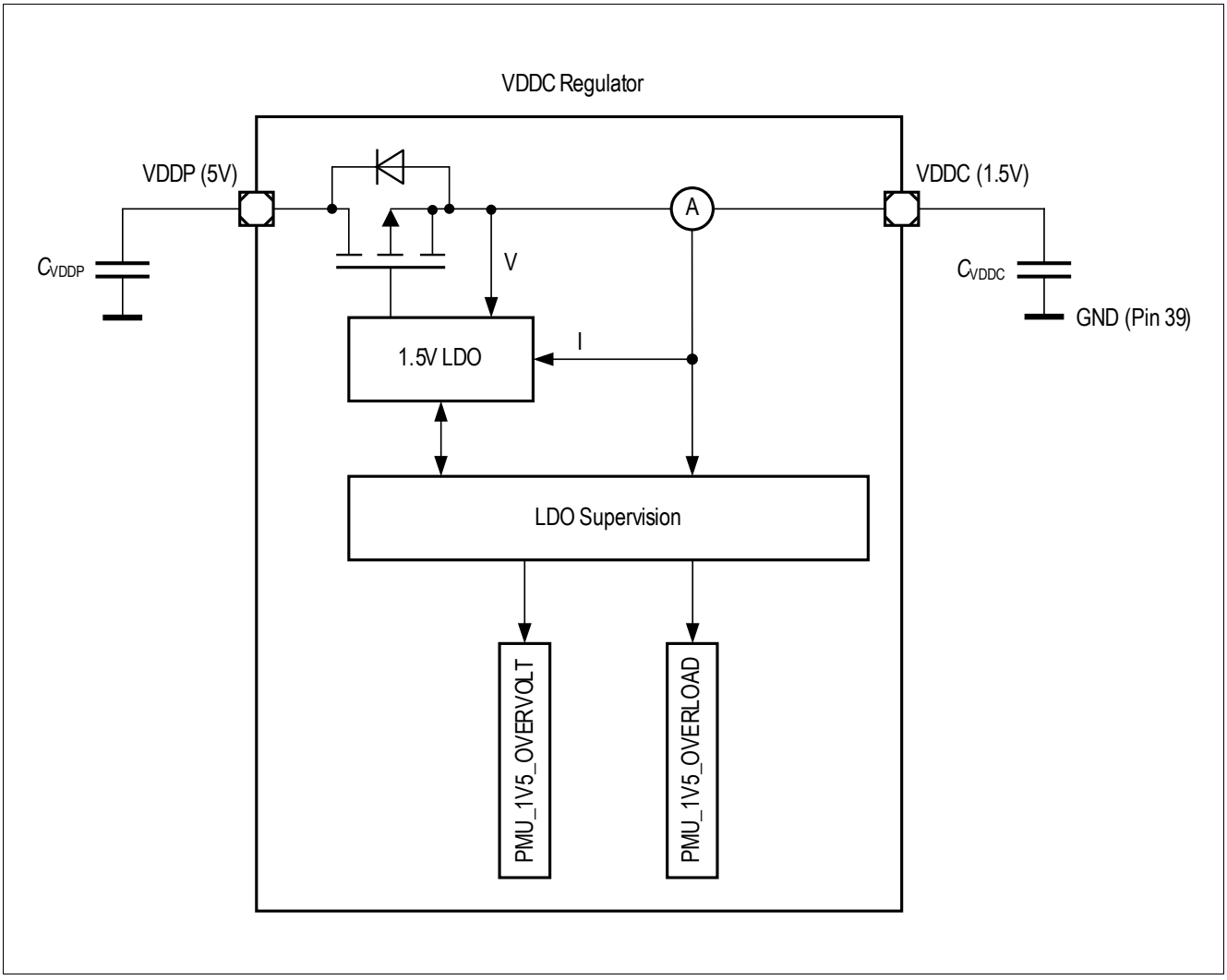


Figure 6 Module Block Diagram of VDDC Voltage Regulator

5.3.3 External Voltage Regulator 5.0V (VDDEXT)

This module represents the 5 V voltage regulator, which serves as a supply for external circuits. It can be used e.g. to supply an external sensor, LEDs or potentiometers.

Features

- Switchable +5 V, low-drop voltage regulator
- Switch-on overcurrent blanking time in order to drive small capacitive loads
- Overcurrent monitoring and shutdown with MCU signaling (interrupt)
- Overvoltage monitoring with MCU signaling (interrupt)
- Undervoltage monitoring with MCU signaling (interrupt)
- Pull Down current source at the output for Sleep Mode only (typ. 100 µA)
- Cyclic sense option together with GPIOs

The output capacitor C_{VDDEXT} is mandatory to ensure a proper regulator functionality.

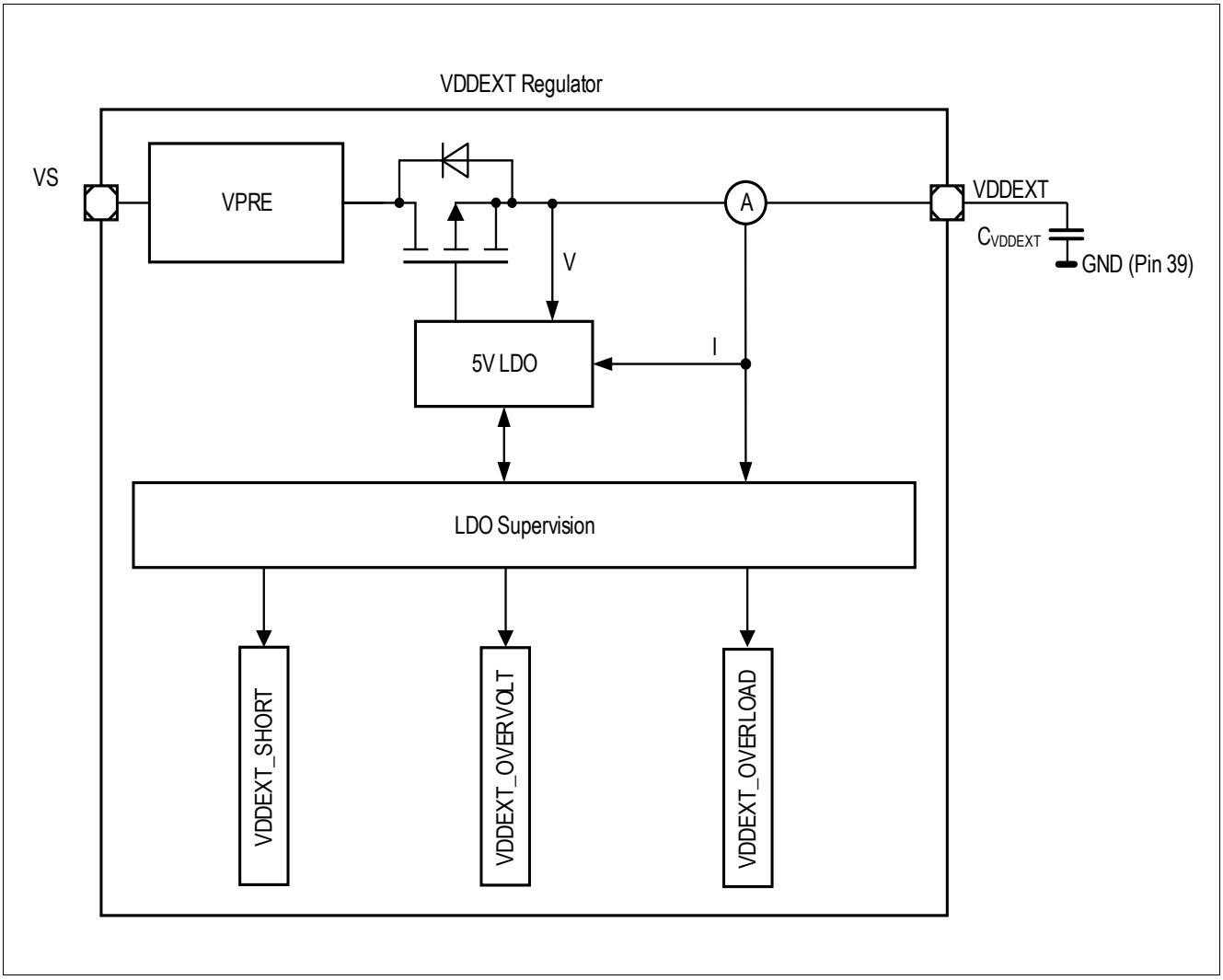


Figure 7 Module Block Diagram of External Voltage Regulator

6 System Control Unit - Digital Modules (SCU-DM)

6.1 Features

- Flexible clock configuration features
- Reset management of all system resets
- System modes control for all power modes (active, power down, sleep)
- Interrupt enabling for many system peripherals
- General purpose input output control
- Debug mode control of system peripherals

6.2 Introduction

The System Control Unit (SCU) supports all central control tasks in the TLE9879QXW40. The SCU is made up of the following sub-modules:

- Clock System and Control
- Reset Control
- Power Management
- Interrupt Management
- General Port Control
- Flexible Peripheral Management
- Module Suspend Control
- Watchdog Timer
- Error Detection and Correction in Data Memory
- Miscellaneous Control