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TLF50281EL

2.2 MHz Step-Down Regulator 500 mA, 5 V, low quiescent current

Data Sheet

Rev. 1.01, 2013-04-30

Automotive Power

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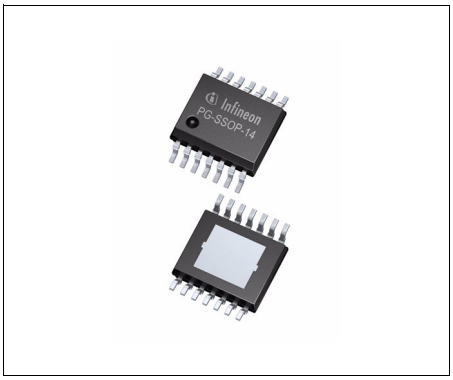
1 Overview

- 500 mA step down voltage regulator
- 5 V Output voltage
- ± 2% output voltage tolerance
- Low quiescent current (less than 45µA at nominal battery voltage)
- Integrated power transistor
- Current mode PWM regulation
- PFM mode for light load current
- Input voltage range from 4.75V to 45V
- 2.2 MHz switching frequency
- 100% Duty cycle
- Synchronization input
- Very low shutdown current consumption (<2 µA)
- Soft-start function
- Reset generator
- Watchdog
- Input undervoltage lockout
- Suited for automotive applications: T_j = -40 °C to +150 °C
- Green Product (RoHS compliant)
- AEC Qualified



PG-SSOP-14

Description

The TLF50281EL is a high frequency PWM step-down DC/DC converter with an integrated PMOS power switch, packaged in a small PG-SSOP-14 with exposed pad. The wide input voltage range from 4.75 to 45 V makes the TLF50281EL suitable for a wide variety of applications. The device is designed to be used under harsh automotive environmental conditions.

The switching frequency of nominal 2.2 MHz allows the use of small and cost-effective inductors and capacitors, resulting in a low, predictable output voltage ripple and in minimized consumption of board space.

In light load condition the device operates in Pulse Frequency Modulation (PFM) to optimize the efficiency. Between the single pulses, all internal controlling circuitry is switched off to reduce the internal power consumption.

Type	Package	Marking
TLF50281EL	PG-SSOP-14	TLF50281

The TLF50281EL includes protection features such as a cycle-by-cycle current limitation, over-temperature shutdown and input under voltage lockout. The enable function, in shutdown mode with less than 2 µA current consumption, enables easy power management in battery-powered systems.

The voltage regulation loop provides an excellent line and load regulation, the stability of the loop is ensured by an internal compensation network. This compensation network combined with a current mode regulation control guarantees a highly effective line transient rejection. During start-up the integrated soft-start limits the inrush current peak and prevents from an output voltage overshoot.

2 Block Diagram

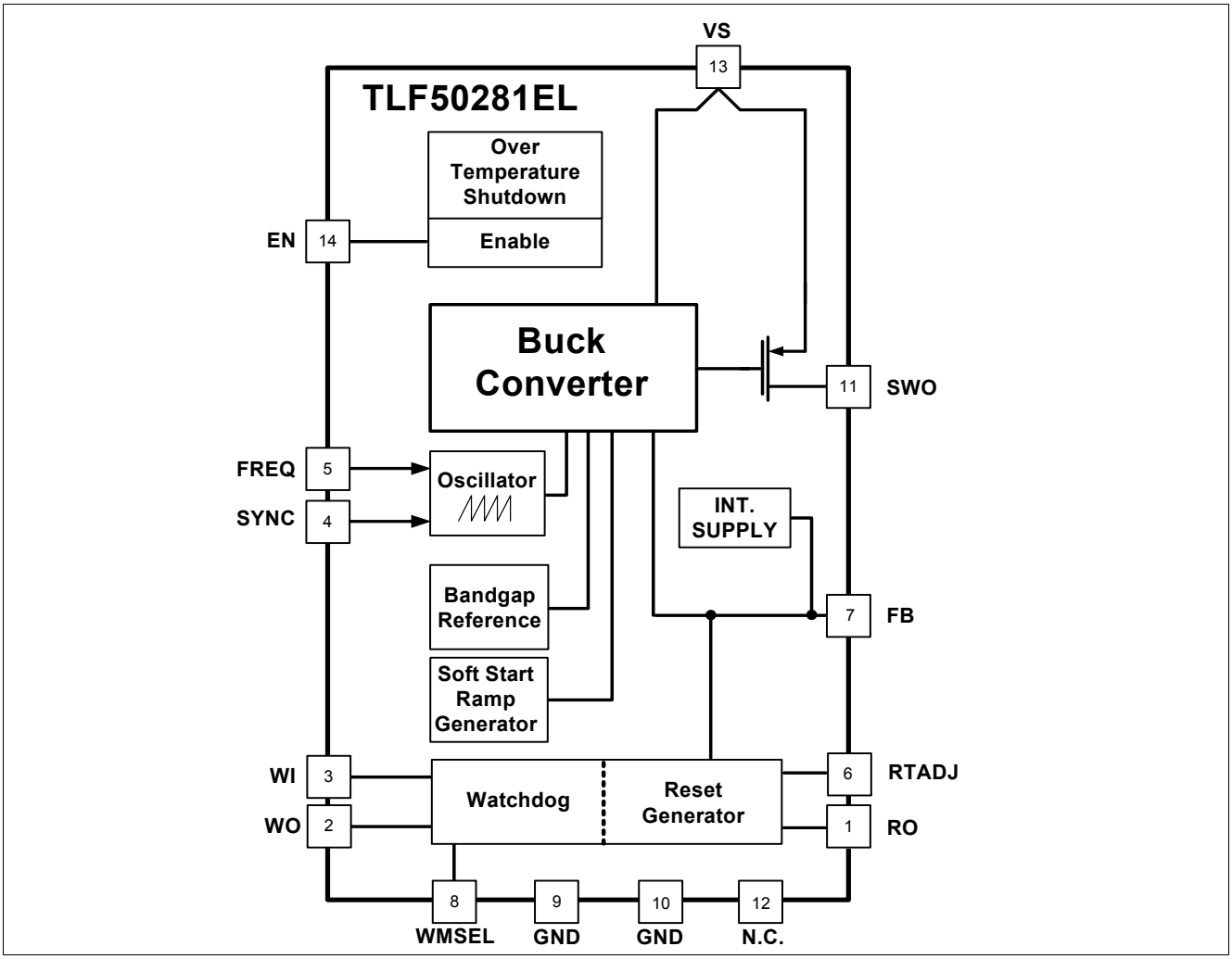


Figure 1 Block Diagram

3 Pin Configuration

3.1 Pin Assignment

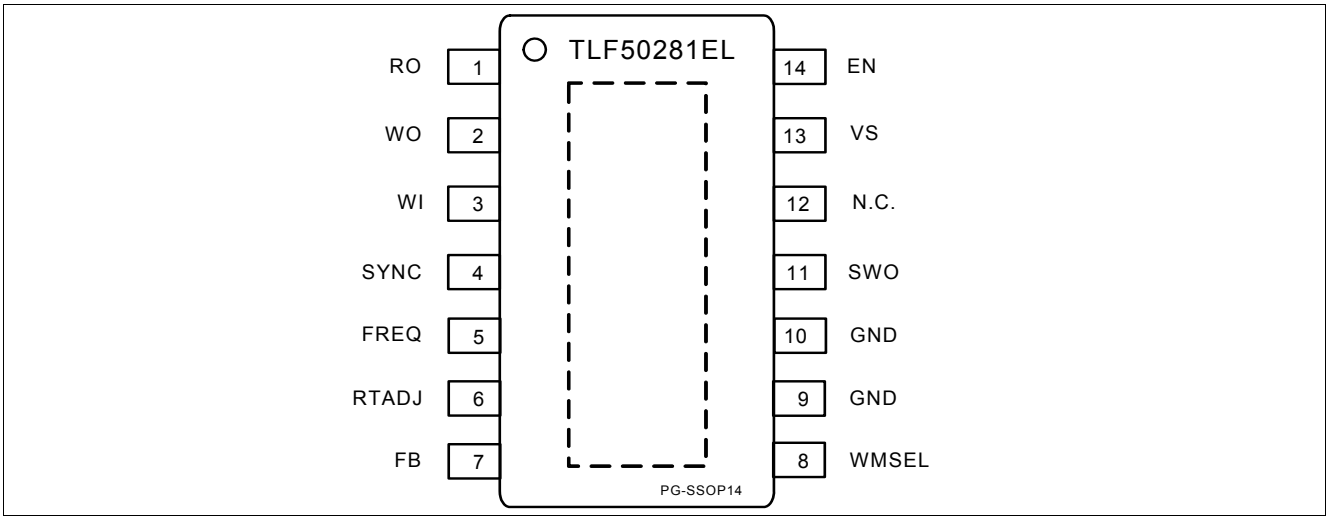


Figure 2 Pin Configuration

3.2 Pin Definitions and Functions

Pin	Symbol	Function
1	RO	**Reset Output** Provides the reset output signal. Open collector output, connect a pull up resistor to V_{CC} or another voltage source, if feature is used, if not, leave open. Might be connected in parallel with pin WO, if necessary.
2	WO	**Watchdog Output** Provides the watchdog output signal. Open collector output, connect a pull up resistor to V_{CC} or another voltage source, if feature is used, if not, leave open. Might be connected in parallel with pin RO, if necessary.
3	WI	**Watchdog Input** Connect Watchdog Input signal, if feature is used. If not used, connect to GND
4	SYNC	**Synchronization Input** Connect to an external clock signal in order to synchronize/adjust the switching frequency. This feature is not functionally in PFM mode.
5	FREQ	**Frequency Adjustment Pin** Connect an external resistor to GND to adjust the switching frequency, do not leave open. In case the synchronization option is used, the resistor must be dimensioned close to the desired synchronization frequency.
6	RTADJ	**Reset Threshold Adjust Pin** Connect an external resistor divider to adjust the Reset threshold. If function is not used, connect to V_{CC}.
7	FB	**Feedback Input** Connect this pin directly to the output capacitor. Also input for internal power supply. The internal power supply is taken from the output voltage.

Pin	Symbol	Function
8	WMSEL	**Watchdog Mode Select Pin** Connect to V_{CC} for Watchdog slow mode or to GND for Watchdog fast mode. If not used, connect to GND to avoid EMC related influence to Watchdog function.
9	GND	**Ground** Connect this pin directly with low inductive and broad trace to ground, do not leave open.
10	GND	**Ground** Connect this pin directly with low inductive and broad trace to ground, do not leave open.
11	SWO	**Buck Switch Output** Drain of the integrated power-PMOS transistor. Connect directly to the cathode of the catch diode and the buck circuit inductance.
12	N.C.	**Not Connected.** Internally not connected. Leave open or connect to GND.
13	VS	**Supply Voltage Input** Connect to supply voltage source.
14	EN	**Enable Input** Switch to high level to enable the device, switch to low level to disable the device.
Exposed Pad		Connect to heatsink area and GND by low inductance wiring.

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Absolute Maximum Ratings[1)]

T_j = -40 °C to +150 °C; all voltages with respect to ground (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
Voltages						
4.1.1	Enable input	V_{EN}	-40	45	V	–
4.1.2	Synchronization input	V_{SYNC}	-0.3	5.5	V	–
4.1.3				6.2	V	t < 10s [2)]
4.1.4	Frequency adjustment pin	V_{FREQ}	-0.3	5.5	V	–
4.1.5				6.2	V	t < 10s [2)]
4.1.6	Watchdog input	V_{WI}	-0.3	5.5	V	–
4.1.7				6.2	V	t < 10 [2)]
4.1.8	Watchdog output	V_{WO}	-0.3	5.5	V	–
4.1.9				6.2	V	t < 10s [2)]
4.1.10	Watchdog mode selection pin	V_{WMSEL}	-0.3	5.5	V	–
4.1.11				6.2	V	t < 10s [2)]
4.1.12	Reset threshold adjust pin	V_{RTADJ}	-0.3	5.5	V	–
4.1.13				6.2	V	t < 10s [2)]
4.1.14	Reset output	V_{RO}	-0.3	5.5	V	–
4.1.15				6.2	V	t < 10s [2)]
4.1.16	Feedback Input	V_{FB}	-0.3	5.5	V	–
4.1.17				6.2	V	t < 10s [2)]
4.1.18	Buck switch output	V_{SWO}	-2.0	V_{VS} + 0.3	V	–
4.1.19	Supply voltage input	V_{VS}	-0.3	45	V	–
Temperatures						
4.1.20	Junction temperature	T_j	-40	150	°C	–
4.1.21	Storage temperature	T_{stg}	-55	150	°C	–
ESD Susceptibility						
4.1.22	ESD resistivity	V_{ESD}	-2	2	kV	HBM
4.1.23	ESD resistivity to GND	V_{ESD}	-500	500	V	CDM [3)]
4.1.24	ESD resistivity corner pins to GND	V_{ESD}	-750	750	V	CDM [3)]

1) Not subject to production test, specified by design

2) ESD susceptibility HBM according to ANSI/ESDA/JEDEC JS-001.

3) ESD susceptibility, Charged Device Model “CDM” EIA/JESD22-C101 or ESDA STM5.3.1

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

4.2 Functional Range

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
4.2.1	Supply voltage	V_S	4.75	45	V	–
4.2.2	Buck inductor	L_{BU}	3.3	22	µH	–
4.2.3	Buck capacitor	C_{BU1}	10	50	µF	–
4.2.4	Buck capacitor ESR	ESR_{BU1}	0.015	0.100	Ω	– 1)
4.2.5	Junction temperature	T_j	-40	150	°C	–

1) See section "**"Application Information" on Page 31**" for loop compensation requirements and refer to Application Note for dimensioning the output filter.

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

4.3 Thermal Resistance

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
4.3.1	Junction to case[1)]	R_{thJC}	–	10	–	K/W	–
4.3.2	Junction to ambient[1) 2)]	R_{thJA}	–	47	–	K/W	2s2p
4.3.3		R_{thJA}	–	54	–	K/W	1s0p + 600 mm^2
4.3.4		R_{thJA}	–	64	–	K/W	1s0p + 300 mm^2

1) Not subject to production test, specified by design.

2) Specified R_{thJA} value is according to JEDEC 2s2p (JESD 51-7) + (JESD 51-5) and JEDEC 1s0p (JESD 51-3) + heatsink area at natural convection on FR4 board.

5 Buck Regulator

5.1 Description

The TLF50281EL is a monolithic current mode step down converter with adjustable switching frequency f_{OSC}. It is capable to operate either in Pulse Width Modulation (PWM) or in Pulse Frequency Modulation (PFM) Mode.

5.1.1 Regulator Loop

Power stage:

The supply voltage is connected to pin VS. Between pin VS and pin SWO there is an internal shunt resistor and the internal PMOS power stage. The PMOS is driven by the driver stage.

Regulator Block:

The feedback signal V_{FB} is connected to pin FB. Between pin FB and pin GND is an internal resistor divider. An error amplifier and a comparator are connected to this resistor divider: The error amplifier EA-gmV, which is controlling the output voltage in PWM mode, and the PFM comparator, which will switch the TLF50281EL into PFM mode and trigger the pulses. The error amplifier EA-gmV is connected to the PWM comparator. The regulation loop operates in current mode: The output current of EA-gmV is subtracted from the sum of the current loop CS-gmI and the slope compensation I_{SLOPE}. The result is evaluated by PWM Comp (a current comparator). The output of PWM Comp defines duty cycle (pulse-width-modulated signal) in PWM mode.

The Slope Compensation added to the signal from the error amplifier EA-gmV to the PWM Comparator ensures that no sub harmonics will occur on the input current.

The PWM comparator output and the PFM comparator output are connected to the PWM /PFM logic.

An external resistor at pin FREQ is required to set the switching frequency (for details please refer to chapter 8 Module Oscillator). The TLF50281EL may also be synchronized to an external frequency. In this case an external clock signal should be connected to pin SYNC. The frequency setting resistor at pin FREQ is still necessary, it has to be selected according to the desired synchronization frequency (for details please refer to **Chapter 8, Oscillator**.

The TLF50281EL can only be synchronized to an external frequency source in PWM mode, this function does not work in PFM mode.

The clock manager is clocking the PWM/PFM logic. The PWM/PFM logic is triggering the driver to apply pulses to the internal PMOS power stage.

Safety Features:

The shunt resistor in line with the internal PMOS power stage (between pin VS and the power stage) is connected to a current sense amplifier CS-gmI. It detects the voltage above the shunt resistor. The amplifier creates a signal which shuts the pulse down in case that the shunt voltage exceeds the reference limit. The current limitation acts as a cycle-by-cycle limitation. Cycle-by-cycle limitation means, that every pulse is switched off as soon as the current through the PMOS exceeds the buck peak over current limit I_{BUOC}. The next pulse starts and will also be switched off as soon as the current limit is exceeded again. This results in a lowered output voltage whilst the output current is limited to a certain value.

Input undervoltage shutdown: If the input voltage is below the input undervoltage shutdown threshold $V_{S,off}$ the device will shut down.

Output overvoltage protection: If the output voltage exceeds the PFM threshold the device will switch from PWM to PFM. Pulses will then be generated only depending on the value of the output voltage V_{CC}.

Soft start function: An integrated soft start function of duration t_{start} ensures, that the inrush current will be limited. After an over-temperature shutdown the regulator always restarts with a soft start.

Over-temperature shutdown: An internal temperature sensor detects the temperature of the device. It will be switched off if the junction temperature exceeds the over temperature shutdown threshold $T_{j,sd}$ and restart with a certain hysteresis T_{j,sd_hyst} (for details please refer to **Chapter 7, Enable and Thermal Shutdown**).

Biasing:

The internal biasing is taken from pin VS as well as from pin FB (connected to V_{CC}) (for details please refer to **Chapter 7, Enable and Thermal Shutdown**). Thus the power consumption from the supply voltage V_S can be minimized.

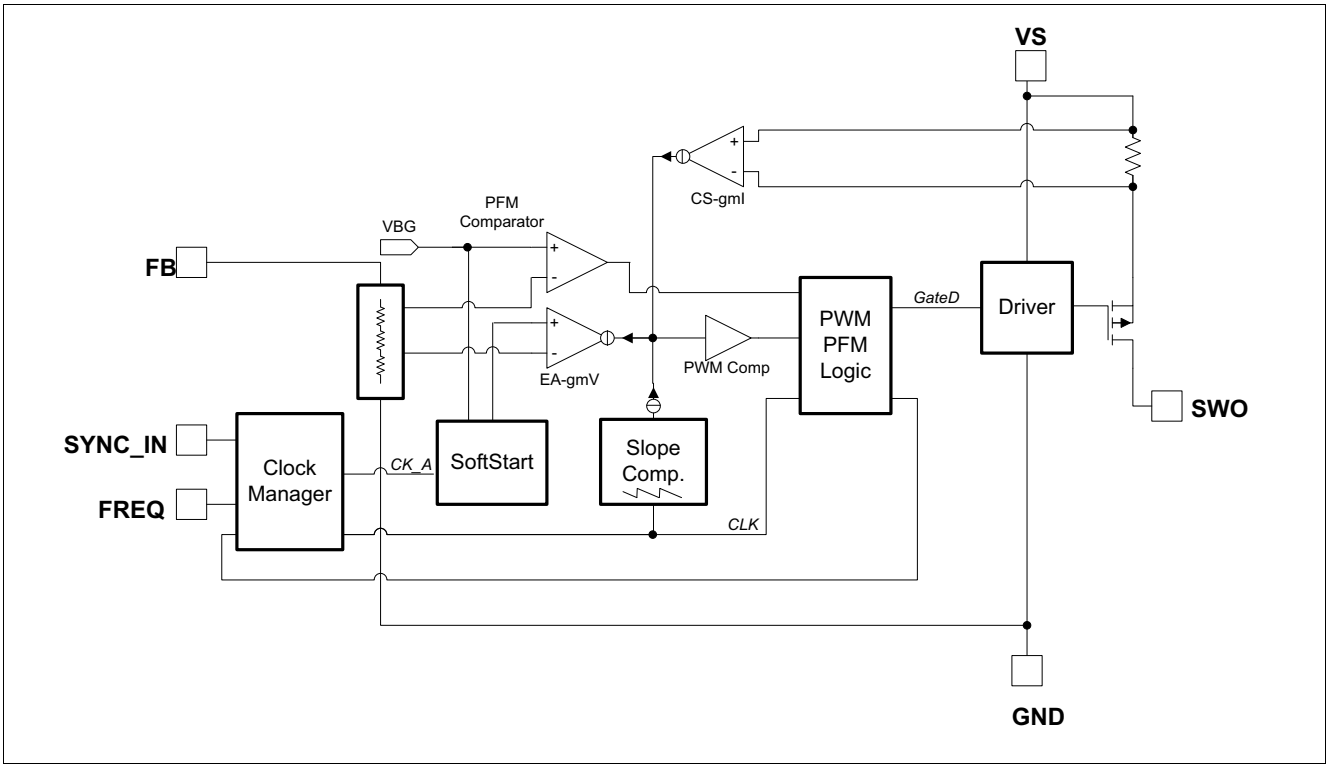


Figure 3 Block Diagram Buck Regulator

5.1.2 PWM (Pulse Width Modulation) Mode

Under normal conditions the TLF50281EL will operate with a constant switching frequency f_{OSC} in PWM mode. The ratio between switch-on-time T_{ON} and switch-off-time T_{OFF} is mainly determined by the ratio between the input voltage V_S and the output voltage V_{CC} and is influenced by the output current I_{CC}.

In PWM mode the device may operate with 100% duty cycle, in this case the internal PMOS is constantly conducting current. The current limitation feature is operating under this condition.

If the switch-on-time T_{ON} should theoretically be below the minimum threshold $T_{ON,min}$ (due to low load or due to the ratio between input voltage V_S and output voltage V_{CC} depending on the switching frequency), it will be reduced to the minimum value switch-on-time $T_{ON,min}$ and stay there. As a consequence the output voltage V_{CC} will increase. The PFM comparator detects the PFM threshold and will then switch the device into PFM mode. There is no possibility to disable the PFM function.

5.1.3 PFM (Pulse Frequency Modulation) Mode

To optimize the efficiency and to reduce the current consumption, the TLF50281EL automatically switches to PFM mode under low load conditions. In PFM mode the internal power stage including the driver stage is switched off and will only be switched on for applying pulses to charge the output capacitor. The pulses will be created by monitoring the voltage of the output filter capacitor C_{OUT}. Thus in PFM mode the repetition time of pulses depend on the output current and/or the ratio between input voltage V_S and output voltage V_{CC}.

Transition from PWM to PFM:

Figure 4 is showing the transition from Pulse Width Modulation to Pulse Frequency Modulation under the assumption, that the input voltage V_S will be constant and only the output current I_{CC} will vary. The diagram shows the principle, in reality the signals might look slightly different. The diagram is without scale in respect of time, voltage and current values.

Starting from left of the figure a certain output current, here named $\boldsymbol{i_1}$, is applied to the regulator output. This results in a duty cycle D_1 with the on-time T_{ON1} of the internal power stage. The switching frequency f_{OSC} is constant as set by the frequency setting resistor R_{FREQ}. The regulator is in PWM mode, the output voltage is V_{REF_PWM} which is equal to V_{FB} in PWM mode.

At point t_1 the output current decreases from $\boldsymbol{i_1}$ to a lower $\boldsymbol{i_2}$. This results in a duty cycle D_2 with the on-time T_{ON2} of the internal power stage. Due to the reduced output load the on-time T_{ON2} is shorter (the regulator is in Discontinuous Conduction Mode DCM) than T_{ON1}. The switching frequency f_{OSC} is constant as set by the frequency setting resistor R_{FREQ}. The regulator is still in PWM mode, the output voltage is V_{REF_PWM} which is equal to V_{FB} in PWM mode. In Continuous Conduction Mode CCM the variation from T_{ON1} to T_{ON2} will be very small due to smaller conduction losses.

At point t_2 the output current decreases again from $\boldsymbol{i_2}$ to a lower $\boldsymbol{i_3}$. As a consequence the on-time T_{ON} will be reduced also. The output current $\boldsymbol{i_3}$ is so low, that the on-time T_{ON3} would be smaller than the $T_{ON,min}$. The regulator does not allow a on-time smaller than $T_{ON,min}$. Therefore we can say that the output current $\boldsymbol{i_3}$ is under the imaginary current threshold for transition from PWM to PFM $\boldsymbol{i_{PWM/PFM}}$. With the pulse staying at on-time $T_{ON,min}$ the output voltage V_{CC} will rise. The regulator is still in PWM mode, but the output voltage rises.

At point t_3 after a normal time period T_{PWM} as adjusted by the frequency setting resistor R_{FREQ}, a further pulse of the duration $T_{ON,min}$ is applied, the output voltage V_{CC} keeps on rising. The regulator is still in PWM mode.

At point t_4 the output voltage V_{CC} touches (or exceeds) the voltage threshold for transition from PWM to PFM $V_{PWM/PFM}$. The regulator is now switching internally from PWM to PFM. In PFM mode the power consumption of the internal blocks is reduced. The reference for the output voltage V_{CC} is switched from V_{REF_PWM} (which is equal to V_{FB} in PWM mode) to V_{REF_PFM} (which is equal to V_{FB} in PFM mode). The reference for V_{FB} in PFM mode is higher than the reference in PWM mode to avoid voltage dumps at the output voltage V_{CC} due to sudden load steps and to give the regulator more reaction time to switch back to PWM mode.

The regulator is now in PFM mode, the output voltage is V_{REF_PFM} which is equal to V_{FB} (or slightly higher) in PFM mode.

The output voltage V_{CC} is monitored and as soon as it touches the PFM reference voltage V_{REF_PFM} a pulse of the on-time $T_{ON,min}$ is triggered. The time between two pulses is depending on the discharging of the output capacitor C_{OUT}.

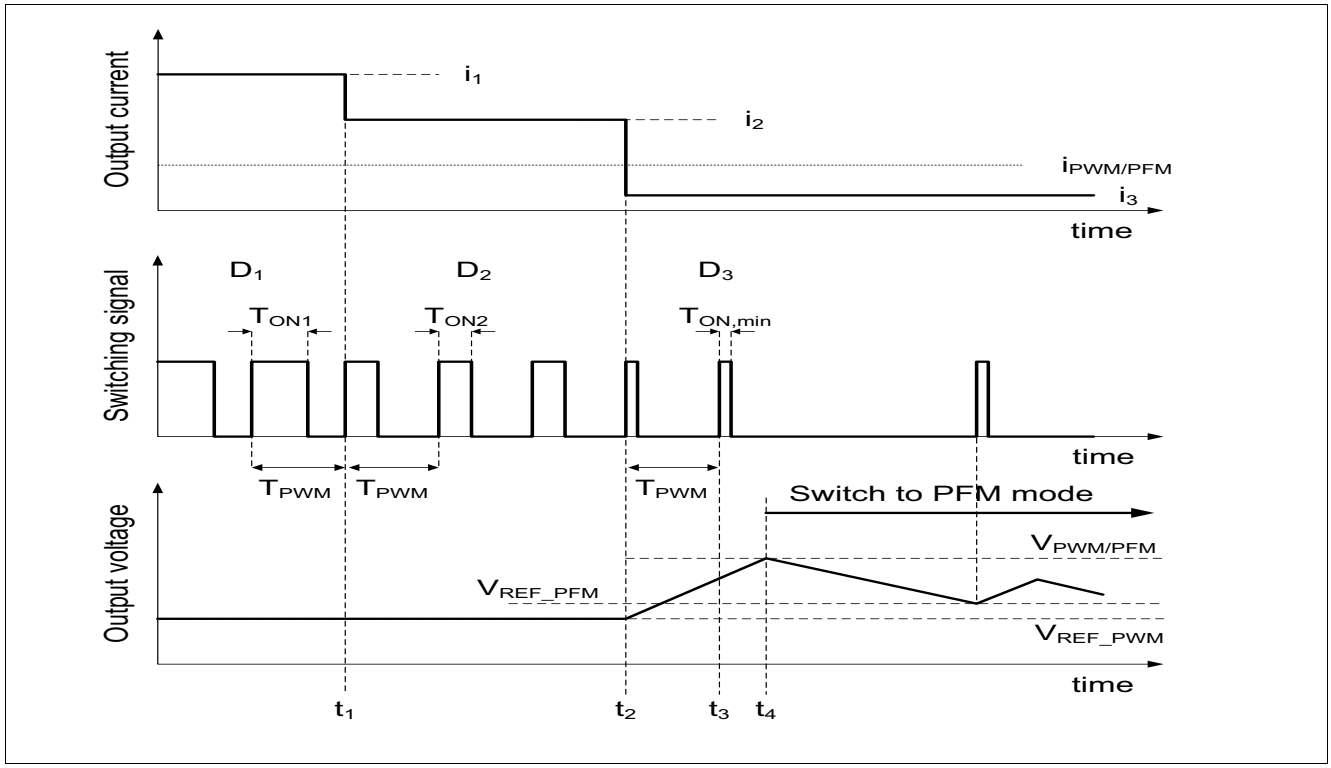


Figure 4 PWM to PFM Transition (Timing Diagram)

Transition from PFM to PWM:

Figure 5 is showing the transition from Pulse Frequency Modulation to Pulse Width Modulation under the assumption, that the input voltage V_S will be constant, and only the output current $\boldsymbol{I_{CC}}$ will vary. The diagram shows the principle, in reality the signals might look slightly different. The diagram is without scale in respect of time, voltage and current values.

Starting from left of the figure a certain output current, here named $\boldsymbol{i_3}$, is applied to the regulator output. $\boldsymbol{i_3}$ shall be below the imaginary current threshold for transition from PFM to PWM $\boldsymbol{i_{PFM/PWM}}$. The regulator is in PFM mode, the output voltage is V_{REF_PFM}, which is equal to V_{FB} in PFM mode (or slightly higher).

Pulses of the duration $T_{ON,min}$ are triggered whenever the output voltage V_{CC} touches the PFM reference voltage V_{REF_PFM}.

At point t_5 the output current increases from $\boldsymbol{i_3}$ to a higher $\boldsymbol{i_2}$, that shall be above the imaginary current threshold for transition from PFM to PWM $\boldsymbol{i_{PFM/PWM}}$. Due to the higher output current more pulses of the duration $T_{ON,min}$ have to be triggered, the frequency of these pulses is monitored. The frequency of these pulses increases until it is higher than the switching frequency f_{OSC} set by the frequency setting resistor R_{FREQ}. The regulator is still in PFM mode

At point t_6 the frequency monitoring detects that the frequency of the PFM pulses is being higher than the frequency threshold for transition from PFM to PWM $f_{PFM/PWM}$. Therefore the regulator switches back to PWM mode. This results in a certain duty cycle D_2 with the on-time T_{ON2} of the internal power stage. The time period T_{PWM} is as adjusted by the frequency setting resistor R_{FREQ}.

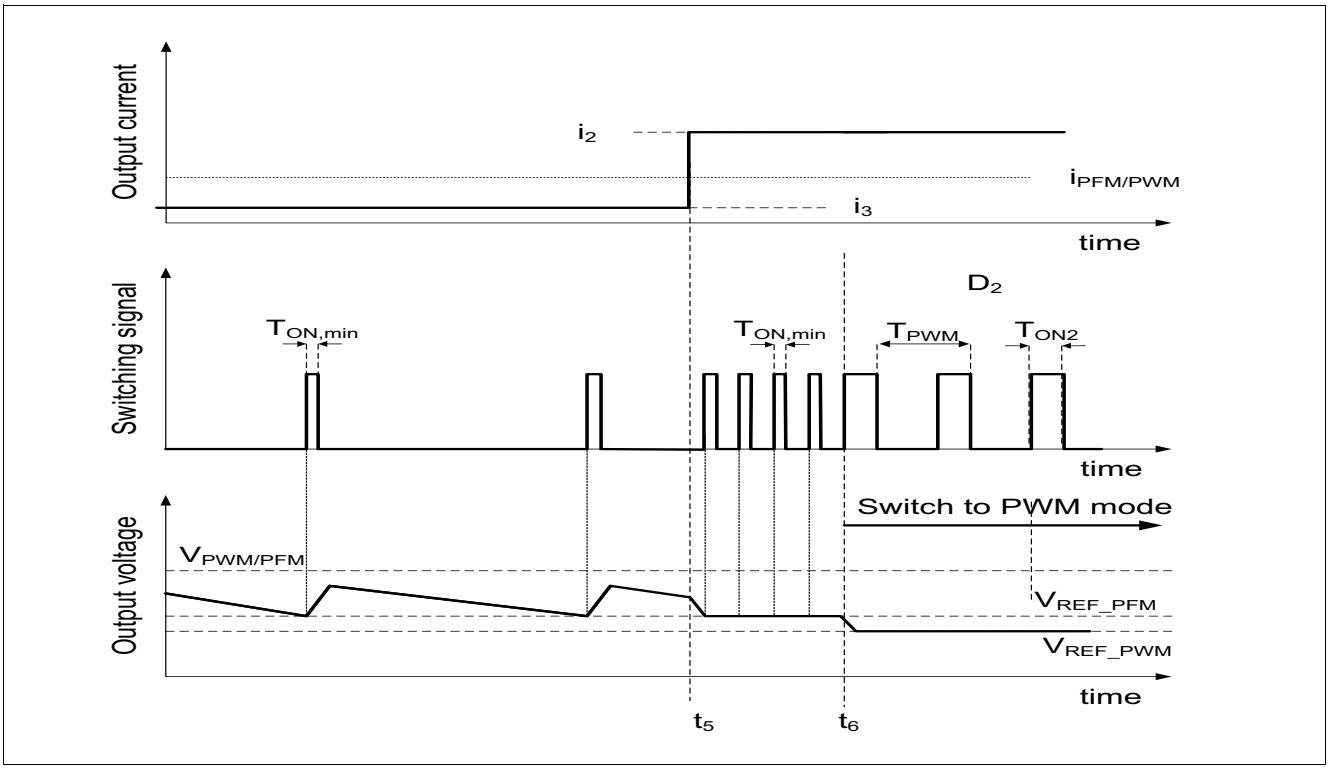


Figure 5 PFM to PWM Transition (Timing Diagram)

Frequency Variation during PWM/PFM Transition:

Figure 6 is showing the transition from Pulse Frequency Modulation to Pulse Width Modulation (and vice versa) in relation to output current and switching frequency. The diagram shows the principle, in reality the signals might be slightly different. The diagram is without scale in respect of frequency and current values.

The transition from PWM to PFM is shown in a grey line. Starting from right the switching frequency f_{PWM} is constant as set by the frequency setting resistor R_{FREQ}. The output current I_{CC} is decreasing.

As soon as the output current I_{CC} is below the imaginary current threshold for transition from PWM to PFM $i_{PWM/PFM}$, the regulator will be switched from PWM to PFM mode depending on the output voltage V_{CC}. With the output current I_{CC} decreasing, the switching frequency will also decrease, as the pulses are triggered by monitoring the output voltage V_{CC} at capacitor C_{OUT}.

The transition from PFM to PWM is shown in a black line. Starting from left the switching frequency is increasing with the increasing output current I_{CC}.

As soon as the switching frequency is crossing the frequency threshold for transition from PFM to PWM $f_{PFM/PWM}$ (which is above the switching frequency f_{OSC} set by the frequency setting resistor R_{FREQ}) the regulator will switch from PFM to PWM.

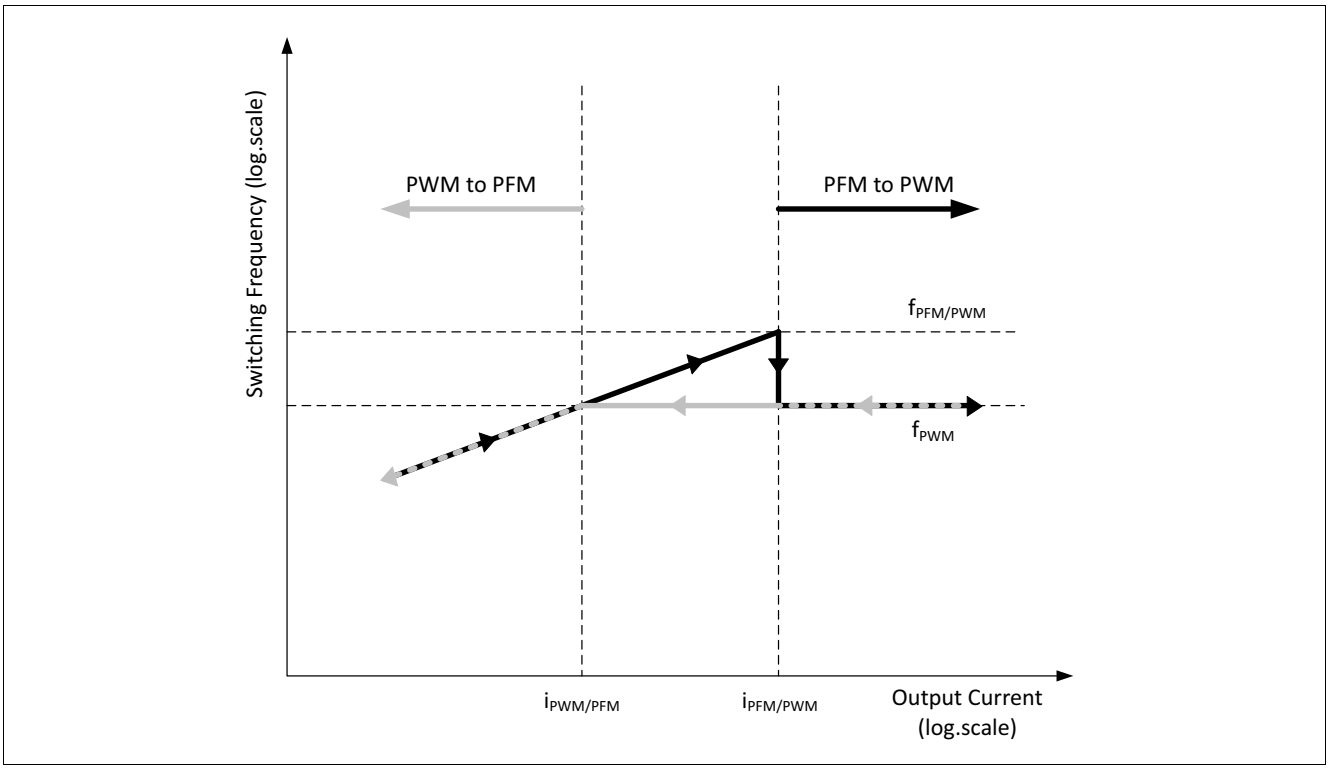


Figure 6 PWM <-> PFM Transitions

5.2 Electrical Characteristics

Electrical Characteristics: Buck Regulator

V_S = 6.0 V to 40 V, T_j = -40 °C to +150 °C, all voltages with respect to ground (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.2.1	Output voltage	V_{FB}	4.90	5.00	5.10	V	V_{EN} = 5.0V 7 V < V_S < 12V 100 mA < I_{CC} < 610 mA PWM Mode
5.2.2	Output voltage	V_{FB}	4.90	5.10	5.30	V	V_{EN} = 5.0V 10V < V_S < 35V I_{CC} = 100 µA PFM Mode
5.2.3	Power stage on-resistance	R_{on}	–	1.5	2.3	Ω	tested at 100 mA, V_S = 7.0V
5.2.4	Buck peak over current limit	I_{BUOC}	0.85	–	1.7	A	–
5.2.5	Current transition rise/fall time	t_R	–	100	–	mA/ns	1)
5.2.6	Maximum duty cycle	D_{max}	–	–	100	%	2)
5.2.7	Minimum switch on-time	$T_{ON,min}$	–	100	–	ns	1)
5.2.8	Minimum switch off- Time	$T_{OFF,min}$	–	200	–	ns	1) PFM mode
5.2.9	Soft start ramp	t_{start}	300	450	750	µs	V_{FB} rising from 5% to 95% of $V_{FB,nom}$
5.2.10	Input under voltage shutdown threshold	$V_{S,off}$	3.75	–	–	V	V_S decreasing
5.2.11	Input voltage startup threshold	$V_{S,on}$	–	–	4.75	V	V_S increasing
5.2.12	Input under voltage shutdown hysteresis	$V_{S,hyst}$	130	300	–	mV	–
5.2.13	Voltage threshold for transition from PWM to PFM	$V_{PWM/PFM}$	–	–	5.3	V	1)
5.2.14	Frequency ratio for transition from PFM to PWM	$f_{PFM/PWM}/f_{osc}$	–	1.20	–	–	1)

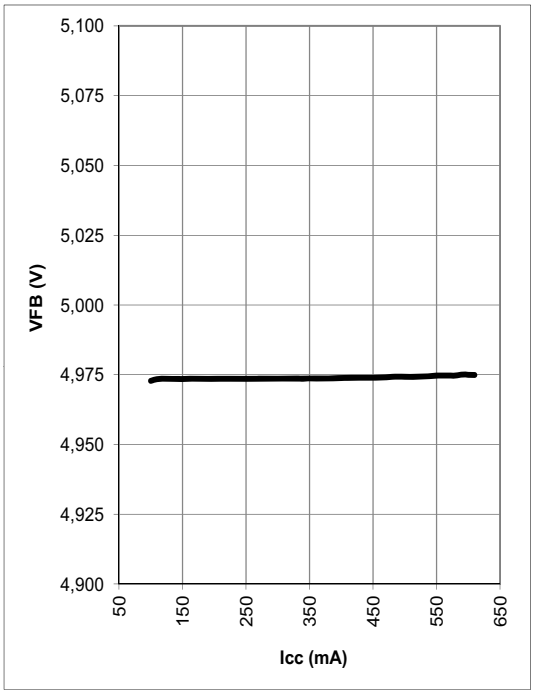
1) Specified by design. Not subject to production test.

2) Consider “**Chapter 4.2, Functional Range**”.

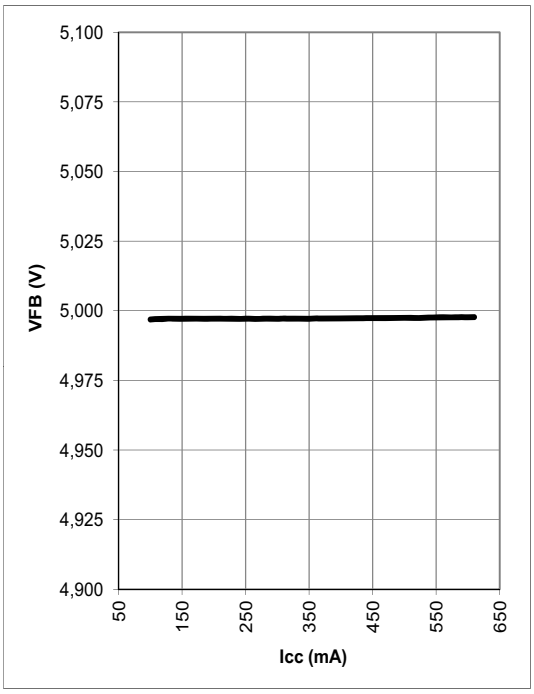
5.3 Performance Graphs

Typical Performance Characteristics

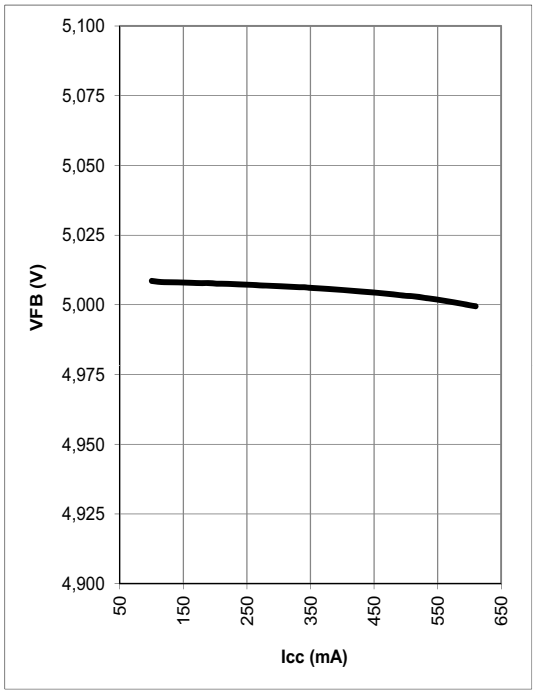
Load Regulation PWM Mode
V_S = 12 V; T_J = - 43 °C



Load Regulation PWM Mode
V_S = 12 V; T_J = + 25°C

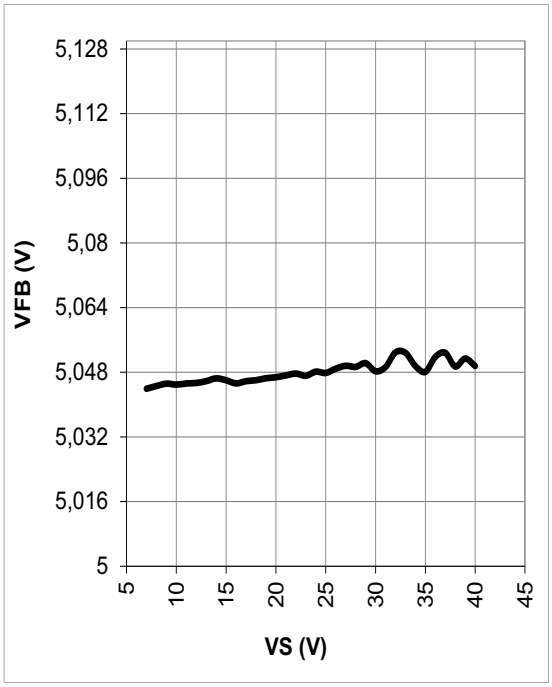


Load Regulation PWM Mode
V_S = 12 V; T_J = + 150°C

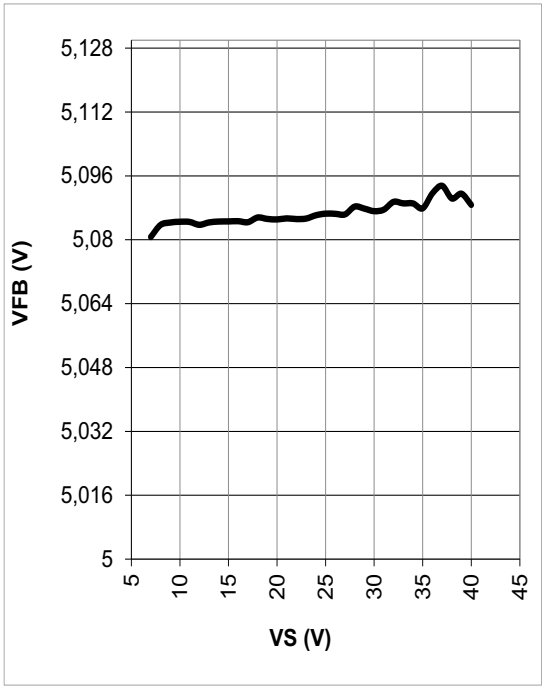


Typical Performance Characteristics

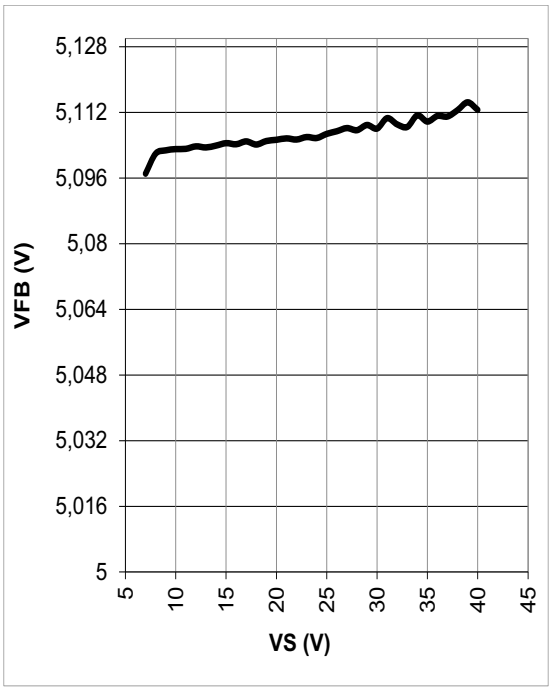
Line Regulation PFM Mode
I_{CC} = 100 µA; T_J = - 43°C



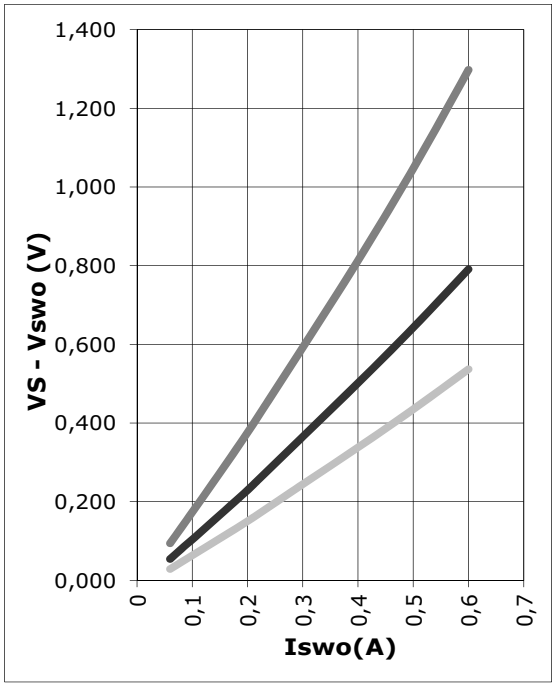
Line Regulation PFM Mode
I_{CC} = 100 µA; T_J = + 25°C



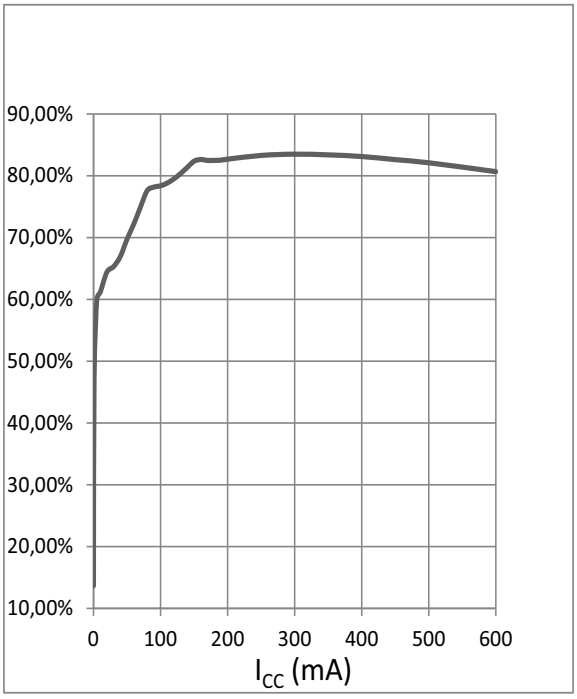
Line Regulation PFM Mode
I_{CC} = 100 µA; T_J = + 150°C



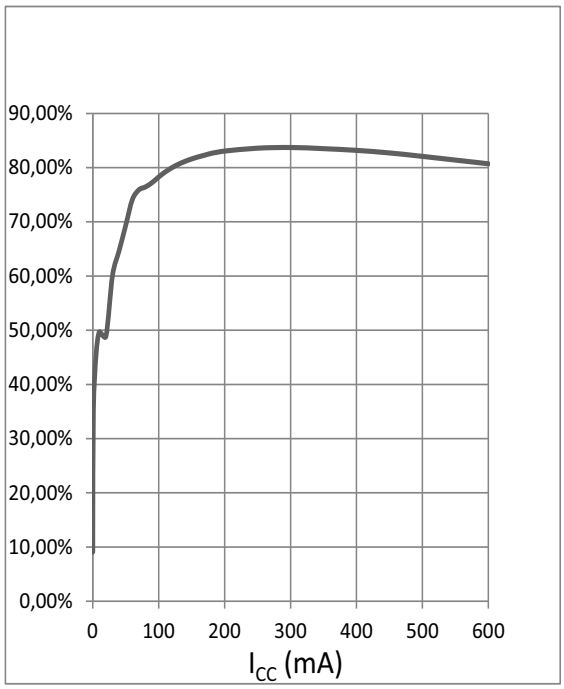
Power Stage On Resistance: Black T_J = + 25°C
Light Grey T_J = - 43 °C, Dark Grey T_J = + 150 °C



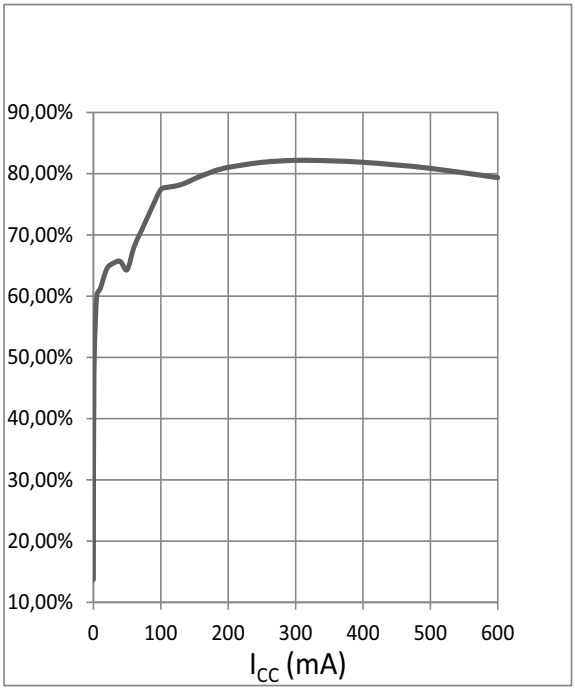
Efficiency for
V_S = 13 V, f_{OSC} = 1.65 MHz, L_{OUT} = 4.7 µH



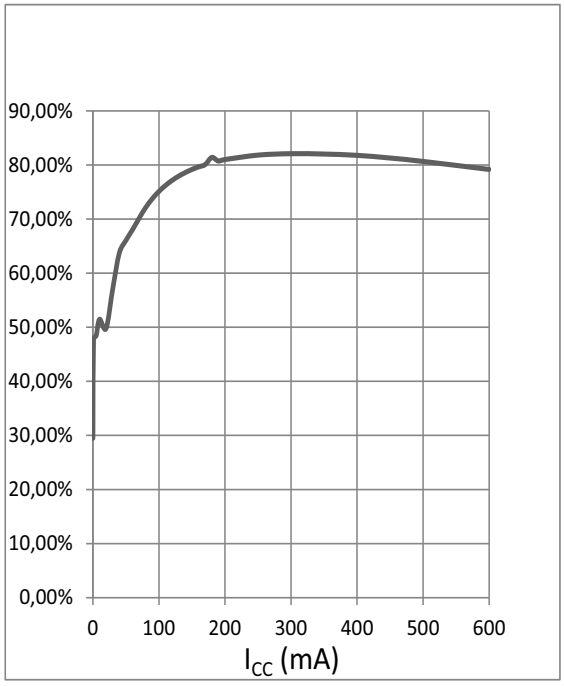
Efficiency for
V_S = 13 V, f_{OSC} = 1.65 MHz, L_{OUT} = 10 µH



Efficiency for
V_S = 13 V, f_{OSC} = 2.2 MHz, L_{OUT} = 4.7 µH



Efficiency for
V_S = 13 V, f_{OSC} = 2.2 MHz, L_{OUT} = 10 µH



6 Reset and Watchdog

6.1 Description Reset Function

Principle:

The reset function supervises the value of the regulator output voltage V_{CC}. The result is monitored by the status of pin RO. A high level at pin RO means that the output voltage V_{CC} is above the desired reset threshold. A low level at pin RO means that the output voltage V_{CC} is below the desired reset threshold. The reset function does not work, if the supply (V_{FB}) voltage is below 1 V.

Adjustment of reset threshold:

The reset generator consists of an internal comparator with a reset threshold $V_{RO,T}$. By adding an external resistor divider between the output voltage V_{CC} and ground (GND) and connecting the point between the upper (R1) and lower (R2) resistor to pin RTADJ the desired reset threshold V_{RT} (where the reset generator indicates an under voltage) might be adjusted.

If reset function is not used please connect pin RTADJ to V_{CC}.

$$\text{Desired reset threshold} = V_{RO,T}\left(\frac{R1 + R2}{R2}\right) = V_{RT}$$

Operation mode (please refer to Figure 7):

The reset generator starts operating as soon as the regulator is activated by supplying the device with an input (battery) voltage higher than the input voltage startup threshold $V_{S,ON}$ and a valid high signal $V_{EN,hi}$ at pin EN.

The pin RO is low at this time.

When the regulator starts to operate, V_{CC} ramps up and passes the desired reset threshold. The reset delay time t_{RD} is the time duration between that point and pin RO turning to high level.

The reset reaction time t_{RR} is the maximum duration or time, the output voltage V_{CC} may dip below the desired reset threshold, before a reset is indicated and pin RO is pulled to low level. This is implemented to avoid wrong reset triggering by short “glitches” on the output voltage V_{CC}. If the output voltage V_{CC} dips below the desired reset threshold V_{RT} for more than t_{RR} , t_{RR} is also the time until pin RO is pulled below $V_{RO,L}$.

A voltage dip at the output voltage V_{CC} leads to a low level at pin RO under the following condition:

$$V_{CC} < V_{RO,T}\left(\frac{R1 + R2}{R2}\right) (\text{for } t > t_{RR})$$

In case the pin RO is pulled to low level, it stays low for the time until the output voltage V_{CC} is higher than the desired reset threshold V_{RT} plus the reset delay time t_{RD}.

Reset output pin (please refer to Figure 7):

The reset output is an open collector structure. As soon as a reset condition occurs, the pin is pulled to ground. A pull up resistor (R4) connected to V_{CC} or another voltage source is necessary. If the supply (V_{FB}) voltage is below 1 V the open collector structure does no longer pull pin RO to ground. In this case pin RO goes up to the pull-up voltage (if not supplied by voltage V_{CC}).

The reset output pin RO might be connected in parallel to the watchdog output pin WO, if application requires this.

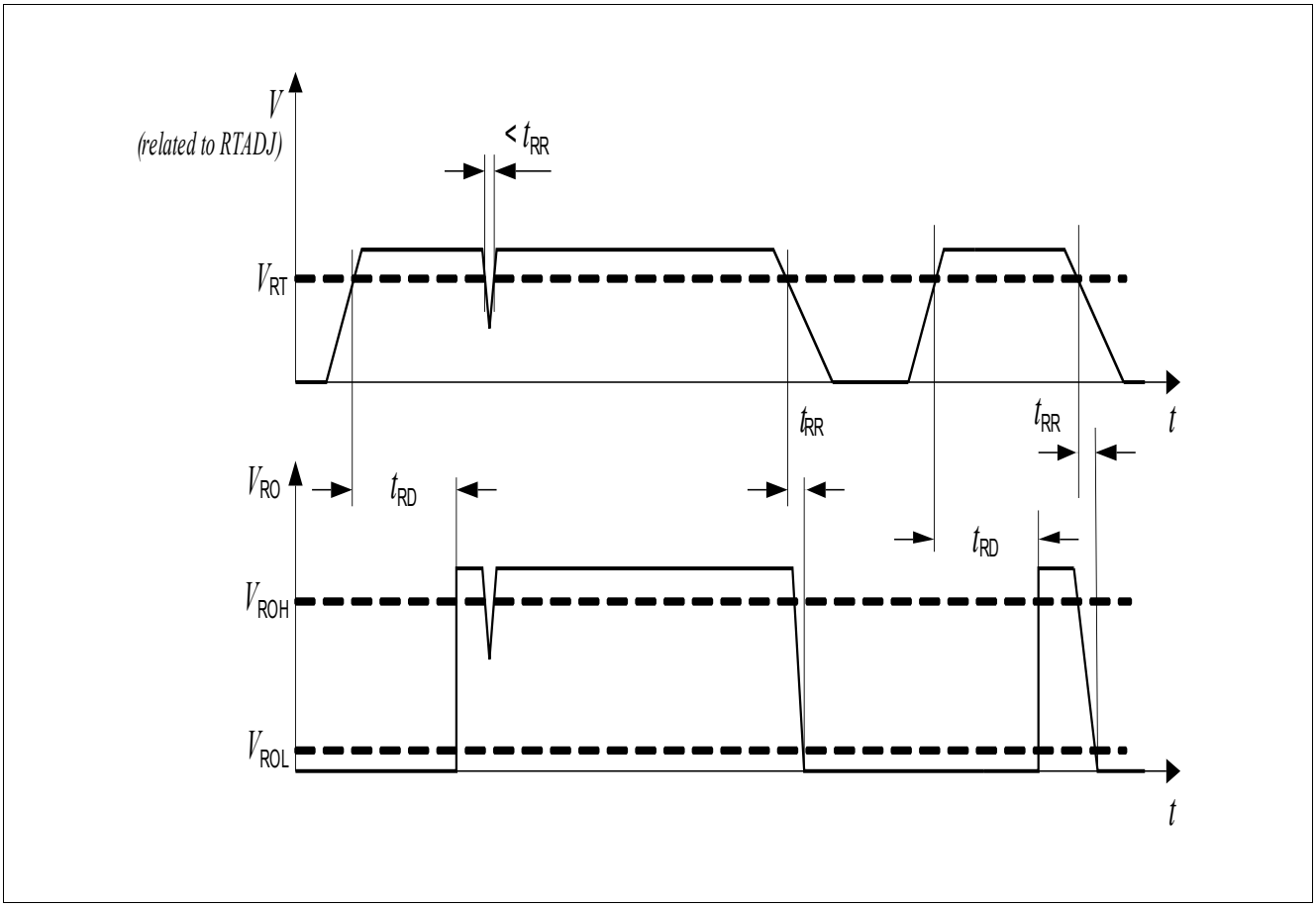


Figure 7 Reset Function and Timing Diagram

- ROH:= Reset Output High Level, depending on voltage sourcing the pull-up resistor at pin RO
- ROL:= Reset Output Low Level, Reset signal valid.

The recommended maximum value

for the sum of both resistors R1 and R2 of the external resistor divider is 1.2 MΩ

6.2 Electrical Characteristics Reset Function

Electrical Characteristics: Reset

V_S = 6.0 V to 40 V, T_j = -40 °C to +150 °C, all voltages with respect to ground (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Reset Output RO							
6.2.1	Output voltage low	$V_{RO,L}$	–	0.2	0.4	V	$V_{CC} \geq$ 1V; V_{RTADJ} < 0.9V, I_{RO} = 1 mA
6.2.2	Sink current limit	$I_{R,S,MAX}$	1	–	–	mA	V_{CC} = 5V; V_{RTADJ} < 0.9V, V_{RO} = 0.4V
6.2.3	Leakage current	$I_{RO,L,MAX}$	–	–	1	µA	V_{RO} = 5V
6.2.4	Output undervoltage threshold decreasing	$V_{RO,T}$	0.96	1.00	1.04	V	–
6.2.5	Output undervoltage hysteresis	$V_{RO,T,Hyst}$	50	–	150	mV	Output voltage decreasing
6.2.6	Pin RTADJ input current	$I_{RTADJ,MAX}$	-1	0.1	1	µA	V_{RTADJ} = 1.2V
6.2.7	Delay time	t_{RD}	6	8	10	ms	–
6.2.8	Reset reaction time	t_{RR}	2	–	10	µs	Output voltage decreasing

6.3 Description Watchdog Function

Principle:

The watchdog supervises the operation of the microprocessor. The result is monitored by the status of pin WO. A high level at pin WO means, that so far no microprocessor failure did occur. A low level at pin WO means, that a microprocessor failure did occur. The watchdog signal is only valid for input (battery) voltage higher than $V_{S,off}$. The pin WO is also pulled to low, if the reset signal is pulled to low.

Watchdog mode select WMSEL:

The watchdog offers two operation modes: Slow watchdog timing and fast watchdog timing. For slow watchdog timing please connect pin WMSEL to output voltage V_{CC}. For fast watchdog timing please connect WMSEL to ground (GND). The watchdog mode select pin WMSEL has an integrated pull-down resistor $R_{WMSEL,INT}$.

It is possible to change the time base during operation by switching the level at pin WMSEL from high to low or from low to high. The new timing is valid from the beginning of the new period (beginning of new trigger window). From this time on, the frequency of the microprocessor signal at pin WI has to be adapted, please refer to **Figure 11** and **Figure 12.** If the watchdog function is not used, please connect pin WMSEL to ground (GND) to avoid EMC related influence.

Watchdog input pin WI:

The watchdog input pin WI is connected to the microprocessor (only if watchdog is used). If watchdog is not used, please connect to ground (GND).

Initialization:

The watchdog initializes as soon as the reset signal at pin RO turns to high level. With a delay time equal to t_{RD} after the rising edge of the reset signal, the so-called “Ignore Window” starts. The duration of the “Ignore Window” (IW) depends on the selected mode of the watchdog operation, either slow watchdog timing or fast watchdog timing. Within this “Ignore Window” the microprocessor must initialize; during the “Ignore Window” any signal at watchdog input pin WI is ignored. The watchdog input pin WI has an integrated pull-down resistor $R_{WI,INT}$.

Normal operation (please refer to Figure 9 and Figure 10):

After closing the “Ignore Window” the watchdog opens the first “Trigger Window” (duration: watchdog period $t_{WD,p}$ minus the watchdog sampling time t_{sam}). Both watchdog period $t_{WD,p}$ and watchdog sampling time t_{sam} are depending on the selected mode of the watchdog operation, either slow watchdog timing or fast watchdog timing. Within the “Trigger Window” a valid trigger signal must be applied to the watchdog input WI. A valid trigger signal is a falling edge from $V_{WI,H}$ to $V_{WI,L}$. After receiving a valid trigger signal within the “Trigger Window” the watchdog immediately terminates the “Trigger Window” and opens the next “Trigger Window” after a time duration t_{sam}.

A trigger signal should not be applied during the time duration t_{sam} before the beginning of the “Trigger Window”, because this will not be detected.

The watchdog period $t_{WD,p}$ determines the frequency of the watchdog signal at pin WI coming from the microprocessor. The watchdog output WO stays high as long as the watchdog input WI is triggered correctly.

If no valid trigger signal is applied to the pin WI during the “Trigger Window”, either a missing trigger signal or an invalid trigger signal (please refer to explanation below), the watchdog output pin WO will be pulled to ground with the falling edge of the “Trigger Window”. The watchdog pin WO stays at low level for the reset delay time t_{RD}. Then the watchdog output pin WO turns back to high level again. With the rising edge of the watchdog signal a new “Ignore Window” is opened.

The watchdog signal WO does not influence the reset signal RO, but the reset signal RO influences the watchdog signal WO.

If a reset condition occurs, the watchdog output pin WO is pulled to ground together with the reset output pin RO. The watchdog output pin stays at low level as long as the reset output pin RO is pulled to ground plus the reset delay time t_{RD}; t_{RD} is not depending on the selected mode of the watchdog operation. Then the watchdog output pin WO turns back to high level again. With the rising edge of the watchdog signal a new “Ignore Window” is opened.

Valid trigger signal (please refer to Figure 8):

Watchdog input WI is periodically sampled with a period of t_{sam}. The watchdog sampling time t_{sam} depends on the selected mode of the watchdog operation, either slow watchdog timing or fast watchdog timing. A valid trigger signal is a falling edge from $V_{WI,H}$ to $V_{WI,L}$. To improve immunity against noise or glitches on the watchdog input, at least two high samples followed by two low samples are required for a valid trigger signal. For example, if the first three samples (two high one low) of the trigger pulse at pin WI are inside the watchdog period $t_{WD,p}$ and only the fourth sample (the second low sample) is taken in the following period $t_{WD,p}$, then the watchdog output WO will be pulled to low. The frequency of the triggering signal at watchdog input pin WI must be determined, so that valid triggering is ensured under all operating conditions.

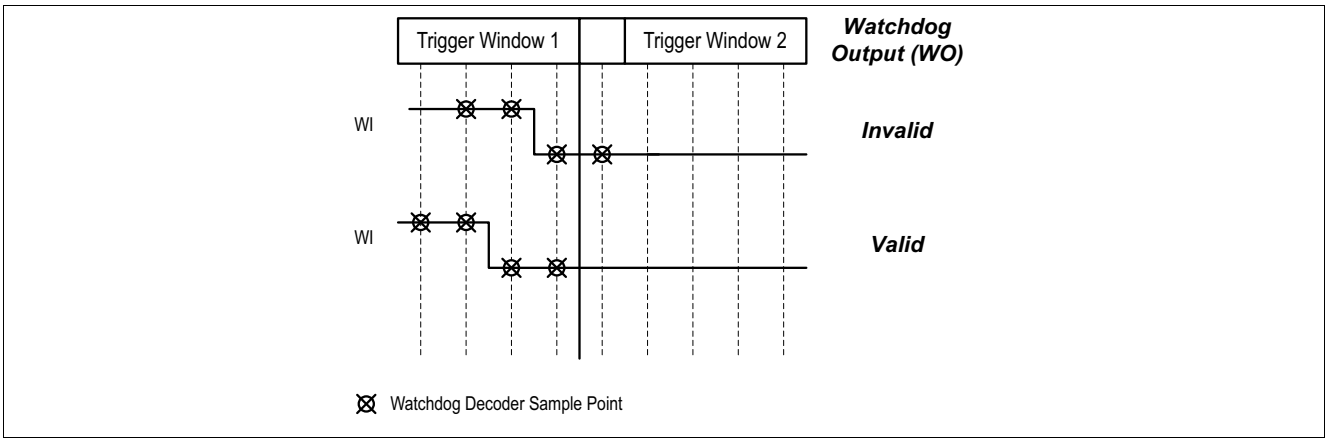


Figure 8 Valid triggering

Watchdog output pin WO:

The watchdog output is an open collector structure. As soon as the watchdog detects a microprocessor failure, the pin is pulled to ground. A pull up resistor (R3) connected to V_{CC} or another voltage source is necessary. If the input (battery) voltage is below the input under voltage shutdown threshold $V_{S,off}$ the pin RO is pulled to ground (GND) and consequently pin WO is also pulled to ground (GND). As soon as the internal supply of the chip drops down, the open collector structure is no longer able to pull pin WO to ground therefore pin WO goes up to the pull-up voltage (if not supplied by voltage V_{CC}).

The watchdog output pin WO might be connected in parallel to the reset output pin RO, if application requires this.

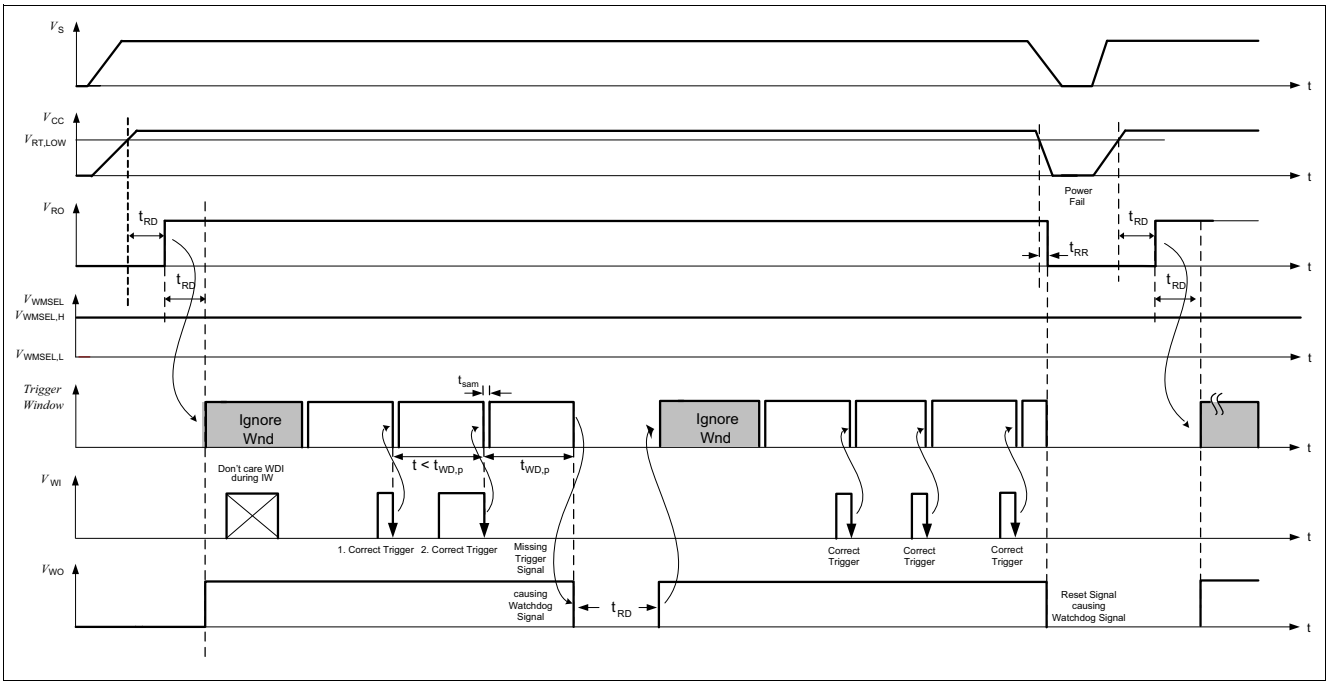


Figure 9 Watchdog Timing Diagram, Slow Watchdog timing

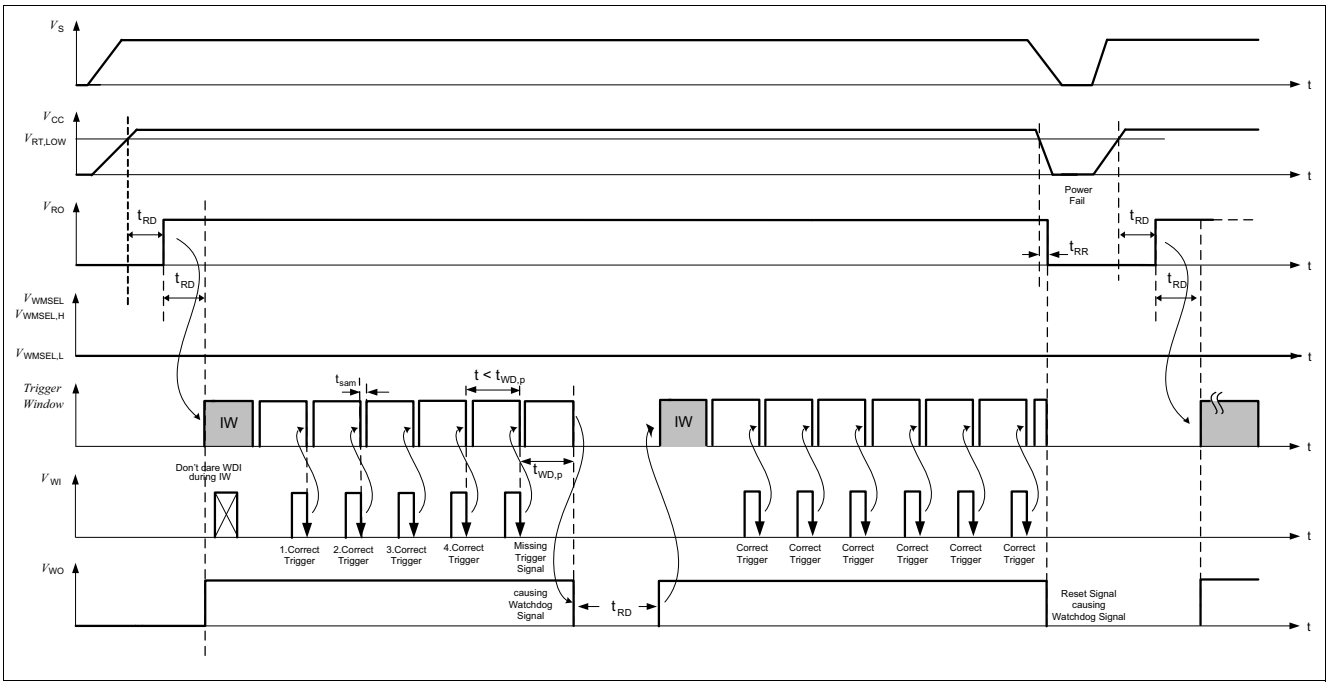


Figure 10 Watchdog Timing Diagram, Fast Watchdog timing