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# TLS203B0

Linear Voltage Post Regulator  
Low Dropout, Low Noise, 3.3 V, Adjustable, 300 mA

TLS203B0EJV  
TLS203B0EJV33  
TLS203B0LDV  
TLS203B0LDV33

## Data Sheet

Rev. 1.2, 2015-01-12

# Linear Voltage Post Regulator

## Low Dropout, Low Noise, 3.3 V, Adjustable, 300 mA

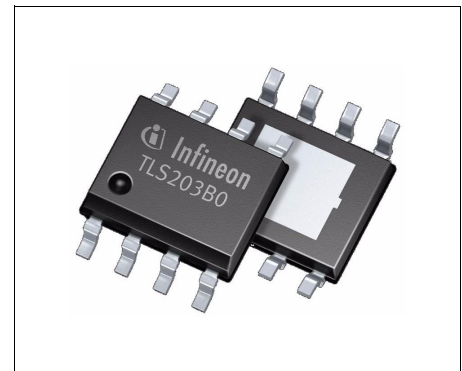
TLS203B0



## 1 Overview

### Features

- Low Noise down to  $24 \mu V_{RMS}$  (BW = 10 Hz to 100 kHz)
- 300 mA Current Capability
- Low Quiescent Current: 30  $\mu A$
- Wide Input Voltage Range up to 20 V
- Internal circuitry working down to 2.3 V
- 2.5% Output Voltage Accuracy (over full temperature and load range)
- Low Dropout Voltage: 270 mV
- Very low Shutdown Current: < 1  $\mu A$
- No Protection Diodes Needed
- Fixed Output Voltage: 3.3 V
- Adjustable Version with Output from 1.22 V to 20 V
- Stable with  $\geq 3.3 \mu F$  Output Capacitor
- Stable with Aluminium, Tantalum or Ceramic Output Capacitors
- Reverse Polarity Protection
- No Reverse Current
- Overcurrent and Overtemperature Protected
- PG-DSO-8 Exposed Pad and PG-TSON-10 Exposed Pad Package
- Suitable for Use in Automotive Electronics as Post Regulator
- Green Product (RoHS compliant)
- AEC Qualified



PG-DSO-8 Exposed Pad



PG-TSON-10

The TLS203B0 is a micropower, low noise, low dropout voltage regulator. The device is capable of supplying an output current of 300 mA with a dropout voltage of 270 mV. Designed for use in battery-powered systems, the low quiescent current of 30  $\mu A$  makes it an ideal choice.

A key feature of the TLS203B0 is its low output noise. By adding an external 10 nF bypass capacitor output noise values down to  $24 \mu V_{RMS}$  over a 10 Hz to 100 kHz bandwidth can be reached. The TLS203B0 voltage regulator

Type	Package	Marking
TLS203B0EJV	PG-DSO-8 Exposed Pad	203B0V
TLS203B0EJV33	PG-DSO-8 Exposed Pad	203B0V33
TLS203B0LDV	PG-TSON-10	203B0V
TLS203B0LDV33	PG-TSON-10	203B0V3

is stable with output capacitors as small as 3.3  $\mu\text{F}$ . Small ceramic capacitors can be used without the series resistance required by many other linear voltage regulators.

Internal protection circuitry includes reverse battery protection, current limiting and reverse current protection. The TLS203B0 comes as fixed output voltage variant 3.3 V as well as adjustable device with a 1.22 V reference voltage. It is available in a PG-DSO-8 Exposed Pad and as well as in a PG-TSON-10 Exposed Pad package.

## 2 Block Diagram

Note: Pin numbers in block diagrams refer to the PG-DSO-8 Exposed Pad package type.

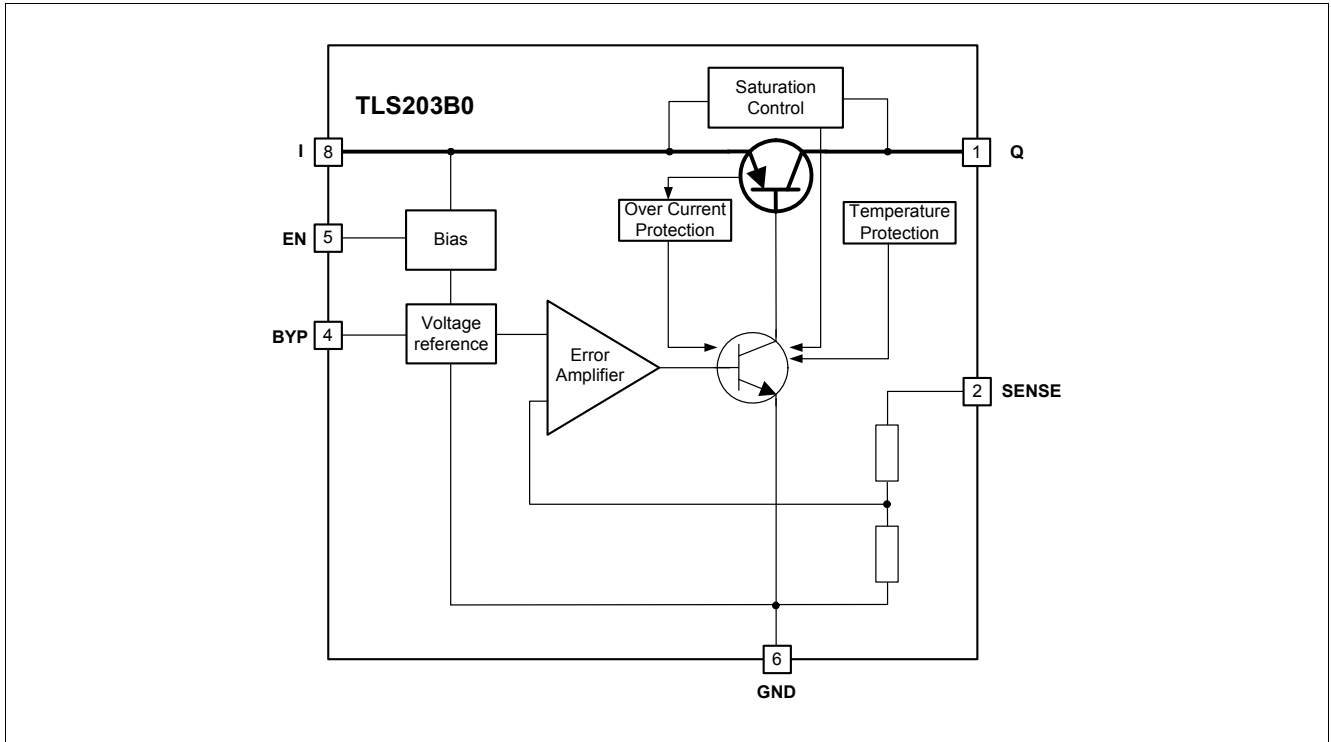


Figure 1 Block Diagram TLS203B0 V33 fixed voltage version

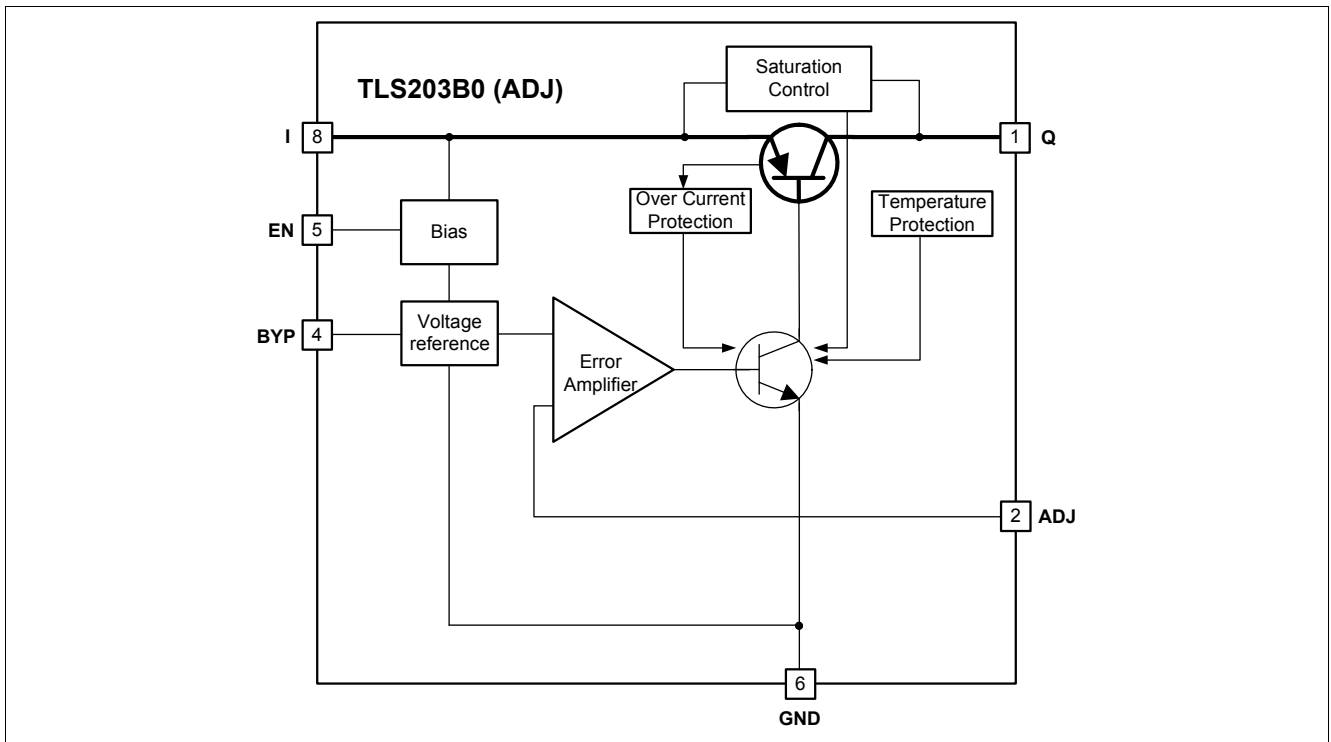


Figure 2 Block Diagram TLS203B0 V adjustable version

### 3 Pin Configuration

#### 3.1 Pin Assignment

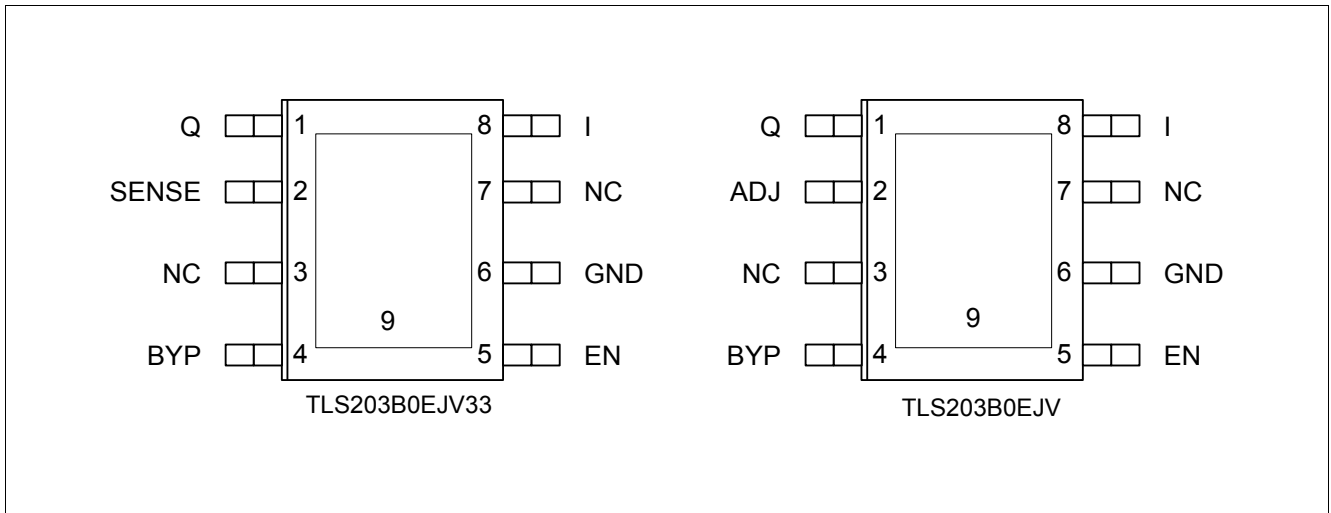


Figure 3 Pin Configuration of TLS203B0 in PG-DSO-8 Exposed Pad for fixed voltage and adjustable version

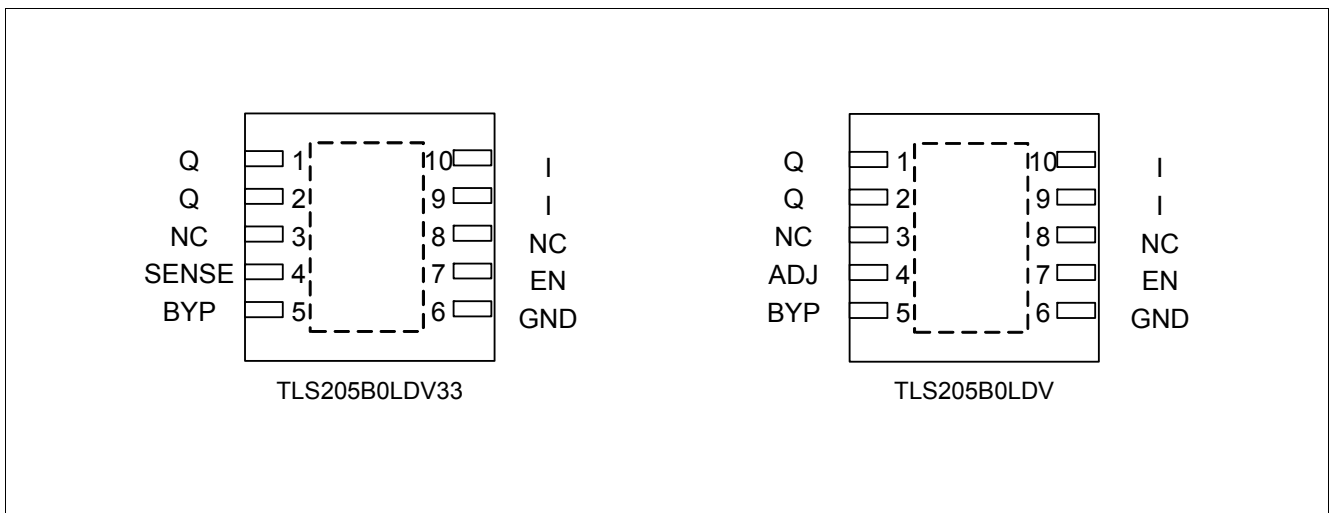


Figure 4 Pin Configuration of TLS203B0 in PG-TSON-10 for fixed voltage and adjustable version.

### 3.2 Pin Definitions and Functions

Pin	Symbol	Function
1 (DSO-8 EP) 1,2 (TSON-10)	Q	<b>Output.</b> Supplies power to the load. For this pin a minimum output capacitor of 3.3 $\mu$ F is required to prevent oscillations. Larger output capacitors may be required for applications with large transient loads in order to limit peak voltage transients or when the regulator is applied in conjunction with a bypass capacitor. For more details please refer to <b>“Application Information” on Page 24.</b>
2 (DSO-8 EP) 4 (TSON-10)	SENSE (fix voltage version)	<b>Output Sense.</b> For the fixed voltage version the SENSE pin is the input to the error amplifier. This allows to achieve an optimized regulation performance in case of small voltage drops $R_p$ that occur between regulator and load. In applications where such drops are relevant they can be eliminated by connecting the SENSE pin directly at the load. In standard configuration the SENSE pin can be directly connected to Q. For further details please refer to the section <b>“Kelvin Sense Connection” on Page 25.</b>
2 (DSO-8 EP) 4 (TSON-10)	ADJ (adjustable version)	<b>Adjust.</b> For the adjustable version the ADJ pin is the input to the error amplifier. The ADJ pin voltage is 1.22 V referenced to ground and allows a output voltage range from 1.22 V to $20 V - V_{DR}$ . The ADJ pin is internally clamped to $\pm 7$ V. Please note that the bias current of the ADJ pin is flowing into the pin. Its typical value of 60 nA shows a good stability with temperature. For further details please refer to Typical Performance Graph <b>“Adjust Pin Bias Current versus Junction Temperature T<sub>J</sub>” on Page 20.</b>
3, 7 (DSO-8 EP) 3, 8 (TSON-10)	NC	<b>No Connect.</b> The NC Pins have no connection to any internal circuitry. Connect either to GND or leave open.
4 (DSO-8 EP) 5 (TSON-10)	BYP	<b>Bypass.</b> The BYP pin is used to bypass the reference of the TLS203B0 to achieve low noise performance. The BYP-pin is clamped internally to $\pm 0.6$ V (i.e. one $V_{BE}$ ). A small capacitor from the output Q to the BYP pin will bypass the reference to lower the output voltage noise <sup>1)</sup> . If not used this pin must be left unconnected.
5 (DSO-8 EP) 7 (TSON-10)	EN	<b>Enable.</b> With the EN pin the TLS203B0 can be put into a low power shutdown state. The output will be off when the EN is pulled low. The EN pin can be driven either by 3.3 V or 5 V logic or as well by open-collector logic with pull-up resistor. The pull-up resistor is required to supply the pull-up current of the open-collector gate <sup>2)</sup> and the EN pin current <sup>3)</sup> . Please note that if the EN pin is not used it must be connected to $V_i$ . It must not be left floating.
6 (DSO-8 EP) 6,(TSON-10)	GND	<b>Ground.</b> For the ADJ version connect the bottom of the output voltage setting resistor divider directly to the GND pin for optimum load regulation performance.

Pin Configuration

Pin	Symbol	Function
8 (DSO-8 EP) 9, 10 (TSON-10)	I	<b>Input.</b> The device is supplied by the input pin I. A capacitor at the input pin is required if the device is more than 6 inches away from the main input filter capacitor or if a non-negligible inductance is present at the input I <sup>4)</sup> . The TLS203B0 is designed to withstand reverse voltages on the input pin I with respect to GND and output Q. In the case of reverse input (e.g. due to a wrongly attached battery) the device will act as if there is a diode in series with its input. In this way there will be no reverse current flowing into the regulator and no reverse voltage will appear at the load. Hence, the device will protect both - the device itself and the load.
9 (DSO-8 EP) 11 (TSON-10)	Tab	<b>Exposed Pad.</b> To ensure proper thermal performance, solder Pin 11 of TSON-10 to the PCB ground and tie directly to Pin 6. In the case of DSO-8 EP as well solder Pin 9 to the PCB ground and tie directly to Pin 6 (GND).

- 1) A maximum value of 10 nF can be used for reducing output voltage noise over the bandwidth from 10 Hz to 100 kHz.
- 2) Normally several microamperes.
- 3) Typical value is 1  $\mu$ A.
- 4) In general the output impedance of a battery rises with frequency, so it is advisable to include a bypass capacitor in battery-powered circuits. Depending on actual conditions an input capacitor in the range of 1 to 10  $\mu$ F is sufficient.



## 4 General Product Characteristics

### 4.1 Absolute Maximum Ratings

**Table 1 Absolute Maximum Ratings** <sup>1)</sup>

$T_j = -40\text{ °C}$  to  $+150\text{ °C}$ ; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
<b>Input Voltage</b>							
Voltage	$V_I$	-20	–	20	V	–	P_4.1.1
<b>Output Voltage</b>							
Voltage	$V_Q$	-20	–	20	V	–	P_4.1.2
Input to Output Differential Voltage	$V_I - V_Q$	-20	–	20	V	–	P_4.1.3
<b>Sense Pin</b>							
Voltage	$V_{SENSE}$	-20	–	20	V	–	P_4.1.4
<b>ADJ Pin</b>							
Voltage	$V_{ADJ}$	-7	–	7	V	–	P_4.1.5
<b>BYP Pin</b>							
Voltage	$V_{BYP}$	-0.6	–	0.6	V		P_4.1.6
<b>Enable Pin</b>							
Voltage	$V_{EN}$	-20	–	20	V	–	P_4.1.7
<b>Temperatures</b>							
Junction Temperature	$T_j$	-40	–	150	°C	–	P_4.1.8
Storage Temperature	$T_{stg}$	-55	–	150	°C	–	P_4.1.9
<b>ESD Susceptibility</b>							
All Pins	$V_{ESD}$	-2	–	2	kV	HBM <sup>2)</sup>	P_4.1.10
All Pins	$V_{ESD}$	-1	–	1	kV	CDM <sup>3)</sup>	P_4.1.11

1) Not subject to production testing, specified by design.

2) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS001 (1.5 kΩ, 100 pF)

3) ESD susceptibility, Charged Device Model "CDM" according JEDEC JESD22-C101

#### Notes

1. Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

## 4.2 Functional Range

**Table 2 Functional Range**

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Input Voltage Range (fix voltage version)	$V_I$	3.8	–	20	V	–	P_4.2.1
Input Voltage Range (adjustable voltage version)	$V_I$	2.3	–	20	V	– <sup>1)</sup>	P_4.2.2
Output Capacitor's Requirements for Stability	$C_Q$	3.3	–	–	$\mu\text{F}$	$C_{\text{BYP}} = 0 \text{ nF}$ <sup>2)</sup>	P_4.2.3
Output Capacitor's Requirements for Stability	$C_Q$	6.8	–	–	$\mu\text{F}$	$0 < C_{\text{BYP}} \leq 10 \text{ nF}$ <sup>2)</sup>	P_4.2.4
ESR	$ESR$	– <sup>3)</sup>	–	3	$\Omega$	– <sup>2)</sup>	P_4.2.5
Operating Junction Temperature	$T_j$	-40	–	125	$^{\circ}\text{C}$	–	P_4.2.6

- 1) For the TLS203B0 adjustable version the minimum limit of the functional range  $V_I$  is tested and specified with the ADJ pin connected to the Q pin.
- 2) for further details see corresponding graph.
- 3)  $C_{\text{BYP}} = 0 \text{ nF}$ ,  $C_Q \geq 3.3 \mu\text{F}$ ; please note that for cases where a bypass capacitor at BYP is used – depending on the actual applied capacitance of  $C_Q$  and  $C_{\text{BYP}}$  a minimum requirement for ESR of  $C_Q$  may apply.

Note: Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the Electrical Characteristics table.

## 4.3 Thermal Resistance

Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to [www.jedec.org](http://www.jedec.org).

**Table 3 Thermal Resistance<sup>1)</sup>**

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
<b>TLS203B0EJ (PG-DSO-8 Exposed Pad)</b>							
Junction to Case	$R_{\text{thJC}}$	–	7.0	–	K/W	–	P_4.3.1
Junction to Ambient	$R_{\text{thJA}}$	–	39	–	K/W	– <sup>2)</sup>	P_4.3.2
Junction to Ambient	$R_{\text{thJA}}$	–	155	–	K/W	Footprint only <sup>3)</sup>	P_4.3.3
Junction to Ambient	$R_{\text{thJA}}$	–	66	–	K/W	300 mm <sup>2</sup> heatsink area on PCB <sup>3)</sup>	P_4.3.4
Junction to Ambient	$R_{\text{thJA}}$	–	52	–	K/W	600 mm <sup>2</sup> heatsink area on PCB <sup>3)</sup>	P_4.3.5
<b>TLS203B0LD (PG-TSON-10)</b>							
Junction to Case	$R_{\text{thJC}}$	–	6.4	–	K/W	–	P_4.3.6
Junction to Ambient	$R_{\text{thJA}}$	–	53	–	K/W	– <sup>2)</sup>	P_4.3.7
Junction to Ambient	$R_{\text{thJA}}$	–	183	–	K/W	Footprint only <sup>3)</sup>	P_4.3.8

**Table 3 Thermal Resistance** <sup>1)</sup>

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Junction to Ambient	$R_{thJA}$	–	69	–	K/W	300 mm <sup>2</sup> heatsink area on PCB <sup>3)</sup>	P_4.3.9
Junction to Ambient	$R_{thJA}$	–	57	–	K/W	600 mm <sup>2</sup> heatsink area on PCB <sup>3)</sup>	P_4.3.10

1) Not subject to production test, specified by design.

2) Specified  $R_{thJA}$  value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70 μm Cu, 2 x 35 μm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

3) Specified  $R_{thJA}$  value is according to JEDEC JESD 51-3 at natural convection on FR4 1s0p board; The Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm<sup>3</sup> board with 1 copper layer (1 x 70 μm Cu).

## 5 Electrical Characteristics

**Table 4 Electrical Characteristics**

-40 °C <  $T_j$  < 125 °C; all voltages with respect to ground; positive current defined flowing out of pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
<b>Minimum Operating Voltage</b> <sup>1)</sup>							
Minimum Operating Voltage	$V_{I,min}$	–	1.8	2.3	V	$I_Q = 300 \text{ mA}$ <sup>2) 3)</sup>	P_5.0.1
<b>Output Voltage</b> <sup>4)</sup>							
TLS203B0EJV33 TLS203B0LDV33	$V_Q$	3.220	3.30	3.380	V	$1 \text{ mA} < I_Q < 300 \text{ mA}$ ; $4.3 \text{ V} < V_I < 20 \text{ V}$	P_5.0.2
TLS203B0EJV TLS203B0LDV	$V_Q$	1.190	1.220	1.250	V	$1 \text{ mA} < I_Q < 300 \text{ mA}$ ; $2.3 \text{ V} < V_I < 20 \text{ V}$ <sup>3)</sup>	P_5.0.3
<b>Line Regulation</b>							
TLS203B0EJV33 TLS203B0LDV33	$\Delta V_Q$	–	1	20	mV	$\Delta V_I = 3.8 \text{ V to } 20 \text{ V}$ ; $I_Q = 1 \text{ mA}$	P_5.0.4
TLS203B0EJV TLS203B0LDV	$\Delta V_Q$	–	1	20	mV	$\Delta V_I = 2.0 \text{ V to } 20 \text{ V}$ ; $I_Q = 1 \text{ mA}$ <sup>3)</sup>	P_5.0.5
<b>Load Regulation</b>							
TLS203B0EJV33 TLS203B0LDV33	$\Delta V_Q$	–	6	15	mV	$T_J = 25 \text{ }^\circ\text{C}$ ; $V_I = 4.3 \text{ V}$ ; $\Delta I_Q = 1 \text{ to } 300 \text{ mA}$	P_5.0.6
TLS203B0EJV33 TLS203B0LDV33	$\Delta V_Q$	–	–	28	mV	$V_I = 4.3 \text{ V}$ ; $\Delta I_Q = 1 \text{ to } 300 \text{ mA}$	P_5.0.7
TLS203B0EJV TLS203B0LDV	$\Delta V_Q$	–	3	8	mV	$T_J = 25 \text{ }^\circ\text{C}$ ; $V_I = 2.3 \text{ V}$ ; $\Delta I_Q = 1 \text{ to } 300 \text{ mA}$ <sup>3)</sup>	P_5.0.8
TLS203B0EJV TLS203B0LDV	$\Delta V_Q$	–	–	12	mV	$V_I = 2.3 \text{ V}$ ; $\Delta I_Q = 1 \text{ to } 300 \text{ mA}$ <sup>3)</sup>	P_5.0.9
<b>Dropout Voltage</b> <sup>2) 5) 6)</sup>							
Dropout Voltage	$V_{DR}$	–	130	190	mV	$I_Q = 10 \text{ mA}$ ; $V_I = V_{Q,nom}$ ; $T_J = 25 \text{ }^\circ\text{C}$	P_5.0.10
Dropout Voltage	$V_{DR}$	–	–	250	mV	$I_Q = 10 \text{ mA}$ ; $V_I = V_{Q,nom}$	P_5.0.11
Dropout Voltage	$V_{DR}$	–	170	220	mV	$I_Q = 50 \text{ mA}$ ; $V_I = V_{Q,nom}$ ; $T_J = 25 \text{ }^\circ\text{C}$	P_5.0.12
Dropout Voltage	$V_{DR}$	–	–	320	mV	$I_Q = 50 \text{ mA}$ ; $V_I = V_{Q,nom}$	P_5.0.13
Dropout Voltage	$V_{DR}$	–	200	240	mV	$I_Q = 100 \text{ mA}$ ; $V_I = V_{Q,nom}$ ; $T_J = 25 \text{ }^\circ\text{C}$	P_5.0.14
Dropout Voltage	$V_{DR}$	–	–	340	mV	$I_Q = 100 \text{ mA}$ ; $V_I = V_{Q,nom}$	P_5.0.15
Dropout Voltage	$V_{DR}$	–	270	300	mV	$I_Q = 300 \text{ mA}$ ; $V_I = V_{Q,nom}$ ; $T_J = 25 \text{ }^\circ\text{C}$	P_5.0.16
Dropout Voltage	$V_{DR}$	–	–	400	mV	$I_Q = 300 \text{ mA}$ ; $V_I = V_{Q,nom}$	P_5.0.17
<b>Quiescent Current</b>							
Quiescent Current <sup>7)</sup> (Active-Mode, EN-pin high)	$I_q$	–	30	60	$\mu\text{A}$	$V_I = V_{Q,nom}$ ; $I_Q = 0 \text{ mA}$	P_5.0.18

**Table 4 Electrical Characteristics (cont'd)**

-40 °C <  $T_J$  < 125 °C; all voltages with respect to ground; positive current defined flowing out of pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Quiescent Current (Off-Mode, EN-pin low)	$I_Q$	–	0.1	1	µA	$V_I = 6\text{ V}; V_{EN} = 0\text{ V};$ $T_J = 25\text{ °C}$	P_5.0.19
<b>GND Pin Current</b> <sup>5) 7)</sup>							
GND Pin Current	$I_{GND}$	–	50	100	µA	$V_I = V_{Q,nom};$ $I_Q = 1\text{ mA}$	P_5.0.20
GND Pin Current	$I_{GND}$	–	300	850	µA	$V_I = V_{Q,nom};$ $I_Q = 50\text{ mA}$	P_5.0.21
GND Pin Current	$I_{GND}$	–	0.7	2.2	mA	$V_I = V_{Q,nom};$ $I_Q = 100\text{ mA}$	P_5.0.22
GND Pin Current	$I_{GND}$	–	4	12	mA	$V_I = V_{Q,nom};$ $I_Q = 300\text{ mA}$	P_5.0.23
<b>Enable</b>							
Enable Threshold High	$V_{th,EN}$	–	0.8	2.0	V	$V_Q = \text{Off to On}$	P_5.0.24
Enable Threshold Low	$V_{tl,EN}$	0.25	0.65	–	V	$V_Q = \text{On to Off}$	P_5.0.25
EN Pin Current <sup>8)</sup>	$I_{EN}$	–	0.01	–	µA	$V_{EN} = 0\text{ V}; T_J = 25\text{ °C}$	P_5.0.26
EN Pin Current <sup>8)</sup>	$I_{EN}$	–	1	–	µA	$V_{EN} = 20\text{ V}; T_J = 25\text{ °C}$	P_5.0.27
<b>Adjust Pin Bias Current</b> <sup>9) 10)</sup>							
ADJ Pin Bias Current	$I_{bias,ADJ}$	–	60	–	nA	$T_J = 25\text{ °C}$	P_5.0.28
<b>Output Voltage Noise</b> <sup>10)</sup>							
Output Voltage Noise TLS203B0EJV <sup>11)</sup> TLS203B0LDV <sup>11)</sup>	$e_{no}$	–	41	–	$\mu V_{RMS}$	$C_Q = 10\text{ }\mu\text{F};$ $C_{BYP} = 10\text{ nF};$ $I_Q = 300\text{ mA};$ BW = 10 Hz to 100 kHz	P_5.0.29
Output Voltage Noise TLS203B0EJV <sup>11)</sup> TLS203B0LDV <sup>11)</sup>	$e_{no}$	–	28	–	$\mu V_{RMS}$	$C_Q = 10\text{ }\mu\text{F}$ +250mΩ resistor in series; $C_{BYP} = 10\text{ nF};$ $I_Q = 300\text{ mA};$ BW = 10 Hz to 100 kHz	P_5.0.30
Output Voltage Noise TLS203B0EJV <sup>11)</sup> TLS203B0LDV <sup>11)</sup>	$e_{no}$	–	29	–	$\mu V_{RMS}$	$C_Q = 22\text{ }\mu\text{F}$ $C_{BYP} = 10\text{ nF};$ $I_Q = 300\text{ mA};$ BW = 10 Hz to 100 kHz	P_5.0.31
Output Voltage Noise TLS203B0EJV <sup>11)</sup> TLS203B0LDV <sup>11)</sup>	$e_{no}$	–	24	–	$\mu V_{RMS}$	$C_Q = 22\text{ }\mu\text{F}$ +250mΩ resistor in series; $C_{BYP} = 10\text{ nF};$ $I_Q = 300\text{ mA};$ BW = 10 Hz to 100 kHz	P_5.0.32
Output Voltage Noise TLS203B0EJV33 TLS203B0LDV33	$e_{no}$	–	45	–	$\mu V_{RMS}$	$C_Q = 10\text{ }\mu\text{F};$ $C_{BYP} = 10\text{ nF};$ $I_Q = 300\text{ mA};$ BW = 10 Hz to 100 kHz	P_5.0.33

**Table 4 Electrical Characteristics (cont'd)**

-40 °C <  $T_j$  < 125 °C; all voltages with respect to ground; positive current defined flowing out of pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Output Voltage Noise TLS203B0EJV33 TLS203B0LDV33	$e_{no}$	–	35	–	$\mu V_{RMS}$	$C_Q = 10 \mu F$ +250m $\Omega$ resistor in series; $C_{BYP} = 10 \text{ nF}$ ; $I_Q = 300 \text{ mA}$ ; BW = 10 Hz to 100 kHz	P_5.0.34
Output Voltage Noise TLS203B0EJV33 TLS203B0LDV33	$e_{no}$	–	33	–	$\mu V_{RMS}$	$C_Q = 22 \mu F$ $C_{BYP} = 10 \text{ nF}$ ; $I_Q = 300 \text{ mA}$ ; BW = 10 Hz to 100 kHz	P_5.0.35
Output Voltage Noise TLS203B0EJV33 TLS203B0LDV33	$e_{no}$	–	30	–	$\mu V_{RMS}$	$C_Q = 22 \mu F$ +250m $\Omega$ resistor in series; $C_{BYP} = 10 \text{ nF}$ ; $I_Q = 300 \text{ mA}$ ; BW = 10 Hz to 100 kHz	P_5.0.36
<b>Power Supply Ripple Rejection <sup>10)</sup></b>							
Power Supply Ripple Rejection	$PSRR$	–	65	–	dB	$V_I - V_Q = 1.5 \text{ V (avg)}$ ; $V_{RIPPLE} = 0.5 \text{ Vpp}$ ; $f_r = 120 \text{ Hz}$ ; $I_Q = 300 \text{ mA}$	P_5.0.37
<b>Output Current Limitation</b>							
Output Current Limit	$I_{Q,limit}$	320	–	–	mA	$V_I = 7 \text{ V}$ ; $V_Q = 0 \text{ V}$	P_5.0.38
Output Current Limit	$I_{Q,limit}$	320	–	–	mA	$V_I = V_{Q,nom} + 1 \text{ V}$ or 2.3 V <sup>12)</sup> ; $\Delta V_Q = -0.1 \text{ V}$	P_5.0.39
<b>Input Reverse Leakage Current</b>							
Input Reverse Leakage	$I_{leak,rev}$	–	–	1	mA	$V_I = -20 \text{ V}$ ; $V_Q = 0 \text{ V}$	P_5.0.40
<b>Reverse Output Current <sup>13)</sup></b>							
Fixed Voltage Versions	$I_{Reverse}$	–	10	20	$\mu A$	$V_Q = V_{Q,nom}$ ; $V_I < V_{Q,nom}$ ; $T_J = 25 \text{ }^\circ C$	P_5.0.41
Adjustable Voltage Version	$I_{Reverse}$	–	5	10	$\mu A$	$V_Q = 1.22 \text{ V}$ ; $V_I < 1.22 \text{ V}$ ; $T_J = 25 \text{ }^\circ C$ <sup>3)</sup>	P_5.0.42

- 1) This parameter defines the minimum input voltage for which the device is powered up and provides the maximum nominal output current of 300 mA. The output voltage of the adjustable version in this condition depends on the chosen setting of the external voltage divider as well as on the applied conditions – thus the device is either regulating its nominal output voltage or is in tracking mode. The 3.3 V fixed voltage version is by definition in tracking mode for such low input voltages.
- 2) For the adjustable version of the TLS203B0 the dropout voltage for certain output voltage / load conditions will be restricted by the minimum input voltage specification.
- 3) The adjustable version of the TLS203B0 is tested / specified for these conditions with the ADJ pin connected to the Q pin.
- 4) The operation conditions are limited by the maximum junction temperature. The regulated output voltage specification will only apply for conditions where the limit of the maximum junction temperature is fulfilled. It will therefore not apply for all possible combinations of input voltage and output current at a given output voltage. When operating at maximum input voltage, the output current must be limited for thermal reasons. The same holds true when operating at maximum output current where the input voltage range must be limited for thermal reasons.
- 5) To satisfy requirements for minimum input voltage, the TLS203B0 adjustable version is tested and specified for these conditions with an external resistor divider (two 250 k resistors) for an output voltage of 2.44 V. The external resistors will add a 5  $\mu A$  DC load on the output.

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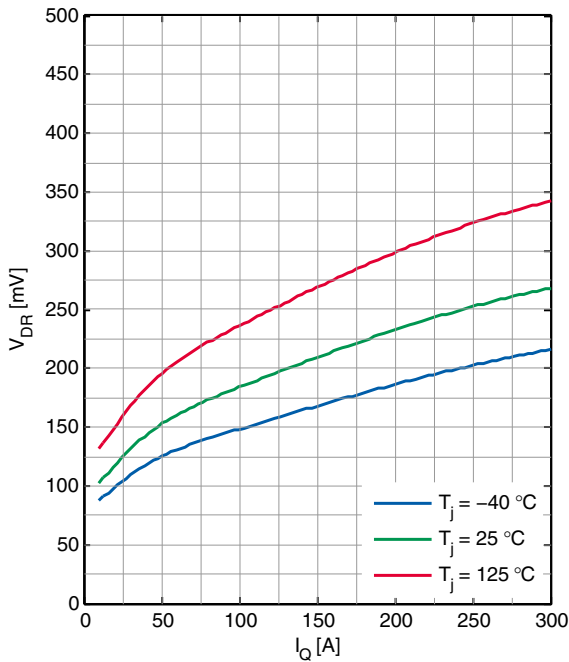
**Electrical Characteristics**

- 6) The dropout voltage is the minimum input to output voltage differential needed to maintain regulation at a specified output current. In dropout, the output voltage will be equal to  $V_I - V_{DR}$
- 7) GND-pin current is tested with  $V_I = V_{Q,nom}$  and a current source load. This means that this parameter is tested while being in the dropout region. The GND pin current will in most cases decrease slightly at higher input voltages - please also refer to the corresponding typical performance graphs.
- 8) The EN pin current flows into EN pin.
- 9) The ADJ pin current flows into ADJ pin.
- 10) Not subject to production test, specified by design.
- 11) ADJ pin connected to output pin Q.
- 12) Whichever of the two values of  $V_I$  is greater in order to also satisfy the requirements for  $V_{I,min}$ .
- 13) Reverse output current is tested with the I pin grounded and the Q pin forced to the rated output voltage. This current flows into the Q pin and out of the GND pin.

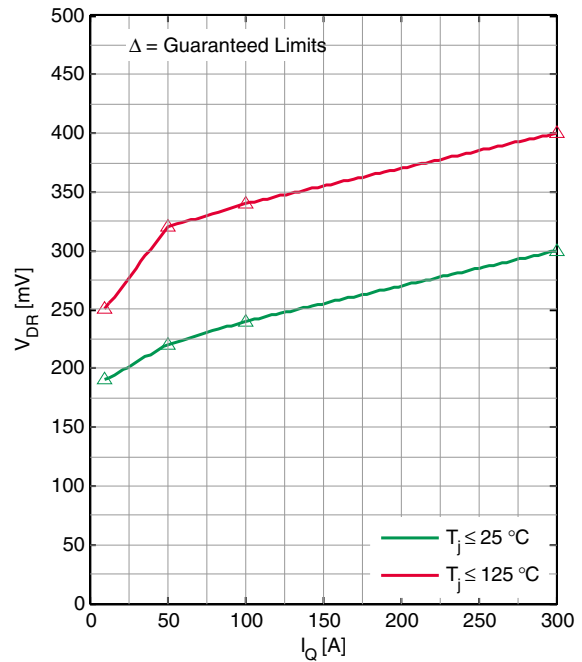
*Note: The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specified mean values expected over the production spread. If not otherwise specified, typical characteristics apply at  $T_A = 25\text{ °C}$  and the given supply voltage.*

### 5.1 Typical Performance Characteristics

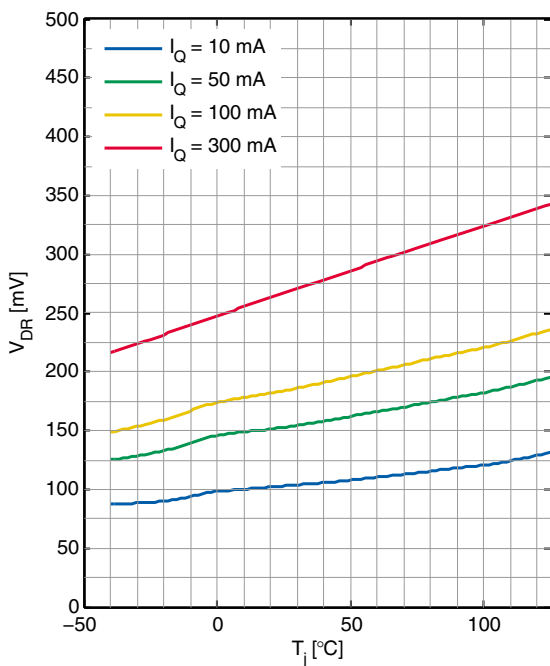
Dropout Voltage  $V_{DR}$  versus Output Current  $I_Q$



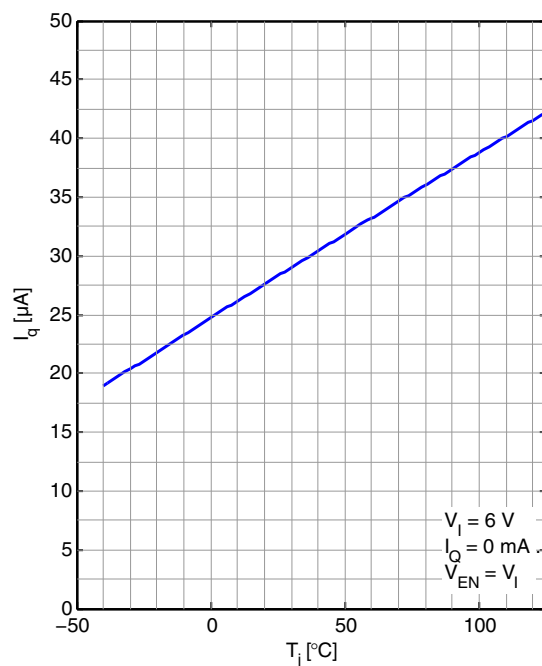
Guaranteed Dropout Voltage  $V_{DR}$  versus Output Current  $I_Q$



Dropout Voltage  $V_{DR}$  versus Junction Temperature  $T_j$

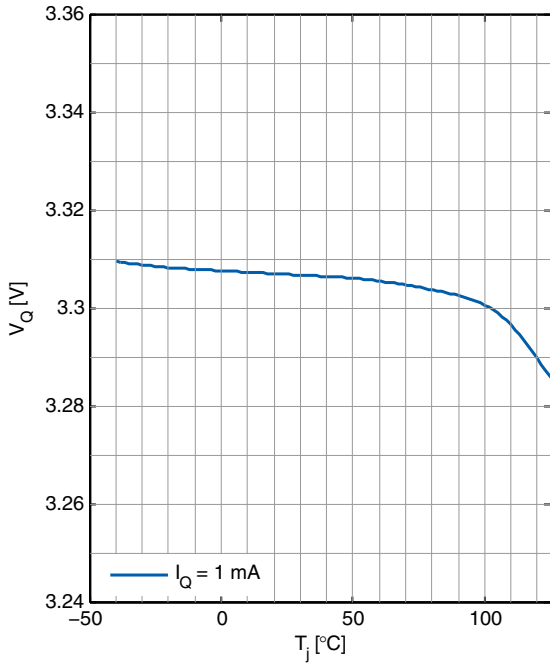


Quiescent Current versus Junction Temperature  $T_j$

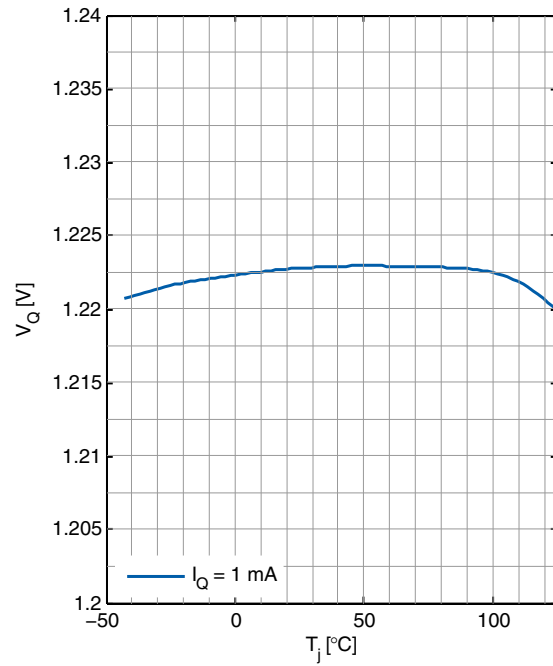




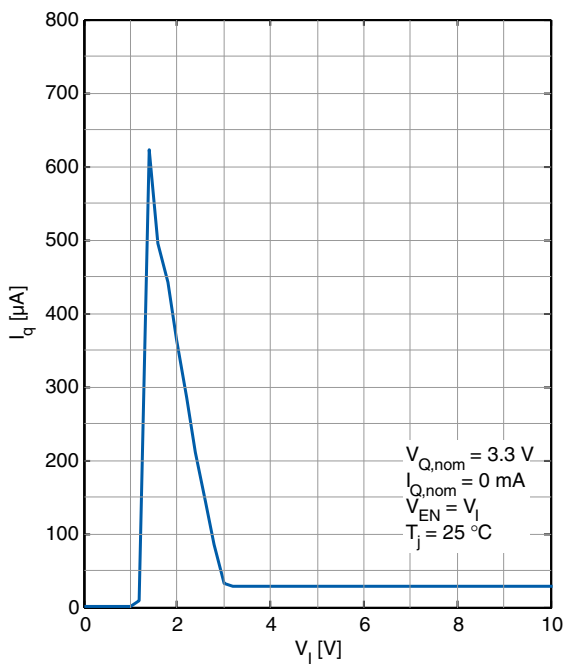
**Output Voltage  $V_Q$  versus Junction Temperature  $T_J$  (TLS203B0EJV33)**



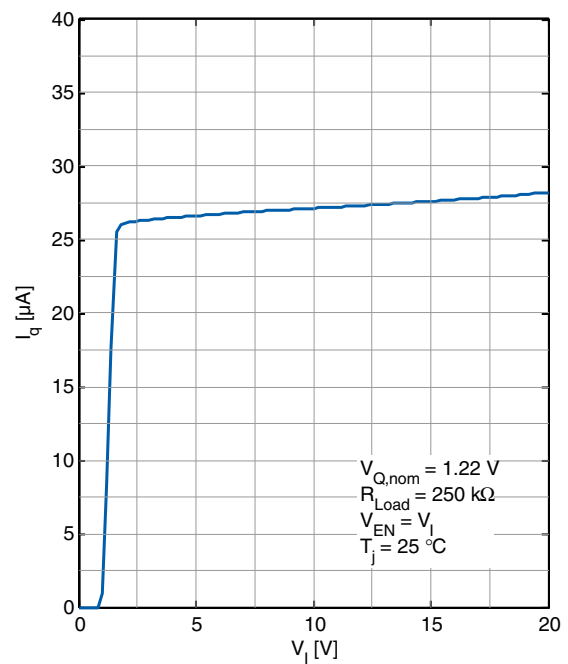
**Output Voltage  $V_Q$  versus Junction Temperature  $T_J$  (TLS203B0EJV)**



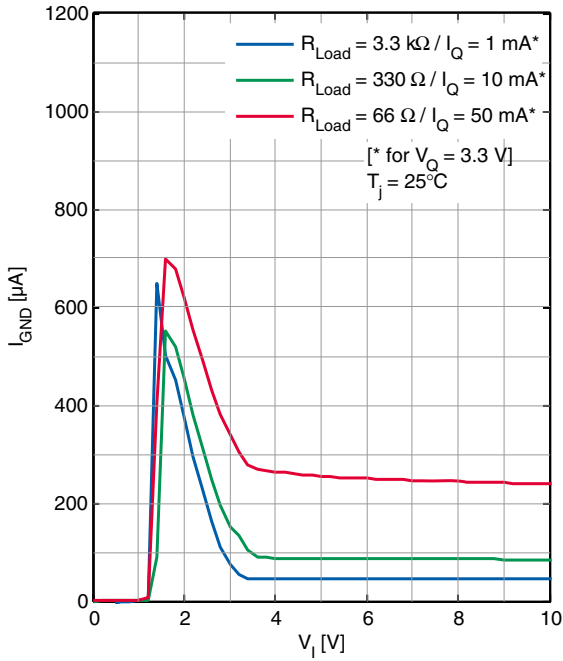
**Quiescent Current  $I_q$  versus Input Voltage  $V_I$  (TLS203B0EJV33)**



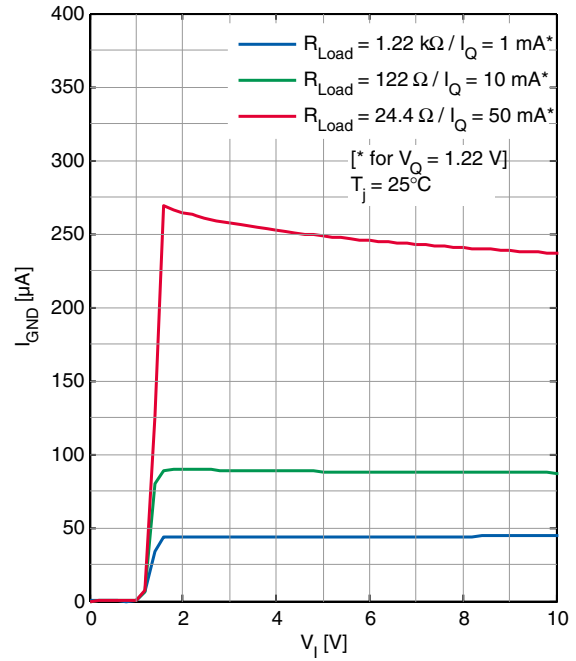
**Quiescent Current  $I_q$  versus Input Voltage  $V_I$  (TLS203B0EJV)**



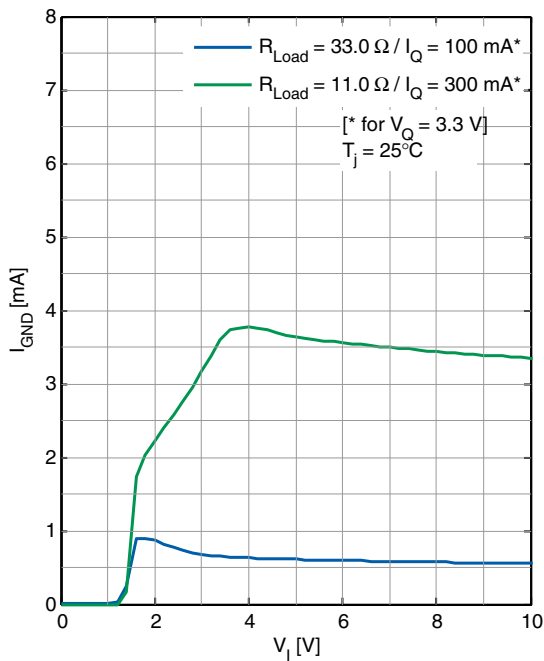
**GND Pin Current  $I_{GND}$  versus Input Voltage  $V_I$  (TLS203B0EJV33)**



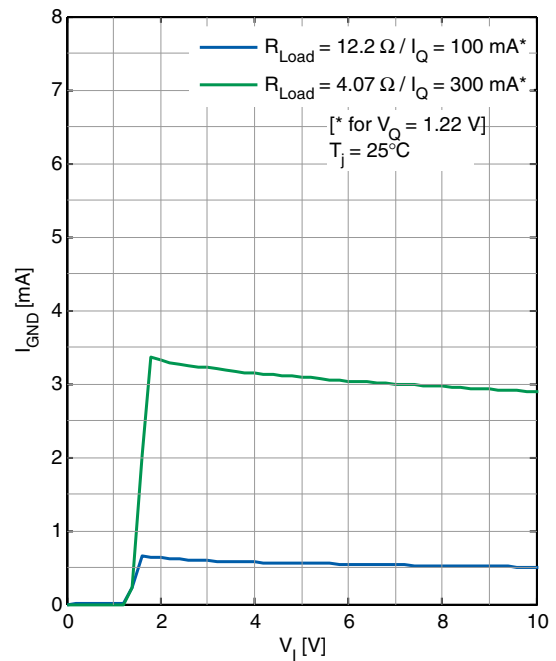
**GND Pin Current  $I_{GND}$  versus Input Voltage  $V_I$  (TLS203B0EJV)**



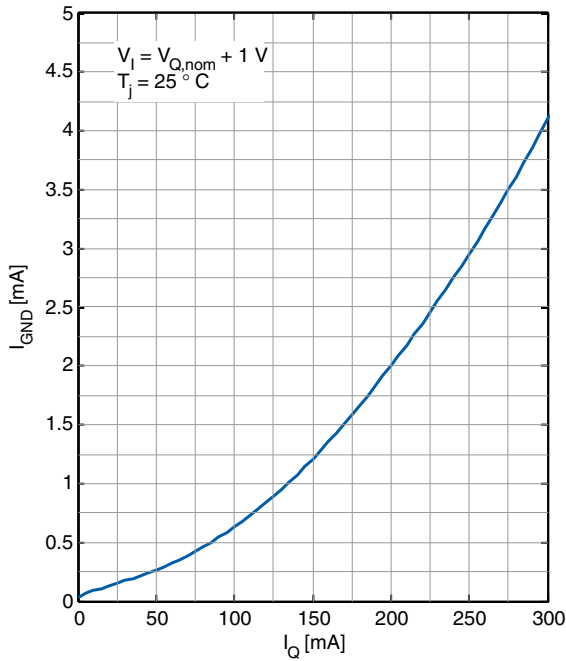
**GND Pin Current  $I_{GND}$  versus Input Voltage  $V_I$  (TLS203B0EJV33)**



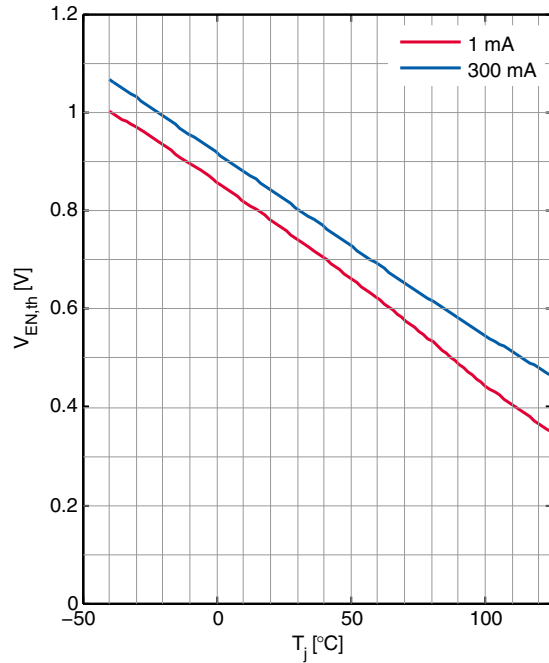
**GND Pin Current  $I_{GND}$  versus Input Voltage  $V_I$  (TLS203B0EJV)**



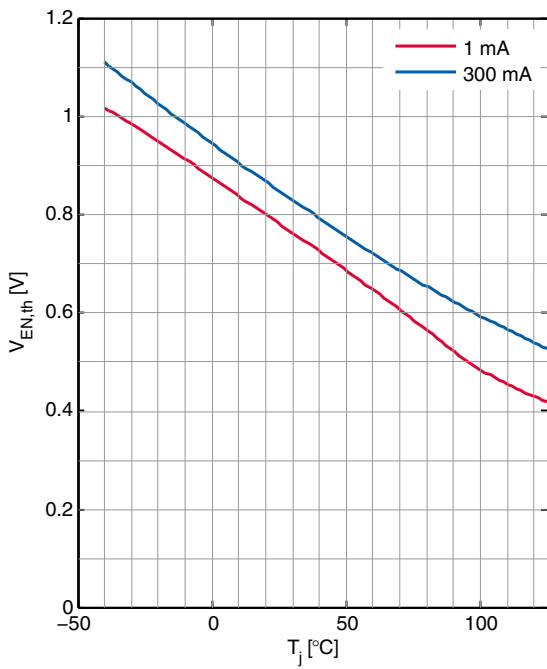
**GND Pin Current  $I_{GND}$  versus Output Current  $I_Q$**



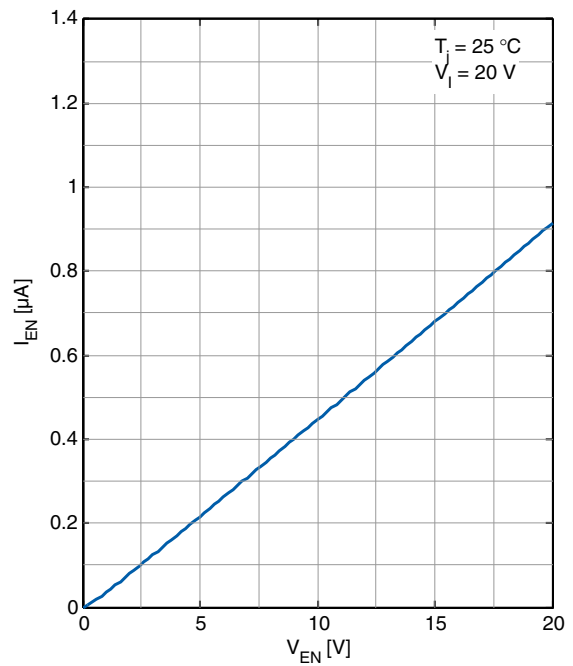
**EN Pin Threshold (On-to-Off) versus Junction Temperature  $T_j$**



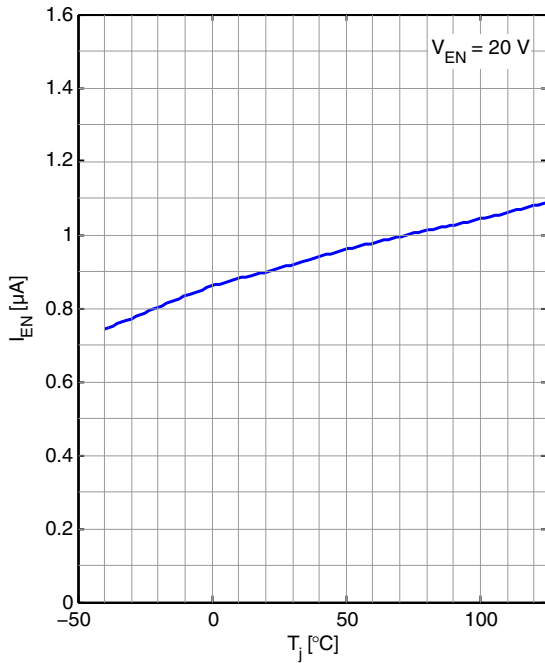
**EN Pin Threshold (Off-to-On) versus Junction temperature  $T_j$**



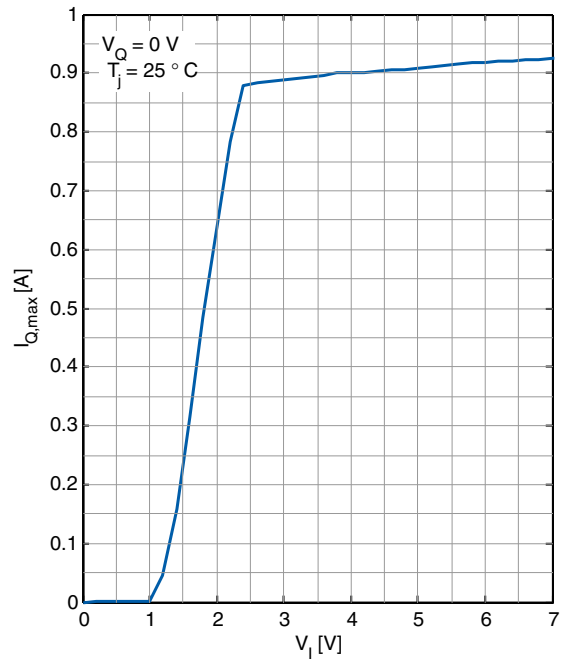
**EN Pin Input Current (On-to-Off) versus EN Pin Voltage  $V_{EN}$**



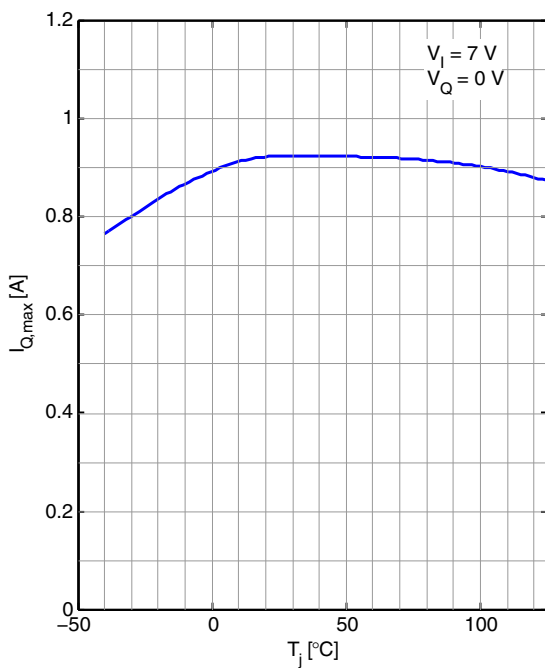
**EN Pin Current versus Junction Temperature  $T_j$**



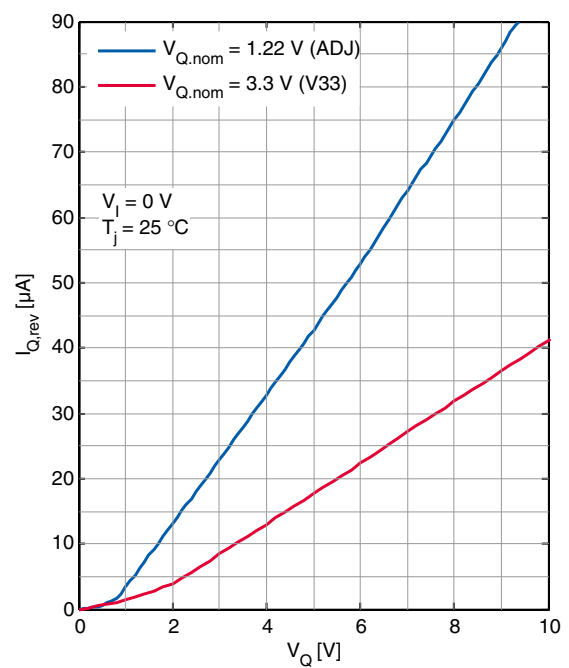
**Current Limit versus Input Voltage  $V_I$**



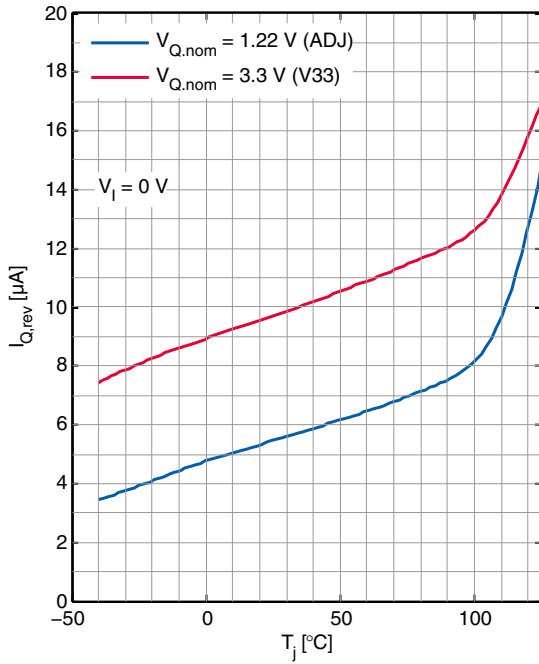
**Current Limit versus Junction Temperature  $T_j$**



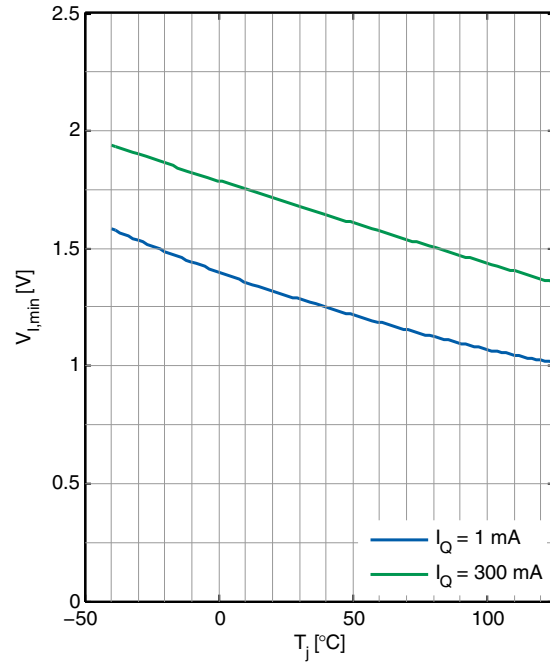
**Reverse Output Current versus Output Voltage  $V_Q$**



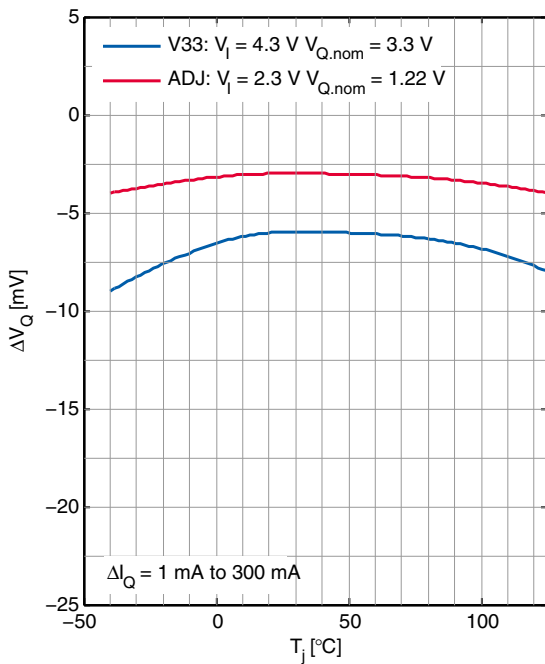
**Reverse Output Current versus Junction Temperature  $T_J$**



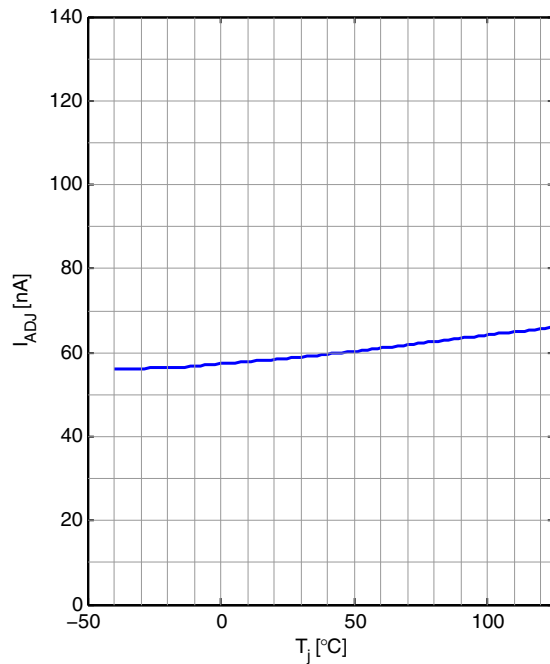
**Minimum Input Voltage <sup>1)</sup> versus Junction Temperature  $T_J$**



**Load Regulation versus Junction Temperature  $T_J$**

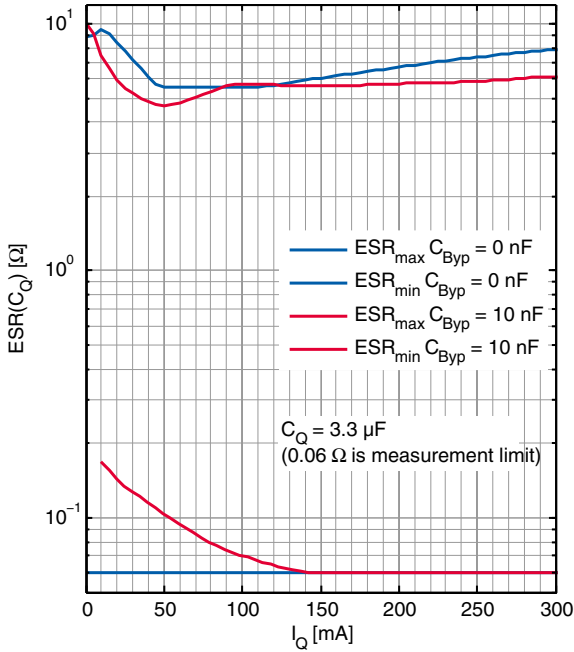


**Adjust Pin Bias Current versus Junction Temperature  $T_J$**

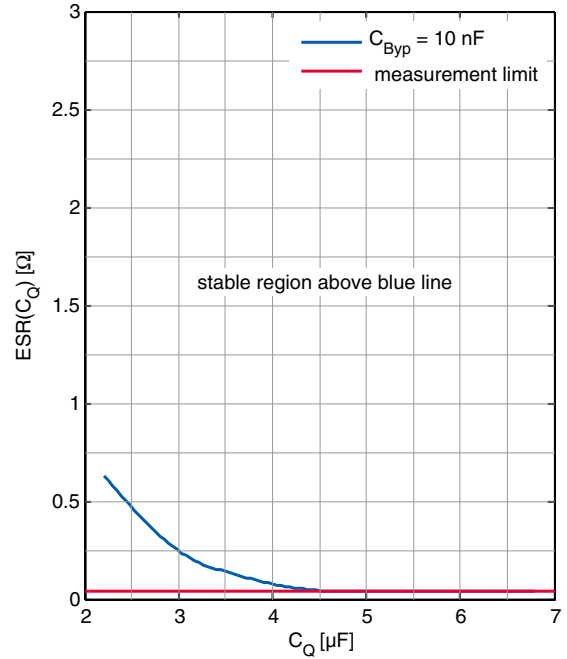


1)  $V_{I,min}$  is referred here as the minimum input voltage for which the requested current is provided and  $V_Q$  reaches 1 V.

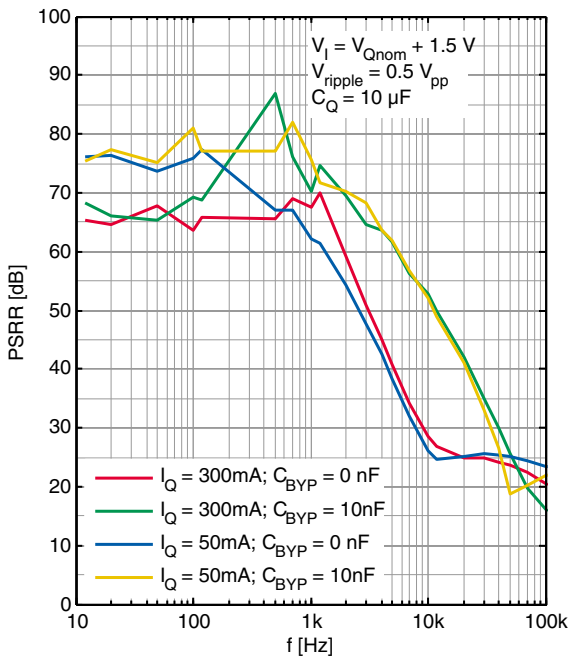
**ESR Stability versus Output Current  $I_Q$  (for  $C_Q = 3.3 \mu\text{F}$ )**



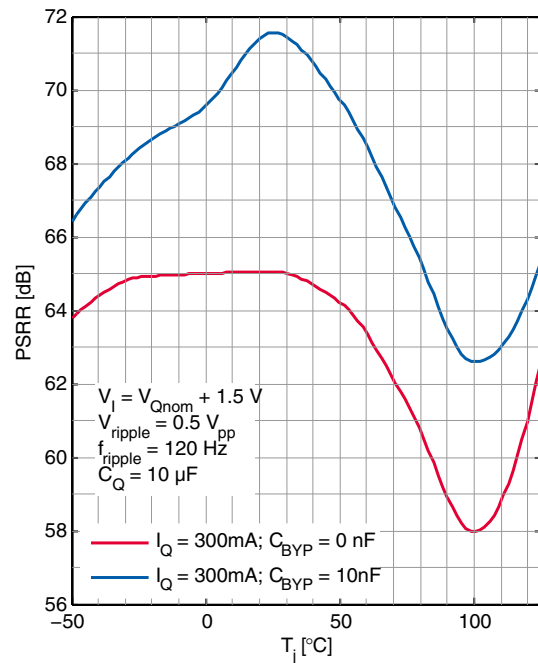
**ESR( $C_Q$ ) with  $C_{BYP} = 10 \text{ nF}$  versus Output Capacitance  $C_Q$**



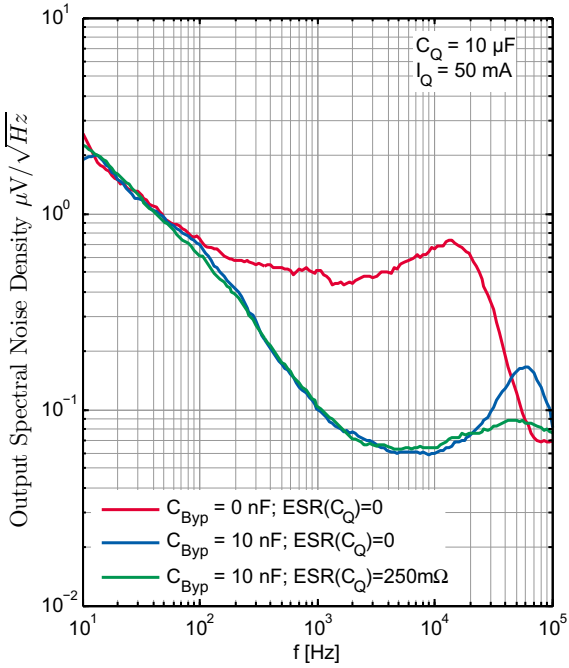
**Input Ripple Rejection PSRR versus Frequency  $f$**



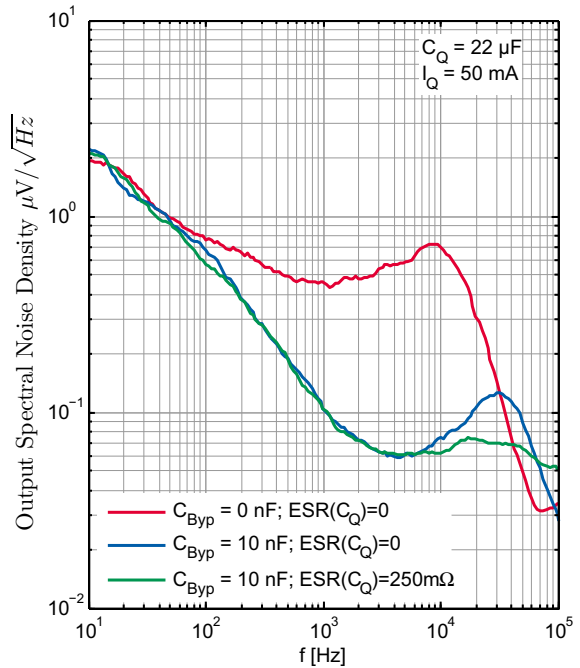
**Input Ripple Rejection PSRR versus Junction Temperature  $T_J$**



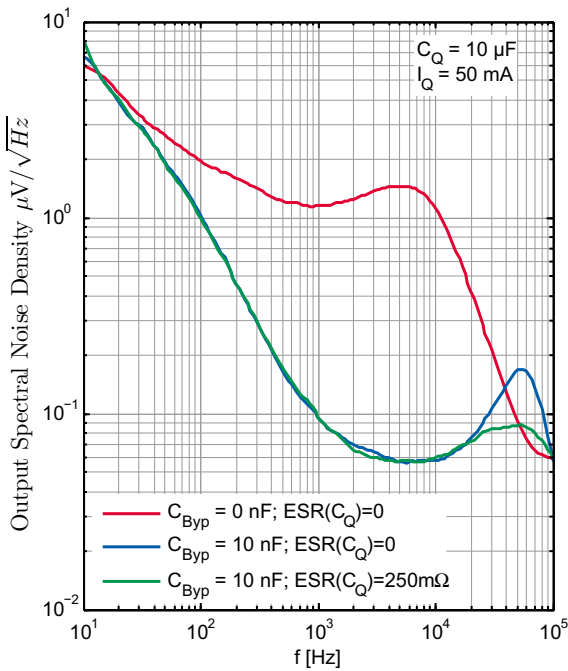
**Output Noise Spectral Density (ADJ) versus Frequency  $f$  ( $C_Q = 10 \mu\text{F}$ ,  $I_Q = 50 \text{ mA}$ )**



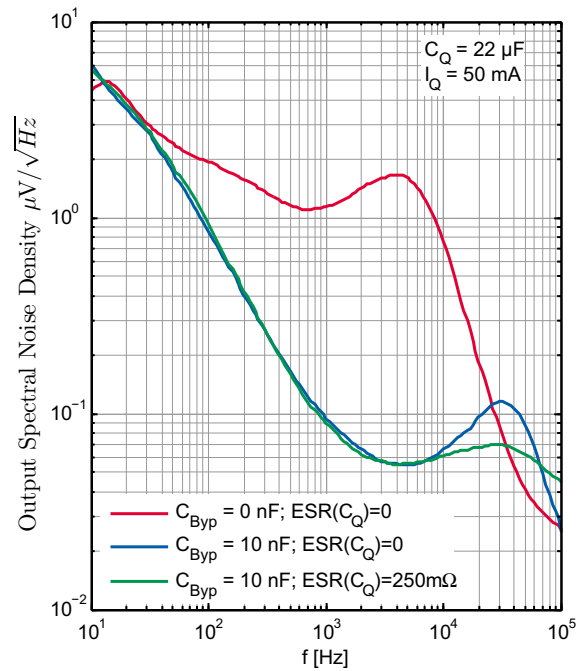
**Output Noise Spectral Density (ADJ) versus Frequency  $f$  ( $C_Q = 22 \mu\text{F}$ ,  $I_Q = 50 \text{ mA}$ )**



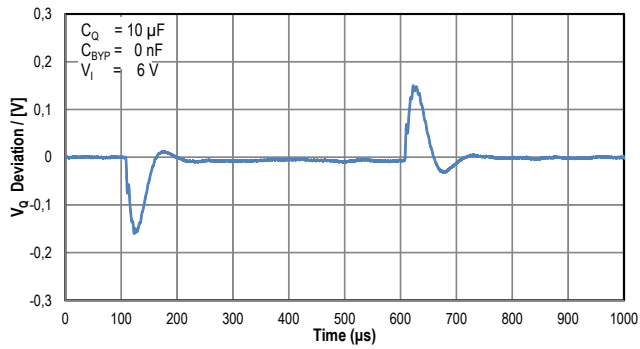
**Output Noise Spectral Density (3.3V) versus Frequency  $f$  ( $C_Q = 10 \mu\text{F}$ ,  $I_Q = 50 \text{ mA}$ )**



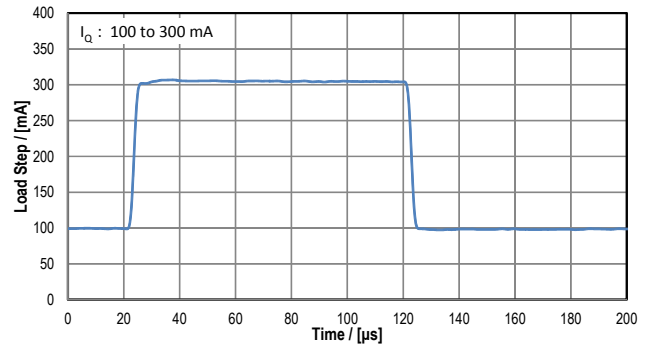
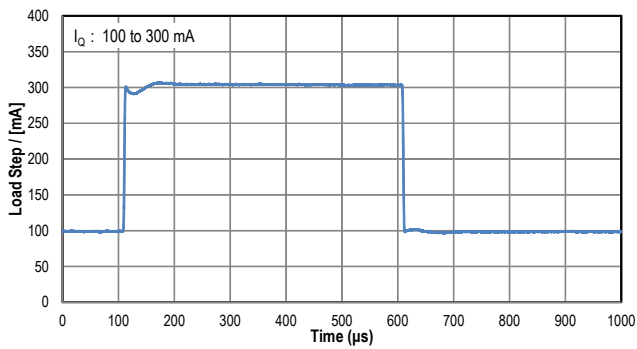
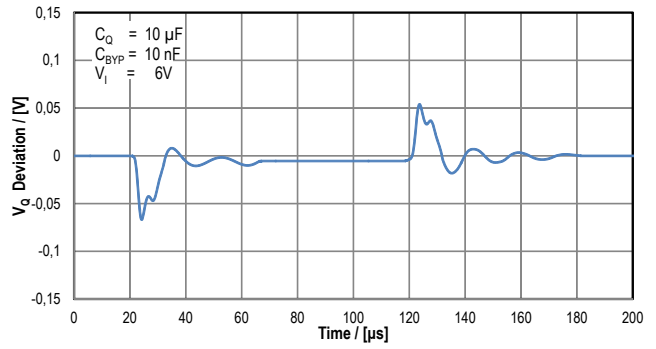
**Output Noise Spectral Density (3.3V) versus Frequency  $f$  ( $C_Q = 22 \mu\text{F}$ ,  $I_Q = 50 \text{ mA}$ )**



Transient Response  $C_{BYP} = 0$  nF (TLS203B0EJV33)



Transient Response  $C_{BYP} = 10$  nF (TLS203B0EJV33)





## 6 Application Information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

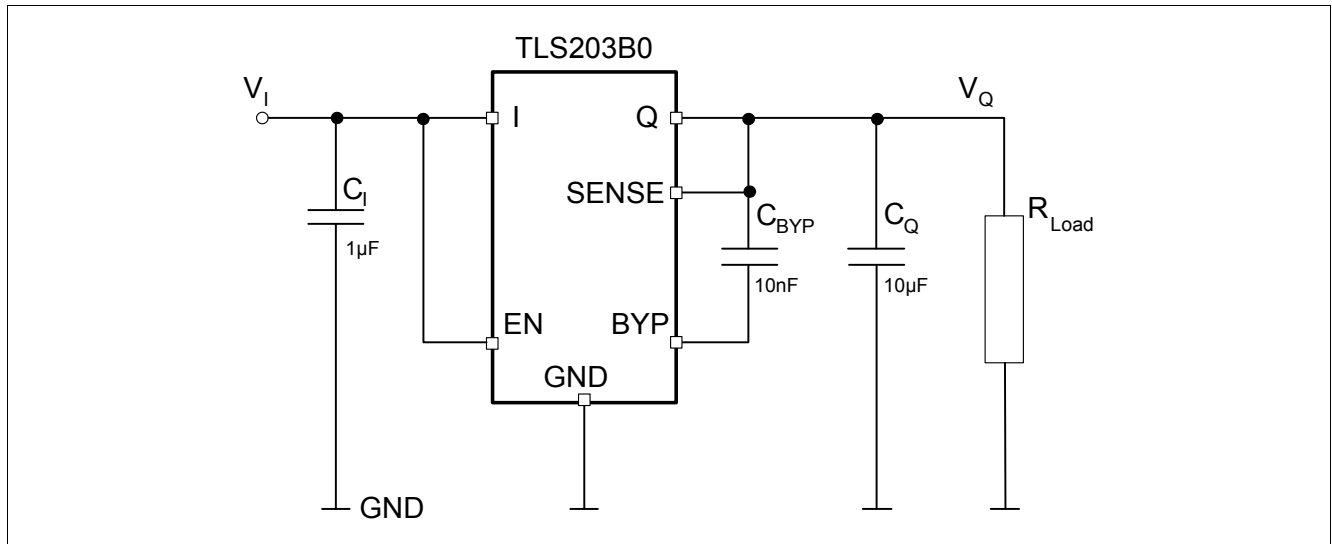


Figure 5 Typical Application Circuit TLS203B0 (fixed voltage version)

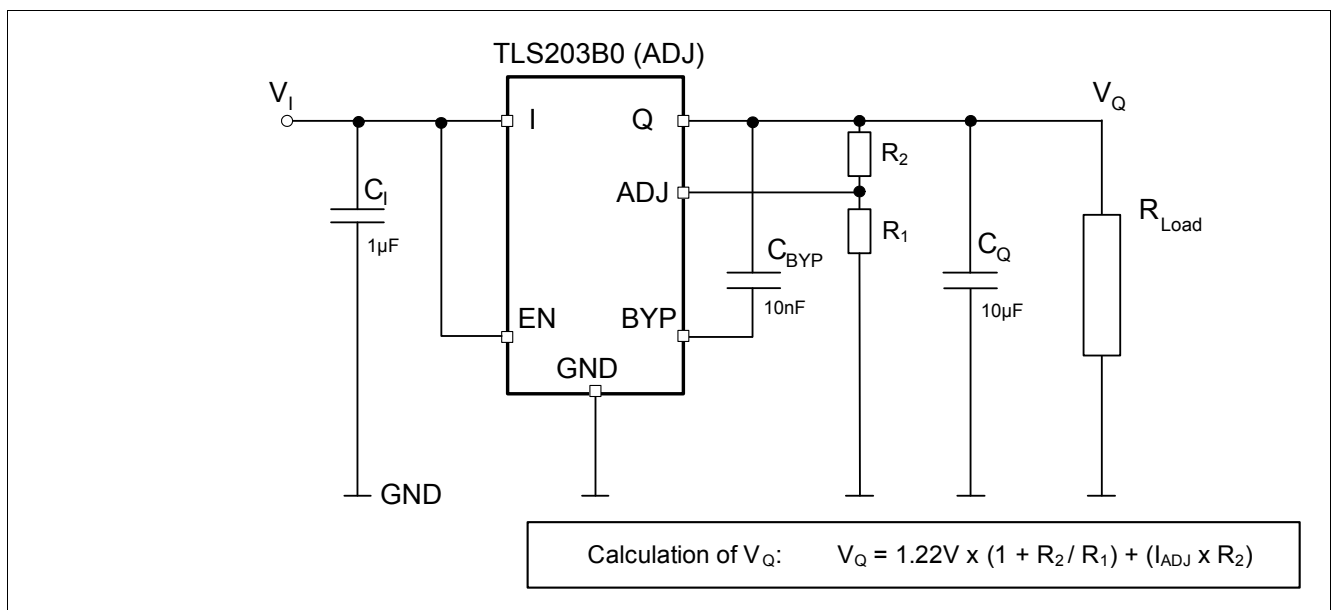


Figure 6 Typical Application Circuit TLS203B0 (adjustable version)

Note: This is a very simplified example of an application circuit. The function must be verified in the real application. <sup>1) 2)</sup>

- 1) Please note that in case a non-negligible inductance at the input pin I is present, e.g. due to long cables, traces, parasitics, etc, a bigger input capacitor  $C_I$  may be required to filter its influence. As a rule of thumb if the I pin is more than six inches away from the main input filter capacitor an input capacitor value of  $C_I = 10 \mu F$  is recommended.
- 2) For specific needs a small optional resistor may be placed in series to very low ESR output capacitors  $C_Q$  for enhanced noise performance (for details please see ["Bypass Capacitance and Low Noise Performance"](#) on Page 25).

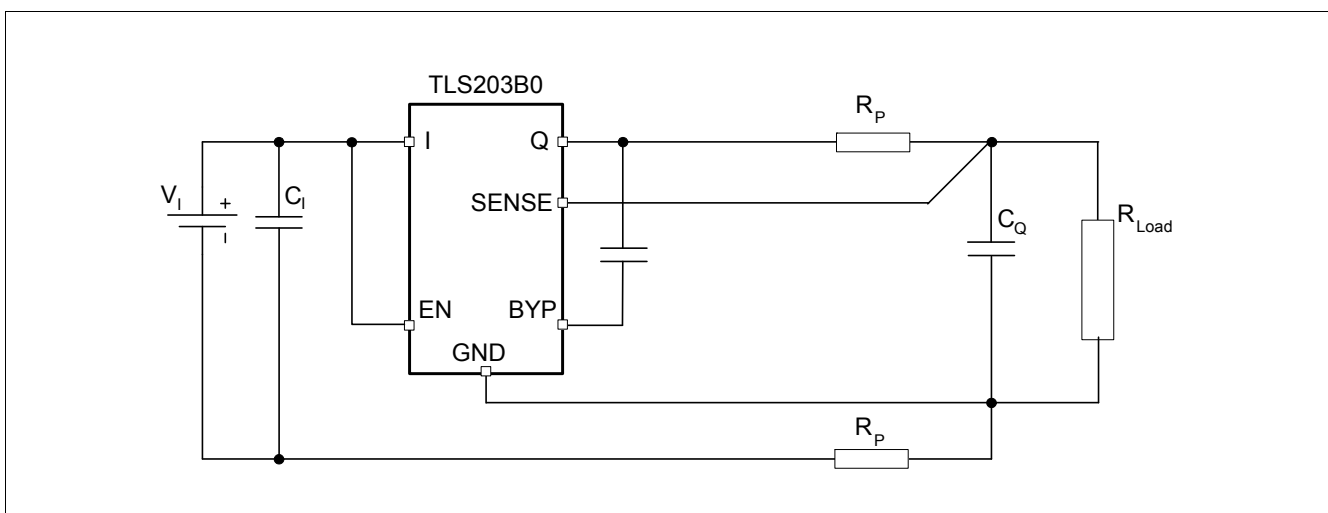
The TLS203B0 is a 300 mA low dropout regulator with very low quiescent current and Enable-functionality. The device is capable of supplying 300 mA at a dropout voltage of 270 mV. Output voltage noise numbers down to  $24 \mu V_{RMS}$  can be achieved over a 10 Hz to 100 kHz bandwidth with the addition of a 10 nF reference bypass capacitor. The usage of a reference bypass capacitor will additionally improve transient response of the regulator, lowering the settling time for transient load conditions. The device has a low operating quiescent current of typical 30  $\mu A$  that drops to less than 1  $\mu A$  in shutdown (EN-pin pulled to low level). The device also incorporates several protection features which makes it ideal for battery-powered systems. It is protected against both reverse input and reverse output voltages.

## 6.1 Adjustable Operation

The adjustable version of the TLS203B0 has an output voltage range of 1.22 V to  $20 V - V_{DR}$ . The output voltage is set by the ratio of two external resistors, as it can be seen in [Figure 6](#). The device controls the output to maintain the ADJ pin at 1.22 V referenced to ground. The current in R1 is then equal  $1.22 V / R1$  and the current in R2 equals the current in R1 plus the ADJ pin bias current. The ADJ pin bias current, which is  $\sim 60 \text{ nA}$  @ 25 °C, flows through R2 into the ADJ pin. The value of R1 should be not greater than 250 k $\Omega$  in order to minimize errors in the output voltage caused by the ADJ pin bias current. Note that when the device is shutdown (i.e. low level applied to EN pin) the output is turned off and consequently the divider current will be zero. For details of the ADJ Pin Bias current see also the corresponding typical performance graph “[Adjust Pin Bias Current versus Junction Temperature T<sub>J</sub>](#)” on [Page 20](#).

## 6.2 Kelvin Sense Connection

For the fixed voltage version of the TLS203B0 the SENSE pin is the input to the error amplifier. An optimum regulation will be obtained at the point where the SENSE pin is connected to the output pin Q of the regulator. In critical applications however small voltage drops may be caused by the resistance  $R_p$  of the PC-traces and thus may lower the resulting voltage at the load. This effect may be eliminated by connecting the SENSE pin to the output as close as possible at the load (see [Figure 7](#)). Please note that the voltage drop across the external PC trace will add up to the dropout voltage of the regulator.



**Figure 7 Kelvin Sense Connection**

## 6.3 Bypass Capacitance and Low Noise Performance

The TLS203B0 regulator may be used in combination with a bypass capacitor connecting the output pin Q to the BYP pin in order to minimize output voltage noise <sup>1)</sup>. This capacitor will bypass the reference of the regulator,

1) a good quality low leakage capacitor is recommended.