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TLS208D1

Linear Voltage Post Regulator

TLS208D1EJV
TLS208D1EJV33
TLS208D1LDV
TLS208D1LDV33

Data Sheet

Rev. 1.0, 2015-02-26

Automotive Power

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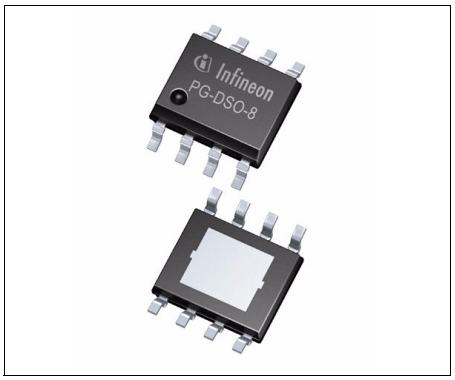
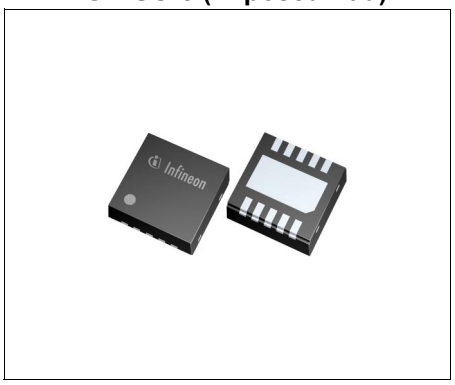
1 Overview



PG-DSO-8 (Exposed Pad)



PG-TSON10

Features

- 3.3 V Fixed and Adjustable Output Voltage from 0.8 V to 5.25 V
- Output Voltage Accuracy of ± 2 %
- Static Output Currents up to 800 mA
- Enable Functionality
- Undervoltage Reset with Power-On Reset Delay
- Adjustable Reset Threshold
- Extended Input Voltage Operating Range of 2.7 V to 18 V
- Low Dropout Voltage: typ. 400mV at 400mA
- Very Low Current Consumption: typ. 90 µA
- Very High PSRR: typ. 62dB at 10kHz
- Output Current Limitation
- Overtemperature Shutdown
- Wide Temperature Range From -40 °C up to 150 °C
- Suitable for Use in Automotive Electronics as Post Regulator
- Green Product (RoHS compliant)
- AEC Qualified

Description

The TLS208D1 is a monolithic integrated linear voltage post regulator. The IC regulates an input voltage V_I in the range of 2.7 V ≤ V_I ≤ 18 V to an adjustable output voltage of 0.8 V to 5.25 V or to a fixed output voltage with a precision of ±2 %. The TLS208D1 is especially designed for applications with a permanent connection to preregulators like DCDC converters. The device is available in the small surface mounted PG-DSO-8 (Exposed Pad) package. In addition to the enable functionality, the feature set includes a reset with an adjustable reset threshold. This threshold can be modified by an external resistor divider. The device is designed for the harsh environment of automotive applications. Therefore it is protected against overload, short circuit and overtemperature conditions by the implemented output current limitation and the overtemperature shutdown circuit. The TLS208D1 can be also used in all other applications requiring a stabilized voltage of 0.8 V to 5.25 V.

The input capacitor C_I is recommended for compensating line influences. The output capacitor C_Q is necessary for the stability of the regulating circuit. Stability is guaranteed at values specified in **“Functional Range” on Page 8** within the whole operating temperature range.

Type	Package	Marking
TLS208D1EJV	PG-DSO-8 (Exposed Pad)	208D1V
TLS208D1EJV33	PG-DSO-8 (Exposed Pad)	208D1V33
TLS208D1LDV	PG-TSON10	208DV
TLS208D1LDV33	PG-TSON10	208DV33

2 Block Diagram

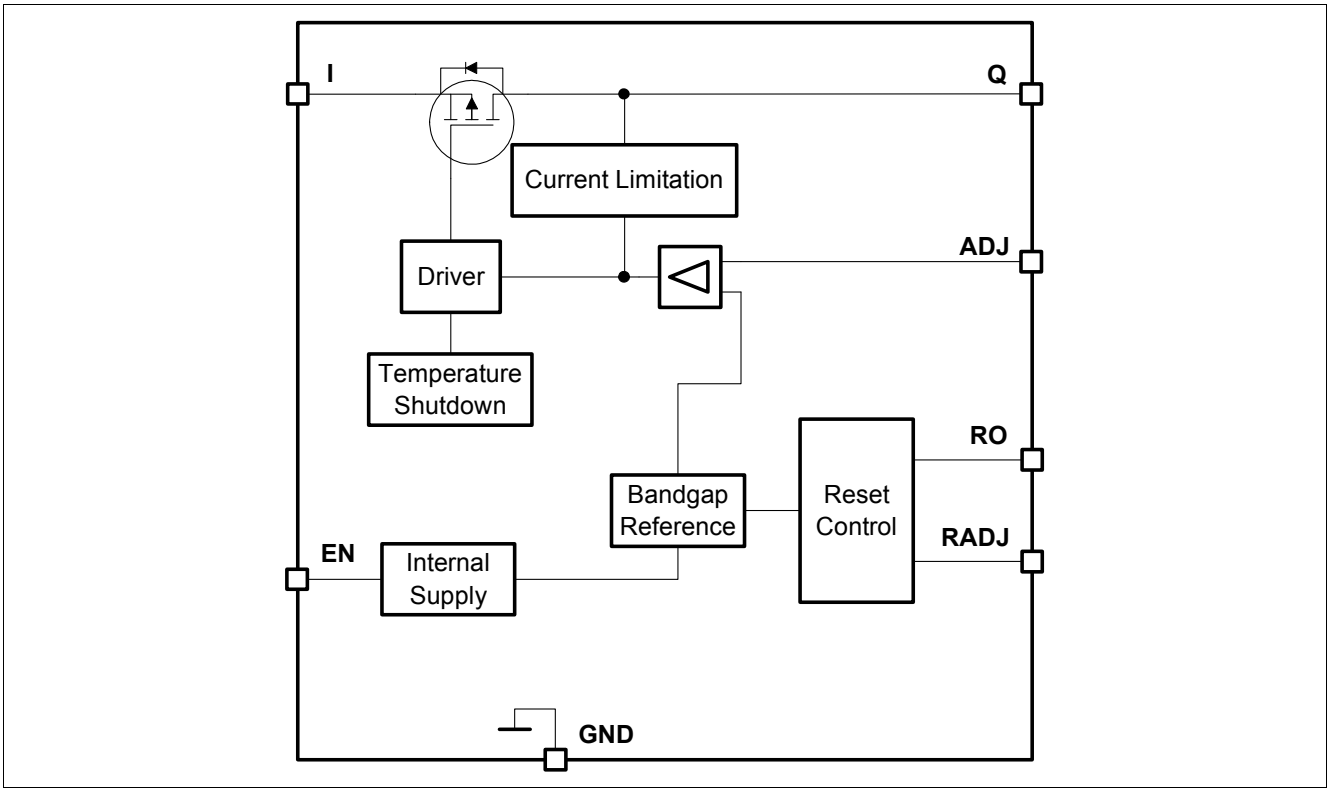


Figure 1 Block Diagram Adjustable Version (e.g. TLS208D1EJV)

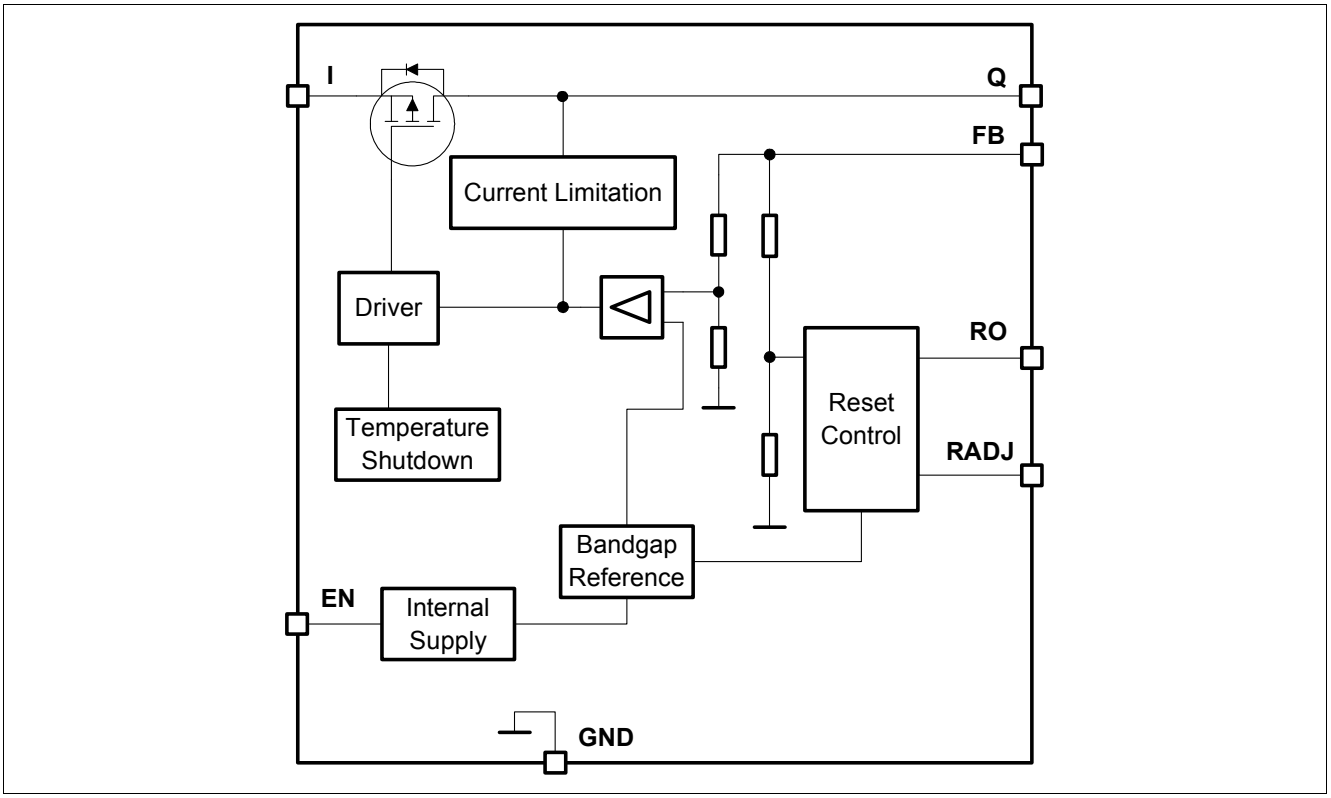


Figure 2 Block Diagram Fixed Voltage Version (e.g. TLS208D1EJV33)

3 Pin Configuration

3.1 Pin Assignment PG-DSO-8 (Exposed Pad)

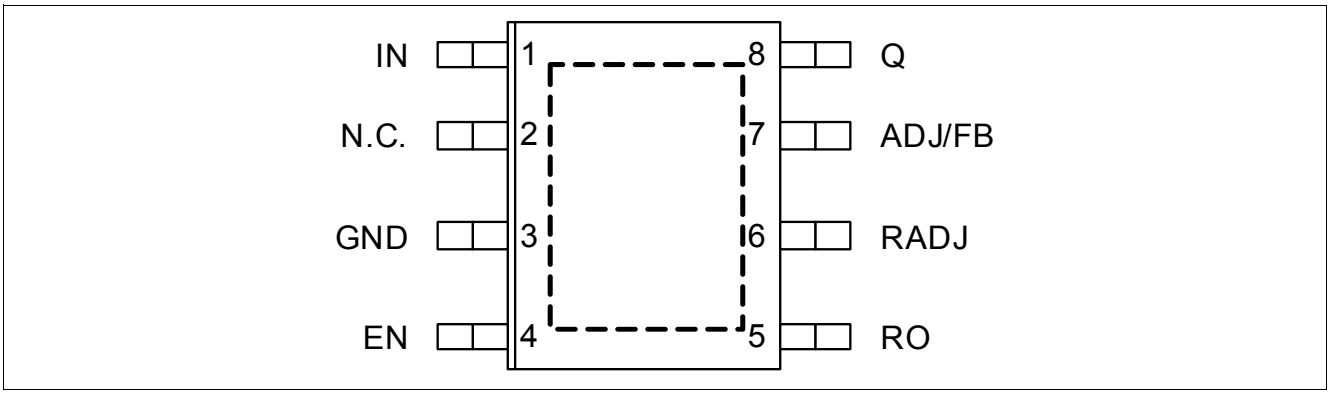


Figure 3 Pin Configuration Package PG-DSO-8 (Exposed Pad)

3.2 Pin Definitions and Functions PG-DSO-8 (Exposed Pad)

Pin	Symbol	Function
1	I	**Input.** IC supply. For compensating line influences, a capacitor of 220 nF close to the IC pins is recommended.
2	N.C	**Not Connected.**
3	GND	**Ground Reference.** Connect this pin low ohmic to GND.
4	EN	**Enable.** A low signal disables the IC. A high signal switches it on. Connect to the input I, if the enable functionality is not required.
5	RO	**Reset Output** The open collector output can be connected to a microcontroller using a external pull up resistor. If the functionality is not required, the pin can be left open.
6	RADJ	**Reset Adjust.** For reset threshold adjustment connect to a voltage divider from output Q to GND. (**“Description Reset Function” on Page 20**)
7	ADJ FB	**Adjust. (Only Adjustable Version TLS208D1EJV)** The reference voltage can be connected to the output pin directly or by a voltage divider for higher output voltages (see application information). **Feedback. (Only Fixed Voltage Versions e.g. TLS208D1EJV33)** The Feedback pin has to be connected to the output voltage.
8	Q	**Output.** Block to GND with a capacitor close to the IC terminals, respecting capacitance and ESR requirements given in the table **“Functional Range” on Page 8**.
Pad	EP	**Exposed Pad.** Connect to PCB heat sink area and GND.

3.3 Pin Assignment PG-TSON10

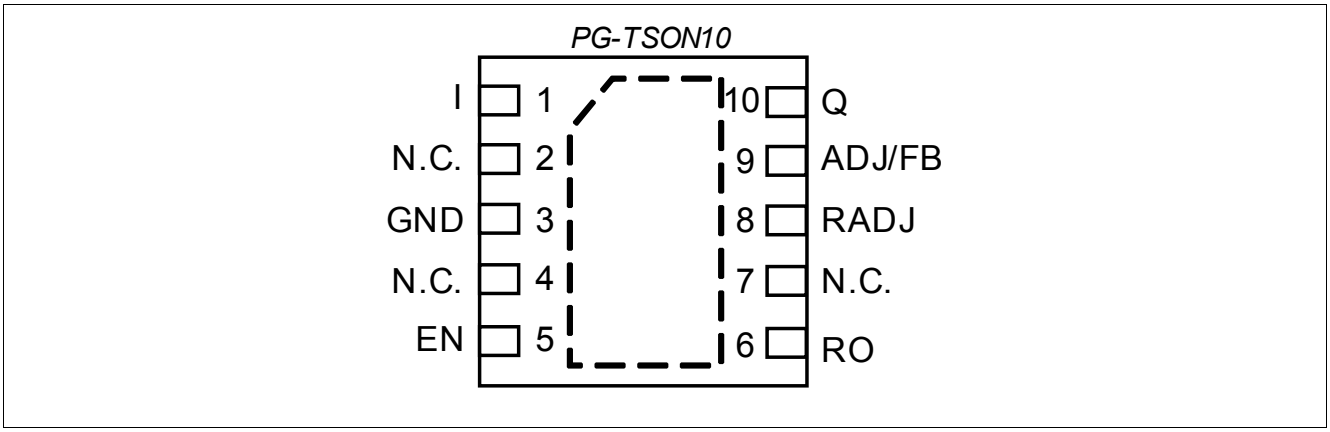


Figure 4 Pin Configuration Package PG-TSON10

3.4 Pin Definitions and Functions PG-TSON10

Pin	Symbol	Function
1	I	**Input.** IC supply. For compensating line influences, a capacitor of 220 nF close to the IC pins is recommended.
2	N.C	**Not Connected.**
3	GND	**Ground Reference.** Connect this pin low ohmic to GND.
4	N.C	**Not Connected.**
5	EN	**Enable.** A low signal disables the IC. A high signal switches it on. Connect to the input I, if the enable functionality is not required.
6	RO	**Reset Output** The open collector output can be connected to a microcontroller using a external pull up resistor. If the functionality is not required, the pin can be left open.
7	N.C	**Not Connected.**
8	RADJ	**Reset Adjust.** For reset threshold adjustment connect to a voltage divider from output Q to GND. (**“Description Reset Function” on Page 20**)
9	ADJ FB	**Adjust. (Only Adjustable Version TLS208D1LDV)** The reference voltage can be connected to the output pin directly or by a voltage divider for higher output voltages (see application information). **Feedback. (Only Fixed Voltage Versions e.g. TLS208D1LDV33)** The Feedback pin has to be connected to the output voltage.
10	Q	**Output.** Block to GND with a capacitor close to the IC terminals, respecting capacitance and ESR requirements given in the table **“Functional Range” on Page 8**.
Pad	EP	**Exposed Pad.** Connect to PCB heat sink area and GND.

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Table 1 Absolute Maximum Ratings [1] T_j = -40 °C to +150 °C; all voltages with respect to ground, (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Input I							
Voltage	V_I	-0.3	–	20	V	–	P_4.1.1
Output Q							
Voltage	V_Q	-0.3	–	5.5	V	–	P_4.1.2
Adjust ADJ							
Voltage	V_{ADJ}	-0.3	–	5.5	V	–	P_4.1.3
Feedback FB							
Voltage	V_{FB}	-0.3	–	5.5	V	–	P_4.1.4
Enable EN							
Voltage	V_{EN}	-0.3	–	20	V	–	P_4.1.5
Reset Output							
Voltage	V_{RO}	-0.3	–	5.5	V	–	P_4.1.6
Reset Adjust							
Voltage	V_{RADJ}	-0.3	–	5.5	V	–	P_4.1.7
Temperature							
Junction temperature	T_j	-40	–	150	°C	–	P_4.1.8
Storage temperature	T_{stg}	-50	–	150	°C	–	P_4.1.9
ESD Susceptibility							
ESD Absorption	$V_{ESD,HBM}$	-2	–	2	kV	Human Body Model (HBM) [2]	P_4.1.10
ESD Absorption	$V_{ESD,CDM}$	-750	–	750	V	Charge Device Model (CDM) [3]	P_4.1.11

1) not subject to production test, specified by design

2) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS001 (1.5 kΩ, 100 pF)

3) ESD susceptibility, Charged Device Model “CDM” ESDA STM5.3.1 or ANSI/ESD S.5.3.1

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.*

4.2 Functional Range

Table 2 Functional Range

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Input voltage	V_I	2.7	–	18	V	–	P_4.2.1
Output Capacitor Requirements for Stability	C_Q	1	–	–	µF	1)–	P_4.2.2
Output Capacitor Requirements for Stability	$ESR(C_Q)$	–	–	10	Ω	2)	P_4.2.3
Junction temperature	T_j	-40	–	150	°C	–	P_4.2.4

1) The minimum output capacitance requirement is applicable for a worst case capacitance tolerance of 30%

2) relevant ESR value at f = 10 kHz

Note: Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the Electrical Characteristics table.

4.3 Thermal Resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to **www.jedec.org**.*

Table 3 Thermal Resistance

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
PG-DSO-8 (Exposed Pad)							
Junction to Ambient 1)	R_{thJA}	–	42	–	K/W	2s2p board 2)	P_4.3.1
Junction to Ambient	R_{thJA}	–	150	–	K/W	Footprint only 3)	P_4.3.2
Junction to Ambient	R_{thJA}	–	66	–	K/W	300 mm² PCB heatsink area 3)	P_4.3.3
Junction to Ambient	R_{thJA}	–	55	–	K/W	600 mm² PCB heatsink area 3)	P_4.3.4
Junction to Case	R_{thJC}	–	9.5	–	K/W		P_4.3.5
PG-TSON10							
Junction to Ambient 1)	R_{thJA}	–	57	–	K/W	2s2p board 2)	P_4.3.6
Junction to Ambient	R_{thJA}	–	176	–	K/W	Footprint only 3)	P_4.3.7
Junction to Ambient	R_{thJA}	–	70	–	K/W	300 mm² PCB heatsink area 3)	P_4.3.8
Junction to Ambient	R_{thJA}	–	59	–	K/W	600 mm² PCB heatsink area 3)	P_4.3.9
Junction to Case	R_{thJC}	–	9	–	K/W		P_4.3.10

1) Not subject to production test, specified by design.

2) Specified R_{thJA} value is according to JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The product (chip+package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layer (2 x 70µm Cu, 2 x 35µm Cu). Where applicable a thermal via array under the exposed pad contacted to the first inner copper layer.

3) Package mounted on PCB FR4; 80 x 80 x 1.5 mm; 35 µm Cu, 5 µm Sn; horizontal position; zero airflow.

5 Voltage Regulator

5.1 Description Voltage Regulator

The output voltage V_Q is controlled as follows: it is divided by the resistor divider. This fraction is then compared to an internal reference and drives the pass transistor accordingly.

By connecting the ADJ pin directly to the output Q the device will regulate to its reference voltage. In this case a minimum load resistance of less than 300 kΩ needs to be ensured for stability reasons.

The control loop stability depends on the output capacitor C_Q, the load current, the chip temperature and the circuit design. To ensure stable operation, the requirements for output capacitance and equivalent series resistance ESR, given in the **“Functional Range” on Page 8**, have to be maintained. For details see also the typical stability graph of ESR versus load current on **Page 17**. As the output capacitor also has to buffer load steps it should be sized according to the needs of the application.

An input capacitor C_I of at least 220 nF is recommended to compensate line influences. Connect the capacitors close to the terminals of the component.

In case the load current is above the specified limit, e.g. in case of a short circuit, the output current limitation limits the current. The output voltage is therefore decreasing at the same time.

The overtemperature shutdown circuit prevents the IC from immediate destruction under fault conditions (e.g. output continuously short-circuited) by switching off the power stage. After the chip has cooled down, the regulator restarts. This leads to an oscillatory behavior of the output voltage until the fault is removed. However, junction temperatures above 150 °C are outside the maximum ratings and therefore significantly reduce the IC’s lifetime.

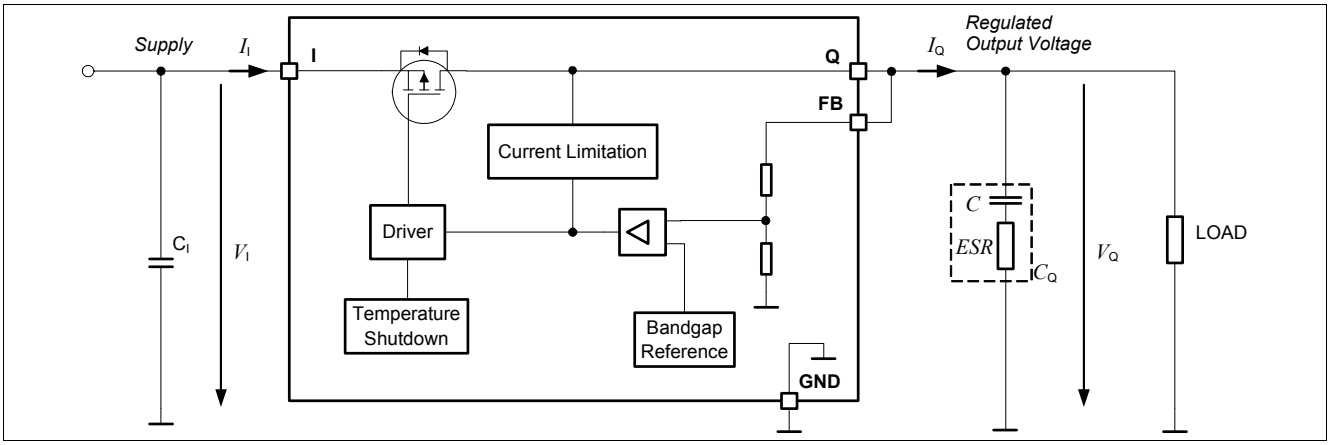


Figure 5 Block Diagram Voltage Regulator Circuit (Fixed Voltage Variant e.g. TLS208D1EJV33)

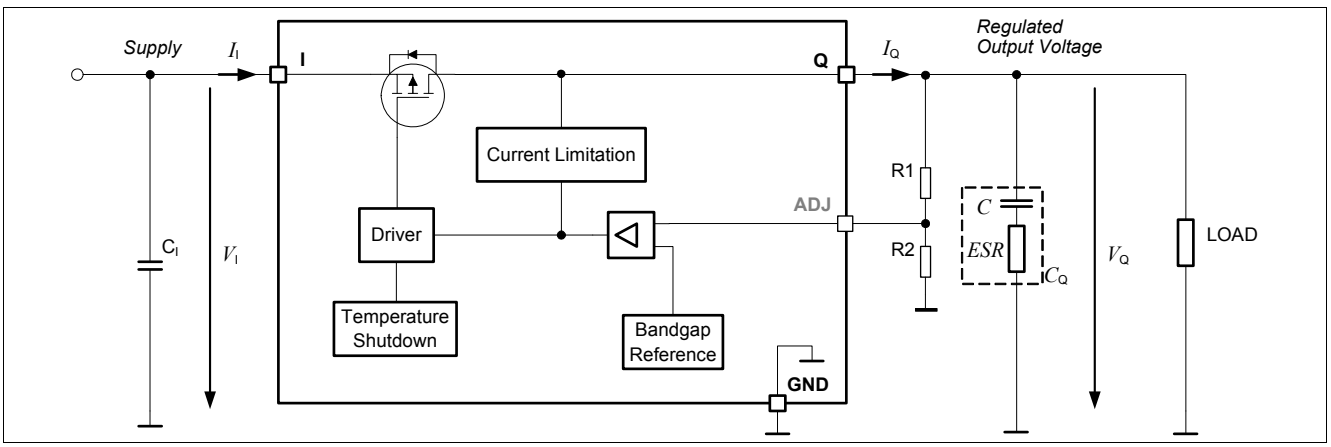


Figure 6 Block Diagram Voltage Regulator Circuit (Adjustable Voltage Variant e.g. TLS208D1EJV)

5.2 Electrical Characteristics Voltage Regulator

Table 4 Electrical Characteristics V_I = $V_{Q,nom}$ + 1 V and V_I ≥ 2.7 V; T_j = -40 °C to +150 °C; all voltages with respect to ground (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Characteristic Adjustable Output Voltage (TLS208D1EJV, TLS208D1LDV)							
Reference Voltage	V_{ref}	–	0.8	–	V		P_5.2.1
Output Voltage [1] TLS208D1EJV TLS208D1LDV	V_Q	-1%	$V_{Q,nom}$	+1%	V	I_Q = 100 mA ; T_j = 25 °C	P_5.2.2
Output Voltage [1] TLS208D1EJV TLS208D1LDV	V_Q	-2%	$V_{Q,nom}$	+2%	V	I_Q = 100 mA ;	P_5.2.3
Adjustable Voltage Range [2] TLS208D1EJV TLS208D1LDV	V_Q	0.8	–	5.25	V		P_5.2.4
Load Regulation TLS208D1EJV TLS208D1LDV	$\Delta V_{Q,load}$ / $V_{Q,nom}$	–	5	10	mV/V	I_Q = 100 mA to 1 mA ; $V_I \geq V_{Q,nom} + V_{dr,max}$ + 100 mV [3] [4]	P_5.2.5
Load Regulation TLS208D1EJV TLS208D1LDV	$\Delta V_{Q,load}$ / $V_{Q,nom}$	-10	-5	–	mV/V	I_Q = 100 mA to 800 mA ; $V_I \geq V_{Q,nom} + V_{dr,max}$ + 100 mV and $V_I \geq$ 3.8 V [3] [4]	P_5.2.6
Line Regulation TLS208D1EJV TLS208D1LDV	($\Delta V_{Q,line}$ / $V_{Q,nom}$) / ΔV_I	–	0.01	0.2	%/V	V_I = ($V_{Q,nom}$ + 1 V) to 10 V ; $V_I \geq$ 2.7 V ; I_Q = 1 mA [4]	P_5.2.7
Characteristic Fixed Output Voltage (TLS208D1EJV33, TLS208D1LDV33)							
Output Voltage TLS208D1EJV33 TLS208D1LDV33	V_Q	3.267	3.3	3.333	V	I_Q = 100 mA ; T_j = 25 °C	P_5.2.8
Output Voltage TLS208D1EJV33 TLS208D1LDV33	V_Q	3.234	3.3	3.366	V	1 mA ≤ I_Q ≤ 800 mA	P_5.2.9
Load Regulation TLS208D1EJV33 TLS208D1LDV33	$\Delta V_{Q,load}$	–	16	33	mV	I_Q = 100 mA to 1 mA ; $V_I \geq$ 4.4 V [3]	P_5.2.10
Load Regulation TLS208D1EJV33 TLS208D1LDV33	$\Delta V_{Q,load}$	-33	-16	–	mV	I_Q = 100 mA to 800 mA ; $V_I \geq$ 4.4 V [3]	P_5.2.11
Line Regulation TLS208D1EJV33 TLS208D1LDV33	$\Delta V_{Q,line}$	–	1.88	37.6	mV	V_I = 4.3V to 10 V ; I_Q = 1 mA	P_5.2.12
Dropoutvoltage Characteristic							
Dropout Voltage [5]	V_{dr}	–	0.9	1.0	V	$V_Q \geq$ 3.3 V ; I_Q = 800 mA	P_5.2.13
Dropout Voltage [5]	V_{dr}	–	0.45	0.54	V	$V_Q \geq$ 3.3 V ; I_Q = 400 mA	P_5.2.14
Dropout Voltage [5]	V_{dr}	–	1.0	1.2	V	$V_Q \geq$ 2.5 V ; I_Q = 800 mA	P_5.2.15
Dropout Voltage [5]	V_{dr}	–	0.5	0.68	V	$V_Q \geq$ 2.5 V ; I_Q = 400 mA	P_5.2.16

Table 4 Electrical Characteristics $V_I = V_{Q,nom}$ + 1 V and $V_I \geq$ 2.7 V; T_j = -40 °C to +150 °C; all voltages with respect to ground (unless otherwise specified) (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Dropout Voltage [5]	V_{dr}	–	1.19	1.35	V	$V_Q \geq$ 1.8 V ; I_Q = 700 mA	P_5.2.17
Dropout Voltage [5]	V_{dr}	–	0.65	0.96	V	$V_Q \geq$ 1.8 V ; I_Q = 400 mA [6]	P_5.2.18
Dropout Voltage [5]	V_{dr}	–	1.59	1.85	V	$V_Q \geq$ 1.2 V ; I_Q = 700 mA	P_5.2.19
Power Supply Ripple Rejection [2]	$PSRR$	–	62	–	dB	f_f = 10 kHz ; I_Q = 200 mA ; T_j = 25 °C ; $V_{in} = V_Q$ + 1.5 V and $V_{in} \geq$ 3.2 V ; ΔV_I = 1 V_{pp} ; C_Q = 1 µF(Ceramic Capacitor)	P_5.2.20
Protection Features							
Output Current Limitation	I_Q	801	1150	1350	mA	0 V ≤ V_Q ≤ 0.9 * $V_{Q,nom}$	P_5.2.21
Overtemperature Shutdown Threshold [2]	$T_{j,sd}$	151	175	200	°C	T_j increasing	P_5.2.22
Overtemperature Shutdown Hysteresis [2]	$T_{j,sd,Hyst}$	–	15	–	°C	T_j decreasing	P_5.2.23
Adjust Pin Characteristic (TLS208D1EJV)							
Adjust Pin Pull Up Current [7]	I_{ADJ}	–	–	500	nA	–	P_5.2.24

1) Referring to the device tolerance only, the tolerance of the resistor divider can cause additional deviation. Parameter is tested with ADJ-Pin directly connected to the output Q.

2) This parameter is not subject to production test, specified by design

3) The input voltage condition is intended to ensure that the device is out of the drop condition.

4) Tested with ADJ-Pin directly connected to the output Q.

5) Dropout voltage is defined as the difference between input and output voltage when the output voltage decreases 100 mV from output voltage measured at $V_I = V_{Q,nom} + V_{dr,max}$ + 100 mV.

6) The dropout voltage might be limited to the minimum input voltage as defined in P_4.2.1 on Page 8

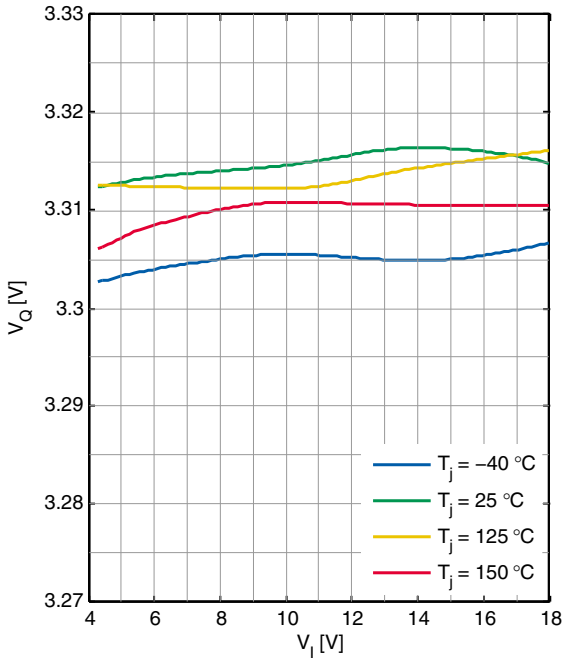
7) ADJ pin pull up current flows out of the ADJ pin.

5.3 Typical Performance Characteristics Voltage Regulator

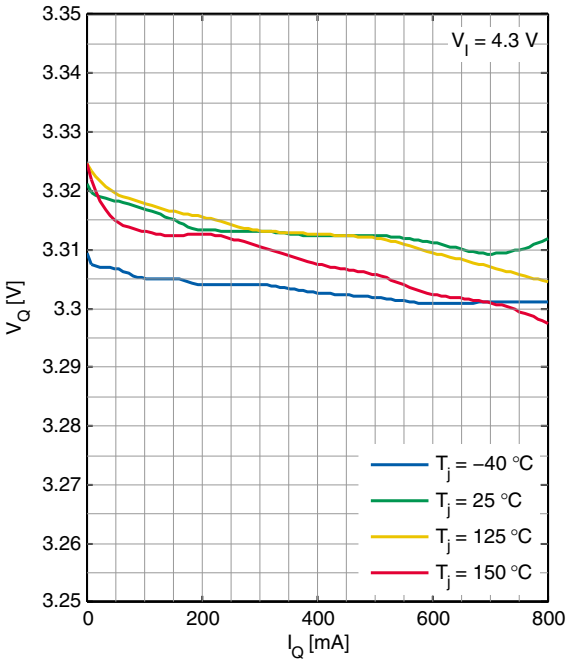
V_{EN} = 5 V (unless otherwise noted)

Typical Performance Characteristics

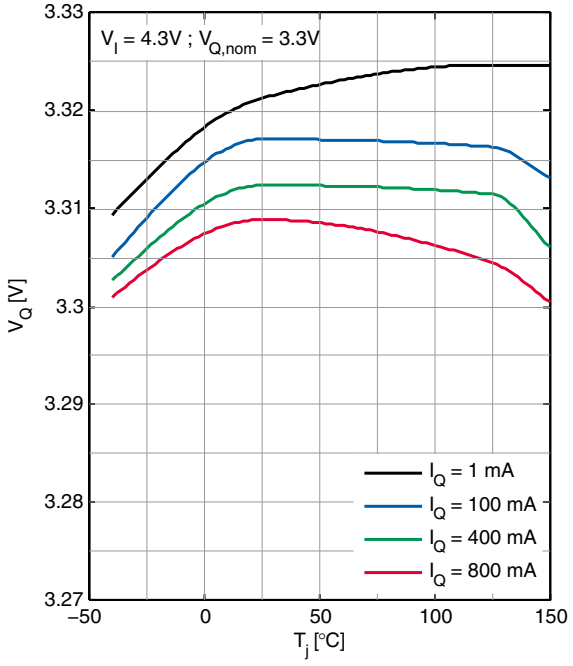
**Output Voltage V_Q vs.
Input Voltage V_I (Line Regulation)**



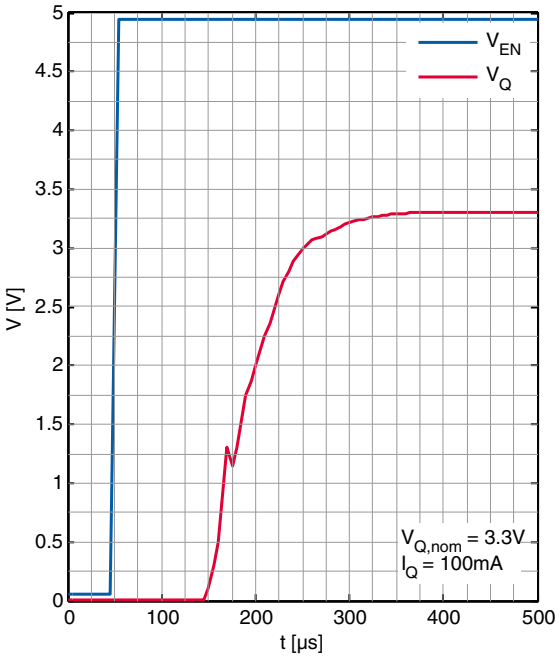
**Output Voltage V_Q vs.
Load Current I_Q (Load Regulation)**



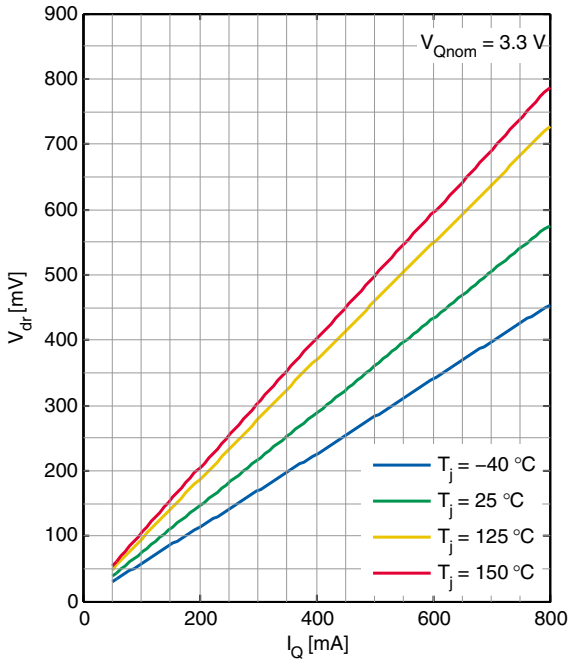
**Output Voltage V_Q vs.
Junction Temperature T_j**



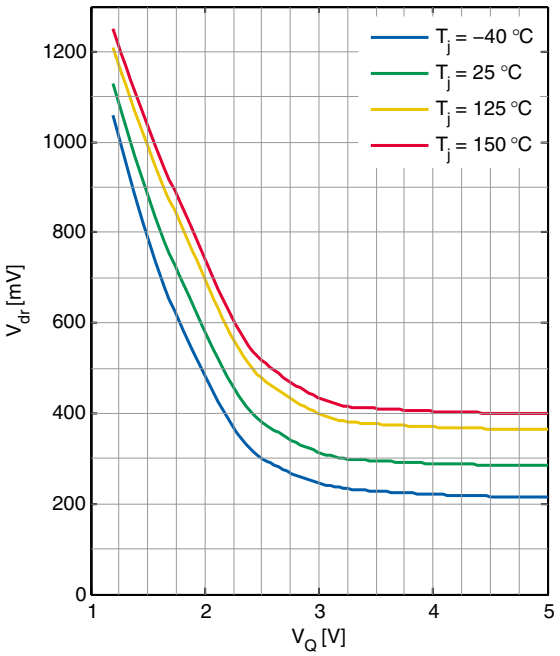
Power Up Timing V_Q



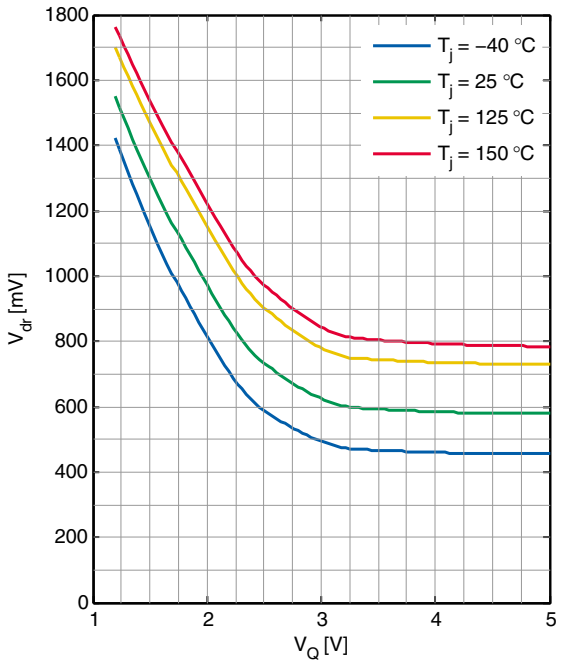
**Dropout Voltage V_{dr} vs.
Load Current I_Q ($V_{Q,nom}$ = 3.3V)**



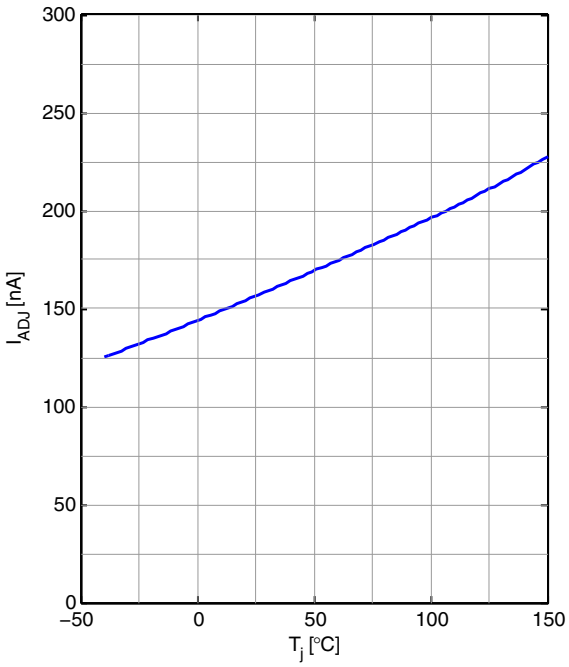
**Dropout Voltage V_{dr} vs.
Output Voltage V_Q (I_Q = 400 mA)**



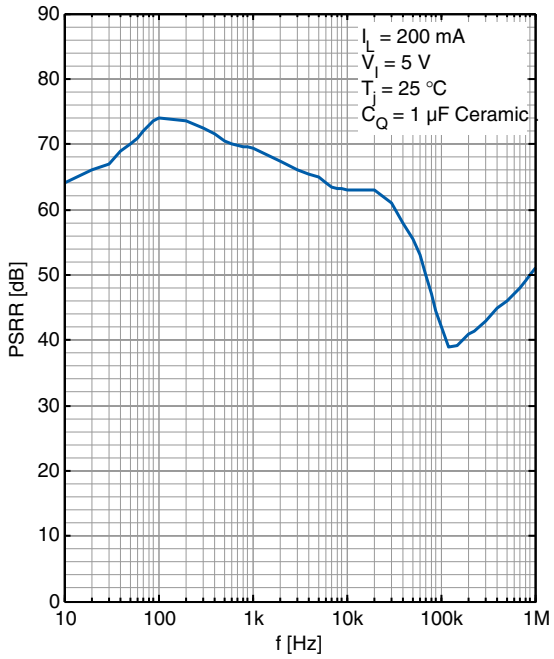
**Dropout Voltage V_{dr} vs.
Output Voltage V_Q (I_Q = 800 mA)**



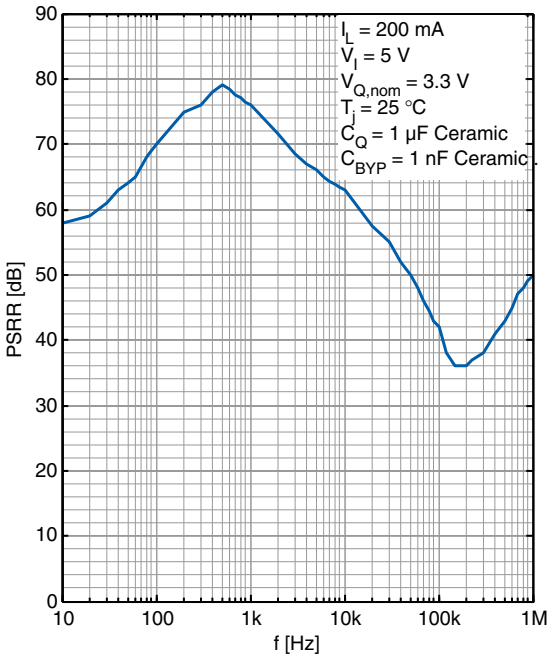
**Adjust Pin Current I_{ADJ} vs.
Junction Temperature T_j**



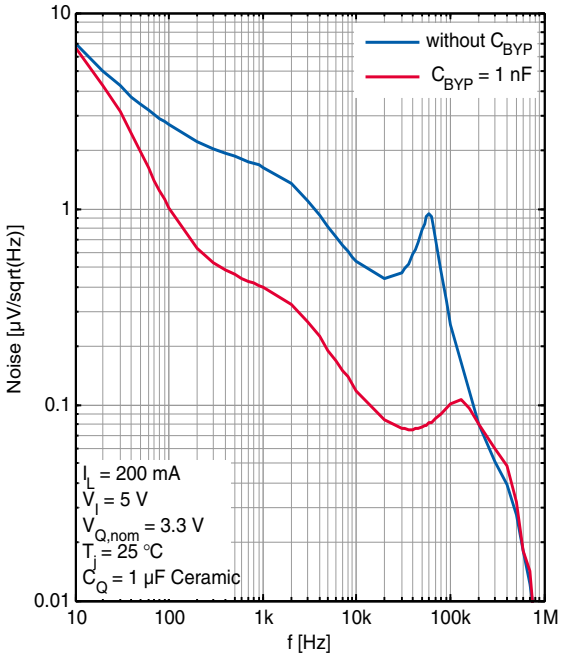
PSRR vs. Frequency TLS208D1xxV33



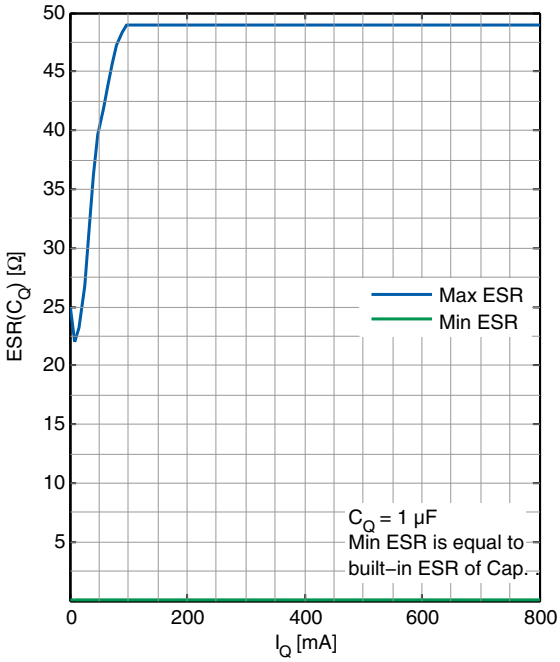
PSRR vs. Frequency TLS208D1xxV (adjusted to $V_{Q,nom}$ = 3.3 V)



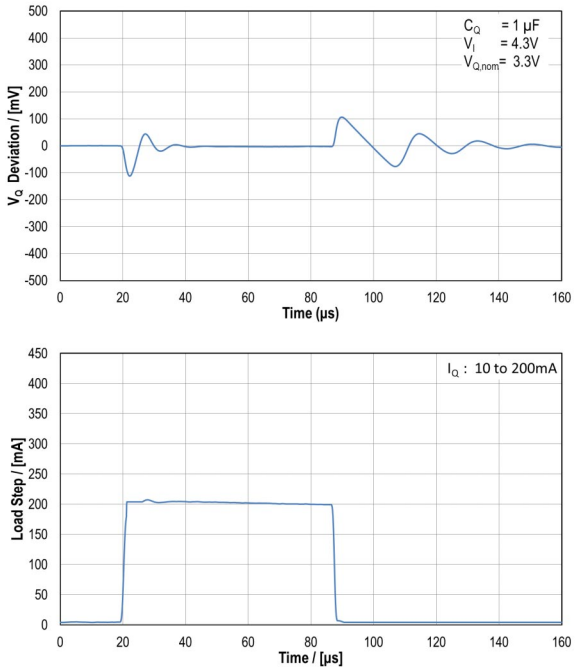
Noise Graph TLS208D1xxV (adjusted to $V_{Q,nom}$ = 3.3 V)



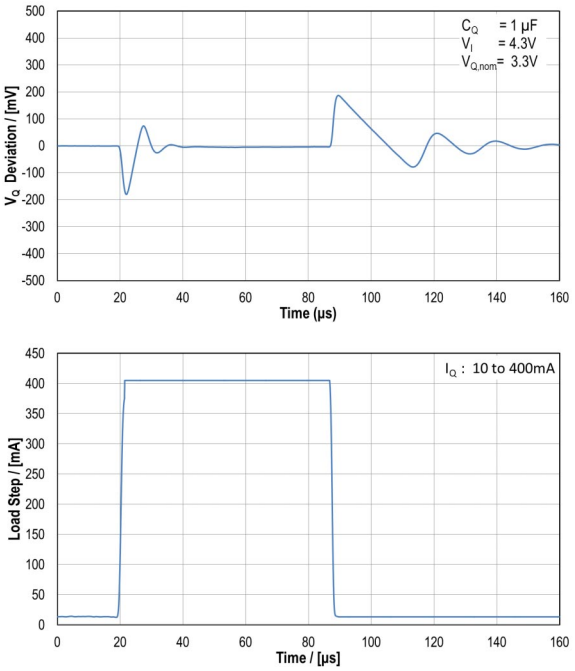
Output Capacitor Series Resistance ESR(C_Q) vs. Output Current I_Q (C_Q = 1 µF)



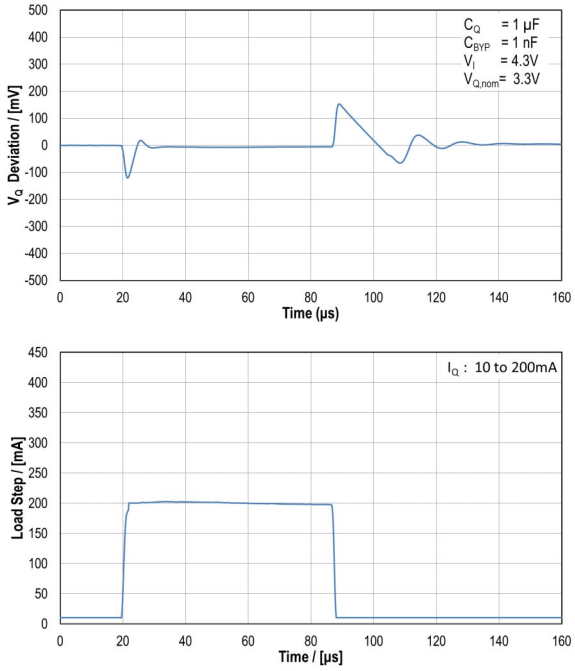
Dynamic Load Response TLS208D1xxV33 (10mA to 200mA)



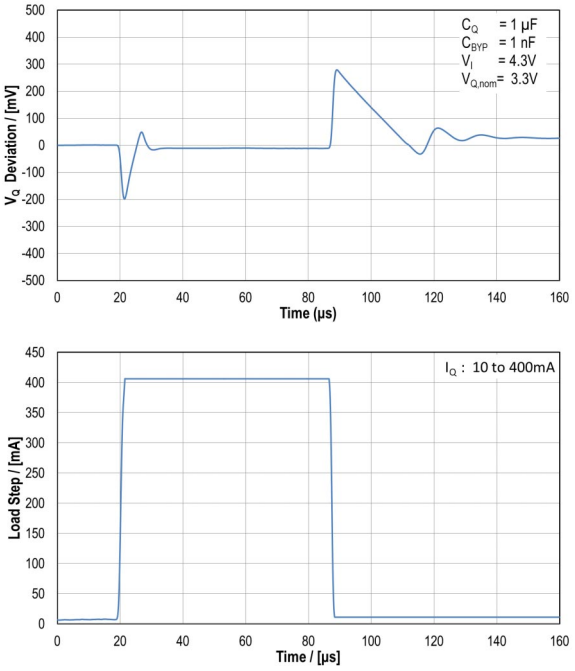
Dynamic Load Response TLS208D1xxV33 (10mA to 400mA)



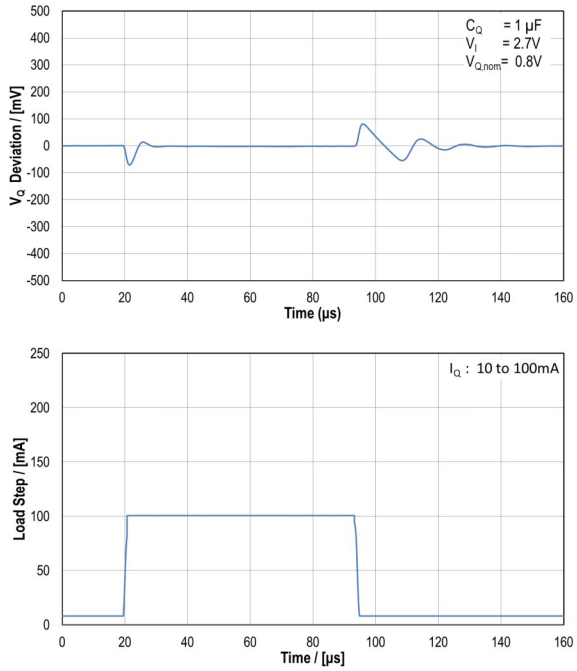
Dynamic Load Response TLS208D1xxV (adjusted to $V_{Q,nom}$ = 3.3 V) (10mA to 200mA)



Dynamic Load Response TLS208D1xxV (adjusted to $V_{Q,nom}$ = 3.3 V) (10mA to 400mA)



Dynamic Load Response TLS208D1xxV (adjusted to $V_{Q,nom}$ = 0.8 V) (10mA to 100mA)



6 Current Consumption

6.1 Description Current Consumption

The Current Consumption of the device is characterizing the current the device needs to operate. The Quiescent Current is describing the Current Consumption in a very low load condition (e.g. the supplied microcontroller is in sleep mode). The TLS208D1 has an Enable functionality to shutdown the device, in case it is not needed. During shutdown the device has a very low Current Consumption. The Current Consumption of the device can be determined by measuring the Current flowing out of the GND Pin and defined as the delta between I_I and (I_Q+I_{EN}).

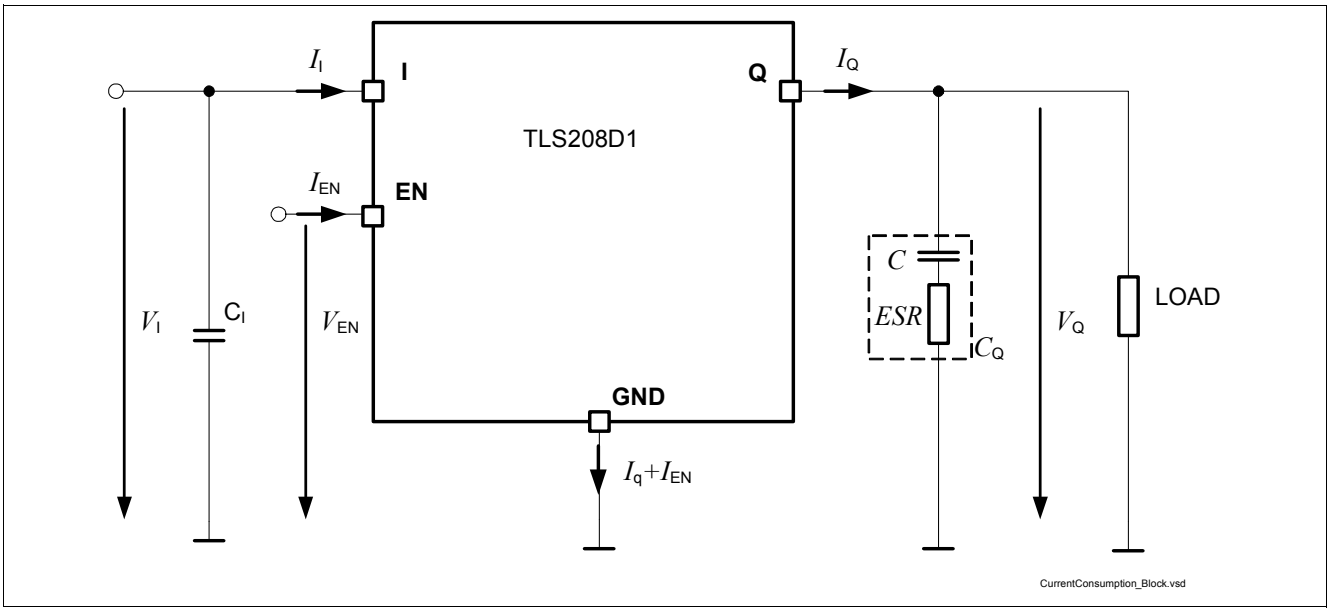


Figure 7 Parameter Definition Current Consumption

6.2 Electrical Characteristics Current Consumption

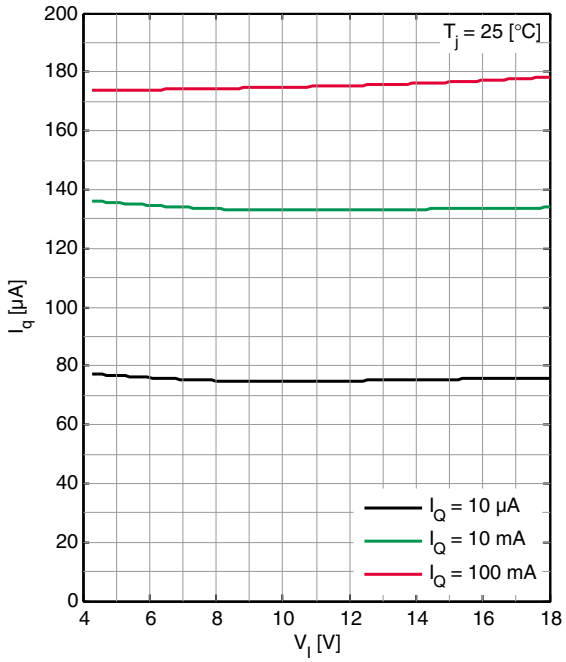
Table 5 Electrical Characteristics V_I = $V_{Q,nom}$ + 1 V and V_I ≥ 2.7 V ; T_j = -40 °C to +150 °C , V_{RADJ} ≥ 1.3 V; all voltages with respect to ground (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Quiescent Current $I_q = I_I - I_Q$	I_q	–	90	170	µA	I_Q = 10 µA	P_6.2.1
Current Consumption $I_q = I_I - I_Q$	I_q	–	200	250	µA	I_Q = 50 mA	P_6.2.2
Quiescent Current in Shutdown	$I_{q,off}$	–	0.01	6	µA	V_I = 5 V ; V_{EN} = 0 V ; T_j ≤ 125 °C ; V_Q = 0 V	P_6.2.3

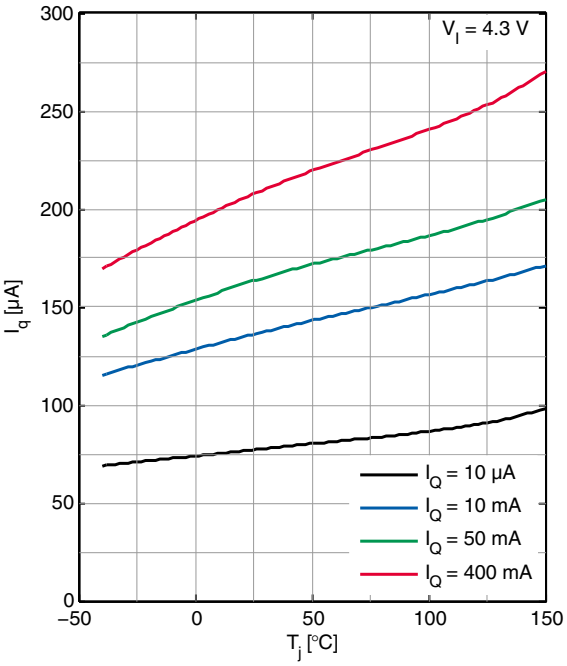
6.3 Typical Performance Characteristics Current Consumption

V_{EN}= 5 V (unless otherwise noted)

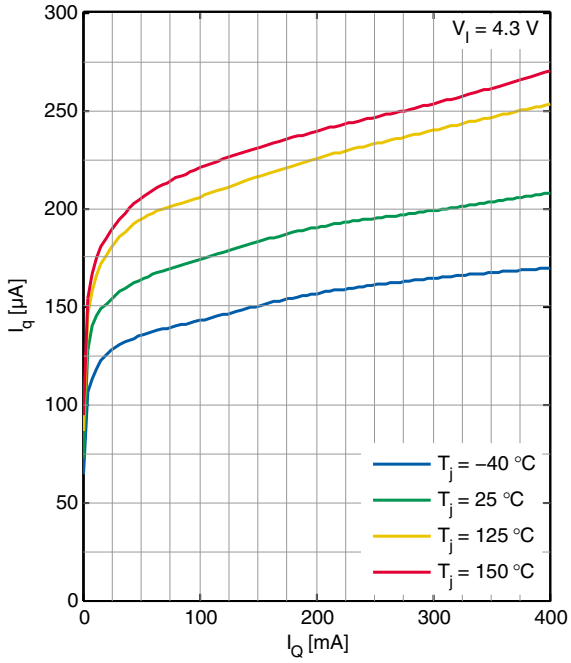
Quiescent Current I_q vs. Input Voltage V_I



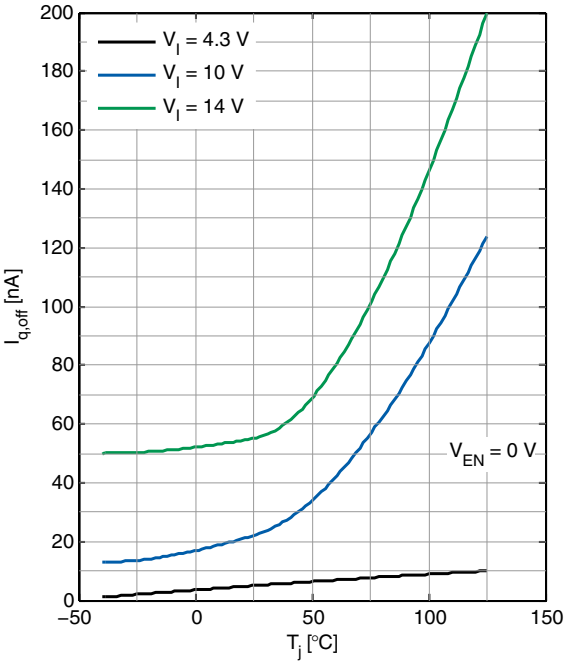
Quiescent Current I_q vs. Junction Temperature T_j



Current Consumption I_q vs. Load Current I_Q



Quiescent Current in Shutdown $I_{q,off}$ vs. Junction Temperature T_j



7 Enable Function

7.1 Description Enable Function

The TLS208D1 can be turned on or turned off by the EN Input. The parameter V_{EN} is the voltage provided to the EN Pin as shown in **Figure 7 "Parameter Definition Current Consumption" on Page 17**.
With voltage levels lower than $V_{EN,Lo}$ applied to the EN Input the device will be turned off. During this state the device is in shutdown with a very low current consumption $I_{q,off}$. Changing the voltage at the EN Input from $V_{EN,Lo}$ to $V_{EN,Hi}$ will trigger the start-up of the device. For voltages higher than $V_{EN,Hi}$ the device will regulate the output voltage to the nominal value as described in **Chapter 5 Voltage Regulator**.

7.2 Electrical Characteristics Enable Function

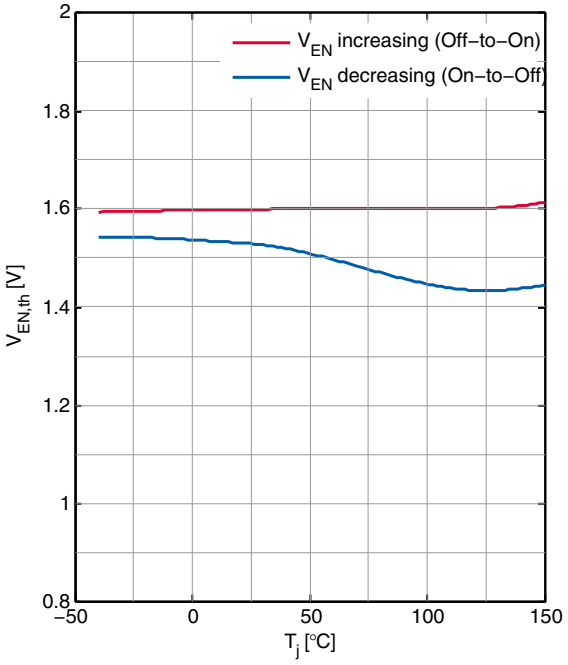
Table 6 Electrical Characteristics V_I = $V_{Q,nom}$ + 1 V and V_I ≥ 2.7 V ; T_j = -40 °C to +150 °C ; all voltages with respect to ground (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Enable High Voltage Level	$V_{EN,Hi}$	2	–	–	V	$V_{Q,on}$ ≥ 0.95 $V_{Q,nom}$	P_7.2.1
Enable Low Voltage Level	$V_{EN,Lo}$	–	–	0.4	V	$V_{Q,off}$ ≤ 200 mV	P_7.2.2
Enable Pin Current [1]	I_{EN}	–	4	5	µA	V_{EN} = 5V	P_7.2.3

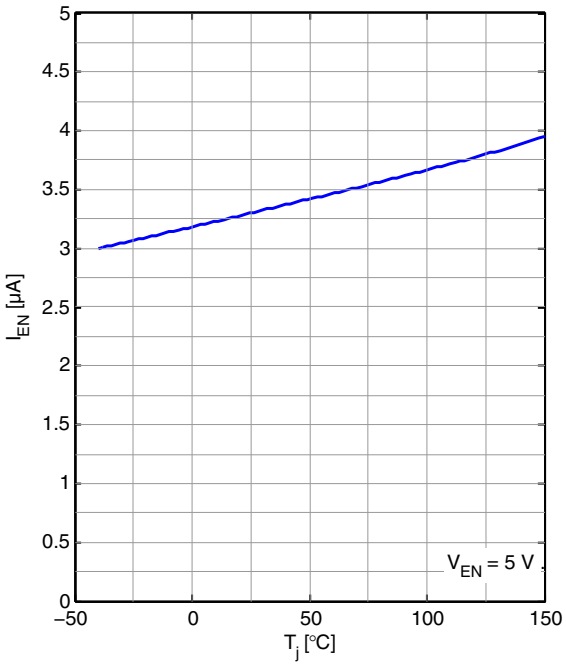
1) Enable pin current flows into the EN pin.

7.3 Typical Performance Characteristics Enable Function

Enable Thresholds V_{EN} vs. Junction Temperature T_j



Enable Pin Current V_{EN} vs. Junction Temperature T_j



8 Reset Function

8.1 Description Reset Function

The TLS208D1's output voltage is supervised by the Reset feature, including Undervoltage Reset, delayed Reset at Power-On and an adjustable Reset Threshold. Furthermore there is an input voltage monitor implemented that is contributing to the reset function.

The Undervoltage Reset sets the pin RO to LOW, in case V_Q is falling for any reason below the Reset Threshold $V_{RT,low}$.

When the regulator is powered on, the pin RO is held at LOW for the duration of the Power-On Reset Delay Time t_{rd}.

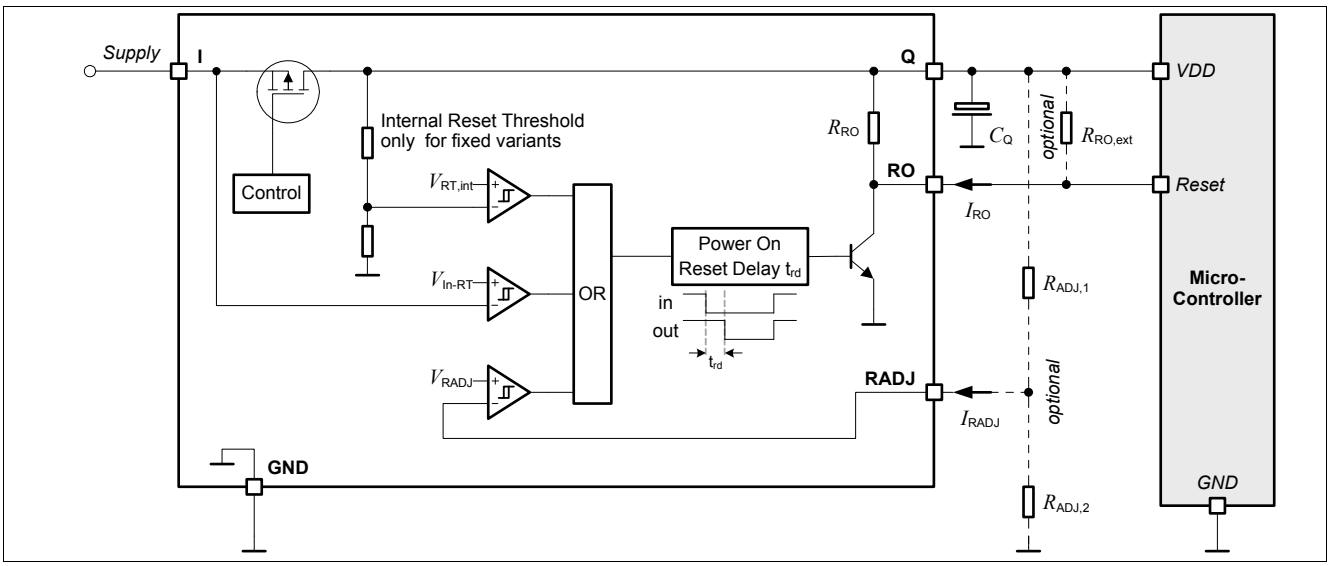


Figure 8 Block Diagram Reset Circuit

Reset Adjust Function

The undervoltage reset switching threshold can be adjusted according to the application's needs by connecting an external voltage divider ($R_{ADJ,1}$, $R_{ADJ,2}$) at pin "RADJ".

In case you are using a device with a fixed output voltage, you can select the default undervoltage reset threshold given in parameter by connecting the pin "RADJ" directly to GND.

By connecting the pin "RADJ" to the output Q the reset threshold is set to the minimum, which corresponds to the specified parameter V_{RADJ}.

When dimensioning the voltage divider, take into consideration that there will be an additional current constantly flowing through the resistors.

With a voltage divider connected, the reset switching threshold $V_{RT,new}$ is calculated as follows (neglecting the Reset Adjust Pin Current I_{RADJ}):

$$V_{RT,new} = V_{RADJ} \cdot \frac{R_{ADJ,1} + R_{ADJ,2}}{R_{ADJ,2}} \quad (1)$$

- $V_{RT,new}$: Desired undervoltage reset switching threshold.
- $R_{ADJ,1}$, $R_{ADJ,2}$: Resistors of the external voltage divider, see **Figure 8**.
- V_{RADJ}: Reset adjust switching threshold given in **Table 7** (**P_8.2.3** to **P_8.2.5** depending on condition).

8.2 Electrical Characteristics Reset Function

Table 7 Electrical Characteristics V_I = $V_{Q,nom}$ + 1 V and V_I ≥ 2.7 V ; T_j = -40 °C to +150 °C ; all voltages with respect to ground (unless otherwise specified)

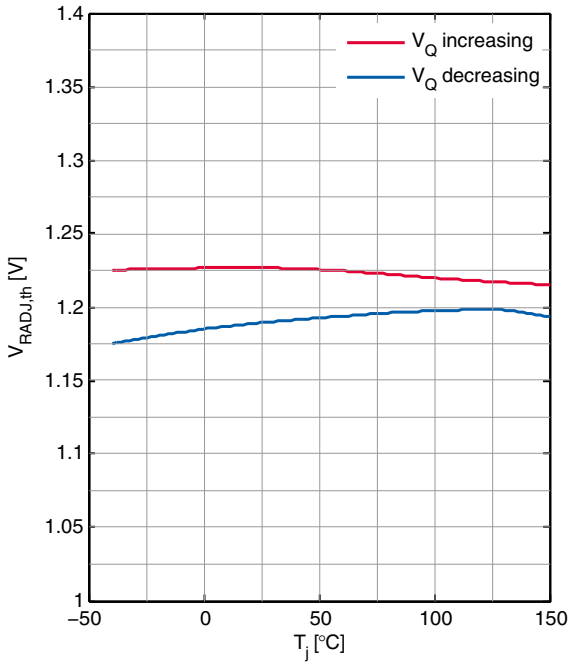
Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Fixed Reset Threshold (TLS208D1EJV33 only)							
Output Undervoltage Reset Threshold (default) only TLS208D1EJV33 and TLS208D1LDV33	$V_{RT,def}$	2.87	2.97	3.07	V	V_{RADJ} = 0V 1.355 V ≤ V_{RT}	P_8.2.1
Output Undervoltage Reset Hysteresis	$V_{RT,hyst}$	33	66	99	mV		P_8.2.2
Adjustable Reset Threshold							
Reset Adjust Lower Switching Threshold TLS208D1EJV33 TLS208D1LDV33	V_{RADJ}	1.14	1.2	1.24	V	$0.8V_{Q,nom} \leq V_{RT} \leq 0.87V_{Q,nom}$	P_8.2.3
Reset Adjust Lower Switching Threshold TLS208D1EJV33 TLS208D1LDV33	V_{RADJ}	1.16	1.2	1.24	V	1.355 V ≤ V_{RT} < $0.8V_{Q,nom}$	P_8.2.4
Reset Adjust Lower Switching Threshold TLS208D1EJV TLS208D1LDV	V_{RADJ}	1.16	1.2	1.24	V	1.355 V ≤ V_{RT} < $0.9V_{Q,nom}$	P_8.2.5
Reset Adjust Switching Threshold Hysteresis [1]	$V_{RADJ,hyst}$	–	25	–	mV		P_8.2.6
Reset Adjust Pull-down Current	I_{RADJ}	–	–	1	µA		P_8.2.7
Input Voltage Monitor							
Input Reset Threshold	V_{In-RT}	2.4	2.5	2.625	V	V_I decreasing	P_8.2.8
Input Reset Threshold Hysteresis [1]	$V_{In-RT,Hyst}$	–	60	–	mV	V_I increasing	P_8.2.9
Reset Timing Characteristic							
Power On Reset Delay Time	t_{rd}	6	10	14	ms		P_8.2.10
Internal Reset Reaction Time	$t_{rr,int}$	–	–	10	µs		P_8.2.11
Reset Output Characteristic							
Reset Pin Leakage	$I_{RO,leak}$	–	–	1	µA	V_{RO} = $V_{Q,nom}$	P_8.2.12
Reset Output Low Voltage	$V_{RO,Low}$	–	–	0.4	V	$R_{RO,ext}$ = 5 kΩ ; 1 V ≤ V_Q ≤ $V_{Q,nom}$	P_8.2.13
Reset Output external Pull-up Resistor to Q	$R_{RO,ext}$	5	–	–	kΩ	V_{RO} ≤ 0.4 V ; 1 V ≤ V_Q ≤ $V_{Q,nom}$	P_8.2.14

1) This parameter is not subject to production test, specified by design

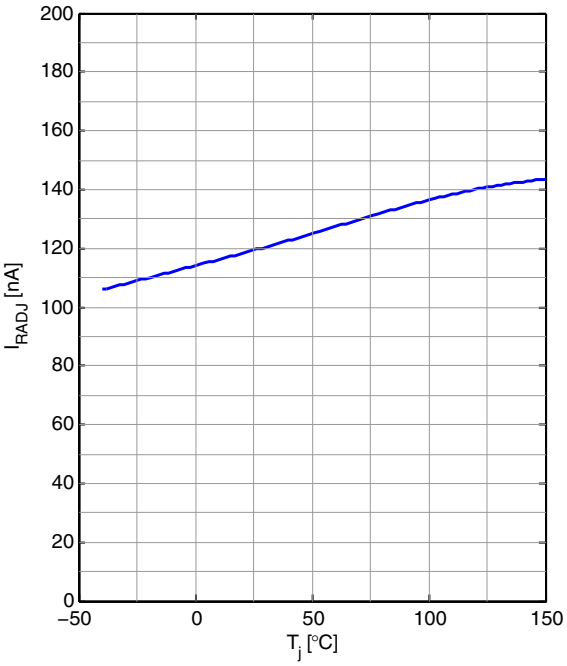
8.3 Typical Performance Characteristics Reset Function

V_{EN} = 5 V (unless otherwise noted)

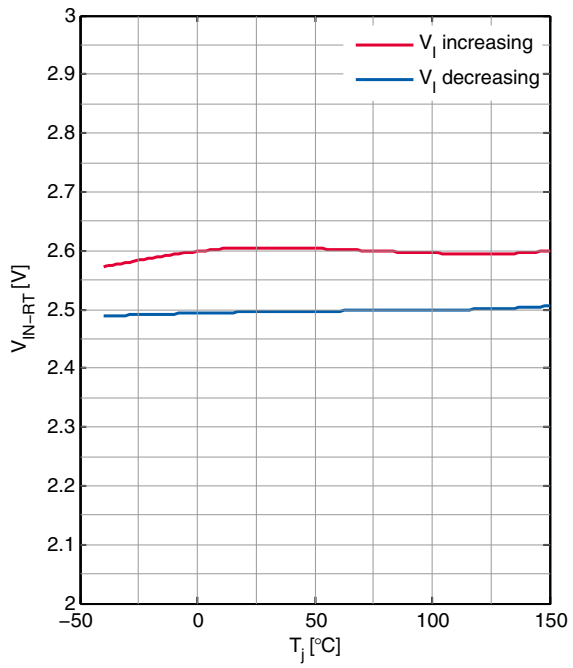
Adjustable Reset Threshold Voltage V_{RADJ} vs. Junction Temperature T_j



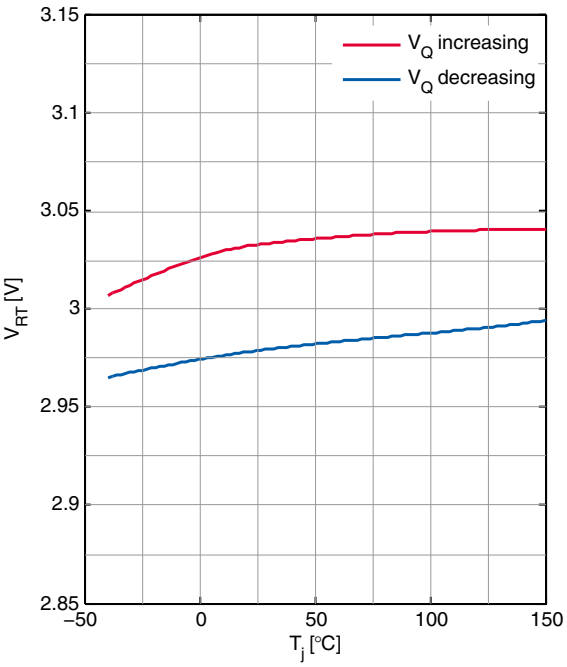
RADJ Input Current I_{RADJ} vs. Junction Temperature T_j



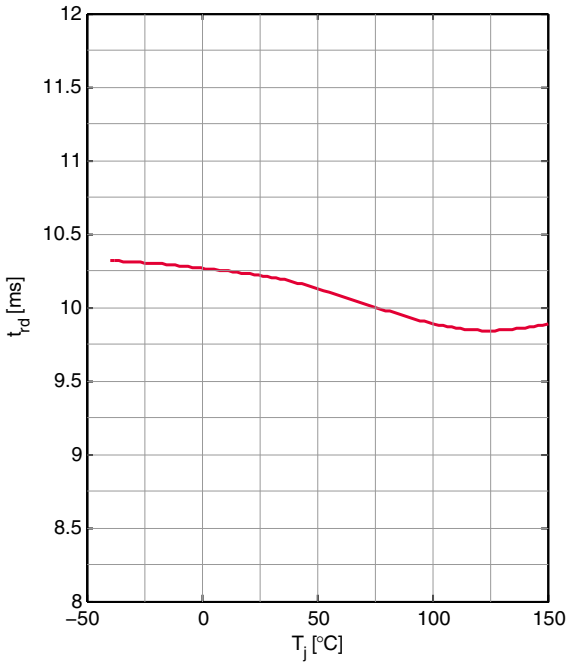
Input Voltage Reset Threshold V_{IN-RT} vs. Junction Temperature T_j



Internal Reset Threshold Voltage V_{RT} vs. Junction Temperature T_j (TLS208D1xxV33)



**Reset Delay Time t_{rd} vs.
Junction Temperature T_j**



9 Application Information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

9.1 Adjustable Version - TLS208D1xxV

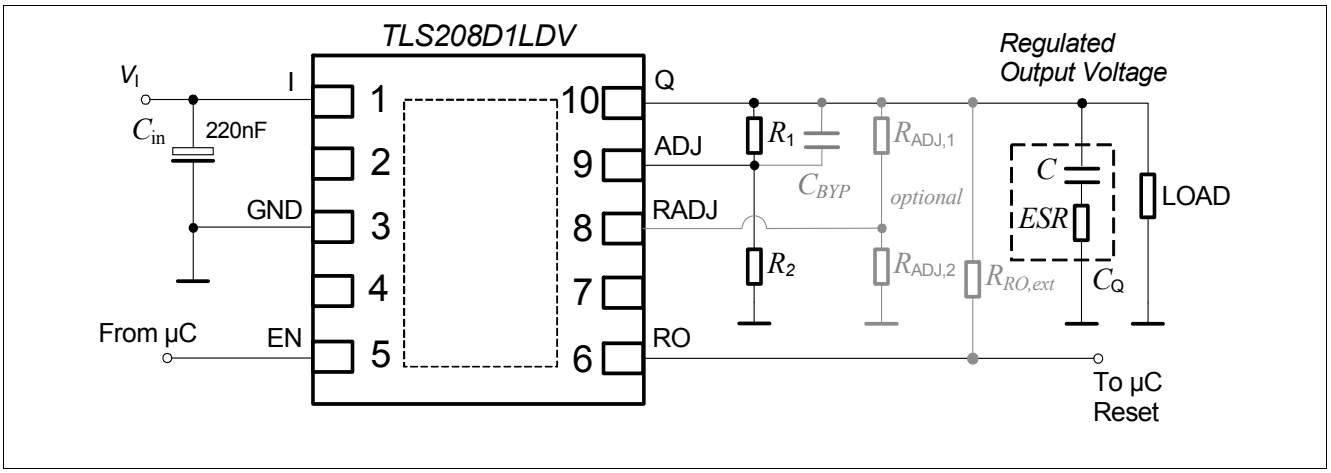


Figure 9 Application Diagram Adjustable Version (e.g. TLS208D1LDV)

Note: This is a very simplified example of an application circuit. The function must be verified in the real application.

The resistor divider for a specific output voltage can be calculated according to **Equation (2)**. The current I_{ADJ}, which flows into the ADJ-Pin, can be neglected, if **Equation (3)** is observed. V_{ADJ} is typically 0.8 V.

$$\frac{R_1}{R_2} = \frac{V_Q}{V_{ADJ}} - 1 \tag{2}$$

$$R_2 \leq 100k\Omega \tag{3}$$

The output capacitor should be sized according to the application needs in terms of load and line variations. Examples for loadsteps are given as typical performance graphs at **Page 15**.

An optional capacitor C_{BYP} can be placed in parallel to R_1 to improve the PSRR, noise and loadstep response of this adjustable regulator. The capacitance depends strongly on the used resistance. Using **Equation (4)** a feasible capacitance value can be determined, the final capacitance is to be evaluated according to the applications need.

$$C_{BYP} = \frac{1}{1 \cdot \pi \cdot R_1 \cdot 4kHz} \tag{4}$$

TLS208D1 is designed to work with ceramic output caps, but allows also the usage of other capacitors according to the allowed ESR range defined in the **Functional Range**. Furthermore there is a typ. performance graph on the stability of the device at **Page 14**.

The adjustable voltage variants have an adjustable reset threshold can be adjusted individually by connecting a resistor divider ($R_{ADJ,1}$ & R_{ADJ2}) between the Q and RADJ. For the calculation of the resistor values please refer to **Equation (1)** in **Chapter 8.1**. There is no default internal reset threshold for the adjustable variants.
In case the device is used to generate output voltages lower than the V_{RADJ} threshold, the reset function cannot be used to supervise the own output voltage. In this case it is recommended to connect the RADJ pin to a voltage higher than V_{RADJ} (e.g. V_I or V_{EN}) in order to avoid additional current consumption due to the reset condition.

9.2 Fixed Voltage Version - TLS208D1xxV33

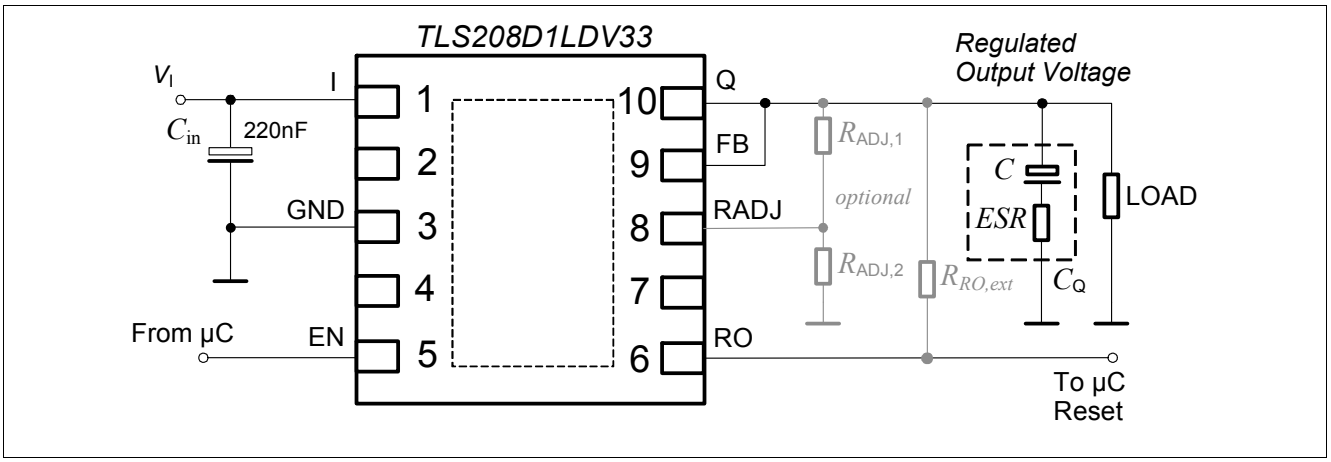


Figure 10 Application Diagram Fixed Voltage Version (e.g. TLS208D1LDV33)

Note: This is a very simplified example of an application circuit. The function must be verified in the real application.

For the fixed voltage variants of the TLS208D1 the feedback pin FB must be connected to the output voltage to be regulated. This connection is mandatory to ensure proper regulation.

The output capacitor should be sized according to the application needs in terms of load and line variations. Examples for loadsteps are given as typical performance graphs at **Page 15**.

TLS208D1 is designed to work with ceramic output caps, but allows also the usage of other capacitors according to the allowed ESR range defined in the **Functional Range**. Furthermore there is a typ. performance graph on the stability of the device at **Page 14**.

The fixed voltage variants have an default internal reset threshold (**P_8.2.1**) which can be used by connecting the RADJ pin to GND. Furthermore the reset threshold can be adjusted to lower values than the internal reset threshold by connecting a resistor divider ($R_{RADJ,1}$ & R_{RADJ2}) between the Q and RADJ. For the calculation of the resistor values please refer to **Equation (1)** in **Chapter 8.1**.