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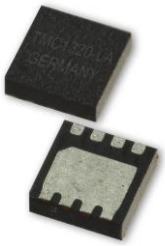
TMC1320-LA DATASHEET

Dual N & P-Channel 30V Power MOSFET with low on-resistance and fast switching performance. High energy efficiency and good thermal performance.



Applications

TMC1320 MOSFETs fit best with TRINAMIC 2-phase bipolar stepper motor drivers:

TMC262: up to 3.5A RMS motor current with 4xTMC1320-LA

TMC248: up to 3A RMS motor current with 4xTMC1320

TMC249: up to 3A RMS motor current with 4xTMC1320-LA

Product Summary

	N-CH	P-CH
BV_{DSS}	30V	-30V
$R_{DS(ON)}$	30mΩ	60mΩ
I_D	7.3A	-5.3A

Features and Benefits

N & P-Channel MOSFET Half Bridge Device

Simple Drive Requirement

Good Thermal Performance

Fast Switching Performance for quick motor reaction

PQFN Package, 3x3mm; similar to DFN3x3 EP

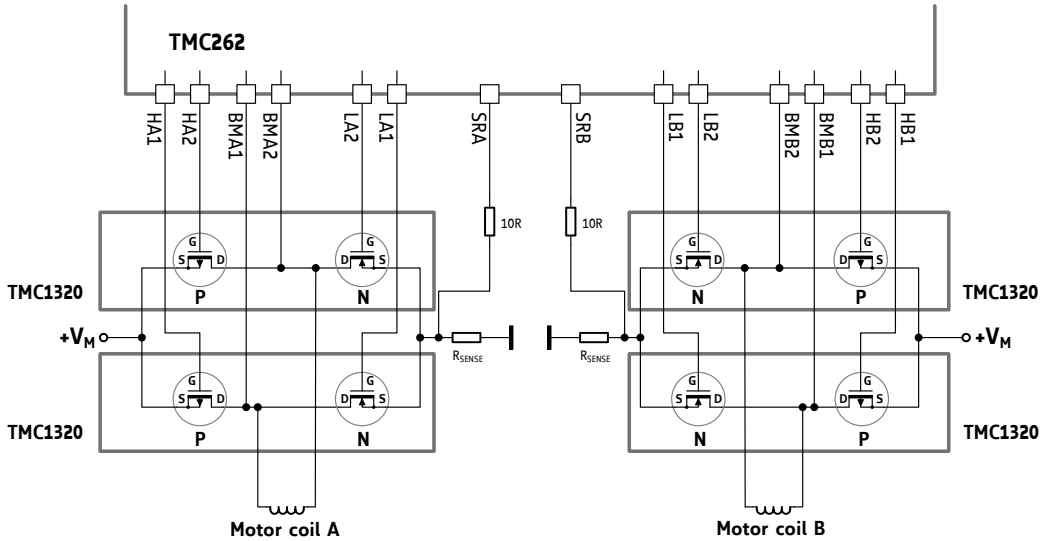
RoHS Compliant and Halogen-Free

Description

The advanced TMC1320-LA Power MOSFET provides the designer with the best combination of fast switching, low on-resistance and cost-effectiveness. The highly energy efficient TMC1320 is intended for power conversion and power management applications that require high efficiency and power density.

The PQFN 3x3 package has a backside heat sink. It is compatible with other DFN3 packages offering attractive thermal and electrical performance combined with a very small footprint.

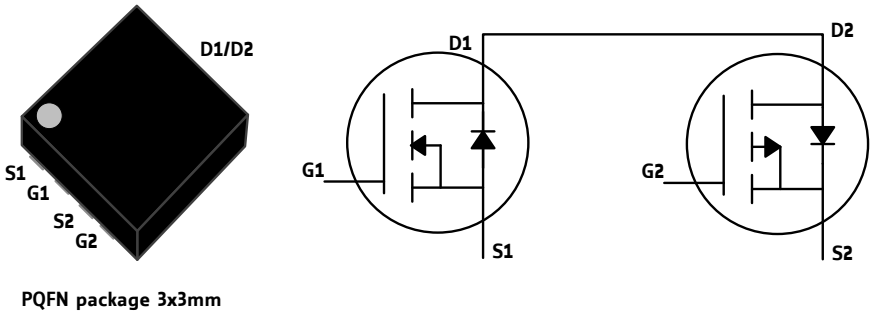
TMC262 with 4x TMC1320-LA MOSFETs



Order code	Description	Size
TMC1320-LA	N and P-channel enhancement mode power MOSFET	3.1 x 3.1 mm²

Table of Contents

1 Pin Assignments



PQFN package 3x3mm

Figure 1.1 TMC1320-LA pin assignments

2 Absolute Maximum Ratings

The maximum ratings may not be exceeded under any circumstances. Operating the circuit at or near more than one maximum rating at a time for extended periods shall be avoided by application design.

Parameter	Symbol	N-channel	P-channel	Unit
Drain-Source Voltage	V_{DS}	30	-30	V
Gate-Source Voltage	V_{GS}	±20	±20	V
Continuous Drain Current*[2]	I_D@T_A = 25°C	7.3	-5.3	A
Continuous Drain Current*[2]	I_D@T_A = 70°C	5.8	-4.2	A
Pulsed Drain Current*[1]	I_{DM}	28	-20	A
Total Power Dissipation	P_D@T_A = 25°C	2.5		W
Linear Derating Factor		0.02		W/°C
Storage Temperature Range	T_{STG}	-55 to 150		°C
Operating Junction Temperature Range	T_J	-55 to 150		°C

*[1] Pulse width is limited by maximum junction temperature.
*[2] Surface mounted on 1 in^2 copper pad of FR4 board, t ≤ 10sec; 90°C/W at steady state.

3 Thermal Data

Parameter	Symbol	Value	Unit
Max. Thermal Resistance, Junction-case	Rthj-c	10	°C/W
Max. Thermal Resistance, Junction-ambient*	Rthj-a	50	°C/W

* Surface mounted on 1 in^2 copper pad of FR4 board, t ≤ 10sec; 90°C/W at steady state.

4 Electrical Characteristics

4.1 N-CH @Tj=25°C *(unless otherwise specified)*

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250µA	30			V
Static Drain-Source On-Resistance*	$R_{DS(ON)}$	V_{GS}=10V, I_D=4A V_{GS}=4.5V, I_D=3A			30 48	mΩ mΩ
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=250µA	1		3	V
Forward Transconductance	g_{fs}	V_{DS}= 10V, I_D=4A		8.5		S
Drain-Source Leakage Current	I_{DSS}	V_{DS}= 24V, V_{GS}=0V			1	mA
Gate-Source Leakage	I_{GSS}	V_{DS}= 0V, V_{GS}=±20V			±100	mA
Total Gate Charge*	Q_g	I_D=4A		4.5	7.2	nC
Gate-Source Charge	Q_{gs}	V_{DS}=15V		1		nC
Gate-Drain ("Miller") Charge	Q_{gd}	V_{GS}=4.5V		2.5		nC
Turn-on Delay Time	$t_{d(on)}$	V_{DS}=15V		8		ns
Rise Time	t_r	I_D=1A		9		ns
Turn-off Delay Time	$t_{d(off)}$	R_G=3.3Ω		16		ns
Fall Time	t_f	V_{GS}=10V		3		ns
Input Capacitance	C_{iss}	V_{GS}=0V		250	400	pF
Output Capacitance	C_{oss}	V_{DS}=25V		55		pF
Reverse Transfer Capacitance	C_{rss}	f=1.0MHz		50		pF

* Pulse width ≤ 300µs, duty cycle ≤ 2%

4.1.1 Source-Drain Diode

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Forward On Voltage*	V_{SD}	V_{GS}=0V, I_S=1.2A			1.2	V
Reverse Recovery Time*	t_{rr}	V_{GS}=0V, I_S=4A		15		ns
Reverse Recovery Charge	Q_{rr}	dI/dt=100A/µs		7		nC

* Pulse width ≤ 300µs, duty cycle ≤ 2%

4.2 P-CH @Tj=25°C *(unless otherwise specified)*

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=-250µA	-30			V
Static Drain-Source On-Resistance*	$R_{DS(ON)}$	V_{GS}=-10V, I_D=-4A V_{GS}=-4.5V, I_D=-3A			60 80	mΩ mΩ
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=-250µA	-1		-3	V
Forward Transconductance	g_{fs}	V_{DS}= -10V, I_D=-4A		9		S
Drain-Source Leakage Current	I_{DSS}	V_{DS}= -24V, V_{GS}=0V			-1	mA
Gate-Source Leakage	I_{GSS}	V_{DS}= 0V, V_{GS}=±20V			±100	mA
Total Gate Charge*	Q_g	I_D=-4A		7	11.2	nC
Gate-Source Charge	Q_{gs}	V_{DS}=-15V		1.5		nC
Gate-Drain ("Miller") Charge	Q_{gd}	V_{GS}=-4.5V		3.5		nC
Turn-on Delay Time*	$t_{d(on)}$	V_{DS}=-15V		10		ns
Rise Time	t_r	I_D=-1A		11		ns
Turn-off Delay Time	$t_{d(off)}$	R_G=3.3Ω		22		ns
Fall Time	t_f	V_{GS}=-10V		9		ns
Input Capacitance	C_{iss}	V_{GS}=0V		570	910	pF
Output Capacitance	C_{oss}	V_{DS}=-25V		80		pF
Reverse Transfer Capacitance	C_{rss}	f=1.0MHz		75		pF

* Pulse width ≤ 300µs, duty cycle ≤ 2%

4.2.1 Source-Drain Diode

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Forward On Voltage*	V_{SD}	V_{GS}=0V, I_S=-1.2A			-1.2	V
Reverse Recovery Time*	t_{rr}	V_{GS}=0V, I_S=-4A		19		ns
Reverse Recovery Charge	Q_{rr}	dI/dt=-100A/µs		13		nC

* Pulse width ≤ 300µs, duty cycle ≤ 2%

5 N-Channel Diagrams

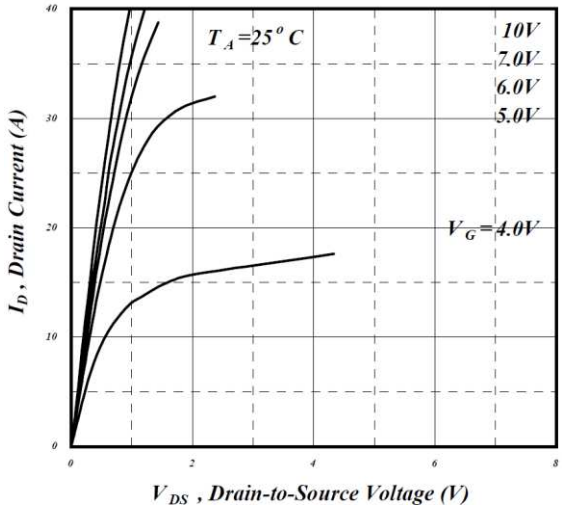


Figure 5.1 Typical output characteristics

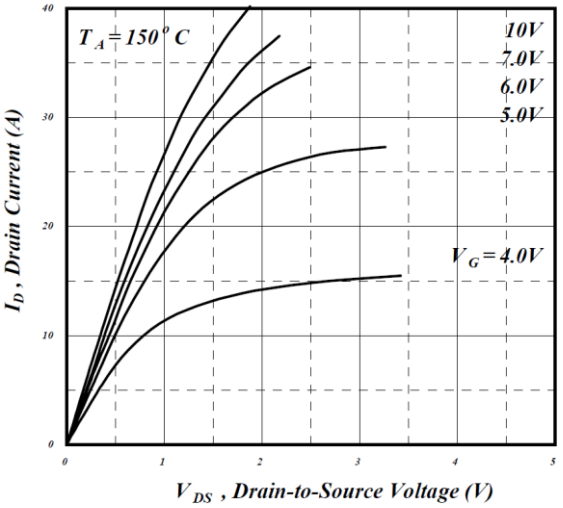


Figure 5.2 Typical output characteristics

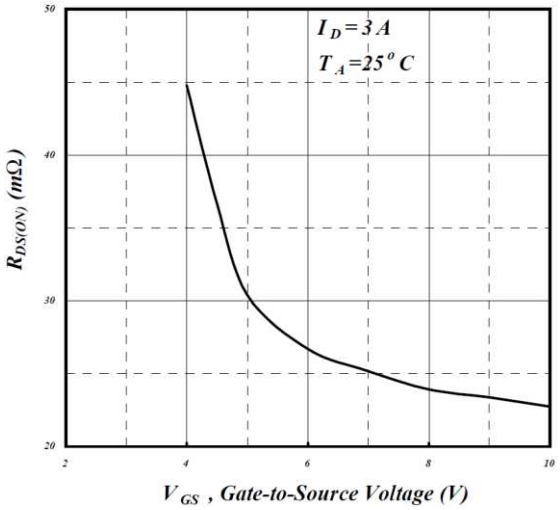


Figure 5.3 On-resistance v.s. gate voltage

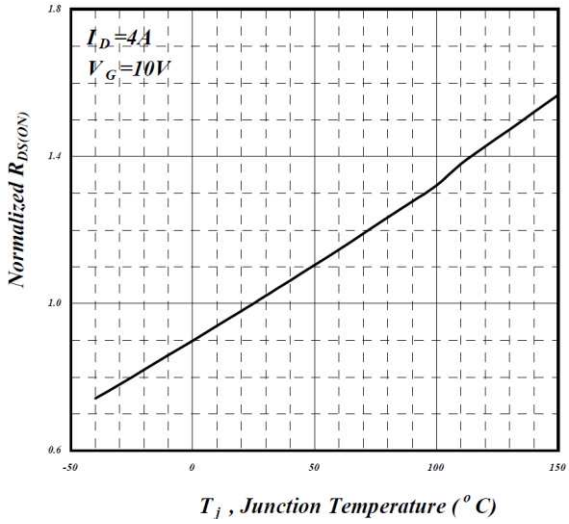


Figure 5.4 Normalized on-resistance v.s. junction temperature

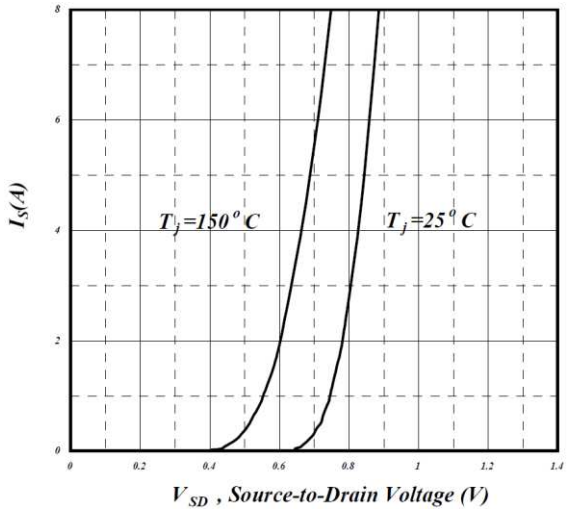


Figure 5.5 Forward characteristic of reverse diode

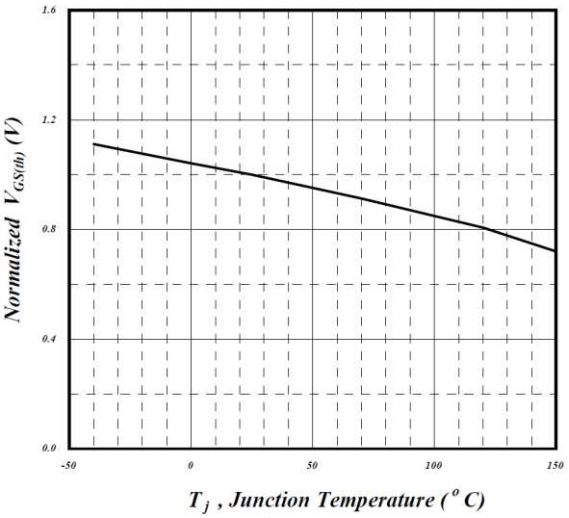


Figure 5.6 Gate threshold voltage v.s. junction temperature

N-Channel Diagrams

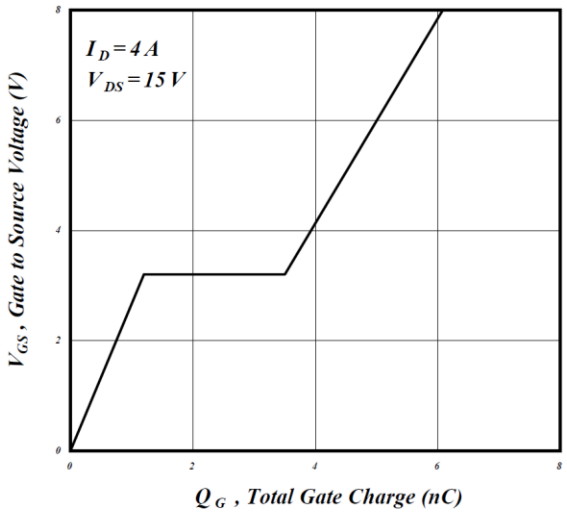


Figure 5.7 Gate charge characteristics

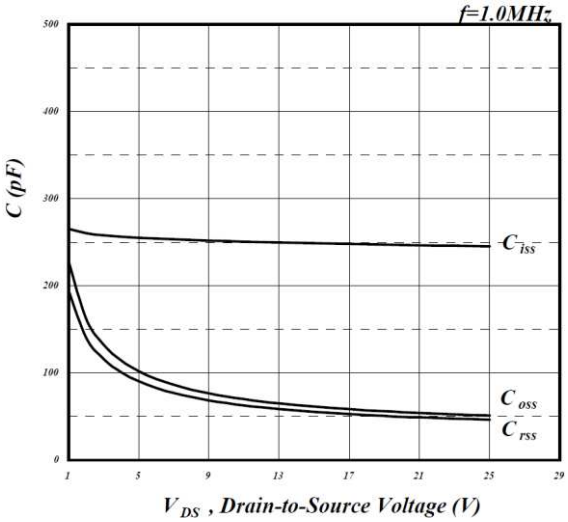


Figure 5.8 Typical capacitance characteristics

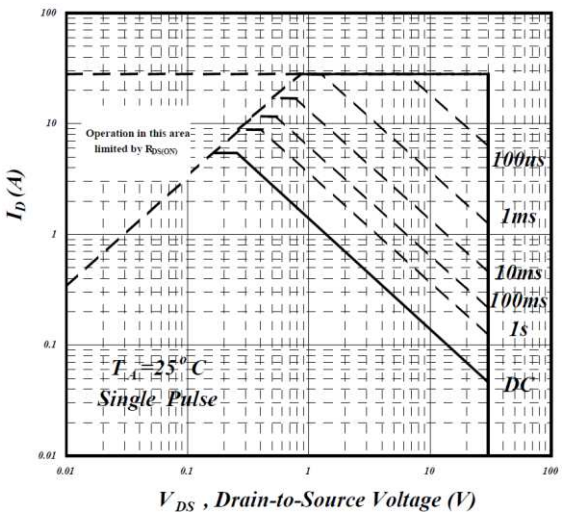


Figure 5.9 Maximum safe operating area

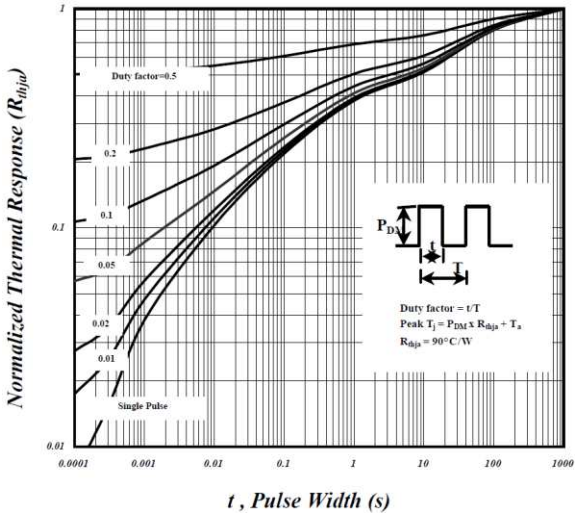


Figure 5.10 Effective transient thermal impedance

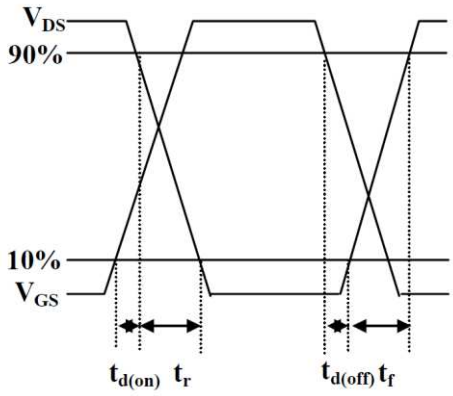


Figure 5.11 Switching time waveform

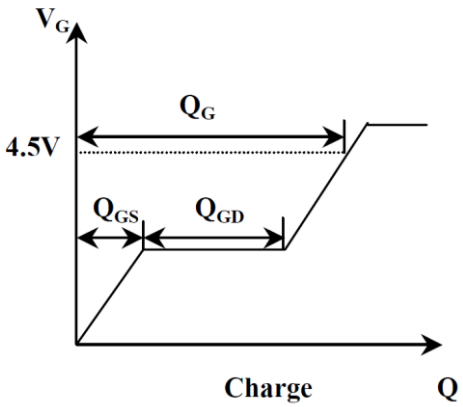


Figure 5.12 Gate charge waveform

6 P-Channel Diagrams

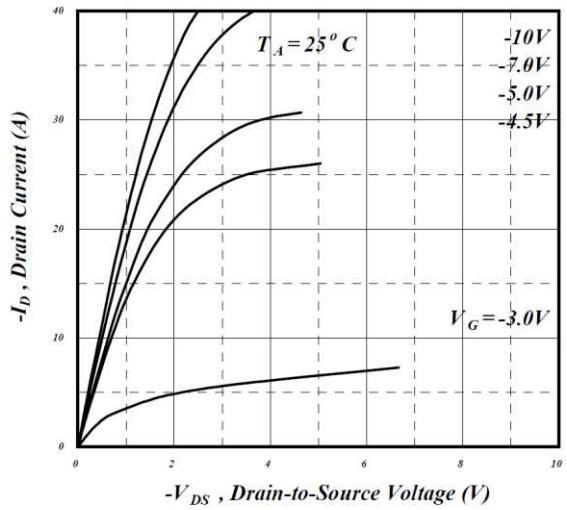


Figure 6.1 Typical output characteristics

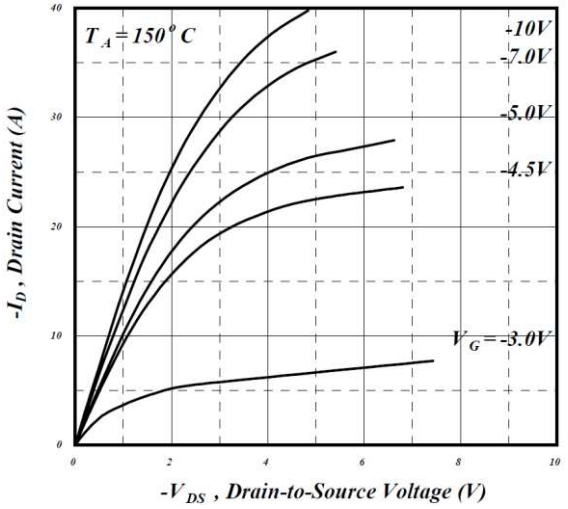


Figure 6.2 Typical output characteristics

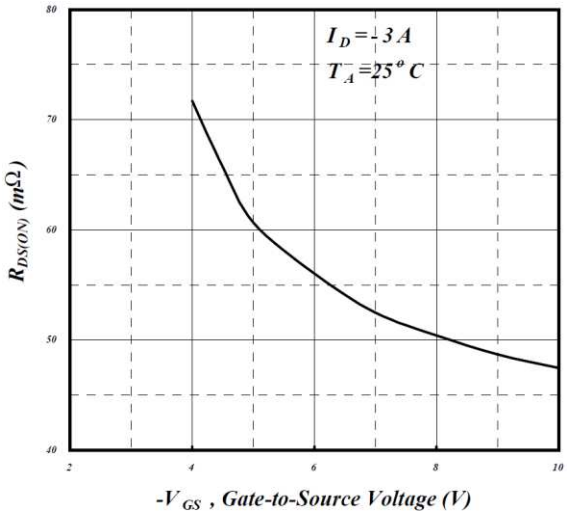


Figure 6.3 On-resistance v.s. gate voltage

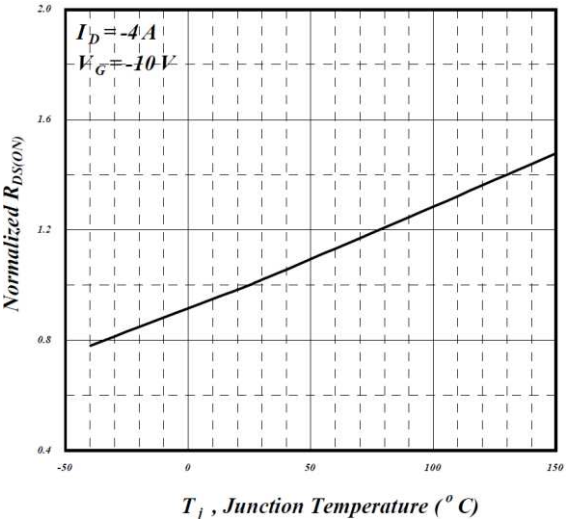


Figure 6.4 Normalized on-resistance v.s. junction temperature

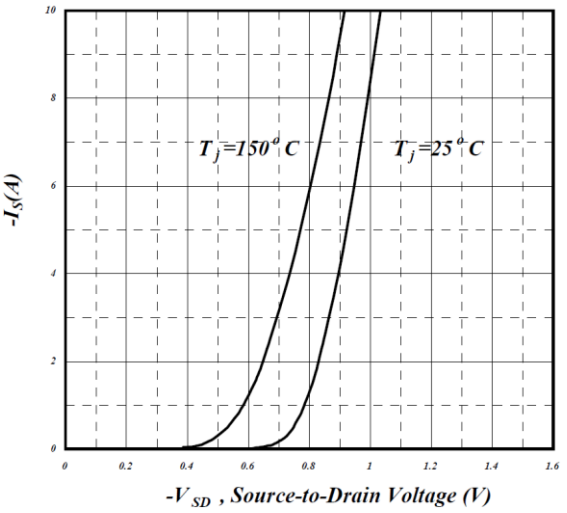


Figure 6.5 Forward characteristic of reverse diode

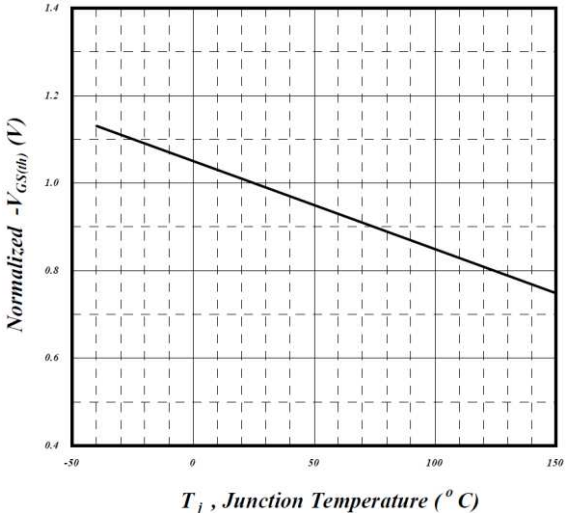


Figure 6.6 Gate Threshold voltage v.s. junction temperature

P-Channel Diagrams

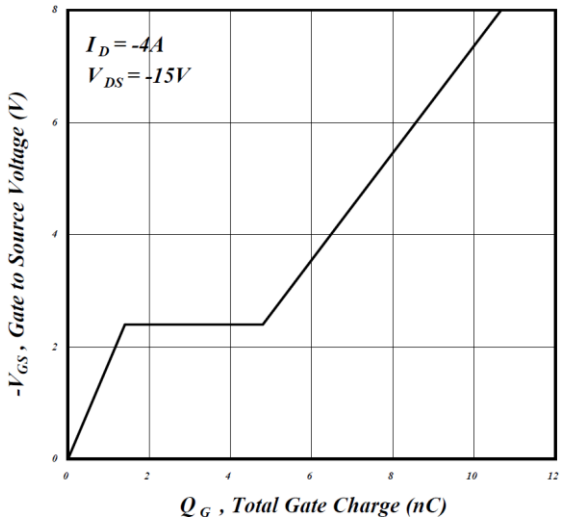


Figure 6.7 Gate charge characteristics

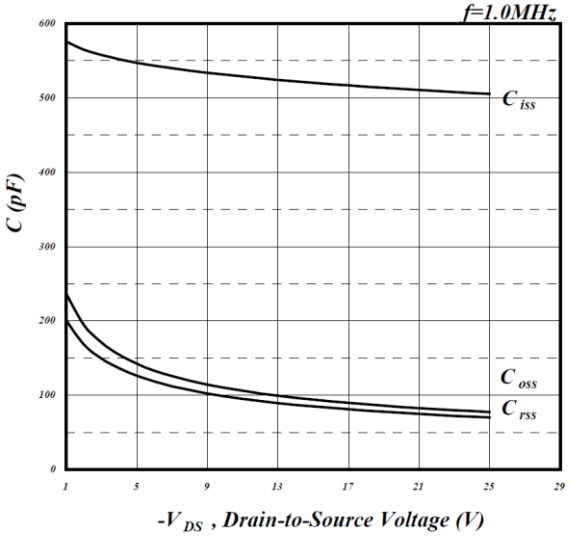


Figure 6.8 Typical capacitance characteristics

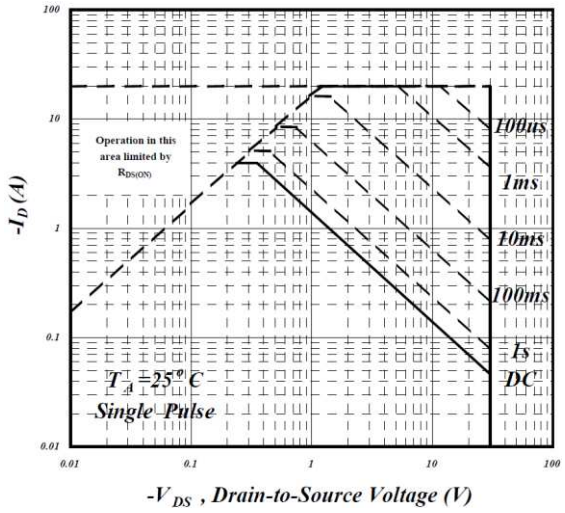


Figure 6.9 Maximum safe operating area

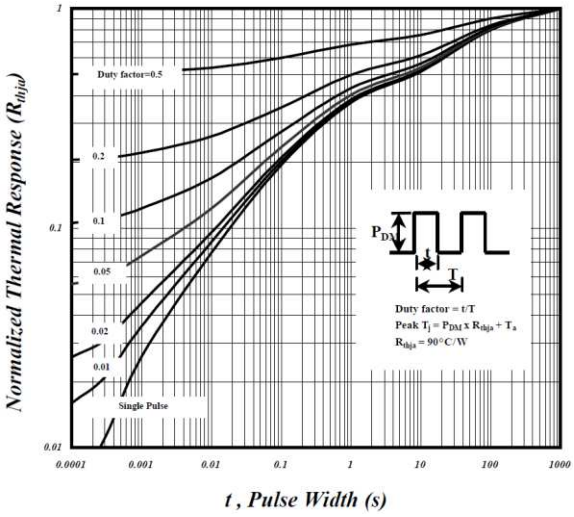


Figure 6.10 Effective transient thermal impedance

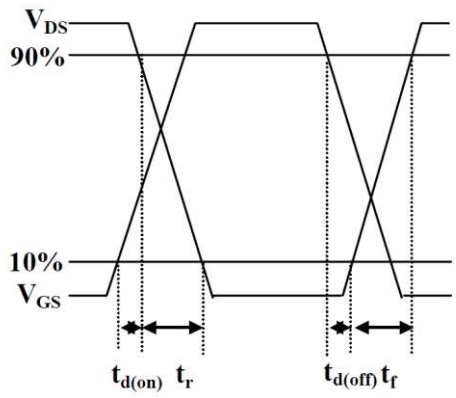


Figure 6.11 Switching time waveform

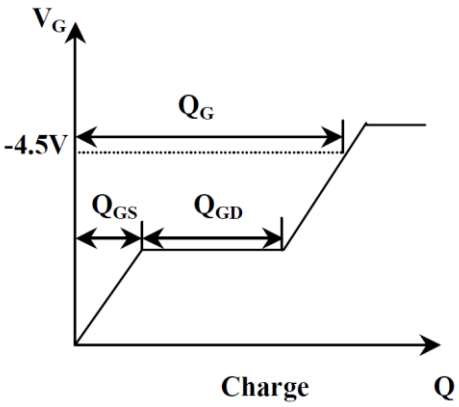
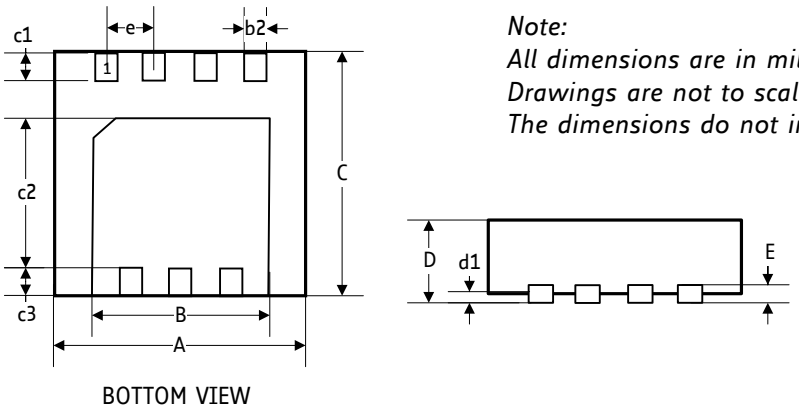


Figure 6.12 Gate charge waveform

7 Package Mechanical Data

7.1 Dimensional Drawings



Note:
All dimensions are in millimeters.
Drawings are not to scale.
The dimensions do not include mold protrusions.

Figure 7.1 Dimensional drawings

Symbols	Min	Nom	Max
A	2.90	3.10	3.40
B	2.20	2.45	2.80
e	0.60	0.65	0.70
b2	0.20	0.30	0.40
C	2.90	3.10	3.40
c1	0.10	0.30	0.50
c2	1.20	1.70	2.20
C3	0.10	0.38	0.65
D	0.65	0.80	1.05
d1	0.00	0.10	0.20
E	0.10	0.18	0.25

7.2 Package Marking Information and Package Code

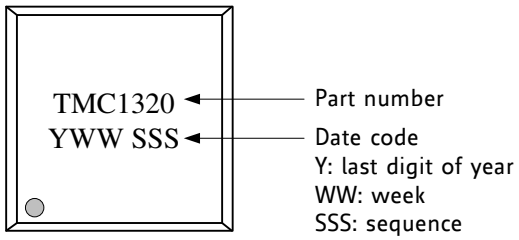


Figure 7.2 Package marking information

Device	Package	Temperature range	Code/ Marking
TMC1320	PQFN 3 x3, I-type	-55° to +150°C	TMC1320-LA

8 Disclaimer

TRINAMIC Motion Control GmbH & Co. KG does not authorize or warrant any of its products for use in life support systems, without the specific written consent of TRINAMIC Motion Control GmbH & Co. KG. Life support systems are equipment intended to support or sustain life, and whose failure to perform, when properly used in accordance with instructions provided, can be reasonably expected to result in personal injury or death.

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9 ESD Sensitive Device

The TMC1320-LA is an ESD sensitive CMOS device sensitive to electrostatic discharge. Take special care to use adequate grounding of personnel and machines in manual handling. After soldering the devices to the board, ESD requirements are more relaxed. Failure to do so can result in defect or decreased reliability.

10 Table of Figures

11 Revision History

Version	Date	Author SD – Sonja Dwersteg	Description
0.92	2014-MAR-13	SD	Initial version
1.00	2014-MAR-18	SD	RMS current corrected. Front picture added. Total gate charge corrected.
1.01	2014-MAY-12	SD	RMS motor current values in combination with TMC262, TMC248, and TMC249 updated.