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TMC2072

Peripheral Mode CircLink™ Controller

Datasheet

PRODUCT FEATURES

- Low Power CMOS, 3.3 Volt Power Supply with 5 Volt Tolerant I/O
- Supports 8/16-Bit Data Bus
  - Both 86xx and 68hxx Platforms
- 1K On-chip Dual Port Buffer Memory
  - Sequential I/O Mapped Access
- Enhanced Token Passing Protocol from ARCNET
  - Maximum 31 Nodes per Network
  - Token Retry Mechanism
  - Maximum 256 Bytes per Packet
  - Consecutive Node ID Assignment
- Memory Mirror
  - Shared Memory within Network
- Network Standard Time
  - Network Time Synchronization
  - Automatic Time Stamping
- Coded Mark Inversion
  - Intelligent 1-Bit Error Correction
  - Magnetic Saturation Prevention
- Single Operation Mode
  - Supports Only Peripheral (Host) Mode Operates with MCU
- Supports 8 Bit Programmable General Purpose I/O
- Dual Communication Modes (with Peripheral Mode)
  - Free Format Mode
  - Remote Buffer Mode
- 3 Port Hub Integrated
  - 1 Internal and 2 External
- Flexible Topologies
  - Bus, Star, and Tree
- Low-Cost Media can be Used
  - RS485 Differential Driver
- Fiber Optics and Twisted Pair Cable Supported
- 100-Pin, TQFP Lead-Free RoHS Compliant Package
- Temperature Range from 0 to 70 Degrees C

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Order Number:

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Chapter 1 General Description

1.1 About CircLink

The CircLink networking controller was developed for small control-oriented local network data communication based on ARCNET's token-passing protocol that guarantees message integrity and calculatable maximum delivery times.

In a CircLink network, when a node receives the token it becomes the temporary master of the network for a fixed, short period of time. No node can dominate the network since token control must be relinquished when transmission is complete. Once a transmission is completed the token is passed on to the next node (logical neighbor), allowing it to be come the master.

Because of this token passing scheme, maximum waiting time for network access can be calculated and the time performance of the network is predictable or deterministic. Industrial network applications require predictable performance to ensure that controlled events occur when required.

However, reconfiguration of a regular ARCNET network becomes necessary when the token is missed due to electronic and magnetic noise. In these cases, the maximum wait time for sending datagrams cannot be guaranteed and the real-time characteristic is impaired. CircLink makes several modification to the original ARCNET protocol (such as maximum and consecutive node ID assignment) to avoid token missing as much as possible and reduce the network reconfiguration time.

CircLink implements other enhancements to the ARCNET protocol including a smaller-sized network , shorter packet size, and remote buffer mode operation that enable more efficient and reliable small, control-oriented LANs. In addition, CircLink introduces several unique features for reducing overall system cost while increasing system reliability.

CircLink can operate under a special mode called "Standalone" or "I/O" mode. In this mode, CircLink does not need an administrating CPU for each node. Only one CPU is needed to manage a CircLink network composed of several nodes, reducing cost and complexity.

In a CircLink network, the data sent by the source node is received by all other nodes in the network and stored according to node source ID. For the target node the received data is executed per ARCNET flow control and the data is stored in its buffer RAM. The receiving node processes the data while the remaining nodes on the network discard the data when the receiving node has completed. This memory-mirroring function assures higher reliability and significantly reduces network traffic.

Network Standard Time (NST) is also a unique CircLink feature. NST is realized by synchronizing the individual local time on each network node to the clock master in the designated node from which the packet is sent. CircLink also uses CMI code for transmitting signals, rather than the dipulse or bipolar signals that are the standard ARCNET signals. Since CMI encoding eliminates the DC element, a simple combination of a standard RS485 IC and a pulse transformer can be used to implement a transformer-coupled network.

1.2 About the TMC2072

The TMC2072 network controller is CircLink technology's flagship product. The TMC2072's flexibility and rich feature set enable a high-reliability and high-performance, real-time and control-oriented network without the cumbersome middle layer protocol stacks and complex packet prioritization schemes typically required.

TMC2072 operates at network data transfer rates up to 5 Mbps. Its embedded 1k Byte RAM can be configured into a maximum of 32 pages to implement a 31-node network where each node in the network has the same local memory.

TMC2072 supports "Peripheral Mode" operation, which includes two selectable communication modes: "Free Format Mode" and "Remote Buffer Mode". Free Format mode, retained from ARCNET, is "packet oriented" communication. Remote Buffer mode communication is a CircLink-specific feature, and is a token oriented communication, which includes automatic data transmission when the token arrives.

The TMC2072 has a flexible 8-bit or 16-bit data bus to interface various CPU types including X86, 68XX, and SHx with multiplexed or non-multiplexed address/data. When operating in Peripheral mode, the TMC2072 has 8-bit programmable I/O available. When operating in Standalone mode, the TMC2072's I/O configuration is16-bit. The TMC2072 also integrates a 3-port hub (two ports for external connection) to accommodate various network topologies (Bus, Star, etc.) and combinations.

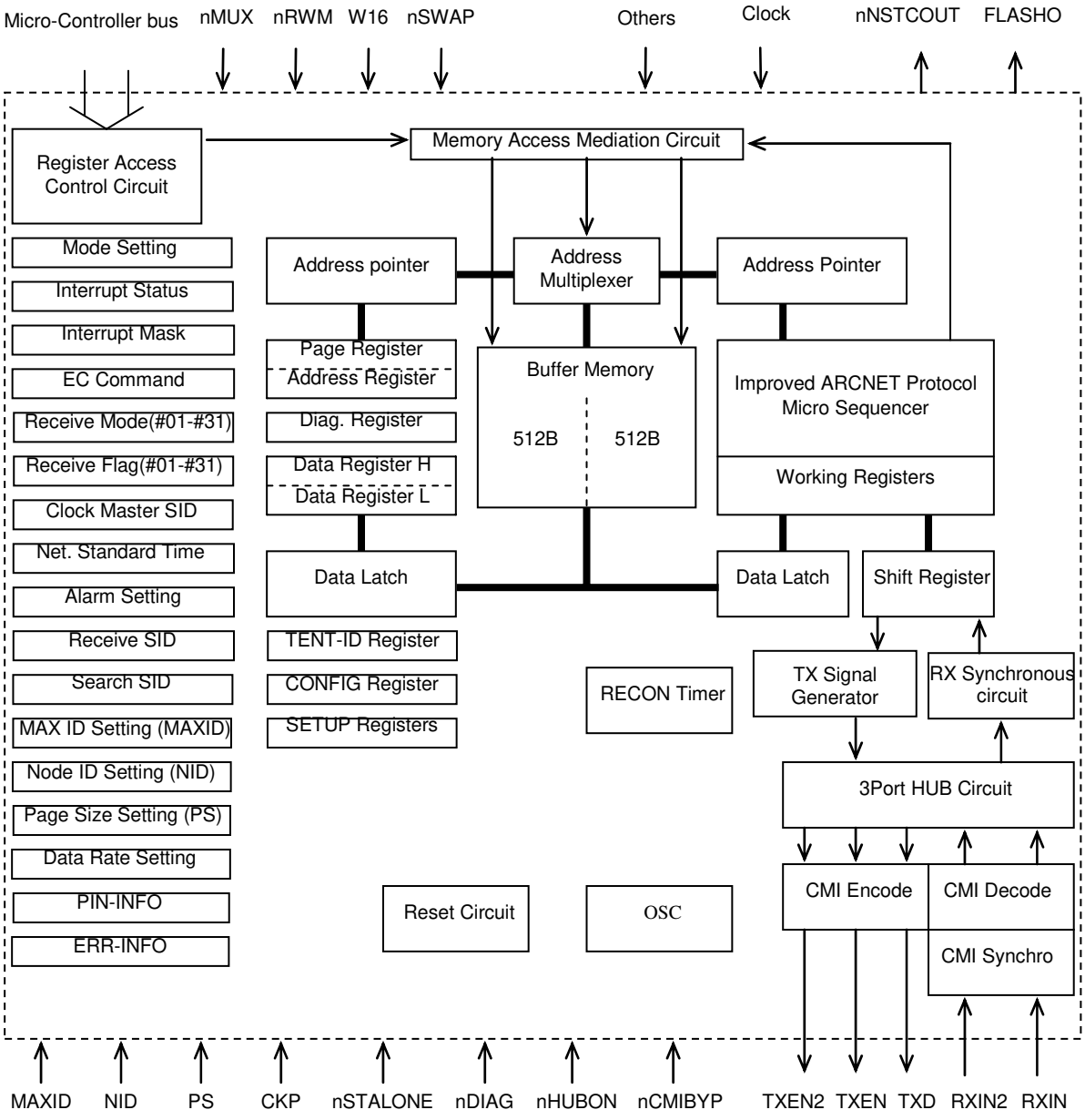


Figure 1 - TMC2072 Internal Block Diagram

1.3 Pin Configuration

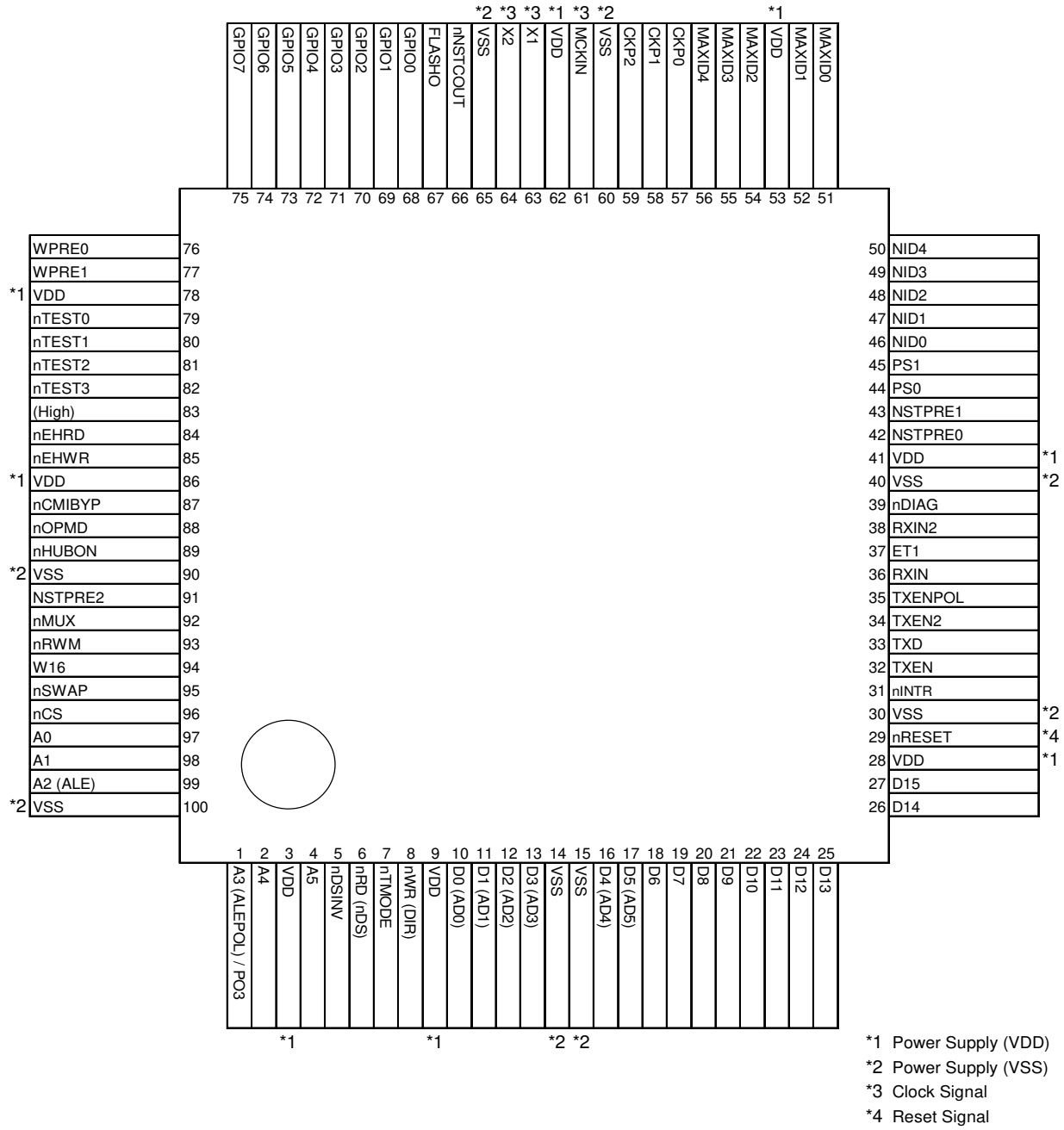


Figure 2 - TMC2072 Pin Configuration

Table 1 - Pin Description

PIN			PERIPHERAL MODE			INPUT BUFFER			OUTPUT BUFFER	
COUNT	**PIN NO.**		**PIN NAME**	**DIRECTION**		**PULL-UP**	**TYPE**		**DRIVE**	**TYPE**
CPU Interface										
1	**29**		nRESET	IN		Internal	T-NRM		---	---
2	**96**		nCS	IN		Internal	T-NRM		---	---
3	**97**		A0	IN		Internal	T-NRM		---	---
4	**98**		A1	IN		Internal	T-NRM		---	---
5	**99**		A2/ALE	IN		Internal	T-NRM		---	---
6	**1**		A3/ALEPOL	IN		Internal	T-NRM		---	---
7	**2**		A4	IN		Internal	T-NRM		---	---
8	**4**		A5	IN		Internal	T-NRM		---	---
9	**6**		nRD/nDS	IN		Internal	T-NRM		---	---
10	**8**		nWR/DIR	IN		Internal	T-NRM		---	---
11	**10**		D0/AD0	BI		Internal	T-NRM		4mA	
12	**11**		D1/AD1	BI		Internal	T-NRM		4mA	
13	**12**		D2/AD2	BI		Internal	T-NRM		4mA	
14	**13**		D3/AD3	BI		Internal	T-NRM		4mA	
15	**16**		D4/AD4	BI		Internal	T-NRM		4mA	
16	**17**		D5/AD5	BI		Internal	T-NRM		4mA	
17	**18**		D6	BI		Internal	T-NRM		4mA	
18	**19**		D7	BI		Internal	T-NRM		4mA	
19	**20**		D8	BI		Internal	T-NRM		4mA	
20	**21**		D9	BI		Internal	T-NRM		4mA	
21	**22**		D10	BI		Internal	T-NRM		4mA	
22	**23**		D11	BI		Internal	T-NRM		4mA	
23	**24**		D12	BI		Internal	T-NRM		4mA	
24	**25**		D13	BI		Internal	T-NRM		4mA	
25	**26**		D14	BI		Internal	T-NRM		4mA	
26	**27**		D15	BI		Internal	T-NRM		4mA	
27	**31**		nINTR	OUT		---	---		2mA	
Total	**27**									

PIN			PERIPHERAL MODE			INPUT BUFFER			OUTPUT BUFFER	
COUNT	**PIN NO.**		**PIN NAME**	**DIRECTION**		**PULL-UP**	**TYPE**		**DRIVE**	**TYPE**
Transceiver Interface										
1	**36**		RXIN	IN		Internal	T-NRM		---	---
2	**32**		TXEN	OUT		---	---		4mA	
3	**33**		TXD	OUT		---	---		4mA	
4	**38**		RXIN2	IN		Internal	T-NRM		---	---
5	**34**		TXEN2	OUT		---	---		4mA	
Total	**5**									
Clock										
1	**63**		X1	IN		---	---		---	---
2	**64**		X2	OUT		---	---		---	---
3	**61**		MCKIN	IN		Internal	T-NRM		---	---
Total	**3**									
Setting Pins										
1	**92**		nMUX	IN		Internal	T-NRM		---	---
2	**93**		nRWM	IN		Internal	T-NRM		---	---
3	**94**		W16	IN		Internal	T-NRM		---	---
4	**95**		nSWAP	IN		Internal	T-NRM		---	---
5	**42**		NSTPRE0	IN		Internal	T-NRM		---	---
6	**43**		NSTPRE1	IN		Internal	T-NRM		---	---
7	**91**		NSTPRE2	IN		Internal	T-NRM		---	---
8	**44**		PS0	IN		Internal	T-NRM		---	---
9	**45**		PS1	IN		Internal	T-NRM		---	---
10	**46**		NID0	IN		Internal	T-NRM		---	---
11	**47**		NID1	IN		Internal	T-NRM		---	---
12	**48**		NID2	IN		Internal	T-NRM		---	---
13	**49**		NID3	IN		Internal	T-NRM		---	---
14	**50**		NID4	IN		Internal	T-NRM		---	---
15	**51**		MAXID0	IN		Internal	T-NRM		---	---
16	**52**		MAXID1	IN		Internal	T-NRM		---	---
17	**54**		MAXID2	IN		Internal	T-NRM		---	---
18	**55**		MAXID3	IN		Internal	T-NRM		---	---
19	**56**		MAXID4	IN		Internal	T-NRM		---	---
20	**57**		CKP0	IN		Internal	T-NRM		---	---
21	**58**		CKP1	IN		Internal	T-NRM		---	---
22	**59**		CKP2	IN		Internal	T-NRM		---	---
23	**39**		nDIAG	IN		Internal	T-NRM		---	---

PIN			PERIPHERAL MODE			INPUT BUFFER			OUTPUT BUFFER	
COUNT	**PIN NO.**		**PIN NAME**	**DIRECTION**		**PULL-UP**	**TYPE**		**DRIVE**	**TYPE**
24	**35**		TXENPOL	IN		Internal	T-NRM		---	---
25	**76**		WPRE0	IN		Internal	T-NRM		---	---
26	**77**		WPRE1	IN		Internal	T-NRM		---	---
27	**83**		Un-USE(High)	IN		Internal	T-NRM		---	---
28	**84**		nEHRD	IN		Internal	T-NRM		---	---
29	**85**		nEHWR	IN		Internal	T-NRM		---	---
30	**5**		nDSINV	IN		Internal	T-NRM		---	---
31	**87**		nCMIBYP	IN		Internal	T-NRM		---	---
32	**89**		nHUBON	IN		Internal	T-NRM		---	---
33	**88**		nOPMD	IN		Internal	T-NRM		---	---
34	**37**		ET1	IN		Internal	T-NRM		---	---
Total	**34**									
Output Pins										
1	**66**		nNSTCOUT	OUT		---	---		4mA	
2	**67**		FLASHO	3s.O		---	---		4mA	
3	**68**		GPIO0	3s.O		Internal	T-NRM		4mA	
4	**69**		GPIO1	3s.O		Internal	T-NRM		4mA	
5	**70**		GPIO2	3s.O		Internal	T-NRM		4mA	
6	**71**		GPIO3	3s.O		Internal	T-NRM		4mA	
7	**72**		GPIO4	3s.O		Internal	T-NRM		4mA	
8	**73**		GPIO5	3s.O		Internal	T-NRM		4mA	
9	**74**		GPIO6	3s.O		Internal	T-NRM		4mA	
10	**75**		GPIO7	3s.O		Internal	T-NRM		4mA	
Total	**10**									
Test Pins										
1	**79**		nTEST0	IN		Nothing	T-NRM		---	---
2	**80**		nTEST1	IN		Nothing	T-NRM		---	---
3	**81**		nTEST2	IN		Nothing	T-NRM		---	---
4	**82**		nTEST3	IN		Nothing	T-NRM		---	---
5	**7**		nTMODE	IN		Internal	T-NRM		---	---
Total	**5**									

PIN			PERIPHERAL MODE			INPUT BUFFER			OUTPUT BUFFER	
COUNT	**PIN NO.**		**PIN NAME**	**DIRECTION**		**PULL-UP**	**TYPE**		**DRIVE**	**TYPE**
Power Pins										
1-8	**3, 9,**		VDD	PWR		---	---		---	---
	28, 41,					---	---		---	---
	53, 62,					---	---		---	---
	78, 86					---	---		---	---
9-16	**14, 15,**		VSS	PWR		---	---		---	---
	30, 40,					---	---		---	---
	60, 65,					---	---		---	---
	90, 100					---	---		---	---
Total	**16**									
Total Pin = 100										
						(High) : Connect to VDD				
						(Open) : Not connected				
						T-NRM	TTL Level Input w/o Schmitt			
						3s/O	Tri-state Output or Normal Output			
						3s.O	Tri-state Output			

1.4 Pin Description by Functions

NOTE: * A pin name starting with "**n**" indicates an active-low pin.

1.4.1 CPU Interface (27)

D[15:6]/	Data Bus (bit15-6)
D[5:0]/AD[5:0]	Data Bus / Address Data Bus (bit5-0)
nCS	Chip Select Input
nWR/DIR	Write Signal Input / Access Direction
nRD/nDS	Read Signal Input / Data strobe
A[5:4]	Address Input
A[3]/ALEPOL	Address Input / ALE Designate Polarity
A[2]/ALE	Address Input / ALE
A[1:0]	Address (bit1-0)
nINTR	Interrupt Output (Active Low)
nRESET	Reset Input (Active Low)

1.4.2 Transceiver Interface (5)

RXIN	Port1 Receive Data Input
TXEN	Port1 Transmit Enable Output
TXD	Transmit Data Output (Port1, 2 Common)
RXIN2	Port2 Receive Data Input
TXEN2	Port2 Transmit Enable Output

1.4.3 Setup Pin (33)

nMUX	Select Address Multiplex Mode
nRWM	Select R/W Mode
W16	Select Data Bus Width
nSWAP	Select Swap Mode

nDSINV	nDS Designate Polarity
PS[1:0]	Determine Page Size (*1)
NID[4:0]	Determine MyID Number (*1)
MAXID[4:0]	Determine MAXID Number (*1)
CKP[2:0]	Determine Data Rate (*1)
NSTPRE[2:0]	NST Resolution
WPRE[1:0]	Select Warning Timer Resolution
nDIAG	Select Diagnostics Mode
ET1	Determine ARCNET Extended Timer (*1)
nEHWR	Select Enhanced Write Mode
nEHRD	Select Enhanced Read Mode
TXENPOL	TXEN,TXEN2 Designate Polarity
nOPMD	Select Optical Transceiver Mode
nCMIBYP	Bypass CMI Modem
nHUBON	ON/OFF Determine of Internal HUB function

NOTE: (*1) Could be also determined by the register at the Peripheral Mode

1.4.4 External Output or Input/output (10)

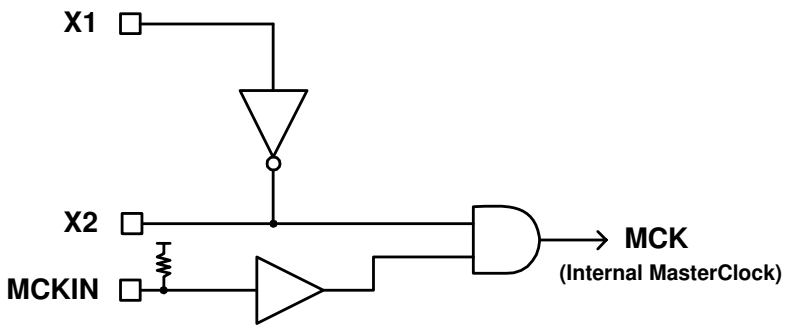
nNSTCOUT	NST Carry Output
FLASHO	Outside Output for FLASH
GPIO[7:0]	General-purpose I/O port (bit7-0)

1.4.5 Other Input (5)

nTEST[3:0]	Test Pins
nTMODE	Test Mode

1.4.6 Clock (3)

X1	Crystal Oscillator
X2	Crystal Oscillator
MCKIN	Master Clock Input



- Using an external clock :

X1 is connected to GND with MCKIN connected to the input of the external clock

- Using XTAL :

MCKIN is connected to VDD with X1, X2 connected to the Crystal Oscillator

1.5 User Setup Pins

Setup pins are strapped high or low to configure options according to system design. For low, strap to ground. Many pins have internal pullups on their input buffers. These pins can be left unconnected to keep them in high state.

1.5.1 CPU Type Selection

(nRWM: Pin)

In Peripheral mode, this pin selects the CPU type; in this case, the definition of nWR/DIR (pin) and nRD/nDS (pin) are selected. (Refer to Figure 3 - MOTOROLA CPU Mode (68hXX) and Figure 4 - INTEL CPU MODE (86XX).

[nRWM=H, nDSINV=H]

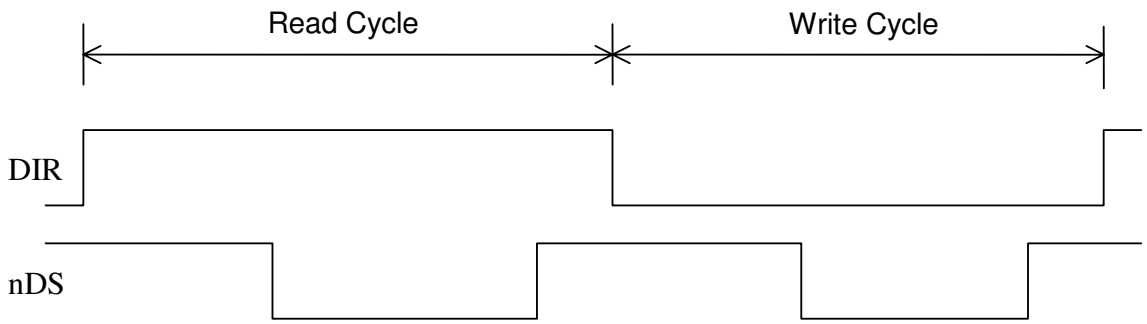


Figure 3 - MOTOROLA CPU Mode (68hXX)

[nRWM=L, nDSINV=L or H]

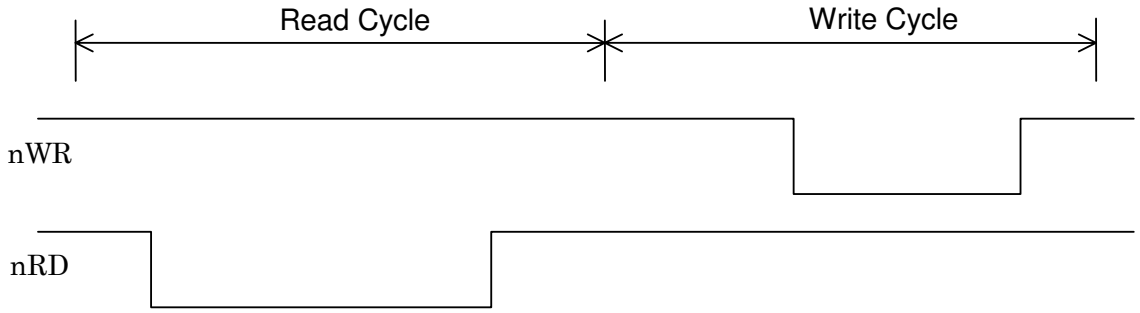


Figure 4 - INTEL CPU MODE (86XX)

1.5.2 Address Multiplex Selection

(nMUX: Pin)

In Peripheral mode, this pin specifies the system data bus from bit 5 to 0 and whether the addresses are multiplexed (Refer to Figure 5 - Non-multiplex Bus, Figure 6 - Multiplex (ALE falling-edge Type) and Figure 7 - Multiplex (ALE rising-edge Type). When the multiplexing bus option is selected, the polarity of A2/ALE is specified based on A3/ALEPOL.

[In case of nMUX=H]

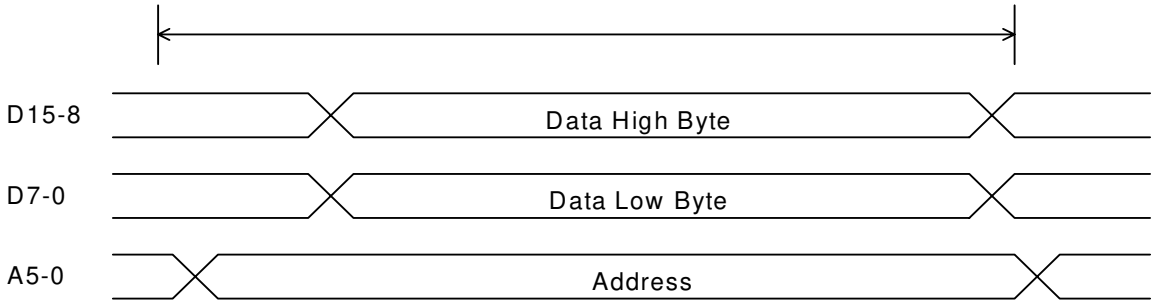


Figure 5 - Non-multiplex Bus

[In Case of nMUX=L, ALEPOL=H]

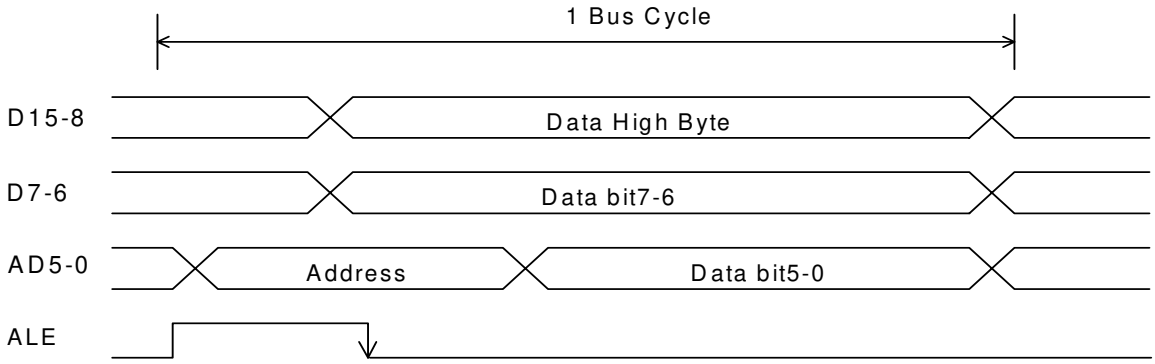


Figure 6 - Multiplex (ALE falling-edge Type)

[In case of nMUX=L, ALEPOL=L]

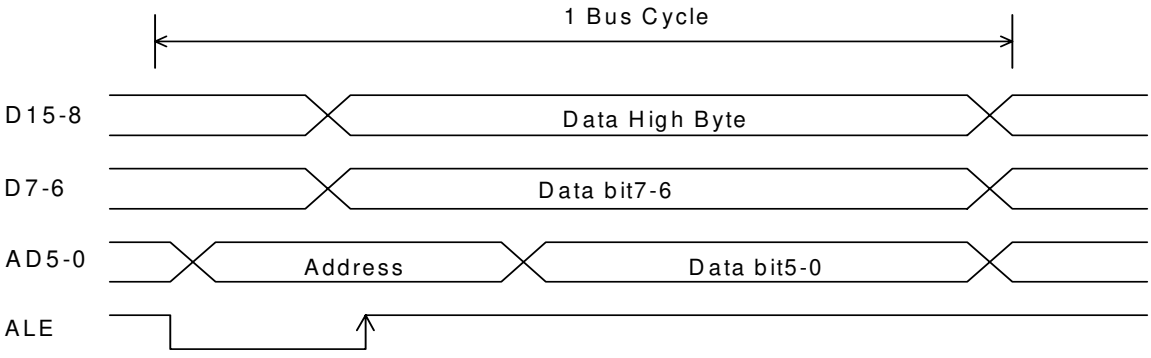


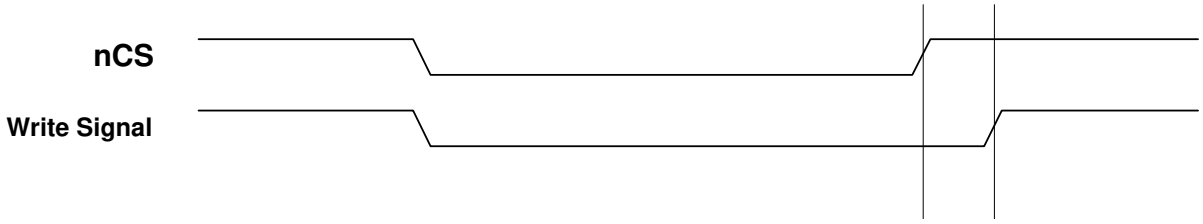
Figure 7 - Multiplex (ALE rising-edge Type)

1.5.3 Write Timing Selection

(nEHWR: Pin)

In Peripheral mode, this pin selects the write timing.

[Example: nMUX=H,nEHWR=H]



Tie to Hi for CPU's where nCS goes Hi before the write signal goes Hi.

[Example: nMUX=H,nEHWR=L]

Tie to Low for CPUs where nCS goes Hi after the write signal goes Hi.

The write signal differs depending on the CPU types.

nRWM = H: nDS signal at DIR = L

nRWM = L: nWR signal

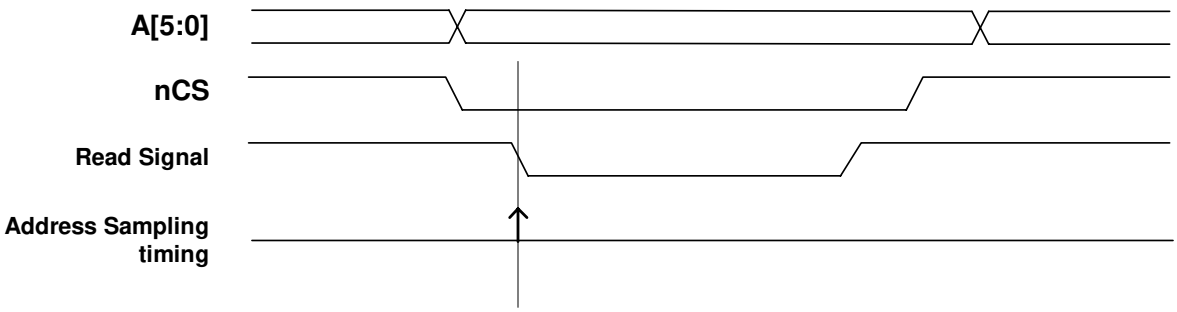
NOTE: Refer to the AC timing specifications (in another document) for details (setup time, hold time, etc.). Compare timing specifications for nEHWR=L and nEHWR=H.

1.5.4 Read Timing Selection

(nEHRD: Pin)

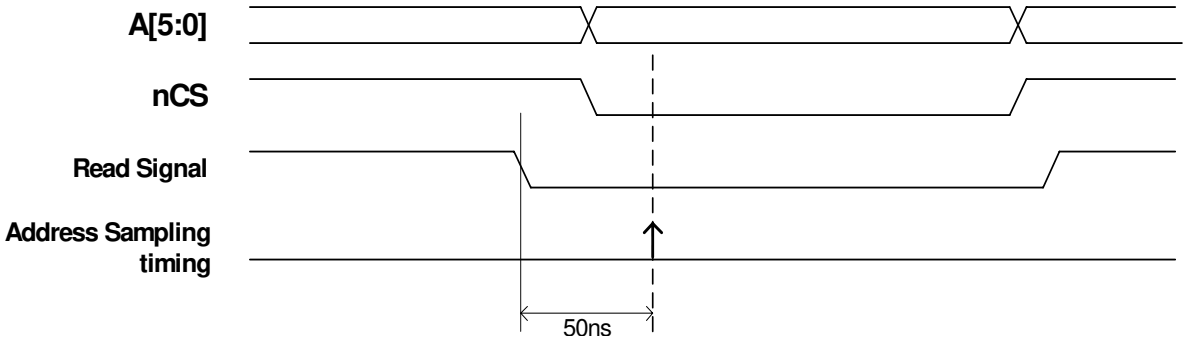
In Peripheral mode, this pin selects the read timing type.

[In case of nMUX=H,nEHRD=H]



Tie to Hi for CPUs with valid address before nCS and the read signal go low.

[Example: nMUX = H and nEHRD = L]



Tie to L for the CPU's where nCS is enabled and addresses are valid after the read signal goes low.

NOTE: Address acquisition timing in the CircLink delays about 50 ns (with 20 MHz-XTAL).

The read signal differs depending on the CPU type:

nRWM = H: nDS signal at DIR = H

nRWM = L: nRD signal

NOTE: Refer to the AC timing specifications (in another document) for details (setup time, hold time, etc.). Compare timing specifications for nEHRD=L and nEHRD=H.

1.5.5 Data Bus Width Selection

(W16: Pin)

This pin selects the bit width of the data bus in Peripheral mode; H: 16-bit mode, L: 8-bit mode. In the 16-bit mode, the LSB address in the CircLink is fixed to 0.

1.5.6 Data Bus Byte Swap

(nSWAP: Pin)

In Peripheral mode, this pin selects the data order at 8-bit access. CircLink registers are defined as 16-bit width, but 8-bit access is available and in this case the assignment of lower/upper byte of registers and odd/even numbers of the address can be changed. nSWAP=L assigns the lower byte to even number address and the upper byte to odd number address, and nSWAP=H assigns the lower byte to odd number address and the upper byte to even number address.

1.5.7 Data Strobe Polarity Specification

(nDSINV: pin)

In Peripheral mode, this pin selects the pin polarity of data strobe (nDS). It is active low with nDSINV = H and active high with nDSINV = L.

1.5.8 Page Size Selection

(PS[1:0]: Pin/Register)

Selects page size per packet. The maximum number of nodes depends on the page size selection since the packet buffer size is limited to 1 kBytes. There are two methods to specify the page size: either through pin or register settings depending on INIMODE (bit 9); 0: selects pin, 1: selects register (The default is 0).

PS[1:0]	Page Size	Max Node Number
00	256 Byte	3 Node
01	128 Byte	7 Node
10	64 Byte	15 Node
11	32 Byte	31 Node

1.5.9 MAXID Number Setup

(MAXID[4:0]: Pin/Register)

The maximum node ID is set based on the number of nodes on the network. All nodes in a CircLink network, therefore, should have the same maximum node ID. This optimizes the time required to reconfigure the network. There are two methods to specify the maximum node ID, Either through pin or register settings depending on INIMODE (bit 9); 0: selects pin, 1: selects register (The default is 0). If the nDIAG pin is set to L as the exception, however, the maximum node ID is automatically set to the largest value. For more details, refer to section 2.10 - Diagnostic Mode.

1.5.10 Node ID Setup

(NID[4:0]: Pin/Register)

Sets node ID. A unique number must be assigned to each node in the network in ascending order starting from ID=01. However, ID = 00 and an ID that is larger than the maximum node ID are not valid. There are two methods to assign the node ID, either through pin or register, settings depending on INIMODE (bit 7) 0: selects pin, 1: select register (The default is 0).

MAXID[4:0] determines the maximum node ID value. The token will only be passed around the nodes whose IDs are equal to or less than the maximum ID value. In the CircLink network, a node whose MAXID[4:0] and NID[4:0] matches is the node initiating the token passing.. Even if this particular node is absent from the network, the network reconfiguration time is greatly reduced because the network will be reconfigured only for the nodes with IDs less than MAXID[4:0]. Also, given that the maximum number of nodes is fixed to 31 in a CircLink network, the original priority time of ARCNET, (255 – ID) x 146 μs* , which determines the waiting time for network reconfiguration initiation, is modified to (31-ID) x 146 μs, greatly reducing reconfiguration time. Refer to section 2.4.2 - Reduction of Network Reconfiguration Time for more details.

NOTE: * 146 μs is defined under operation at 2.5 Mbps based on the ARCNET protocol. The time is half at 5 Mbps.

1.5.11 NST Resolution Setup

(NSTPRE[2:0]: Pin)

Selects the resolution of the network standard time counter (NST). Refer to section 2.11 - Network Standard Time (NST) for details.

1.5.12 Standalone Mode Specification (Not supported)

TMC2072 does not support standalone mode.

1.5.13 Warning Timer Resolution

(WPRE[1:0]: Pin]

These pins select the warning timer resolution in Peripheral mode. Refer to section 2.9.4 - Warning Timer (WT) at Remote Buffer Receive for more details.

1.5.14 Diagnosis Mode

(nDIAG: Pin)

This pin sets CircLink to the diagnosis mode. nDIAG to 0 forcibly fixes the MAXID to “1Fh”. Refer to section 2.10 - Diagnostic Mode for details.

1.5.15 Prescaler Setup for Communication Speed

(CKP[2:0]: Pin/Register)

CKP2-0	Prescale	Communication Speed			
		40MHz XTAL	20MHz XTAL	32MHz XTAL	16MHz XTAL
000	8	5Mbps	2.5Mbps	4Mbps	2Mbps
001	16	2.5Mbps	1.25Mbps	2Mbps	1Mbps
010	32	1.25Mbps	625Kbps	1Mbps	500Kbps
011	64	625Kbps	312.5Kbps	500Kbps	250Kbps
100	128	312.5Kbps	156.25Kbps	250Kbps	125Kbps
101	256	156.25Kbps	78.125Kbps	125Kbps	62.5Kbps
110	reserved	reserved	reserved	reserved	reserved
111	reserved	reserved	reserved	reserved	reserved

Communication speed (transfer rate) selection for CircLink. There are two methods to determine the communication speed, either through pin or register settings, depending on the specification of INIMODE (bit 9); 0: pin, 1: register (Default is 0).

1.5.16 CPU Interface Bus Timing Selection

(nEHWR, nEHRD: Pin)

For the functions using Peripheral mode, refer to sections 1.5.3 and 1.5.4.

1.5.17 CMI Bypass Specification

(nCMIBYP: Pin)

Selects bypassing the CMI code/encoding. nCMIBYP = L bypasses the CMI coding/decoding circuit so that encoding is RZ form signal interface, equivalent to the ARCNET back plane mode.

1.5.18 ON/OFF of HUB Function

(nHUBON: Pin)

Selects ON/OFF ; nHUBON=H selects the HUB function OFF, nHUBON=L selects the HUB function ON and enables the port 2 (RXIN2 and TXEN2) available. (in nHUBON = H, RXIN2 should be fixed to High.)

Refer to section 2.13 - HUB Function for the detailed operations.

1.5.19 Optical Transceiver Mode

(nOPMD: Pin)

Selects the output mode of the sending-enable; nOPMD = H makes the optical transceiver mode unavailable and allows the TXEN and TXEN2 output pins to function as “sending-enable”. Setting nOPMD = L allows TXEN and TXEN2 output pins to function as “sending-enable and sending pulse” to be able to be directly connected to the TTL input pin of the optical transceiver.

1.5.20 TXEN Polarity Select

(TXENPOL: Pin)

Selects the output polarities of the TXEN and TXEN2 signals. TXENPOL = L selects negative logic and TXENPOL = H selects positive logic.

1.5.21 Extension Timer Setting 1

(ET1: Pin/Register)

Refer to section 2.13 - HUB Function for operational details.

1.5.22 Test Pins

(nTEST[3:0], nTMODE: Pin)

All pins must be connected to VDD.

Chapter 2 Functional Description

2.1 Communication Specification

- Data transfer bit rate	78.125 kbps to 2.5 Mbps (at 20 MHz Xtal), (5 Mbps at 40-MHz Xtal)
- The max. number of nodes	31 (ID = 00 is not available for user)
- Data transfer check	Only the destination node can check data transfer. Other nodes, however, can receive (monitor) the same data.
- Protocol	Enhanced version of ARCNET (token passing)
- Packet size	256 bytes max. (User area: 253 bytes max.)

2.2 Message Class

The following five classes of messages are identical to those in the ARCNET protocol. Refer to the ARCNET Controller COM20020 Rev. D Datasheet for more details.

ITT (Token)

ALERT	EOT	DID	DID

FBE (Free Buffer Enquiries)

ALERT	ENQ	DID	DID

ACK (Acknowledgements)

ALERT	ACK

NAK (Negative Acknowledgements)

ALERT	NAK

PACKET (Data Packets)

ALERT	SOH	SID	DID	DID	CP	DATA X n	CRC	CRC

N : MAX253
(ARCNET Layer)