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TMC2074

Dual Mode CircLink™ Controller

Datasheet

PRODUCT FEATURES

- Low Power CMOS, 3.3 Volt Power Supply with 5 Volt Tolerant I/O
- Supports 8/16-Bit Data Bus
  - Both 86xx and 68hxx Platforms
- 1K On-chip Dual Port Buffer Memory
  - Sequential I/O Mapped Access
- Enhanced Token Passing Protocol from ARCNET
  - Maximum 31 Nodes per Network
  - Token Retry Mechanism
  - Maximum 256 Bytes per Packet
  - Consecutive Node ID Assignment
- Memory Mirror
  - Shared Memory within Network
- Network Standard Time
  - Network Time Synchronization
  - Automatic Time Stamping
- Coded Mark Inversion
  - Intelligent 1-Bit Error Correction
  - Magnetic Saturation Prevention
- Dual Operation Modes
  - Peripheral (Host) Mode Operates with MCU
  - Standalone (I/O) Mode Operates without MCU
- Supports 8 Bit Programmable General Purpose I/O at peripheral Mode
- Supports 16 Bit Input and 16 Bit Output at Standalone Mode
- Dual Communication Modes (with Peripheral Mode)
  - Free Format Mode
  - Remote Buffer Mode
- 3 Port Hub Integrated
  - 1 Internal and 2 External
- Flexible Topologies
  - Bus, Star and Tree
- Low Cost Media can be Used
  - RS485 Differential Driver
- Fiber Optics and Twisted Pair Cable Supported
- 128-Pin, VTQFP Lead-free RoHS Compliant Package
- Temperature Range from 0 to 70 Degrees C

ORDERING INFORMATION

Order Number(s):

TMC2074-NU for 128 Pin, VTQFP Lead-Free RoHS Compliant Package

80 ARKAY DRIVE, HAUPPAUGE, NY 11788 (631) 435-6000, FAX (631) 273-3123

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Chapter 1 General Description

1.1 About CircLink

The CircLink networking controller was developed for small control-oriented local network data communication based on ARCNET's token-passing protocol that guarantees message integrity and calculatable maximum cycle time.

In a CircLink network, when a node receives the token it becomes the temporary master of the network for a fixed, short period of time. No node can dominate the network since token control must be relinquished when transmission is complete. Once a transmission is completed the token is passed on to the next node (logical neighbor), allowing it to be come the master.

Because of this token passing scheme, maximum waiting time for network access can be calculated and the time performance of the network is predictable or deterministic. Control networking applications require predictable performance to ensure that controlled events occur when required. However, reconfiguration of a regular ARCNET network becomes necessary when the token is missed due to electronic and magnetic noise. In these cases, the maximum wait time for sending datagrams cannot be guaranteed and the real-time characteristic is impaired. CircLink makes several modification to the original ARCNET protocol (such as maximum and consecutive node ID assignment) to avoid token missing as much as possible and reduce the network reconfiguration time.

CircLink implements other enhancements to the ARCNET protocol including a smaller-sized network , shorter packet size, and remote buffer mode operation that enable more efficient and reliable small, control-oriented LANs. In addition, CircLink introduces several unique features for reducing overall system cost while increasing system reliability.

CircLink can operate under a special mode called "Standalone" or "I/O" mode. In this mode, CircLink does not need an administrating CPU for each node. Only one CPU is needed to manage a CircLink network composed up to maximum 31 nodes, reducing cost and complexity.

In a CircLink network, the data sent by the source node is received by all other nodes in the network and stored according to node source ID. For the target node the received data is executed per ARCNET flow control and the data is stored in its buffer RAM. The receiving node processes the data while the remaining nodes on the network discard the data when the receiving node has completed. This memory-mirroring function assures higher reliability and significantly reduces network traffic.

Network Standard Time (NST) is also a unique CircLink feature. NST is realized by synchronizing the individual local time on each network node to the clock master in the designated node from which the packet is sent. CircLink also uses CMI code for transmitting signals, rather than the dipulse or bipolar signals that are the standard ARCNET signals. Since CMI encoding eliminates the DC element, a simple combination of a standard RS485 IC and a pulse transformer can be used to implement a transformer-coupled network.

1.2 About TMC2074

The TMC2074 network controller is CircLink technology's flagship product. The TMC2074's flexibility and rich feature set enable a high-reliability and high-performance, real-time and control-oriented network without the cumbersome middle layer protocol stacks and complex packet prioritization schemes typically required.

TMC2074 operates at network data transfer rates up to 5 Mbps. Its embedded 1 kByte RAM can be configured into a maximum of 32 pages to implement a 31-node network where each node in the network has the same local memory.

The TMC2074 has two operational modes: "Peripheral Mode" and "Standalone Mode". It can operate with or without the existence of a system CPU on a network node. In Peripheral Mode, the TMC2074 has two selectable communication modes, "Free Format Mode" and "Remote Buffer Mode". Free Format mode, retained from ARCNET, is "packet oriented" communication. Remote Buffer mode communication is a CircLink-specific feature, and is a token oriented communication, which includes automatic data transmission when the token arrives.

The TMC2074 has a flexible 8-bit or 16-bit databus to interface various CPU types including X86, 68XX, and SHX with multiplexed or non-multiplexed address/data. When operating in Peripheral mode, the TMC2074 has 8-bit programmable I/O available. When operating in Standalone mode, the TMC2074's I/O configuration is16-bit. The TMC2074 also integrates a 3-port hub (two ports for external connection) to accommodate various network topologies (Bus, Star, etc.) and combinations.

1.3 Internal Block Diagram

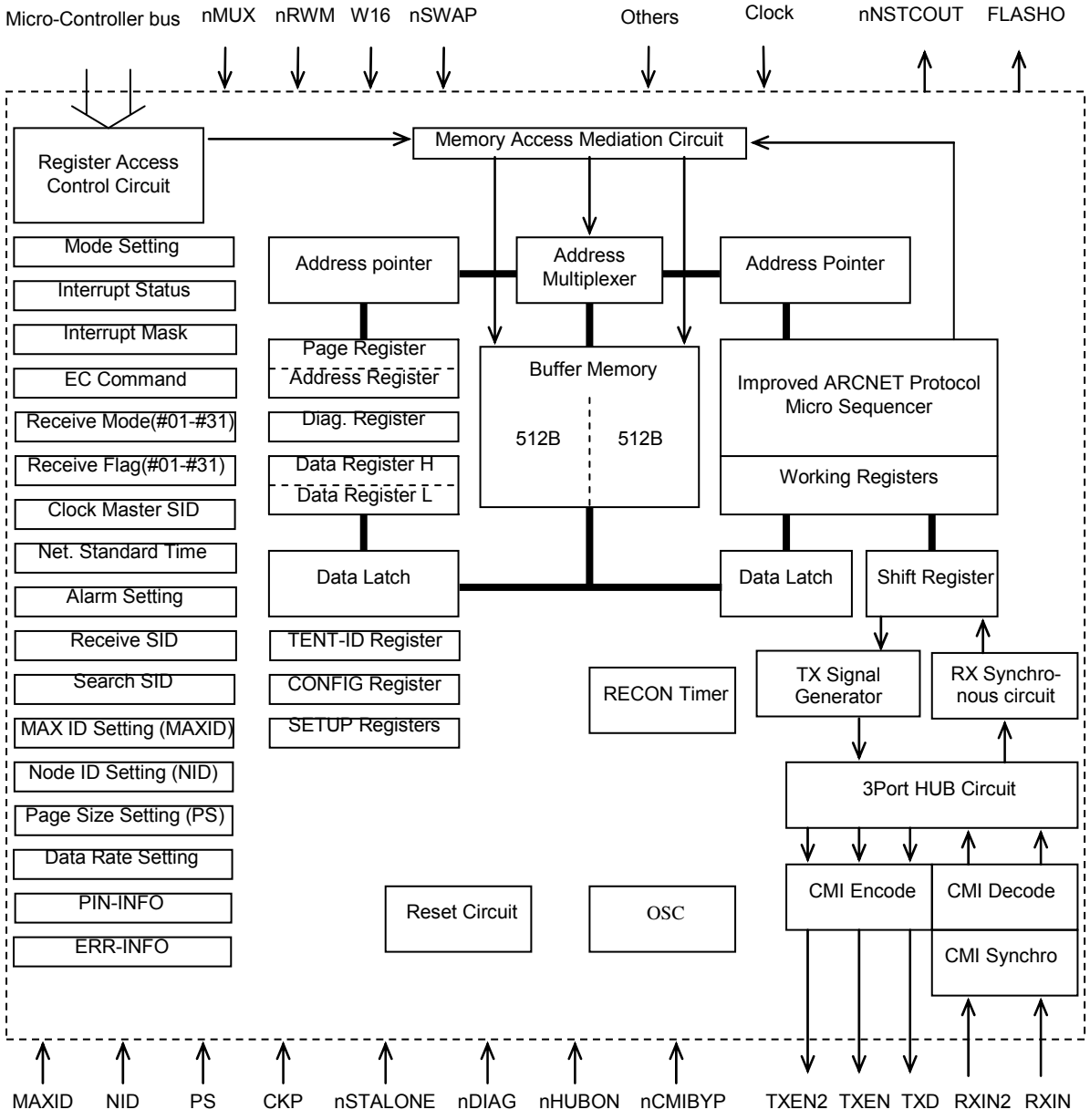


Figure 1 - TMC2074 Block Diagram

1.4 Pin Configuration

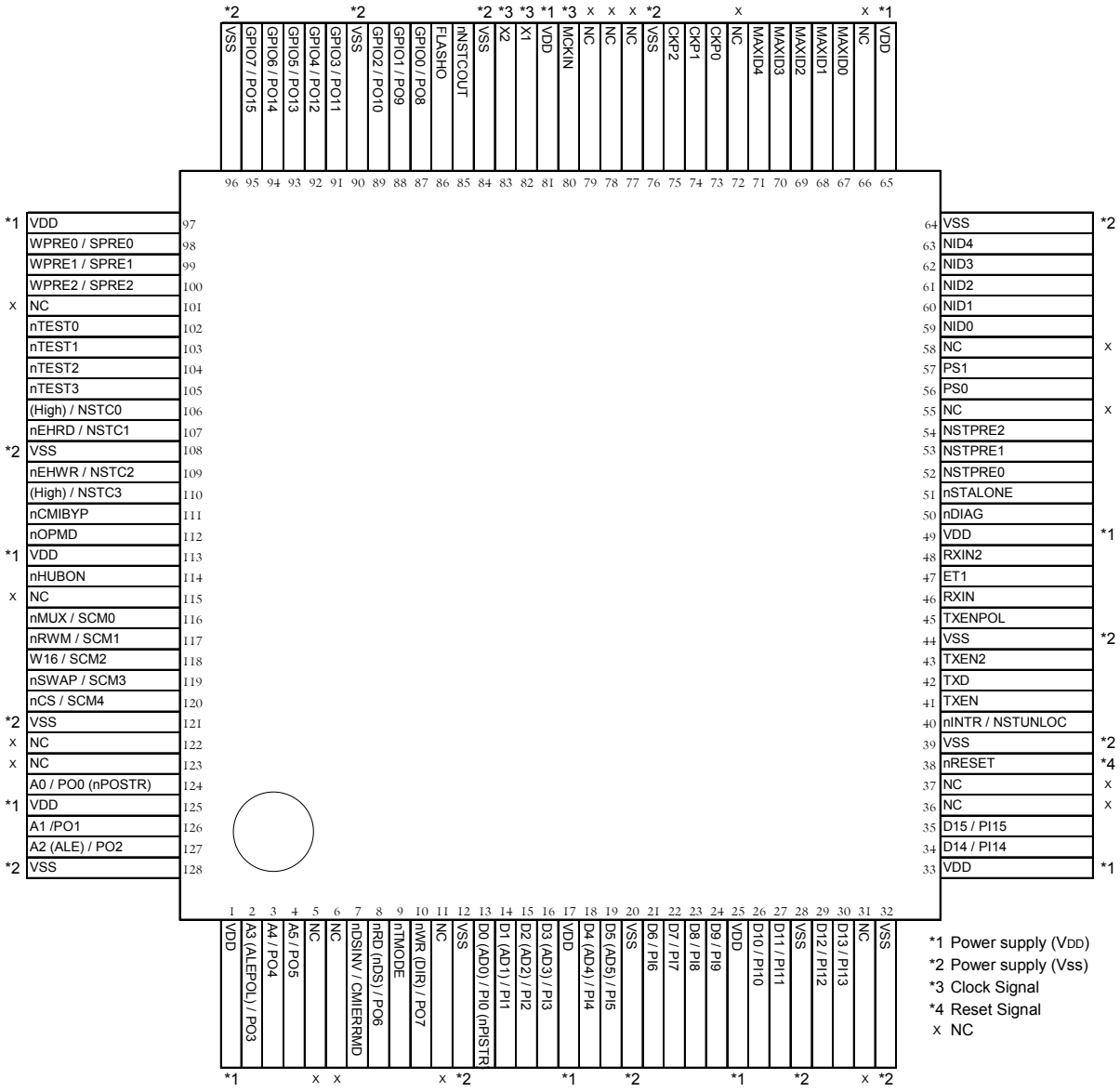


Figure 2 - Pin Names: Pin Name in Peripheral Mode/Pin Name in Standalone Mode

Table 1- Pin Lists Sorted by Function

Pin		Peripheral Mode		Standalone Mode		Input Buffer		Output Buffer	
Count	Pin NO.	Pin Name	Direction	Pin Name	Direction	Pull-Up	Type	Drive	Type
CPU Interface									
1	**38**	nRESET	IN	nRESET	IN	Internal	T-NRM	---	---
2	**120**	nCS	IN	SCM4	IN	Internal	T-NRM	---	---
3	**124**	A0	IN	PO0/nPOSTR	3s/O	Internal	T-NRM	4mA	
4	**126**	A1	IN	PO1	3s.O	Internal	T-NRM	4mA	
5	**127**	A2/ALE	IN	PO2	3s.O	Internal	T-NRM	4mA	
6	**2**	A3/ALEPOL	IN	PO3	3s.O	Internal	T-NRM	4mA	
7	**3**	A4	IN	PO4	3s.O	Internal	T-NRM	4mA	
8	**4**	A5	IN	PO5	3s.O	Internal	T-NRM	4mA	
9	**8**	nRD/nDS	IN	PO6	3s.O	Internal	T-NRM	4mA	
10	**10**	nWR/DIR	IN	PO7	3s.O	Internal	T-NRM	4mA	
11	**13**	D0/AD0	BI	PI0/nPISTR	IN	Internal	T-NRM	4mA	
12	**14**	D1/AD1	BI	PI1	IN	Internal	T-NRM	4mA	
13	**15**	D2/AD2	BI	PI2	IN	Internal	T-NRM	4mA	
14	**16**	D3/AD3	BI	PI3	IN	Internal	T-NRM	4mA	
15	**18**	D4/AD4	BI	PI4	IN	Internal	T-NRM	4mA	
16	**19**	D5/AD5	BI	PI5	IN	Internal	T-NRM	4mA	
17	**21**	D6	BI	PI6	IN	Internal	T-NRM	4mA	
18	**22**	D7	BI	PI7	IN	Internal	T-NRM	4mA	
19	**23**	D8	BI	PI8	IN	Internal	T-NRM	4mA	
20	**24**	D9	BI	PI9	IN	Internal	T-NRM	4mA	
21	**26**	D10	BI	PI10	IN	Internal	T-NRM	4mA	
22	**27**	D11	BI	PI11	IN	Internal	T-NRM	4mA	
23	**29**	D12	BI	PI12	IN	Internal	T-NRM	4mA	
24	**30**	D13	BI	PI13	IN	Internal	T-NRM	4mA	
25	**34**	D14	BI	PI14	IN	Internal	T-NRM	4mA	
26	**35**	D15	BI	PI15	IN	Internal	T-NRM	4mA	
27	**40**	nINTR	OUT	NSTUNLOC	OUT	---	---	4mA	
Total:27									
Transceiver Interface									
1	**46**	RXIN	IN	RXIN	IN	Internal	T-NRM	---	---
2	**41**	TXEN	OUT	TXEN	OUT	---	---	4mA	
3	**42**	TXD	OUT	TXD	OUT	---	---	4mA	
4	**48**	RXIN2	IN	RXIN2	IN	Internal	T-NRM	---	---
5	**43**	TXEN2	OUT	TXEN2	OUT	---	---	4mA	
Total:5									
Clock									
1	**82**	X1	IN	X1	IN	---	---	---	---
2	**83**	X2	OUT	X2	OUT	---	---	---	---
3	**80**	MCKIN	IN	MCKIN	IN	Internal	T-NRM	---	---
Total:3									

Pin		Peripheral Mode		Standalone Mode		Input Buffer		Output Buffer	
Count	Pin NO.	Pin Name	Direction	Pin Name	Direction	Pull-Up	Type	Drive	Type
Setup Pins									
1	**116**	nMUX	IN	SCM0	IN	Internal	T-NRM	—	—
2	**117**	nRWM	IN	SCM1	IN	Internal	T-NRM	—	—
3	**118**	W16	IN	SCM2	IN	Internal	T-NRM	—	—
4	**119**	nSWAP	IN	SCM3	IN	Internal	T-NRM	—	—
5	**52**	NSTPRE0	IN	NSTPRE0	IN	Internal	T-NRM	—	—
6	**53**	NSTPRE1	IN	NSTPRE1	IN	Internal	T-NRM	—	—
7	**54**	NSTPRE2	IN	NSTPRE2	IN	Internal	T-NRM	—	—
8	**56**	PS0	IN	PS0	IN	Internal	T-NRM	—	—
9	**57**	PS1	IN	PS1	IN	Internal	T-NRM	—	—
10	**59**	NID0	IN	NID0	IN	Internal	T-NRM	—	—
11	**60**	NID1	IN	NID1	IN	Internal	T-NRM	—	—
12	**61**	NID2	IN	NID2	IN	Internal	T-NRM	—	—
13	**62**	NID3	IN	NID3	IN	Internal	T-NRM	—	—
14	**63**	NID4	IN	NID4	IN	Internal	T-NRM	—	—
15	**67**	MAXID0	IN	MAXID0	IN	Internal	T-NRM	—	—
16	**68**	MAXID1	IN	MAXID1	IN	Internal	T-NRM	—	—
17	**69**	MAXID2	IN	MAXID2	IN	Internal	T-NRM	—	—
18	**70**	MAXID3	IN	MAXID3	IN	Internal	T-NRM	—	—
19	**71**	MAXID4	IN	MAXID4	IN	Internal	T-NRM	—	—
20	**73**	CKP0	IN	CKP0	IN	Internal	T-NRM	—	—
21	**74**	CKP1	IN	CKP1	IN	Internal	T-NRM	—	—
22	**75**	CKP2	IN	CKP2	IN	Internal	T-NRM	—	—
23	**51**	nSTALONE=H	IN	nSTALONE=L	IN	Internal	T-NRM	—	—
24	**50**	nDIAG	IN	nDIAG	IN	Internal	T-NRM	—	—
25	**45**	TXENPOL	IN	TXENPOL	IN	Internal	T-NRM	—	—
26	**98**	WPRE0	IN	SPRE0	IN	Internal	T-NRM	—	—
27	**99**	WPRE1	IN	SPRE1	IN	Internal	T-NRM	—	—
28	**100**	WPRE2	IN	SPRE2	IN	Internal	T-NRM	—	—
29	**106**	Un-USE(High)	IN	NSTC0	IN	Internal	T-NRM	—	—
30	**107**	nEHRD	IN	NSTC1	IN	Internal	T-NRM	—	—
31	**109**	nEHWR	IN	NSTC2	IN	Internal	T-NRM	—	—
32	**110**	Un-USE(High)	IN	NSTC3	IN	Internal	T-NRM	—	—
33	**7**	nDSINV	IN	CMERRMD	IN	Internal	T-NRM	—	—
34	**111**	nCMBYP	IN	nCMBYP	IN	Internal	T-NRM	—	—
35	**114**	nHUBON	IN	nHUBON	IN	Internal	T-NRM	—	—
36	**112**	nOPMD	IN	nOPMD	IN	Internal	T-NRM	—	—
37	**47**	ET1	IN	ET1	IN	Internal	T-NRM	—	—
Total:37									

Pin		Peripheral Mode		Standalone Mode		Input Buffer		Output Bufer	
Count	Pin NO.	Pin Name	Direction	Pin Name	Direction	Pull-Up	Type	Drive	Type
Output or I/O Pins									
1	**85**	nNSTCOUT	OUT	nNSTCOUT	OUT	---	---	4mA	
2	**86**	FLASHO	3s.O	FLASHO	3s.O	---	---	4mA	
3	**87**	GPIO0	3s.O	PO8	3s.O	Internal	T-NRM	4mA	
4	**88**	GPIO1	3s.O	PO9	3s.O	Internal	T-NRM	4mA	
5	**89**	GPIO2	3s.O	PO10	3s.O	Internal	T-NRM	4mA	
6	**91**	GPIO3	3s.O	PO11	3s.O	Internal	T-NRM	4mA	
7	**92**	GPIO4	3s.O	PO12	3s.O	Internal	T-NRM	4mA	
8	**93**	GPIO5	3s.O	PO13	3s.O	Internal	T-NRM	4mA	
9	**94**	GPIO6	3s.O	PO14	3s.O	Internal	T-NRM	4mA	
10	**95**	GPIO7	3s.O	PO15	3s.O	Internal	T-NRM	4mA	
Total:10									
Test Pins									
1	**102**	nTEST0	IN	nTEST0	IN	Nothing	T-NRM	---	---
2	**103**	nTEST1	IN	nTEST1	IN	Nothing	T-NRM	---	---
3	**104**	nTEST2	IN	nTEST2	IN	Nothing	T-NRM	---	---
4	**105**	nTEST3	IN	nTEST3	IN	Nothing	T-NRM	---	---
5	**9**	nTMODE	IN	nTMODE	IN	Internal	T-NRM	---	---
Total	**5**								
Power Pins									
1-10	1,17,25, 33,49,65 ,81,97, 113,125	VDD	PWR	VDD	PWR	---	---	---	---
11-24	12,20,28, 32,39,44, 64,76,84, 90,96,108 ,121,128	VSS	PWR	VSS	PWR	---	---	---	---
Total	**24**								
NC Pins									
1-17	5,6,11,31, 36,37,55, 58,66,72, 77,78,79, 101,115, 122,123	NC (Open)	---	NC (Open)	---	---	---	---	---
Total	**17**								

Total Pin = 128

(High) : Connect to VDD
(Open) : Not Connect

T-NRM TTL Level Input w/o schmitt
3s/O Tri-state Output or Normal Output
3s.O Tri-state Output

1.5 Pin Description by Functions

* A pin name starting with “n” indicates an active-low pin.

1.5.1 CPU Interface Pins (27)

D[15:6]/PI[15:6]	Data Bus / Standalone Input Port (bit15-6)
D[5:1]/AD[5:1]/PI[5:1]	Data Bus / Address Data Bus / Standalone Input Port (bit5-1)
D[0]//AD[0]//PI[0]/nPISTR	Data Bus / Address Data Bus / Standalone Input Port (bit5-0) /Standalone strobe Input Port
nCS/SCM[4]	Chip Select Input / Standalone Designate CMID (bit4)
nWR/DIR/PO[7]	Write Signal Input / Access Direction / Standalone Input Port (bit7)
nRD/nDS/PO[6]	Read Signal Input / Data strobe / Standalone Input Port (bit6)
A[5:4]/PO[5:4]	Address Input / Standalone Input Port (bit5-4)
A[3]/ALEPOL/PO[3]	Address Input / ALE Designate Polarity / Standalone Output Port (bit3)
A[2]/ALE/PO[2]	Address Input / ALE / Standalone Output Port (bit2)
A[1]/PO[1]	Address Input / Standalone Output Port (bit1)
A[0]/PO[0]]/nPOSTR	Address Input / Standalone Output Port (bit0) / Standalone strobe Input Port
nINTR/NSTUNLOC	Interrupt Output / NSTUNLOC Flag Output for Standalone
nRESET	Reset Input (Active Low)

1.5.2 Transceiver Interface Pins (5)

RXIN	Port1 Receive Data Input
TXEN	Port1 Transmit Enable Output
TXD	Transmit Data Output (Port1 & 2 Common)
RXIN2	Port2 Receive Data Input
TXEN2	Port2 Transmit Enable Output

1.5.3 Setup Pins (37)

nMUX/SCM[0]	Select Address Multiplex Mode/Standalone Designate CMID (bit0)
nRWM/SCM[1]	Select R/W Mode / Standalone Designate CMID (bit1)
W16/SCM[2]	Select Data Bus Width / Standalone Designate CMID (bit2)
nSWAP/SCM[3]	Select Swap Mode / Standalone Designate CMID (bit3)
nDSINV/CMIERRMD	nDS Designate Polarity / Standalone CMI Receive Error Mode
PS[1:0]	Determine Page Size (*1)
NID[4:0]	Determine MyID Number (*1)
MAXID[4:0]	Determine MAXID Number (*1)
CKP[2:0]	Determine Data Rate (*1)
NSTPRE[2:0]	NST Resolution
nSTALONE	Select Standalone Mode
WPRE[2:0]/SPRE[2:0]	Select Warning Timer Resolution / Standalone TX Schedule
nDIAG	Select Diagnostics Mode
ET1	Determine ARCNET Extended Timer (*1)
NSTC[3]	Select NST Carry Output Digit in Standalone Mode bit[3]
nEHWR/NSTC[2]	Enhanced Write / NST Carry Output Digit in Standalone Mode bit[2]
nEHRD/NSTC[1]	Enhanced Read / NST Carry Output Digit in Standalone Mode bit[1]
NSTC[0]	NST Carry Output Digit in Standalone Mode bit[0]
TXENPOL	TXEN,TXEN2 Designate Polarity
nOPMD	Select Optical Transceiver Mode
nCMIBYP	Bypass CMI Modem
nHUBON	ON/OFF Determine of Internal HUB function

(*1) Could be also determined by the register at the Peripheral Mode

1.5.4 External Output or I/O Pins (10)

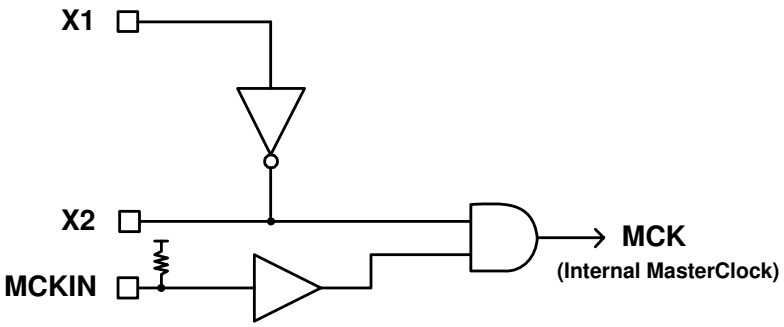
nNSTCOUT	NST Carry Output
FLASHO	Outside Output for FLASH

GPIO[7:0]/PO[15:8]	General-purpose I/O port (bit7-0) / Standalone Output Port (bit15-8)

1.5.5 Test Pins (5)

nTEST[3:0]	Test Pins
nTMODE	Test Mode

1.5.6 Clock Pins (3)



- Using an external clock :

X1 is connected to GND with MCKIN connected to the input of the external clock

- Using XTAL:

MCKIN is connected to VDD with X1 , X2 connected to the Crystal Oscillator

1.6 Setup Pins

Setup pins are strapped high or low to configure options according to system design. For low, strap to ground. Many pins have internal pullups on their input buffers. These pins can be left unconnected to keep them in high state.

1.6.1 CPU Type Selection

(nRWM/SCM[1]: Pin)

- Peripheral mode: This pin selects the CPU type; in this case, the definition of nWR/DIR (pin) and nRD/nDS (pin) are selected (refer to Figure 3 - Motorola CPU Mode (68hxx).
- Standalone mode: This pin is the clock –master-ID-specification input SCM[1].

[nRWM=H, nDSINV=H]

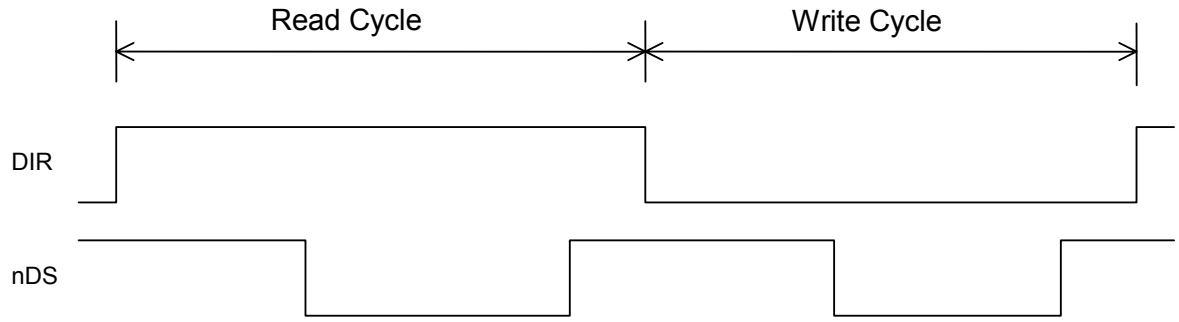


Figure 3- Motorola CPU Mode (68hxx)

[nRWM=L, nDSINV=L or H]

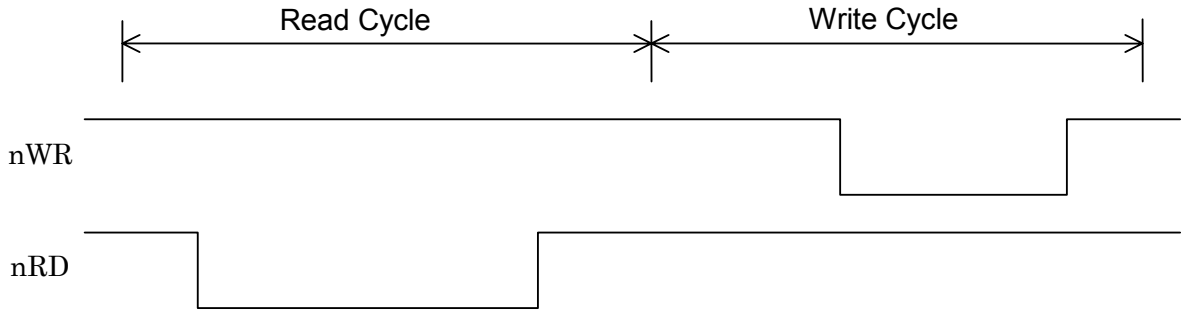


Figure 4 - Intel CPU Mode (86xx)

1.6.2 Address Multiplex Selection

(nMUX/SCM[0]: Pin)

In peripheral mode, this pin specifies the system data bus from bit5 to 0 and whether or not the addresses are multiplexed (Refer to Figure 5 - Non-Multiplex Bus). When the multiplexing bus option is selected, the polarity of A2/ALE is specified based on A3/ALEPOL. In standalone mode, this pin is the clock-master-ID-specification input SCM[0].

[In case of nMUX=H]\

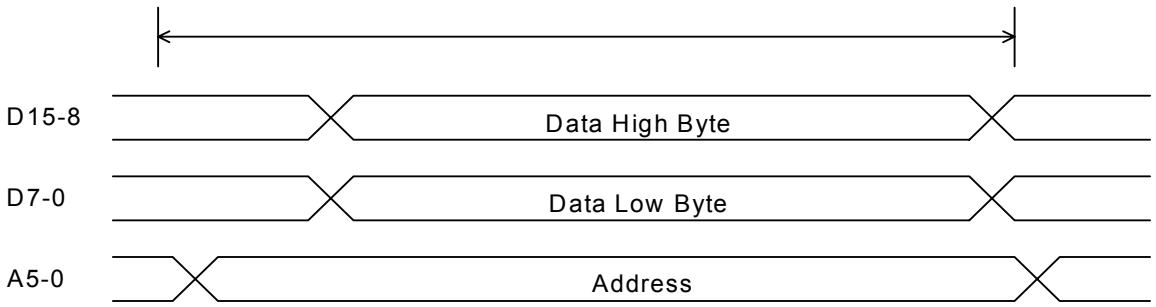


Figure 5 - Non-Multiplex Bus

[In Case of nMUX=L, ALEPOL=H]

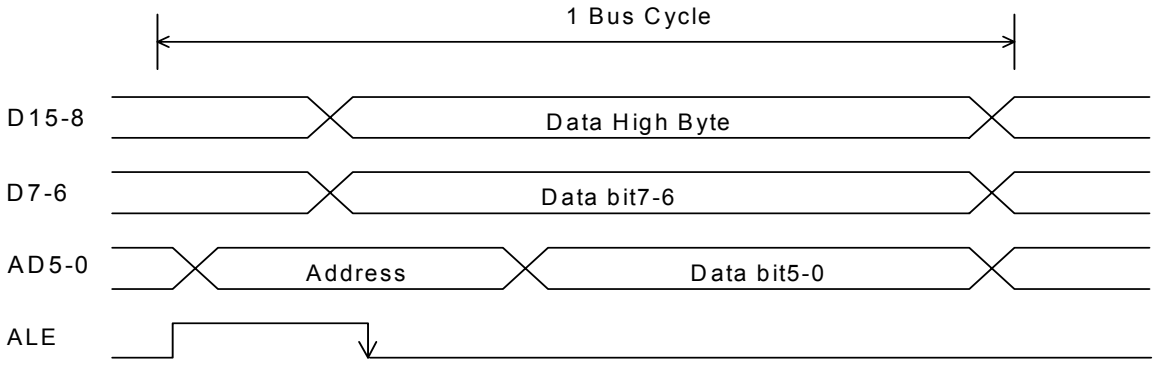


Figure 6 - Multiplex (Ale Falling-Edge Type)

[In case of nMUX=L, ALEPOL=L]

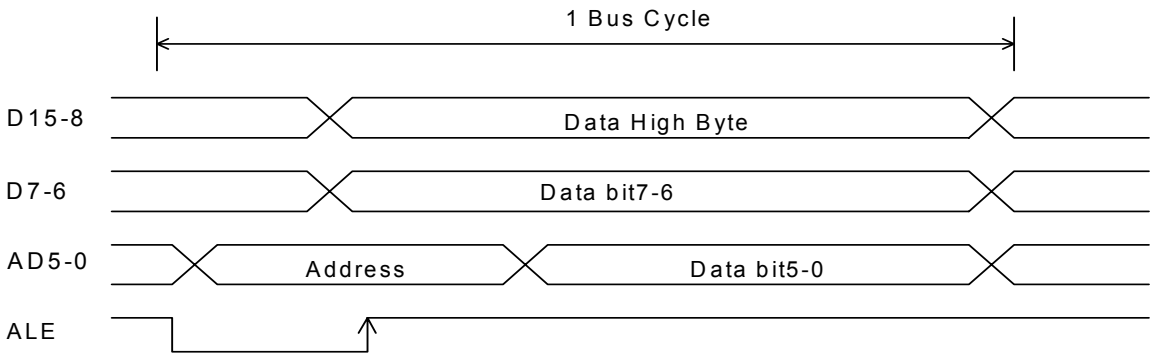


Figure 7 - Multiplex (Ale Rising-Edge Type)

1.6.3 Write Timing Selection

(nEHWR/NSTC[2]: Pin)

- Peripheral mode: This pin selects the write timing.
- Standalone mode: This pin is NST- carry-output-digit-selection NSTC[2].

[Example: nMUX=H,nEHWR=H]

Tie to Hi for CPU's where nCS goes Hi before the write signal goes Hi.

[Example: nMUX=H,nEHWR=L]

Tie to Low for CPUs where nCS goes Hi after the write signal goes Hi.

The write signal differs depending on the CPU type:

nRWM = H: nDS signal at DIR = L

nRWM = L: nWR signal

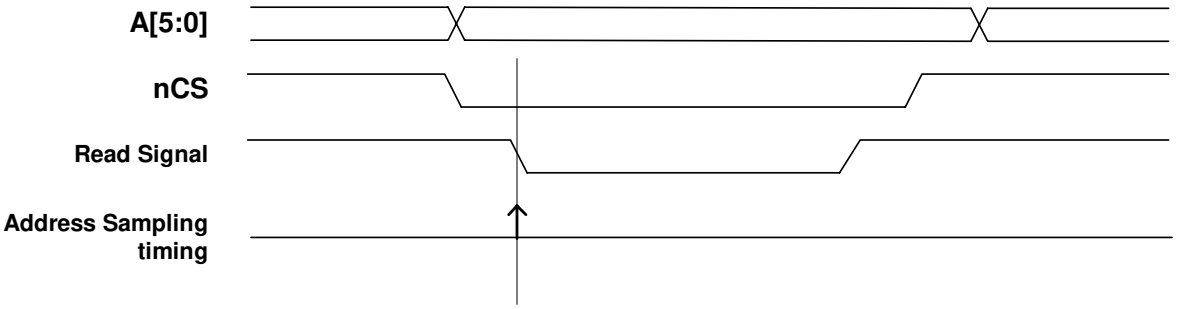
NOTE: Refer to the AC timing specifications (in another document) for details (setup time, hold time, etc.). Compare timing specifications for nEHWR=L and nEHWR=H.

1.6.4 Read Timing Selection

(nEHRD/NSTC[1]: Pin)

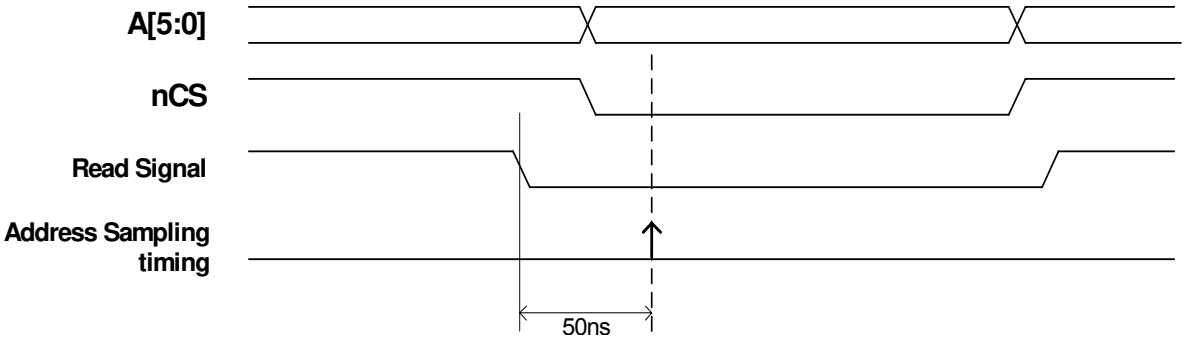
- Peripheral mode: This pin selects the read timing type.
- Standalone mode: This is NST- carry-output-digit selection NSTC[1].

[In case of nMUX=H,nEHRD=H]



Tie to Hi for CPUs with valid address before nCS and the read signal go low.

[Example: nMUX = H and nEHRD = L]



Tie to L for the CPU's where nCS is enabled and addresses are valid after the read signal goes low.

NOTE: Address acquisition timing in the CircLink delays about 50 ns (with 20 MHz-XTAL).

The read signal differs depending on the CPU type:

nRWM = H: nDS signal at DIR = H

nRWM = L: nRD signal

NOTE: Refer to the AC timing specifications (in another document) for details (setup time, hold time, etc.). Compare timing specifications for nEHRD=L and nEHRD=H.

1.6.5 Data Bus Width Selection

(W16/SCM[2]: Pin)

This pin selects the width of the data bus in the peripheral mode; H: 16-bit mode, L: 8-bit mode. In the 16-bit mode, the LSB address in the CircLink is fixed to 0. In the standalone mode, this pin is the clock-master-ID input pin SCM[2].

1.6.6 Data Bus Byte Swap

(nSWAP/SCM[3]: Pin)

In peripheral mode, this pin selects the data order at 8-bit access. Although the registers in the CircLink are defined as 16-bit width, 8-bit access is available, and in this case, the assignment of lower/upper byte of the register and odd/even number of addresses can be changed. The nSWAP=L assigns the lower byte to even number address/ upper byte to odd number address, and the nSWAP=H assigns the lower byte to odd number address /upper byte to even number address. In standalone mode, this pin is the clock master ID input SCM[3].

1.6.7 Data Strobe Polarity Specification

(nDSINV/CMIERRMD: pin)

In peripheral mode, this pin selects the pin polarity of data strobe (nDS). It is active low with nDSINV = H and active high with nDSINV = L. In standalone mode, this pin is equivalent to CMIERRMD (bit 12) in Mode Register. The packet receive stops upon the occurrence of a CMI receive error correction (CMIECC) with CMIERRMD = H.

1.6.8 Page Size Selection

(PS[1:0]: Pin/Register)

Select page size per packet. The maximum number of nodes depends on the page size selection since the packet buffer size is limited to 1 kByte. Page size can be selected by settings using register bits INIMODE (bit 9); 0: selects pin, 1: selects register (The default is 0).

PS[1:0]	Page Size	Max Node Number
00	256 Byte	3 Node
01	128 Byte	7 Node
10	64 Byte	15 Node
11	32 Byte	31 Node

1.6.9 Maximum Node (MAXID) Number Setup

(MAXID[4:0]: Pin/Register)

The maximum node ID is set based on the number of nodes on the network. All nodes in each CircLink network, therefore, should have the same maximum node ID. This minimizes the time required to reconfigure the network. There are two methods to specify the maximum node ID, Either through pin or register settings depending on INIMODE (bit 9); 0: selects pin, 1: selects register (The default is 0). If the nDIAG pin is set to L as the exception, however, the maximum node ID is automatically set to the largest value. For more details, refer to section 2.11 - Diagnostic Mode.

1.6.10 Node ID Setup

(NID[4:0]: Pin/Register)

Set node ID. A unique number must be assigned to each node in the network with ascending order starting from ID=01. ID = 00 and an ID larger than the maximum node ID are not valid. There are two methods to assign the node ID, either through pin or register, settings depending on INIMODE (bit 7) 0: selects pin, 1: select register (default is 0).

MAXID[4:0] determines the maximum node ID value. The token will be passed only around the nodes whose IDs are equal to or less than the maximum ID value. . In the CircLink network, a node whose MAXID[4:0] and NID[4:0] matches is the node initiating the token passing.. Even if this particular node is absent from the network, the network reconfiguration time is greatly reduced because the network will be only reconfigured by the nodes with IDs less than MAXID[4:0]. Since the maximum number of nodes is fixed to MAXID[4:0] in a CircLink network, the original priority timer of ARCNET, (255 – ID) x 146 μs*, which determines the time required for network reconfiguration, is modified to (MAXID[4:0]-ID) x 146 μs, greatly reducing network reconfiguration time. Refer to section 2.4.2 - Reduction of Network Reconfiguration Time for more details.

* 146 μs is defined under operation at 2.5 Mbps based on ARCNET protocol. That number is half at 5 Mbps.

1.6.11 NST Resolution Setup

(NSTPRE[2:0]: Pin)

Select resolution of network standard time counter(NST) . Refer to section 2.12 - Network Standard Time (NST) for details.

1.6.12 Standalone Mode Specification

(nSTALONE: Pin)

This pin enables the Standalone mode operation of CircLink. Refer to section 2.10 - Standalone Mode for the details

1.6.13 Warning Timer Resolution/Standalone Sending Schedule Setup

(WPRE/SPRE[2:0]: Pin)

These pins select the warning timer resolution in peripheral mode and the transmit Schedule (include setup trigger mode) in standalone mode. Refer to sections 2.9.4 and 2.10 for more details.

1.6.14 Diagnosis Mode

(nDIAG: Pin)

This pin places CircLink in Diagnostic mode. It pulls nDIAG low, and sets the MAXID to “1Fh”. Refer to section 2.11 - Diagnostic Mode for the details.

1.6.15 Prescaler Setup for Communication Speed

Communication speed can be selected either through pin or register, depending on the specification of INIMODE (bit 9); 0: pin, 1: register (default is 0).

(CKP[2:0]: Pin/Register)

CKP2-0	Prescale	Communication Speed			
		40MHz XTAL	20MHz XTAL	32MHz XTAL	16MHz XTAL
000	8	5Mbps	2.5Mbps	4Mbps	2Mbps
001	16	2.5Mbps	1.25Mbps	2Mbps	1Mbps
010	32	1.25Mbps	625Kbps	1Mbps	500Kbps
011	64	625Kbps	312.5Kbps	500Kbps	250Kbps
100	128	312.5Kbps	156.25Kbps	250Kbps	125Kbps
101	256	156.25Kbps	78.125Kbps	125Kbps	62.5Kbps
110	reserved	reserved	reserved	reserved	reserved
111	reserved	reserved	reserved	reserved	reserved

1.6.16 NST Carry Output Digit Select

(NSTC[3], nEHWR/NSTC[2], nEHRD/NSTC[1], NSTC[0]: Pin)

These pins are equivalent to the same-symbol signal NSTC[3:0] (bit 7-4) of the carry register in Standalone mode. The output timing of external pulse nNSTCOUT is specified as an NST digit position. For the functions using Peripheral mode, refer to sections 1.6.3 and 1.6.4.

1.6.17 CMI Bypass Specification

(nCMIBYP: Pin)

Selects bypassing the CMI code/encoding. nCMIBYP = L bypasses the CMI coding/decoding circuit so that encoding is RZ form signal interface, equivalent to the ARCNET back plane mode.

1.6.18 HUB Function ON/OFF

(nHUBON: Pin)

Selects ON/OFF ; nHUBON=H selects HUB function OFF, nHUBON=L selects HUB function ON and enables port 2 (RXIN2 and TXEN2) (in nHUBON = H, RXIN2 should be fixed to High).

Refer to section 2.14 - HUB Function for the detailed operations.

1.6.19 Optical Transceiver Mode

(nOPMD: Pin)

Selects the output mode of the sending-enable; nOPMD = H makes the optical transceiver mode unavailable and allows the TXEN and TXEN2 output pins to function as “sending-enable”. Setting nOPMD = L allows TXEN and TXEN2 output pins to function as “sending-enable and sending pulse” to be able to be directly connected to the TTL input pin of the optical transceiver.

1.6.20 TXEN Polarity Select

(TXENPOL: Pin)

Selects the output polarities of the TXEN and TXEN2 signal. TXENPOL = L selects negative logic and TXENPOL = H positive logic.

1.6.21 Extension Timer Setting 1

(ET1: Pin/Register)

Refer to section 2.14 - HUB Function for operational details.

1.6.22 Test Pins

(nTEST[3:0], nTMODE: Pin)

All the pins must be connected to VDD.

Chapter 2 Functional Description

2.1 Communication Specification

- Data transfer bit rate	78.125 kbps to 2.5 Mbps (with 20 MHz Xtal, 5 Mbps with 40 MHz Xtal).
- The max. number of nodes	31 (ID = 00 is not available for use)
- Data transfer check	Only the destination node can check data transfer. Other nodes, however, can receive (monitor) the same data.
- Protocol	Enhanced version of ARCNET (token passing)
- Packet size	256 bytes max. (User area: 253 bytes max.)

2.2 Message Class

The following five classes of messages are identical to those in the ARCNET protocol. Refer to the ARCNET Controller COM20020 Rev. D datasheet for more information.

ITT (Token)

ALERT	EOT	DID	DID

FBE (Free Buffer Enquiries)

ALERT	ENQ	DID	DID

ACK (Acknowledgements)

ALERT	ACK

NAK (Negative Acknowledgements)

ALERT	NAK

PACKET (Data Packets)

ALERT	SOH	SID	DID	DID	CP	DATA X n	CRC	CRC

N : MAX253
(ARCNET Layer)