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TMC2084

Standalone Mode CircLink™ Controller

Datasheet

PRODUCT FEATURES

- Low Power CMOS, 3.3 Volt Power Supply with 5 Volt Tolerant I/O
- Enhanced Token Passing Protocol from ARCNET
  - Maximum 15 node per network
  - Token Retry Mechanism
  - 64/128 Byte Per Packet
  - Consecutive Node ID Assignment
- Memory Mirror
  - Shared Memory Within Network
- Network Standard Time
  - Network Time Synchronization
  - Automatic Time Stamping
- Coded Mark Inversion
  - Intelligent 1-Bit Error Correction
  - Magnetic Saturation Prevention
- Standalone I/O Mode Operates without MCU
  - Supports 16 Bit Input and 16 Bit Output
- Up to 14 Intelligent Remote I/O Ports:
  - Programmable with 8-bit basis (16 to 32 outputs; 0 to 16 inputs)
  - Selectable output type (push-pull or open-drain)
  - The part of port is definable as strobe outputs and/or external trigger inputs
  - The anti-chatter circuit on the input port can be set in ON/OFF
  - The sampling frequency of the anti-chatter circuit can be set (19.1Hz/1.22KHz)
- Feature Rich Transmit Trigger:
  - After receiving OUTPUT DATA packet or expiring on-chip timer
  - Continuous transmission
  - External trigger input
- Flexible Transceiver Interface:
  - RS-485 transceiver + twist pair cable
  - RS-485 transceiver + pulse transformer + twist pair cable
  - Hybrid transceiver (HYC4000 or HYC2000 from SMSC Japan)
  - Fiber Optics also supported
- 48-Pin, TQFP Lead-Free RoHS Compliant Package
  - Body size: 7 × 7mm; pitch: 0.5mm
- Temperature Range from 0 to 70 degrees C

ORDERING INFORMATION

Order Number(s):

TMC2084-HT for 48 pin, TQFP Lead-Free RoHS Compliant Package

80 ARKAY DRIVE, HAUPPAUGE, NY 11788 (631) 435-6000, FAX (631) 273-3123

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Chapter 1 General Description

1.1 About CircLink

The CircLink networking controller was developed for small control-oriented local network data communication based on ARCNET's token-passing protocol that guarantees message integrity and calculatable maximum delivery times.

In a CircLink network, when a node receives the token it becomes the temporary master of the network for a fixed, short period of time. No node can dominate the network since token control must be relinquished when transmission is complete. Once a transmission is completed the token is passed on to the next node (logical neighbor), allowing it to be come the master.

Because of this token passing scheme, maximum waiting time for network access can be calculated and the time performance of the network is predictable or deterministic. Industrial network applications require predictable performance to ensure that controlled events occur when required.

However, reconfiguration of a regular ARCNET network becomes necessary when the token is missed due to electronic and magnetic noise. In these cases, the maximum wait time for sending datagrams can not be guaranteed and the real-time characteristic is impaired. CircLink makes several modification to the original ARCNET protocol (such as maximum and consecutive node ID assignment) to avoid token missing as much as possible and reduce the network reconfiguration time.

CircLink implements other enhancements to the ARCNET protocol including a smaller-sized network , shorter packet size, and remote buffer mode operation that enable more efficient and reliable small, control-oriented LANs. In addition, CircLink introduces several unique features for reducing overall system cost while increasing system reliability.

CircLink can operate under a special mode called "Standalone" or "I/O" mode. In this mode, CircLink does not need an administrating CPU for each node. Only one CPU is needed to manage a CircLink network composed of several nodes, reducing cost and complexity.

In a CircLink network, the data sent by the source node is received by all other nodes in the network and stored according to node source ID. For the target node the received data is executed per ARCNET flow control and the data is stored in its buffer RAM. The receiving node processes the data while the remaining nodes on the network discard the data when the receiving node has completed. This memory-mirroring function assures higher reliability and significantly reduces network traffic.

Network Standard Time (NST) is also a unique CircLink feature. NST is realized by synchronizing the individual local time on each network node to the clock master in the designated node from which the packet is sent. CircLink also uses CMI code for transmitting signals, rather than the dipulse or bipolar signals that are the standard ARCNET signals. Since CMI encoding eliminates the DC element, a simple combination of a standard RS485 IC and a pulse transformer can be used to implement a transformer-coupled network.

1.2 About TMC2084

The TMC2084 is CircLink's standalone mode controller acting as an intelligent remote I/O controller that uses the enhanced token passing protocol. TMC2084 I/O nodes are controlled by the Host node (TMC2074/72) via the network. Thus, TMC2084 enables a single-processor with multi-remote I/O controllers environment at reasonable cost.

The TMC2084 has thirty-two I/O port lines featuring programmable direction, with 8-bit basis (output: 16 to 32 bit; input: 0 to 16 bit). The maximum number of nodes per network is fifteen, including the host node. This configuration enables a processor to control a total of 448 (14 × 32) remote I/O lines.

The Output Port type is selectable from either open-drain or push-pull, while one part of the I/O ports is definable as either output pins for network status monitoring, strobe output pins to handshake with AD or DA converter, or input pins for external trigger.

TMC2084 also has additional functions including the function to notify the host of its status, the states of its Output Ports and settings, the function to send packets with timestamp, and the function to synchronize the on-chip timer to the host.

This rich feature set is contained in a single 48-pin TQFP package.

1.3 Block Diagram

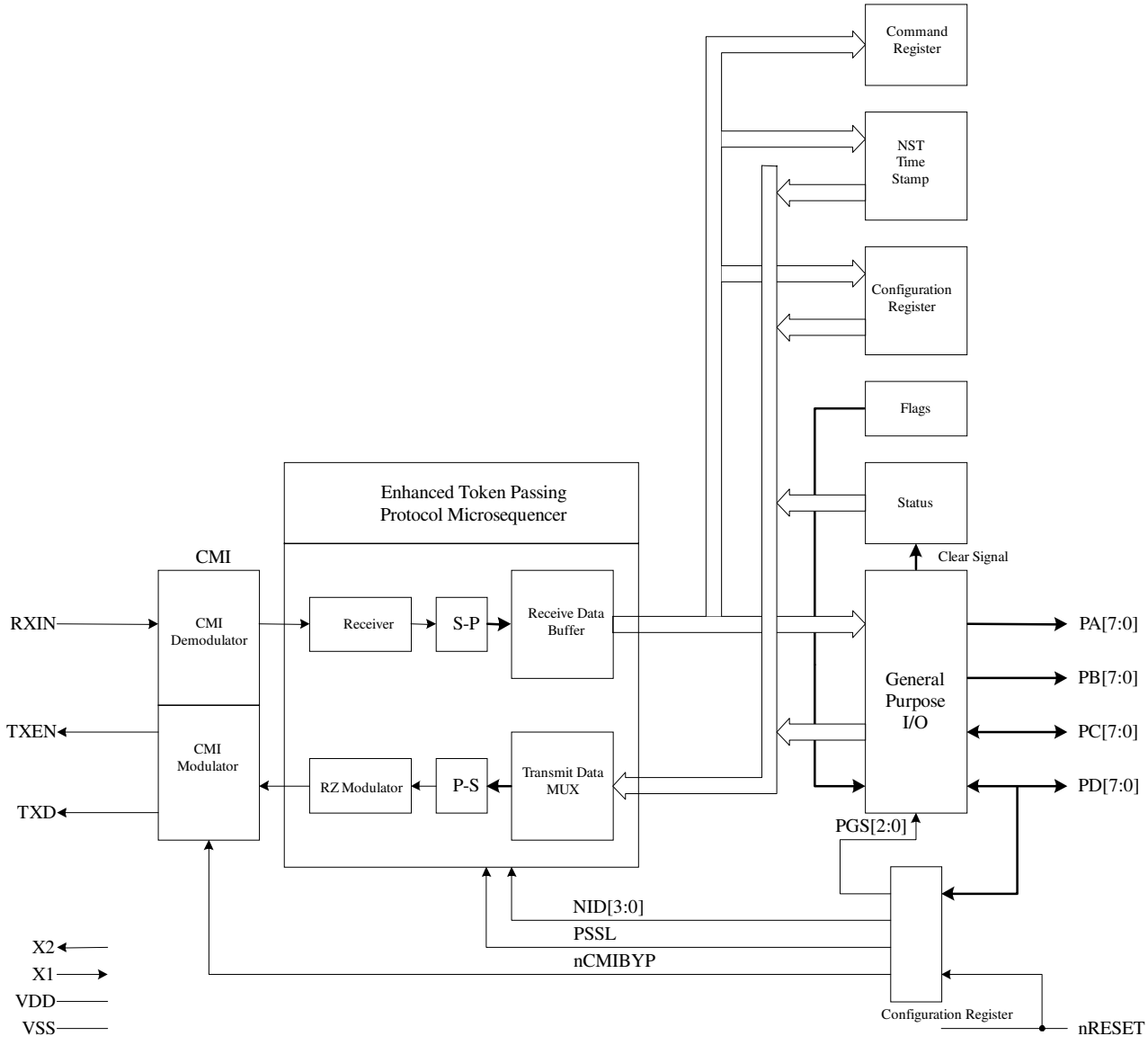


Figure 1 - TMC2084 Block Diagram

1.4 Pin List

PIN NO.	SIGNAL NAME	PIN NAME	BUFFER TYPE BY FUNCTION	DETAILED DESCRIPTION
General Purpose I/O Group A				
2 - 9	Port A bit 0 - 7 (output-only)	PA0 - 7	O42/OD4	General Purpose I/O Port A. An output-only port. The type of output can be selected using the PAOD bit, configured through the network. PAOD = 0 selects push-pull; PAOD = 1 selects open-drain (default).
General Purpose I/O Group B				
10-11, 14-19	Port B bit 0 - 7 (output-only)	PB0 - 7	O42/OD4	General Purpose I/O Port B. An output-only port. The type of output can be selected using PBOD bit, configured through the network. PBOD = 0 selects push-pull; PBOD = 1 selects open-drain (default).
General Purpose I/O Group C				
20	Port C bit 0	PC0	IT/O42/OD4	General Purpose I/O Port Bit 0. A bi-directional port. The port direction can be specified using the shared pin PGS0. PGS0 = L specifies input; PGS0 = H specifies output. The type of output can be selected using PCOD bit, configured through the network. PCOD = 0 selects push-pull; PCOD = 1 selects open-drain (default).
	External Trigger Input 1	nPISTR1	IT	External Trigger Input 1 The input pin for external trigger signal. If the shared pin PGS0 is set to L while "6h" or “7” is set using TXTRG3 - 0 bits that are configured through network then this port is configured for the external trigger input.
21-23, 26-29	Port C bit 1 - 7	PC1 - 7	IT/O42/OD4	General Purpose I/O port C bit 1 to 7. A bi-directional port. The direction of port and the type of output are configured using the same way as PC0.

PIN NO.	SIGNAL NAME	PIN NAME	BUFFER TYPE BY FUNCTION	DETAILED DESCRIPTION
General Purpose I/O Group D				
30	Port D bit 0	PD0	IT/O42	The bit 0 of Port D. A bi-directional port. The port direction can be specified using the shared pin PGS1. PGS1 = L specifies input; PGS1 = H specifies output.
	External Trigger Input 2	nPISTR2	IT	External Trigger Input 2 The input port of external trigger signal. If the shared pins PGS0 and PGS1 are set to L and H respectively while either "6h" or "7h" is set using TXTRG3 – 0 bits that are configured through network, then this port is configured for the external trigger input port.
	(Node ID Configuration Bit 0)	(NID0)	(IT)	The configuration bit 0 of the own node ID. For detailed information, see the section on Configuration Using Shared Pins.
31	Port D bit 1	PD1	IT/O42	The bit 1 of Port D. A bi-directional port. The port direction is configured using the same way as PD0.
	(Node ID Configuration Bit 1)	(NID1)	(IT)	The configuration bit 1 of the own node ID For detailed information, see the section on Configuration Using Shared Pins.
32	Port D bit 2	PD2	IT/O42	The bit 2 of Port D. A bi-directional port. The port direction is configured using the same way as PD0.
	(Node ID Configuration Bit 2)	(NID2)	(IT)	The configuration bit 2 of the own node ID For detailed information, see the section on Configuration Using Shared Pins.
33	Port D bit 3	PD3	IT/O42	The bit 3 of Port D. A bi-directional port. The port direction is configured using the same way as PD0.
	(Node ID Configuration Bit 3)	(NID3)	(IT)	The configuration bit 3 of the own node ID For detailed information, see the section on Configuration Using Shared Pins.
34	Port D bit 4	PD4	IT/O42	The bit 4 of Port D. A bi-directional port. The port direction can be specified using the shared pin PGS1. PGS1 = L specifies input; PGS1 = H specifies output. PGS2 should be set to L.
	FLAG OUTPUT bit0	FO0	O42	The bit0 of FLAG OUTPUT. A bi-directional port. Setting the shared pin PGS2 to H configures FLAG OUTPUT mode. For detailed information of the flag, see the section on Configuration Through Network.
	(Page Size Selection)	(PSSL)	(IT)	Page Size Selection. For detailed information, see the section on Configuration Using Shared Pins.

PIN NO.	SIGNAL NAME	PIN NAME	BUFFER TYPE BY FUNCTION	DETAILED DESCRIPTION
35	Port D bit 5	PD5	IT/O42	The bit 5 of Port D. A bi-directional port. The port direction is configured using the same way as PD4.
	FLAG OUTPUT bit1	FO1	O42	The bit1 of FLAG OUTPUT. The FLAG OUTPUT mode is configured using the same way as PD4. For detailed information of the flag, see the section on Configuration Through Network.
	(Port Direction Configuration - bit 0)	(PGS0)	(IT)	Configuration bit 0 of port direction. For detailed information, see the section on Configuration Using Shared Pins.
37	Port D bit6	PD6	IT/O42	The bit 6 of Port D. A bi-directional port. The port direction is configured using the same way as PD4.
	FLAG OUTPUT bit2	FO2	O42	The bit2 of FLAG OUTPUT. The FLAG OUTPUT mode is configured using the same way as PD4. For detailed information of the flag, see the section on Configuration Through the Network.
	(Port Direction Configuration - bit 1)	(PGS1)	(IT)	Configuration bit 1 of port direction. For detailed information, see the section on Configuration Using Shared Pins.
38	Port D bit 7	PD7	IT/O42	The bit 7 of Port D. A bi-directional port. The port direction is configured using the same way as PD4.
	Network Status Monitoring output	nRCNERR	O42	Network Status Monitoring output. The FLAG OUTPUT mode is configured using the same way as PD4. For detailed information see the section on Configuration Through the Network.
	(Port Direction Configuration - bit 2)	(PGS2)	(IT)	The configuration bit 2 of port direction. For detailed information, see the section on Configuration Using Shared Pins.
Reset and Clock				
41	Reset Input	nRESET	ICS	The input for the reset signal. The signal for hardware reset is connected to this active low pin.
43	Oscillator/ External Clock Input	X1	IC	This pin functions as the input for either the oscillator or the external clock.
44	Oscillator Output	X2	OX	Oscillator output.
Transceiver Interface				
46	Transmit Enable Output	TXEN	O42	Transmit enable output (active high)
47	Transmit Data Output (CMI bypass configuration)	TXD (nCMIBYP)	O42 (IT)	Transmit data output. Specifies bypassing of CMI encoder/ decoder. For detailed information, see the section on Configuration Using Shared Pins.

PIN NO.	SIGNAL NAME	PIN NAME	BUFFER TYPE BY FUNCTION	DETAILED DESCRIPTION
48	Receive Data Input	RXIN	IT	Receive data input.
Test Pin				
39, 40	Test Mode	nTMODE nSMODE	IT_PU	Test mode. **This pin must be tied to Vdd.**
Power Supply Pin				
13, 25, 42	Power Supply	Vdd	-	Power supply pin. This pin is connected to the power supply voltage (3.3V).
1, 12, 24, 36, 45	Ground	Vss	-	Ground pin. This pin is connected to the ground level (0V).

Description of buffer types:

IC	Input, CMOS Level
IT	Input, TTL Level
IT_PU	Input, TTL Level with pull-up
ICS	Input, CMOS Level with Schmitt Trigger
O42	Output, I_{OL} = 4 mA, I_{OH} = -2 mA
OD4	Open-drain Output, I_{OL} = 4 mA
OX	Oscillator Output

1.5 Pinout

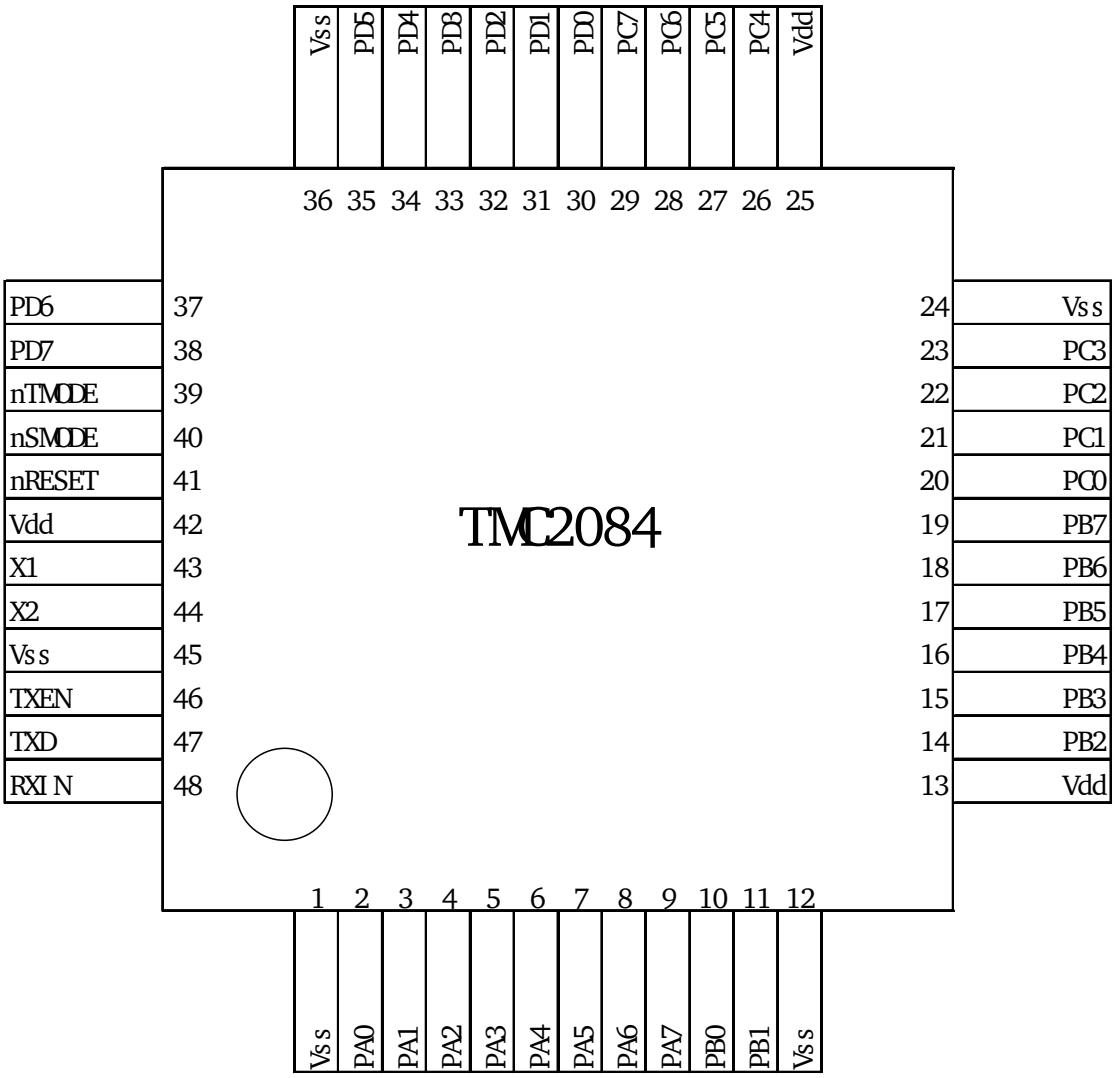


Figure 2 - TMC2084 Pin Configuration

Chapter 2 Functional Description

2.1 Network Configuration

2.1.1 General

Host Node and I/O Node

A CircLink network can consist of a single host node/multi I/O node, or multiple host nodes/single I/O, or multiple host nodes and multiple I/O nodes. The host node is directly connected to the system (external) CPU, which controls all communications to or from it. The device that can be used for the host node should be a TMC2072/74 that is configured to operate in Peripheral mode; the TMC2084 is dedicated for the use as an I/O node only (Standalone mode). The I/O nodes do not require the CPU and they are controlled indirectly via the network by the CPU through the host node.

The CircLink network allows a combination of host nodes and I/O nodes up to 15 nodes total. Every CircLink network must have at least one host node.

The host node controls the following I/O node functions:

- Input and output activities on a port (sending and receiving data and initializing the port)
- Setting various configuration data
- Request for configuration data
- Activation of transmission activity
- Software reset

These functions are controlled through the network.

Section 2.1.2 shows two examples: network configuration example 1 (single host) that includes one host node and fourteen I/O nodes, and network configuration example 2 (dual host) that includes two host nodes and four I/O nodes. When multiple hosts are used, I/O nodes should be grouped so that each host can control its corresponding group as shown in network configuration example 2: Host 1 controls both I/O-1 and -2; Host 2 controls both I/O-3 and -4.

Node ID

Any node that belongs to a network should have a unique identification number (ID). The ID is configured using shared pins NID3 - 0. When shared pin PSSL is set to L, the allowable range of the node ID is 1 trough 7; it is 1 through 15 when the PSSL pin is set to H. 0 is not allowed for any node ID.

Consecutive node ID numbers (beginning with 1) are assigned to nodes in a network. Consecutive node ID numbers should be used, because each unused ID number between 2 working node IDs causes a latency of 93.6 μs (2.5 Mbps operation) every time a token is sent and thus degrades overall network performance.

MAXID

The MAXID defines the maximum node ID of the network and is configured through the network using the MAXID3 – 0 bits. Configuring the MAXID for the network when the number of nodes is less than the upper limit that is defined as 7 for PSSL = L and 15 for PSSL = H in the protocol enables tokens to circulate only among the existing nodes. The allowable MAXID range is 2 through 7 for PSSL = L and 2 through 15 for PSSL = H. Both 0 and 1 are not allowed. The node ID should be assigned consecutively starting with 1 and the MAXID should be equal to the number of nodes.

Typically, all nodes should have the same value for MAXID. However, the node that requires MAXID is the node that has the largest ID number in the network and the remaining nodes can be left to use the default value: 7 for PSSL = L and 15 for PSSL = H (in this case the maximum ID is assigned to the host node). In the case where configuration items other than MAXID also can use their corresponding default values, configuration through the network is not required.

Transmission Rate

Transmission Rate defines a common rate for all nodes. The transmission rate for TMC2072/74 is configured using either an internal register or an external pin; for TMC2084, it is configured by the value that is equal to one eighth of the input clock.

TRANSMISSION RATE	CLOCK FREQUENCY	CLOCK SOURCE
5 Mbps	40 MHz	External clock only
4 Mbps	32 MHz	External clock or crystal resonator
2.5 Mbps	20 MHz	External clock or crystal resonator
2 Mbps	16 MHz	External clock or crystal resonator
1.25 Mbps	10 MHz	External clock or crystal resonator
1 Mbps	8 MHz	External clock only
625 Kbps	5 MHz	External clock only
500 Kbps	4 MHz	External clock only
312.5 Kbps	2.5 MHz	External clock only

The acceptable frequency of an external crystal resonator is limited to the range of 10 MHz to 32 MHz due to the limitation of the onchip oscillator's performance. Please use the external clock module if a frequency other than the above is needed.

2.1.2 Configuration Examples

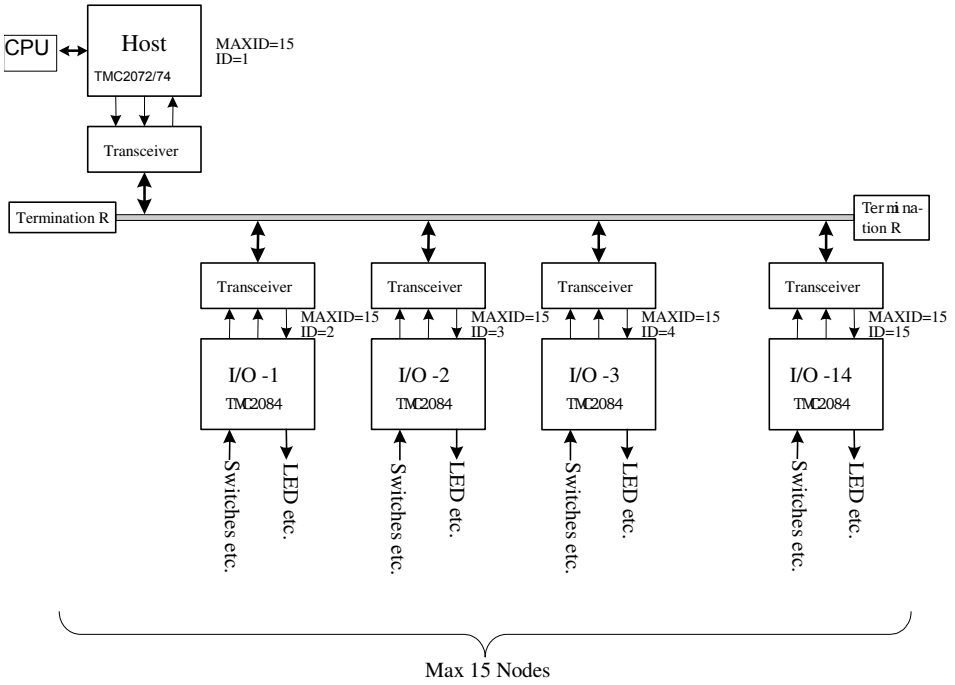
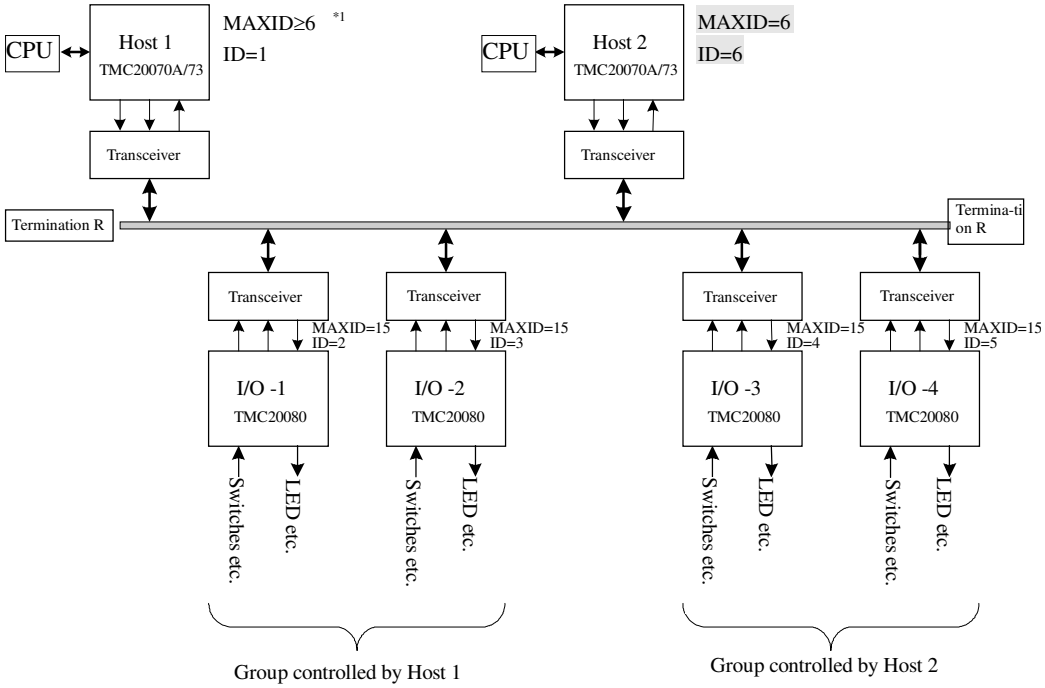


Figure 3 - Network Configuration Example 1: S Single Host and 15 Nodes



*1 Because a token is still passed to node 6 even if nodes 2 to 5 are off.

Figure 4 - Network Configuration Example 2: Dual Hosts and 6 Nodes

2.2 Initial Configuration

Initial configuration can be performed two ways: through shared pins or through the network.

2.2.1 Configuration Using Shared Pins

Basic items related to communication are configured using the shared pins. The configuration is performed after reading the states of pins PD7 - 0 and TXD at the rising edge of the reset signal. Since these pins remain in their high-impedance states (input states) during reset, connecting pull-up resisters to them causes High level input and connecting pull-down resisters to them causes Low level input. The items configured here are essential to send or receive packets within the network. Additional detail items may be configured if necessary using configuration through the network as described below.

nCMIBYP This pin specifies whether CMI coding is bypassed.

(Shared with TXD) Low: the CMI coding is bypassed (RZ coding for HYC4000/2000)

High: the CMI coding is not bypassed. (CMI coding for RS-485/CAN transceiver)

NID3 - 0 These three pins specify the node ID within the range 1 through 15.

(Shared with PD3 - 0) NID3 and NID0 correspond to MSB and LSB respectively. Low causes 0; High causes 1. When PSSL is set to Low, NID3 causes 0.

Note: DO NOT set low level for all pins.

PSSL This pin selects the page size.

(Shared with PD4) Low: 128 bytes/page (the maximum number of nodes = 7): All of the NID3, MAXID3 and CMID3 bits are fixed to 0.

Burst Transmission Period = 1.07 ms × 2.5/R (R = Transmission Rate in Mbps)

High: 64 bytes/page (the maximum number of nodes = 15)

Burst Transmission Period = 0.79 ms × 2.5/R (R = Transmission Rate in Mbps)

Two types of page sizes out of the four types that TMC2072/74 supports can be configured for TMC2084: 64-byte and 128-byte modes. A common page size must be configured for all nodes including host nodes. The data size that TMC2084 can send to or receive from the host in all modes is only the 8 bytes that are taken from the page; 64 bytes or 128 bytes of data can be transmitted only between host nodes.

PGS2 - 0 These three pins specify I/O port direction as shown in the table below.

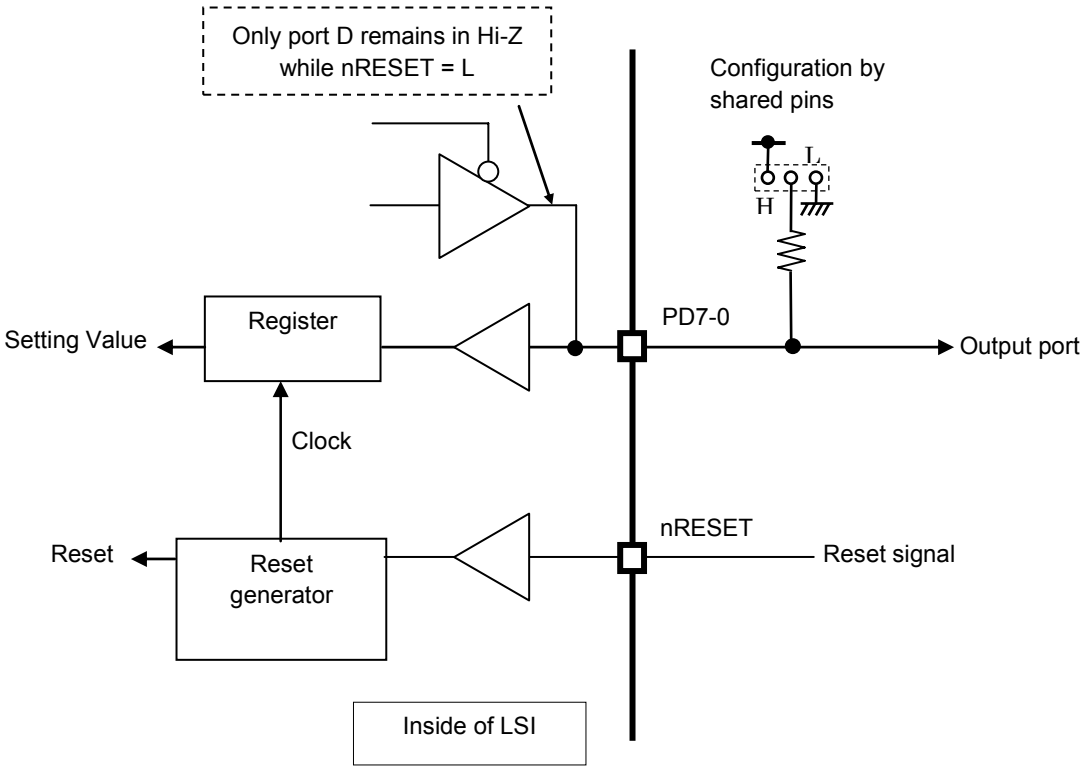
(Shared with PD7 - 5)

PGS2	PGS1	PGS0	Push-pull only		O.D / Push-pull			Input Pins for External Trigger
			PD7 - 4	PD3 - 0	PC7 - 0	PB7 - 0	PA7 - 0	
L	L	L	Input	Input	Input	Output	Output	nPISTR1
L	L	H			Output			nPISTR2
L	H	L	Output	Output	Input			nPISTR1
L	H	H			Output			-
H	L	L	FLAG OUTPUT	Input	Input			nPISTR1
H	L	H			Output			nPISTR2
H	H	L		Output	Input			nPISTR1
H	H	H			Output			-
L : Low ; H : High			O.D : Open-drain. The pins PA7 – 0 and PB7 – 0 are output-only.					

Port D Considerations

Example 1: Configuring Port D as OUTPUT PORT or FLAG OUTPUT - The case where the configuration by the shared pins is the same as the initial data from the OUTPUT PORT configured

The figure below shows the case where the initial data from the OUTPUT PORT does not conflict with the configuration by shared pins even if port D is configured as the OUTPUT PORT or FLAG OUTPUT. Port D remains in high-impedance state while the reset signal (nRESET) remains low. OUTPUT PORT remains in high-impedance state during the period from the falling edge of reset to the beginning of the first output data received. During these high-impedance periods, each input to port D is defined by the external pull-up (High) or pull-down (Low) resister. When port D is configured as FLAG OUTPUT, it starts driving right after the deassertion of the reset signal.

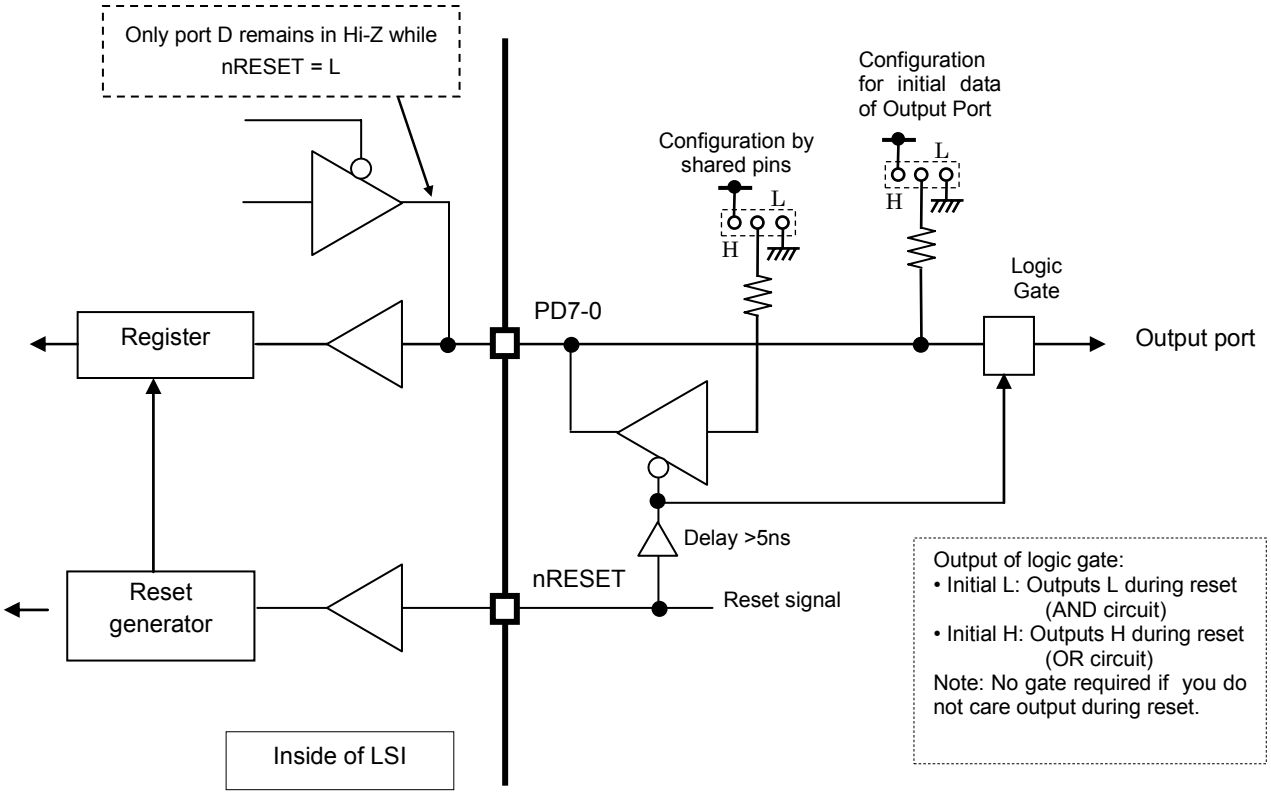


Example 2: Configuring Port D as OUTPUT PORT - The case where the configuration by the shared pins is different from the initial data from the OUTPUT PORT configured**.**

The figure below shows the case where the initial data from the OUTPUT PORT does conflict with the configuration by shared pins when port D is configured as an OUTPUT PORT. Port D remains in high - impedance state while the reset signal (nRESET) remains low. Also, the OUTPUT PORT remains in high-impedance state during the period from the falling edge of reset to the beginning of the first output data received.

During reset, the external tri-state buffer is enabled and the values configured by the shared pins are inputted to port D. After the reset signal is deasserted, the tri-state buffer is disabled and the initial data from the OUTPUT PORT is defined by an external pull-up (High) or pull-down (Low) resister. If initial data from the OUTPUT PORT is needed during the reset, use an external gate as shown in the figure below to define the data from OUTPUT PORT while the nRESET remains at low level.

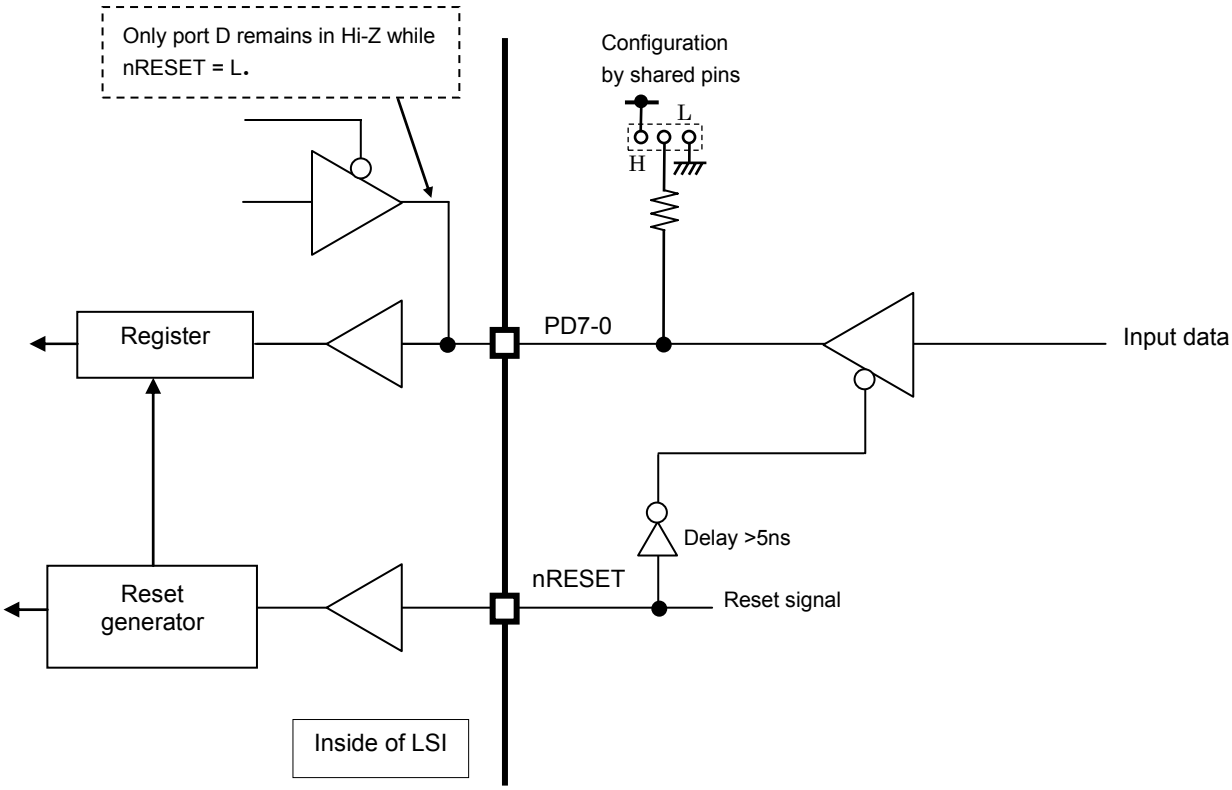
A hold time greater than 5 ns is required to retrieve the data configured by the shared pins and place it in the onchip memory. Thus, a buffer is added to provide a delay time for the control signal of an external tri-state buffer.


Only port D remains in Hi-Z while nRESET = L
Configuration for initial data of Output Port
Configuration by shared pins
L
H
L
H
Logic Gate
PD7-0
Register
Output port
Delay >5ns
nRESET
Reset generator
Reset signal
Inside of LSI
Output of logic gate:
• Initial L: Outputs L during reset (AND circuit)
• Initial H: Outputs H during reset (OR circuit)
Note: No gate required if you do not care output during reset.

Example 3: Configuring Port D as an INPUT PORT

The figure below shows the case where the port D is configured as INPUT PORT. The port D remains in high impedance state while the reset signal (reset) remains low level. During this high-impedance state, data defined by an external pull-up (High) or pull-down (Low) resister must be inputted to port D and any external input data to port D should be inhibited to avoid conflict. This requires the external tri-state buffer to inhibit input data during the reset period.

A hold time greater than 5 ns is required to retrieve the data configured by the shared pins and place it on the onchip memory. Thus, the buffer is added to provide a delay time for the control signal of the external tri-state buffer.



2.2.2 Configuration Through the Network

Additional items configured using this feature. The configuration is performed with an INITIAL SETTING packet received from the host node.

If the default is acceptable for all items that require configuration via the network and the NST carry output (i.e. nNSTCOUT described later) is not used, then configuration by the INITIAL SETTING packet is unnecessary. The configuration by INITIAL SETTING packet is valid only before receiving the START TRANSMIT command (described later). After receiving the START TRANSMIT command, the INITIAL SETTING packet is ignored.

Format of INITIAL SETTING Packet

From host node (transmit) to I/O node (receive)

Name	Adrs. *	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
SID	00h	Host node ID								--
DID	01h	I/O node ID or 00h (broadcasted)								--
C.P	02h	C.P = 38h/78h *								--
	⋮	⋮								--
		PACKET ID code								--
DATA0	38h/78h	**0**	**1**	**0**	0					--
DATA1	39h/79h	0	PCOD	PBOD	PAOD	BSTSEND	CMIERRMD	EMGYMD	BRE	7Fh
DATA2	3Ah/7Ah	POSTRMD	POSTRDLY	ACHTBYP	0	MAXID3 - 0				0Fh
DATA3	3Bh/7Bh	FOSL3 - 0				TXTRG3 - 0				00h
DATA4	3Ch/7Ch	NSTCOMD	ACHTFRQ	0	0	NSTC3 - 0				80h
DATA5	3Dh/7Dh	NSTPRE2 - 0			0	CMID3 - 0				00h
NST-L	3Eh/7Eh	NST7 - 0								--
NST-H	3Fh/7Fh	NST15 - 8								--

Note: *Addresses in 64-byte mode/Addresses in 128-byte mode

Register Description (DATA1: Various Configurations)

Name	Drs.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DATA1	39h/79h	0	PCOD	PBOD	PAOD	BSTSEND	CMIERRMD	EMGYMD	BRE

BRE Enables or disables receiving broadcast

0: Receiving broadcast is disabled.

1: Receiving broadcast is enabled (default).

When the broadcast packet is received by the BRE=0 setting, it is disregarded. (It doesn't become a receiving error.)

EMGYMD Configures emergency mode (Assertion of MYRECON causes dropping from network).

0: Does not initialize OUTPUT PORT (high-impedance state) when MYRECON is asserted.

1: Initializes OUTPUT PORT (high-impedance state) when MYRECON is asserted (default).

CMIERRMD Configures the CMI error mode.

0: Does not discard the packet when CMIECC is asserted in it.

1: Discards the packet when CMIECC is asserted in it (default)

BSTSEND Configures Recon-burst signal transmit (Assertion of MYRECON causes dropping from network).

0: Does not transmit Recon-burst signal when MYRECON is asserted.

1: Transmits Recon-burst signal when MYRECON is asserted (default).

PAOD Configures port A pins (PA7 - 0) as open-drain outputs.

0: Configures port A pins (PA7 - 0) as push-pull outputs (totem pole).

1: Configures port A pins (PA7 - 1) as open-drain outputs (default).

PBOD Configures port B pins (PB7 - 0) as open-drain outputs.

0: Configures port B pins (PB7 - 0) as push-pull output (totem pole).

1: Configures port B pins (PB7 - 1) as open-drain outputs (default).

PCOD Configures port D pins (PD7 - 0) as open-drain outputs.

0: Configures port D pins (PD7 - 0) as push-pull output (totem pole).

1: Configures port D pins (PD7 - 1) as open-drain outputs (default).

Register Description (DATA2: MAXID and nPOSTR Related)

Name	Adrs.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DATA2	3Ah/7Ah	POSTRMD	POSTRDLY	ACHTBYP	0	0			

MAXID3 - 0 Configure the maximum ID number with range 1 to 15 (MAXID4 is fixed to 0)

MAXID3: MSB; MAXID0: LSB

Configuring PSSL = Low causes MAXID3 to be fixed to 0.

Default: MAXID3 - 0 = 1111

ACHTBYP Configures the bypass or not for Anti-chatter circuit on input ports.

0: Enable the anti-chatter circuit (default)

1: Bypass (Disable) the anti-chatter circuit

Note: When the transmit trigger (TXTRG3-0) setting is set to “By the external trigger”, bypass is automatic.

POSTRDLY Configures delay time for the OUTPUT PORT strobe (nPOSTR).

0: From the transition of port A to the falling edge of strobe at least 11 times of Tx (default)

1: From the transition of port A to the falling edge of strobe at least 43 times of Tx.

Note: Tx = Period of input clock (11 × Tx = 550 ns and 43 × Tx = 2.15 μs @20 MHz input)

POSTRMD Configures output mode for the OUTPUT PORT strobe signal (nPOSTR).

0: Asserts OUTPUT PORT strobe signal after initializing OUTPUT PORT and after receiving the OUTPUT DATA packet (default).

1: Asserts only after receiving the OUTPUT DATA packet.

Note: Initializing OUTPUT PORT means Initialization by both the INITIALIZE OUTPUT PORT command and the assertion of MYRECON in emergency mode (EMGYMD = 1).

Register Description (DATA3: This register selects the transmit trigger in FLAG OUTPUT.)

Name	Adrs.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DATA3	3Bh/7Bh	FOSL3 - 0				TXTRG3 - 0			

TXTRG3 - 0 These bits select the transmit trigger.

The trigger condition to send the INPUT DATA packet is configured. The transmit trigger is enabled after receiving the START TRANSMIT command.

TXTRG				The transmit trigger to send the INPUT DATA packet is generated upon ...
3	2	1	0	
0	0	0	0	Receiving the OUTPUT DATA packet
0	0	0	1	Receiving the OUTPUT DATA packet or expiring on-chip timer (3.3 ms)
0	0	1	0	Receiving the OUTPUT DATA packet or expiring on-chip timer (6.6 ms)
0	0	1	1	Receiving the OUTPUT DATA packet or expiring on-chip timer (13.1 ms)
0	1	0	0	Receiving the OUTPUT DATA packet or expiring on-chip timer (26.2 ms)
0	1	0	1	Receiving the OUTPUT DATA packet or expiring on-chip timer (104.8 ms)
0	1	1	0	By the external trigger (with NST latch)
0	1	1	1	By the external trigger (without NST latch)
1	0	0	0	Reserved (unused)
1	0	0	1	Reserved (unused)
1	0	1	0	Reserved (unused)
1	0	1	1	Reserved (unused)
1	1	0	0	Reserved (unused)
1	1	0	1	Reserved (unused)
1	1	1	0	Receiving own token
1	1	1	1	Receiving the COMMAND packet

Receiving the OUTPUT DATA packet:

A single transmit trigger is generated after receiving the OUTPUT DATA packet that is destined for this node or broadcasted is received. The INPUT DATA packet is transmitted after receiving the token (i.e., the token destined for this node).

Receiving the OUTPUT DATA packet or expiring on-chip timer:

A single transmit trigger is generated after either receiving the OUTPUT DATA packet that is destined for this node or broadcasted, or expiring on-chip timer. The INPUT DATA packet is then transmitted after receiving the token.

Note: This on-chip timer is cleared by an of three events: receiving the START TRANSMIT command; receiving the INITIALIZE OUTPUT PORT command; or transmitting an INPUT DATA packet after receiving a data packet.

By the external trigger:

The rising edge on the external trigger input pin (nPISTR1 or nPISTR2) latches the input data and generates the trigger. The INPUT DATA packet is then transmitted after receiving the token.

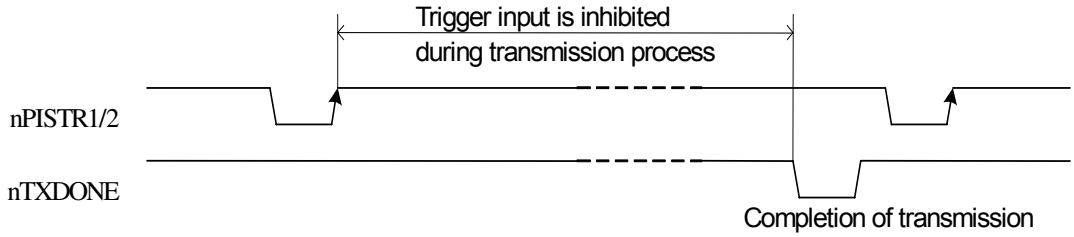
Either nPISTR1 or nPISTR2 is selected as the external trigger input pin depending on the I/O port direction configured by pins PGS2 - 0. If all of ports are configured as OUTPUT PORTs by the configuration feature for I/O port direction, then this external trigger cannot be used.

When the NST value latch is used, both the NST value and input data are latched simultaneously and the latched NST value is transmitted. When the NST value latch is not used, the last NST value is transmitted regardless to latching the input data.

(Both the input data and NST value latches are cleared to zero by hardware at initialization.)

Receiving the token allows the actual transmission of packets. Thus, the delay time from the trigger to the actual transmission can vary. If two consecutive external triggers are inputted, it can not be determined which trigger caused the data transmission since it depends on when the token was received.

Using nTXDONE (transmit completion flag) of the FLAG OUTPUT allows an easy handshake.



Whenever the token is received:

With this condition, the trigger is always generated. The INPUT DATA packet is transmitted whenever own token is received.

Receiving COMMAND packet:

A single transmit trigger is generated whenever either the START TRANSMIT or INITIALIZE OUTPUT PORT command that is destined for this node or broadcasted is received. The INPUT DATA packet is then transmitted upon receiving the token (The transmit trigger caused by the INITIALIZE OUTPUT PORT command is valid after receiving the START TRANSMIT command).

Note that the Return Setting and SOFTWARE RESET commands do not cause any transmit trigger. For detail information on each command, see section 2.4 COMMAND packet.

NOTE: A single transmit trigger is generated each time the START TRANSMIT command is received regardless of the configuration for the transmit trigger. Additionally, a single transmit trigger is generated at the time the INITIALIZE OUTPUT PORT command is received after receiving the START TRANSMIT command.