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TMC2130-LA DATASHEET

Universal high voltage driver for two-phase bipolar stepper motor. stealthChop™ for quiet movement. Integrated MOSFETs for up to 2.0A motor current per coil. With Step/Dir Interface and SPI.

dcStep™

coolStep™

stallGuard2™

APPLICATIONS

Textile, Sewing Machines
Factory Automation
Lab Automation
Liquid Handling
Medical
Office Automation
CCTV, Security
ATM, Cash recycler
POS
Pumps and Valves

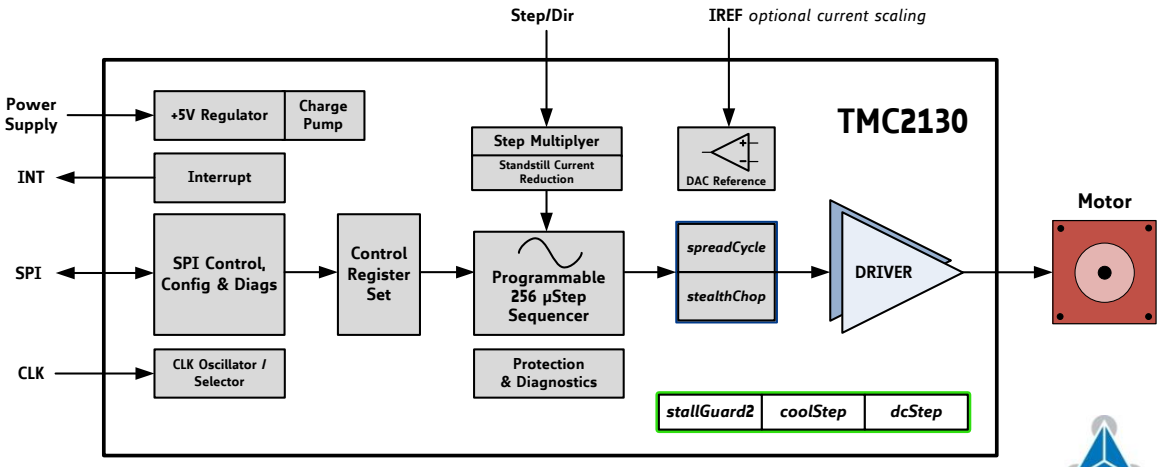
FEATURES AND BENEFITS

2-phase stepper motors up to 2.0A coil current (2.5A peak)
Step/Dir Interface with microstep interpolation **microPlyer™**
SPI Interface
Voltage Range 4.75... 46V DC
Highest Resolution 256 microsteps per full step
stealthChop™ for extremely quiet operation and smooth motion
spreadCycle™ highly dynamic motor control chopper
dcStep™ load dependent speed control
stallGuard2™ high precision sensorless motor load detection
coolStep™ current control for energy savings up to 75%
Integrated Current Sense Option
Passive Braking and freewheeling mode
Full Protection & Diagnostics
Small Size 5x6mm² QFN36 package or TQFP48 package

DESCRIPTION

The TMC2130 is a high performance driver IC for two phase stepper motors. Standard SPI and STEP/DIR simplify communication. TRINAMICs sophisticated stealthChop chopper ensures noiseless operation combined with maximum efficiency and best motor torque. coolStep allows reducing energy consumption by up to 75%. dcStep drives high loads as fast as possible without step loss. Integrated power MOSFETs handle motor currents up to 1.2A RMS (QFN package) / 1.4A RMS (TQFP) or 2.5A short time peak current per coil. Protection and diagnostic features support robust and reliable operation. Industries' most advanced stepper motor driver enables miniaturized designs with low external component count for cost-effective and highly competitive solutions.

BLOCK DIAGRAM



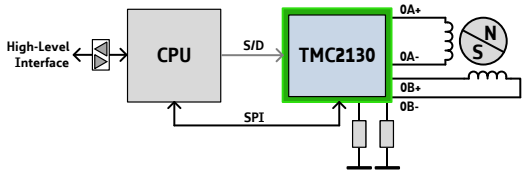
TRINAMIC Motion Control GmbH & Co. KG
Hamburg, Germany

TRINAMIC
MOTION CONTROL

APPLICATION EXAMPLES: HIGH VOLTAGE – MULTIPURPOSE USE

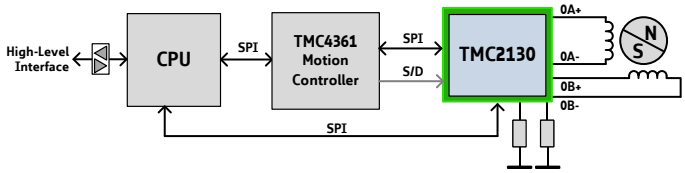
The TMC2130 scores with power density, integrated power MOSFETs, and a versatility that covers a wide spectrum of applications from battery systems up to embedded applications with 2.0A motor current per coil. Based on stallGuard2, coolStep, dcStep, spreadCycle, and stealthChop, the TMC2130 optimizes drive performance and keeps costs down. It considers velocity vs. motor load, realizes energy savings, smoothness of the drive and noiselessness. Extensive support at the chip, board, and software levels enables rapid design cycles and fast time-to-market with competitive products.

MINIATURIZED DESIGN FOR ONE STEPPER MOTOR



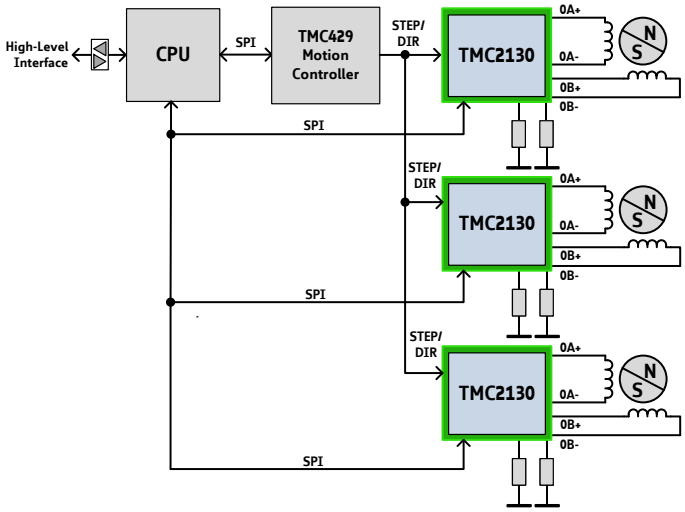
In this application, the CPU initializes the TMC2130 motor driver via SPI interface and controls motor movement by sending step and direction signals. A real time software realizes motion control.

DESIGN FOR DEMANDING APPLICATIONS WITH S-SHAPED RAMP PROFILES



The CPU initializes the TMC4361 motion controller and the TMC2130. Thereafter, it sends target positions to the TMC4361. Now, the TMC4361 takes control over the TMC2130. Combining the TMC4361 and the TMC2130 offers diverse possibilities for demanding applications including servo drive features.

COMPACT DESIGN FOR UP TO THREE STEPPER MOTORS



Here, an application with up to three stepper motors is shown. A single CPU combined with a TMC429 motion controller manages the whole stepper motor driver system. This design is highly economical and space saving if more than one stepper motor is needed.

ORDER CODES

Order code	Description	Size [mm²]
TMC2130-LA	1-axis dcStep, coolStep, and stealthChop driver; QFN36	5 x 6
TMC2130-TA	1-axis dcStep, coolStep, and stealthChop driver; TQFP48	9 x 9
TMC2130-EVAL	Evaluation board for TMC2130 two phase stepper motor controller/driver	85 x 55
TMC4361-EVAL	Motion controller board (part of evaluation board system)	85 x 55
STARTRAMPE	Baseboard for TMC2130-EVAL and further evaluation boards	85 x 55
ESELSBRÜCKE	Connector board for plug-in evaluation board system	61 x 38

Table of Contents

1 Principles of Operation

THE TMC2130 OFFERS THREE BASIC MODES OF OPERATION:

In *Step/Direction Driver Mode*, the TMC2130 is the microstep sequencer and power driver between a motion controller and a two phase stepper motor. Configuration of the TMC2130 is done via SPI. A dedicated motion controller IC or the CPU sends step and direction signals to the TMC2130. The TMC2130 provides the related motor coil currents to operate the motor. In *Standalone Mode*, the TMC2130 can be configured using pins. In this mode of operation CPU interaction is not necessary.
The third mode of operation is the *SPI Driver Mode*, which is used in combination with TRINAMICs TMC4361 motion controller chip. This mode of operation offers several possibilities for sophisticated applications.

OPERATION MODE 1: Step/Direction Driver Mode

An external motion controller is used or a central CPU generates step and direction signals. The motion controller (e.g. TMC429) controls the motor position by sending pulses on the STEP signal while indicating the direction on the DIR signal. The TMC2130 provides a microstep counter and a sine table to convert these signals into the coil currents which control the position of the motor. The TMC2130 automatically takes care of intelligent current and mode control and delivers feedback on the state of the motor. The microPlyer automatically smoothens motion. To optimize power consumption and heat dissipation, software may also adjust coolStep and stallGuard2 parameters in real-time, for example to implement different tradeoffs between speed and power consumption.

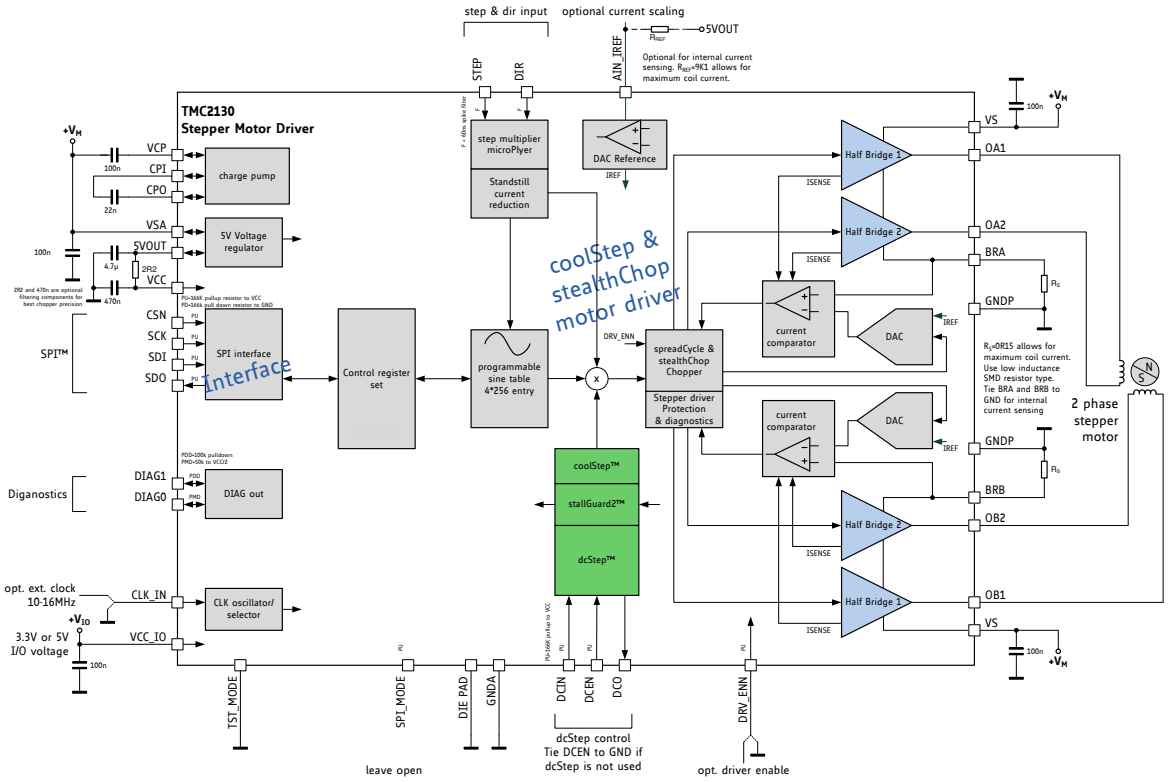


Figure 1.1 TMC2130 STEP/DIR application diagram

OPERATION MODE 2: Standalone Mode

The TMC2130 positions the motor based on step and direction signals. The microPlyer automatically smoothens motion. No CPU interaction is required. Configuration is done by hardware pins. Basic standby current control can be done by the TMC2130. Optional feedback signals allow error detection and synchronization.

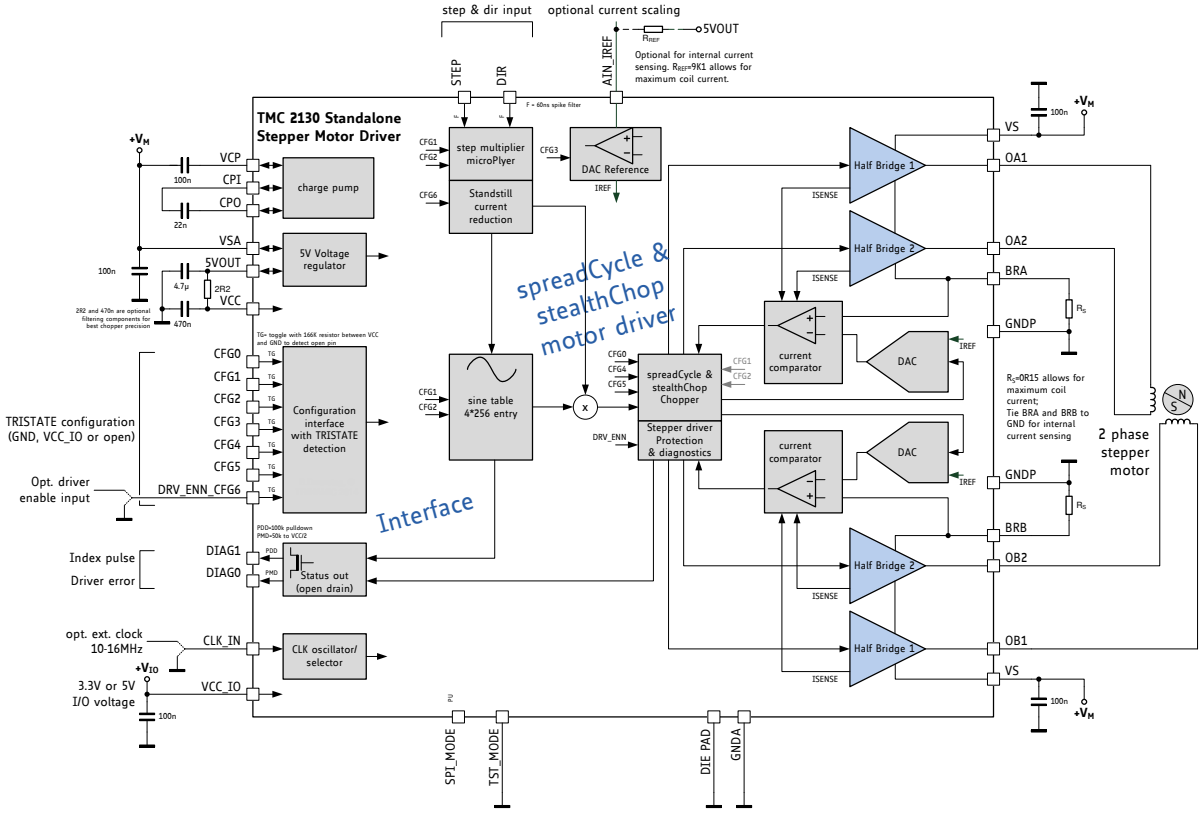


Figure 1.2 TMC2130 standalone driver application diagram

OPERATION MODE 3: SPI Driver Mode

Together with the TMC4361 high-performance S-ramp motion controller the TMC2130 stepper motor driver offers an SPI control mode, which gives full control over the motor coil currents to the TMC4361. Combining these two ICs offers several possibilities for demanding applications including servo features. Please refer to Figure 1.1 for more information about the pinning, which is identical to step/direction driver mode, except that the STEP & DIR pins are not required for operation.

1.1 Key Concepts

The TMC2130 implements advanced features which are exclusive to TRINAMIC products. These features contribute toward greater precision, greater energy efficiency, higher reliability, smoother motion, and cooler operation in many stepper motor applications.

stealthChop™ No-noise, high-precision chopper algorithm for inaudible motion and inaudible standstill of the motor.

spreadCycle™ High-precision chopper algorithm for highly dynamic motion and absolutely clean current wave.

dcStep™ Load dependent speed control. The motor moves as fast as possible and never loses a step.

stallGuard2™ Sensorless stall detection and mechanical load measurement.

coolStep™ Load-adaptive current control reducing energy consumption by as much as 75%.

microPlyer™ Microstep interpolator for obtaining increased smoothness of microstepping when using the STEP/DIR interface.

In addition to these performance enhancements, TRINAMIC motor drivers offer safeguards to detect and protect against shorted outputs, output open-circuit, overtemperature, and undervoltage conditions for enhancing safety and recovery from equipment malfunctions.

1.2 SPI Control Interface

The SPI interface is a bit-serial interface synchronous to a bus clock. For every bit sent from the bus master to the bus slave another bit is sent simultaneously from the slave to the master. Communication between an SPI master and the TMC2130 slave always consists of sending one 40-bit command word and receiving one 40-bit status word.

The SPI command rate typically is a single initialization after power-on.

1.3 Software

From a software point of view the TMC2130 is a peripheral with a number of control and status registers. Most of them can either be written only or read only. Some of the registers allow both read and write access. In case read-modify-write access is desired for a write only register, a shadow register can be realized in master software.

1.4 Moving the Motor

1.4.1 STEP/DIR Interface

The motor can be controlled by a step and direction input. Active edges on the STEP input can be rising edges or both rising and falling edges as controlled by a mode bit (*dedge*). Using both edges cuts the toggle rate of the STEP signal in half, which is useful for communication over slow interfaces such as optically isolated interfaces. On each active edge, the state sampled from the DIR input determines whether to step forward or back. Each step can be a fullstep or a microstep, in which there are 2, 4, 8, 16, 32, 64, 128, or 256 microsteps per fullstep. A step impulse with a low state on DIR increases the microstep counter and a high decreases the counter by an amount controlled by the microstep resolution. An internal table translates the counter value into the sine and cosine values which control the motor current for microstepping.

1.4.2 SPI Direct Mode

The direct mode allows control of both motor coil currents and polarity via SPI. It mainly is intended for use with a dedicated external motion controller IC with integrated sequencer. The sequencer applies sine and cosine waves to the motor coils. This mode also allows control of DC motors, etc.

1.5 stealthChop Driver

stealthChop is a voltage chopper based principle. It guarantees absolutely quiet motor standstill and silent slow motion, except for noise generated by ball bearings. stealthChop can be combined with classic cycle-by-cycle chopper modes for best performance in all velocity ranges. Two additional chopper modes are available: a traditional constant off-time mode and the spreadCycle mode. The constant off-time mode provides high torque at highest velocity, while spreadCycle offers smooth operation and good power efficiency over a wide range of speed and load. spreadCycle automatically integrates a fast decay cycle and guarantees smooth zero crossing performance. The extremely smooth motion of stealthChop is beneficial for many applications.

Programmable microstep shapes allow optimizing the motor performance for low cost motors.

Benefits of using stealthChop:

- Significantly improved microstepping with low cost motors
- Motor runs smooth and quiet
- Absolutely no standby noise
- Reduced mechanical resonances yields improved torque

1.6 stallGuard2 – Mechanical Load Sensing

stallGuard2 provides an accurate measurement of the load on the motor. It can be used for stall detection as well as other uses at loads below those which stall the motor, such as coolStep load-adaptive current reduction. This gives more information on the drive allowing functions like sensorless homing and diagnostics of the drive mechanics.

1.7 coolStep – Load Adaptive Current Control

coolStep drives the motor at the optimum current. It uses the stallGuard2 load measurement information to adjust the motor current to the minimum amount required in the actual load situation. This saves energy and keeps the components cool.

Benefits are:

- *Energy efficiency* — power consumption decreased up to 75%
- *Motor generates less heat* — improved mechanical precision
- *Less or no cooling* — improved reliability
- *Use of smaller motor* — less torque reserve required → cheaper motor does the job

Figure 1.3 shows the efficiency gain of a 42mm stepper motor when using coolStep compared to standard operation with 50% of torque reserve. coolStep is enabled above 60RPM in the example.

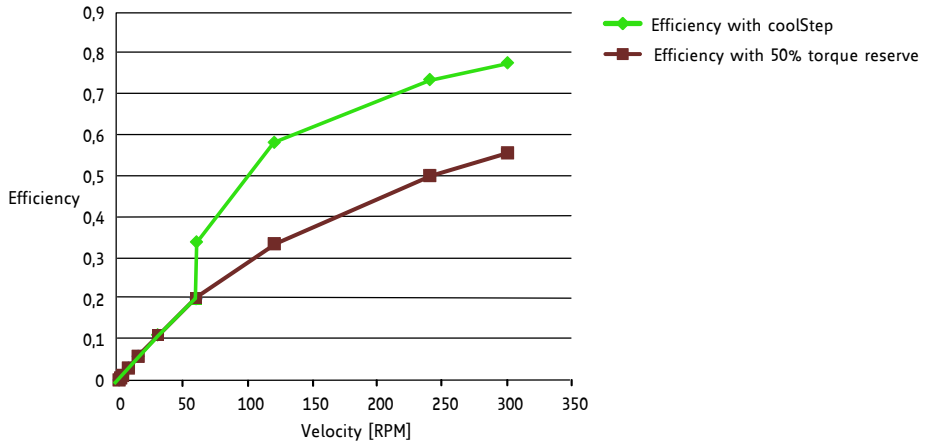


Figure 1.3 Energy efficiency with coolStep (example)

1.8 dcStep – Load Dependent Speed Control

dcStep allows the motor to run near its load limit and at its velocity limit without losing a step. If the mechanical load on the motor increases to the stalling load, the motor automatically decreases velocity so that it can still drive the load. With this feature, the motor will never stall. In addition to the increased torque at a lower velocity, dynamic inertia will allow the motor to overcome mechanical overloads by decelerating. dcStep feeds back status information to the external motion controller or to the system CPU, so that the target position will be reached, even if the motor velocity needs to be decreased due to increased mechanical load. A dynamic range of up to factor 10 or more can be covered by dcStep without any step loss. By optimizing the motion velocity in high load situations, this feature further enhances overall system efficiency.

Benefits are:

- Motor does not loose steps in overload conditions
- Application works as fast as possible
- Highest possible acceleration automatically
- Highest energy efficiency at speed limit
- Highest possible motor torque using fullstep drive
- Cheaper motor does the job

2 Pin Assignments

2.1 Package Outline

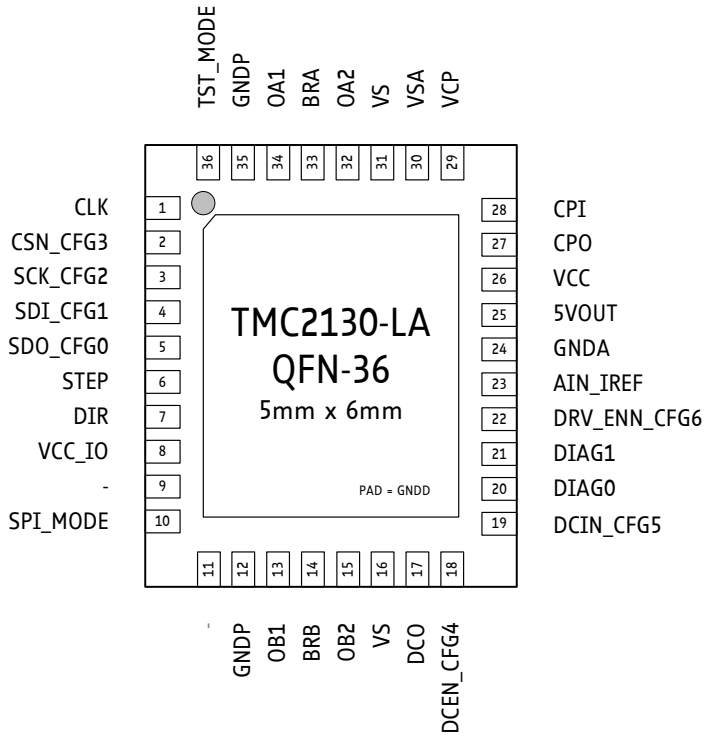


Figure 2.1 TMC2130-LA package and pinning QFN36 (5x6mm² body)

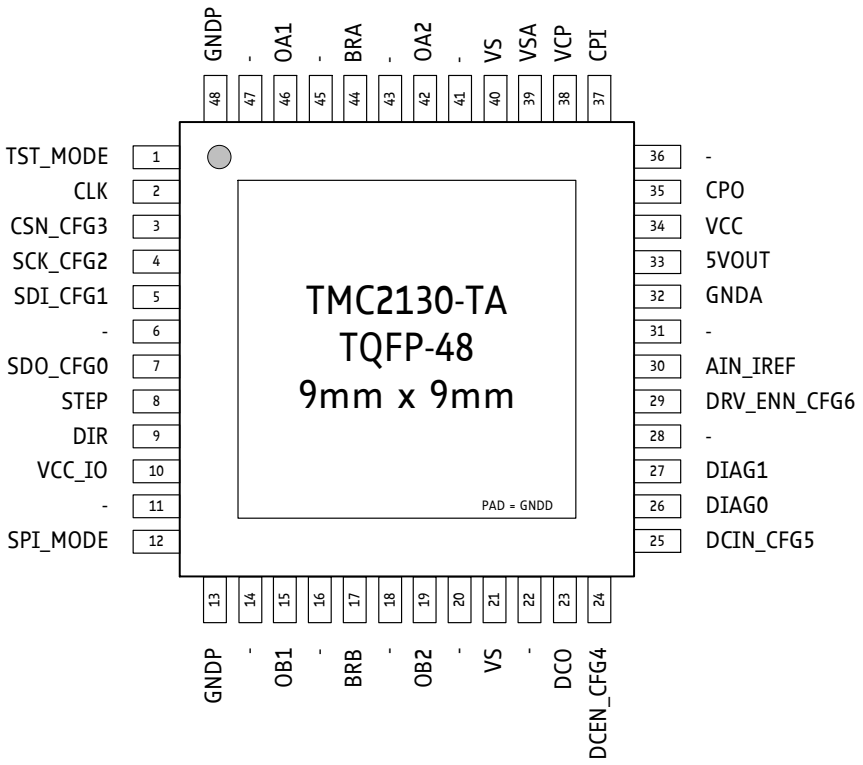


Figure 2.2 TMC2130-TA package and pinning TQFP-EP 48-EP (7x7mm² body, 9x9mm² with leads)

2.2 Signal Descriptions

Pin	QFN36	TQFP48	Type	Function
CLK	1	2	DI	CLK input. Tie to GND using short wire for internal clock or supply external clock.
CSN_CFG3	2	3	DI (tpu)	SPI chip select input (negative active) (SPI_MODE=1) or Configuration input (SPI_MODE=0) (tristate detection).
SCK_CFG2	3	4	DI (tpu)	SPI serial clock input (SPI_MODE=1) or Configuration input (SPI_MODE=0) (tristate detection).
SDI_CFG1	4	5	DI (tpu)	SPI data input (SPI_MODE=1) or Configuration input (SPI_MODE=0) (tristate detection).
SDO_CFG0	5	7	DIO (tpu)	SPI data output (tristate) (SPI_MODE=1) or Configuration input (SPI_MODE=0) (tristate detection).
STEP	6	8	DI	STEP input
DIR	7	9	DI	DIR input
VCC_IO	8	10		3.3V to 5V IO supply voltage for all digital pins.
DNC	9	11, 14, 16, 18, 20, 22, 28, 41, 43, 45, 47	-	Do not connect. Leave open!
SPI_MODE	10	12	DI (pu)	Mode selection input with pullup resistor. When tied low, the chip is in standalone mode and pins have their CFG functions. When tied high, the SPI interface is available for control. Integrated pull-up resistor.
N.C.	11	6, 31, 36		Unused pin, connect to GND for compatibility to future versions.
GNDP	12, 35	13, 48		Power GND. Connect to GND plane near pin.
OB1	13	15		Motor coil B output 1
BRB	14	17		Sense resistor connection for coil B. Place sense resistor to GND near pin. An additional 100nF capacitor to GND (GND plane) is recommended for best performance.
OB2	15	19		Motor coil B output 2
VS	16, 31	21, 40		Motor supply voltage. Provide filtering capacity near pin with short loop to nearest GNDP pin (respectively via GND plane).
DCO	17	23	DIO	dcStep ready output
DCEN_CFG4	18	24	DI (tpu)	dcStep enable input (SPI_MODE=1) - tie to GND for normal operation (no dcStep) or Configuration input (SPI_MODE=0) (tristate detection).
DCIN_CFG5	19	25	DI (tpu)	dcStep gating input for axis synchronization (SPI_MODE=1) or Configuration input (SPI_MODE=0) (tristate detection).
DIAG0	20	26	DIO	Diagnostics output DIAG0. Use external pull-up resistor with 47k or less in open drain mode.
DIAG1	21	27	DIO	Diagnostics output DIAG1. Use external pull-up resistor with 47k or less in open drain mode.
DRV_ENN_ CFG6	22	29	DI (tpu)	Enable input (SPI_MODE=1) or configuration / Enable input (SPI_MODE=0) (tristate detection). The power stage becomes switched off (all motor outputs floating) when this pin becomes driven to a high level.
AIN_IREF	23	30	AI	Analog reference voltage for current scaling (optional mode) or reference current for use of internal sense resistors

Pin	QFN36	TQFP48	Type	Function
GNDA	24	32		Analog GND. Tie to GND plane.
5VOUT	25	33		Output of internal 5V regulator. Attach 2.2µF or larger ceramic capacitor to GNDA near to pin for best performance. May be used to supply VCC of chip.
VCC	26	34		5V supply input for digital circuitry within chip and charge pump. Attach 470nF capacitor to GND (GND plane). May be supplied by 5VOUT. A 2.2 or 3.3 Ohm resistor is recommended for decoupling noise from 5VOUT. When using an external supply, make sure, that VCC comes up before or in parallel to 5VOUT or VCC_IO, whichever comes up later!
CPO	27	35		Charge pump capacitor output.
CPI	28	37		Charge pump capacitor input. Tie to CPO using 22nF 50V capacitor.
VCP	29	38		Charge pump voltage. Tie to VS using 100nF capacitor.
VSA	30	39		Analog supply voltage for 5V regulator. Normally tied to VS. Provide a 100nF filtering capacitor.
OA2	32	42		Motor coil A output 2
BRA	33	44		Sense resistor connection for coil A. Place sense resistor to GND near pin. An additional 100nF capacitor to GND (GND plane) is recommended for best performance.
OA1	34	46		Motor coil A output 1
TST_MODE	36	1	DI	Test mode input. Tie to GND using short wire.
Exposed die pad	-	-		Connect the exposed die pad to a GND plane. Provide as many as possible vias for heat transfer to GND plane. Serves as GND pin for digital circuitry.

*(pu) denominates a pin with pullup resistor; (tpu) denominates a pin with pullup resistor or toggle detection. Toggle detection is active in standalone mode, only (SPI_MODE=0)

3 Sample Circuits

The sample circuits show the connection of external components in different operation and supply modes. The connection of the bus interface and further digital signals is left out for clarity.

3.1 Standard Application Circuit

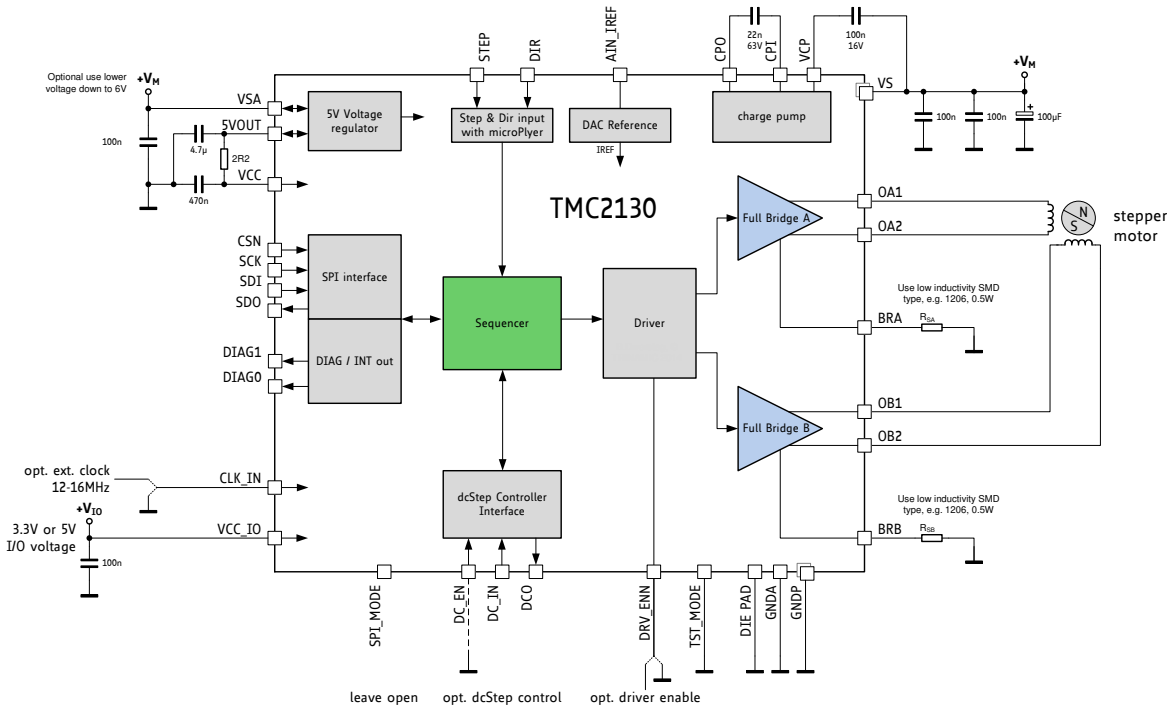


Figure 3.1 Standard application circuit

The standard application circuit uses a minimum set of additional components. Two sense resistors set the motor coil current. See chapter 9 to choose the right sense resistors. Use low ESR capacitors for filtering the power supply. The capacitors need to cope with the current ripple cause by chopper operation. A minimum capacity of 100µF near the driver is recommended for best performance. Current ripple in the supply capacitors also depends on the power supply internal resistance and cable length. VCC_IO can be supplied from 5VOUT, or from an external source, e.g. a low drop 3.3V regulator. In order to minimize linear voltage regulator power dissipation of the internal 5V voltage regulator in applications where VM is high, a different (lower) supply voltage can be used for VSA, if available. For example, many applications provide a 12V supply in addition to a higher driver supply voltage. Using the 12V supply for VSA rather than 24V will reduce the power dissipation of the internal 5V regulator to about 37% of the dissipation caused by supply with the full motor voltage.

Basic layout hints
Place sense resistors and all filter capacitors as close as possible to the related IC pins. Use a solid common GND for all GND connections, also for sense resistor GND. Connect 5VOUT filtering capacitor directly to 5VOUT and GNDA pin. See layout hints for more details. Low ESR electrolytic capacitors are recommended for VS filtering.

Attention
In case VSA is supplied by a different voltage source, make sure that VSA does not exceed VS by more than one diode drop upon power up or power down.

3.2 Reduced Number of Components

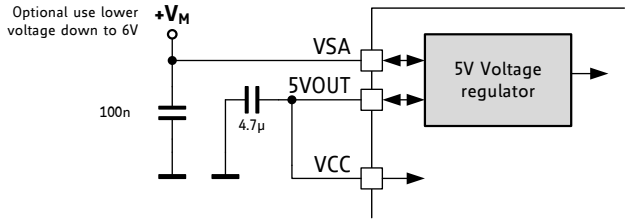


Figure 3.2 Reduced number of filtering components

The standard application circuit uses RC filtering to de-couple the output of the internal linear regulator from high frequency ripple caused by digital circuitry supplied by the VCC input. For cost sensitive applications, the RC-Filtering on VCC can be eliminated. This leads to more noise on 5VOUT caused by operation of the charge pump and the internal digital circuitry. There is a slight impact on microstep vibration and chopper noise performance.

3.3 Internal RDSon Sensing

For cost critical or space limited applications, sense resistors can be omitted. For internal current sensing, a reference current set by a tiny external resistor programs the output current. For calculation of the reference resistor, refer chapter 10.

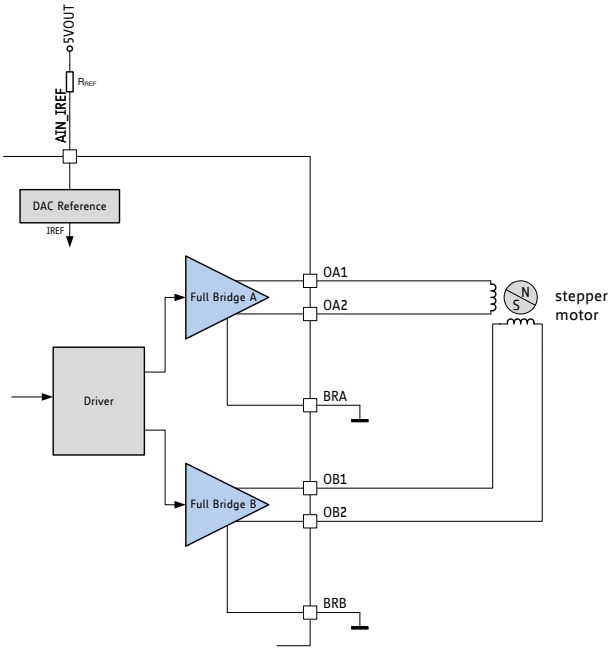


Figure 3.3 RDSon based sensing eliminates high current sense resistors

3.4 External 5V Power Supply

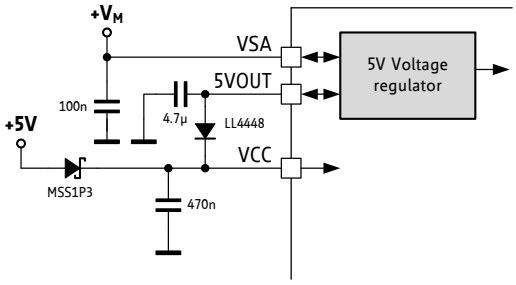
When an external 5V power supply is available, the power dissipation caused by the internal linear regulator can be eliminated. This especially is beneficial in high voltage applications, and when thermal conditions are critical. There are two options for using an external 5V source: either the external 5V source is used to support the digital supply of the driver by supplying the VCC pin, or the complete internal voltage regulator becomes bridged and is replaced by the external supply voltage.

3.4.1 Support for the VCC Supply

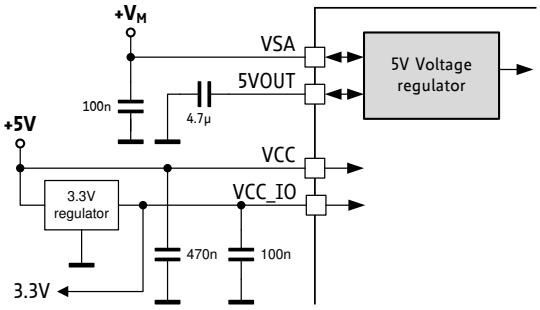
This scheme uses an external supply for all digital circuitry within the driver (Figure 3.4). As the digital circuitry makes up for most of the power dissipation, this way the internal 5V regulator sees only low remaining load. The precisely regulated voltage of the internal regulator is still used as the reference for the motor current regulation as well as for supplying internal analog circuitry.

When cutting VCC from 5VOUT, make sure that the VCC supply comes up before or synchronously with the 5VOUT supply to ensure a correct power up reset of the internal logic. A simple schematic uses two diodes forming an OR of the internal and the external power supplies for VCC. In order to prevent the chip from drawing part of the power from its internal regulator, a low drop 1A Schottky diode is used for the external 5V supply path, while a silicon diode is used for the 5VOUT path. An enhanced solution uses a dual PNP transistor as an active switch. It minimizes voltage drop and thus gives best performance.

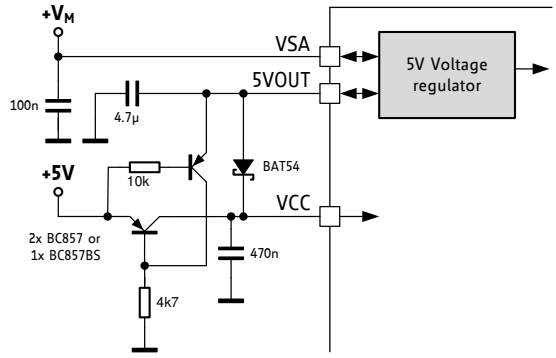
In certain setups, switching of VCC voltage can be eliminated. A third variant uses the VCC_IO supply to ensure power-on reset. This is possible, if VCC_IO comes up synchronously with or delayed to VCC. Use a linear regulator to generate a 3.3V VCC_IO from the external 5V VCC source. This 3.3V regulator will cause a certain voltage drop. A voltage drop in the regulator of 0.9V or more (e.g. LD1117-3.3) ensures that the 5V supply already has exceeded the lower limit of about 3.0V once the reset conditions ends. The reset condition ends earliest, when VCC_IO exceeds the undervoltage limit of minimum 2.1V. Make sure that the power-down sequence also is safe. Undefined states can result when VCC drops well below 4V without safely triggering a reset condition. Triggering a reset upon power-down can be ensured when VSA goes down synchronously with or before VCC.



VCC supplied from external 5V. 5V or 3.3V IO voltage.



VCC supplied from external 5V. 3.3V IO voltage generated from same source.



VCC supplied from external 5V using active switch. 5V or 3.3V IO voltage.

Figure 3.4 Using an external 5V supply for digital circuitry of driver (different options)

3.4.2 Internal Regulator Bridged

In case a clean external 5V supply is available, it can be used for complete supply of analog and digital part (Figure 3.5). The circuit will benefit from a well-regulated supply, e.g. when using a +/-1% regulator. A precise supply guarantees increased motor current precision, because the voltage at 5VOUT directly is the reference voltage for all internal units of the driver, especially for motor current control. For best performance, the power supply should have low ripple to give a precise and stable supply at 5VOUT pin with remaining ripple well below 5mV. Some switching regulators have a higher remaining ripple, or different loads on the supply may cause lower frequency ripple. In this case, increase capacity attached to 5VOUT. In case the external supply voltage has poor stability or low frequency ripple, this would affect the precision of the motor current regulation as well as add chopper noise.

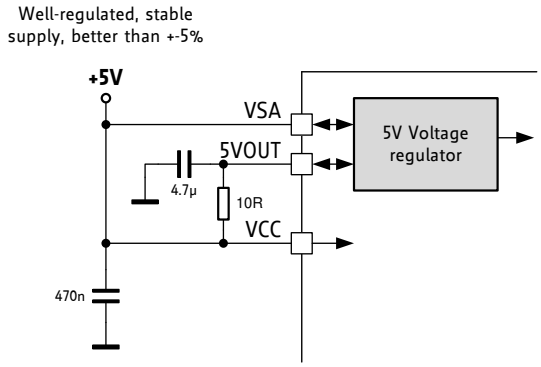


Figure 3.5 Using an external 5V supply to bypass internal regulator

3.5 Pre-Regulator for Reduced Power Dissipation

When operating at supply voltages up to 46V for VS and VSA, the internal linear regulator will contribute with up to 1W to the power dissipation of the driver. This will reduce the capability of the chip to continuously drive high motor current, especially at high environment temperatures. When no external power supply in the range 5V to 24V is available, an external pre-regulator can be built with a few inexpensive components in order to dissipate most of the voltage drop in external components. Figure 3.6 shows different examples. In case a well-defined supply voltage is available, a single 1W or higher power Zener diode also does the job.

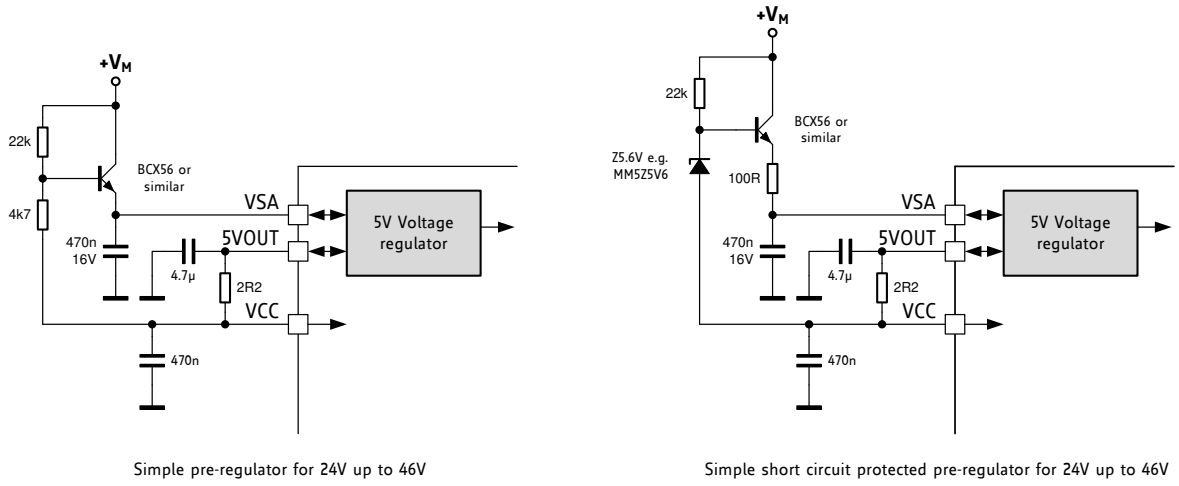


Figure 3.6 Examples for simple pre-regulators

3.6 5V Only Supply

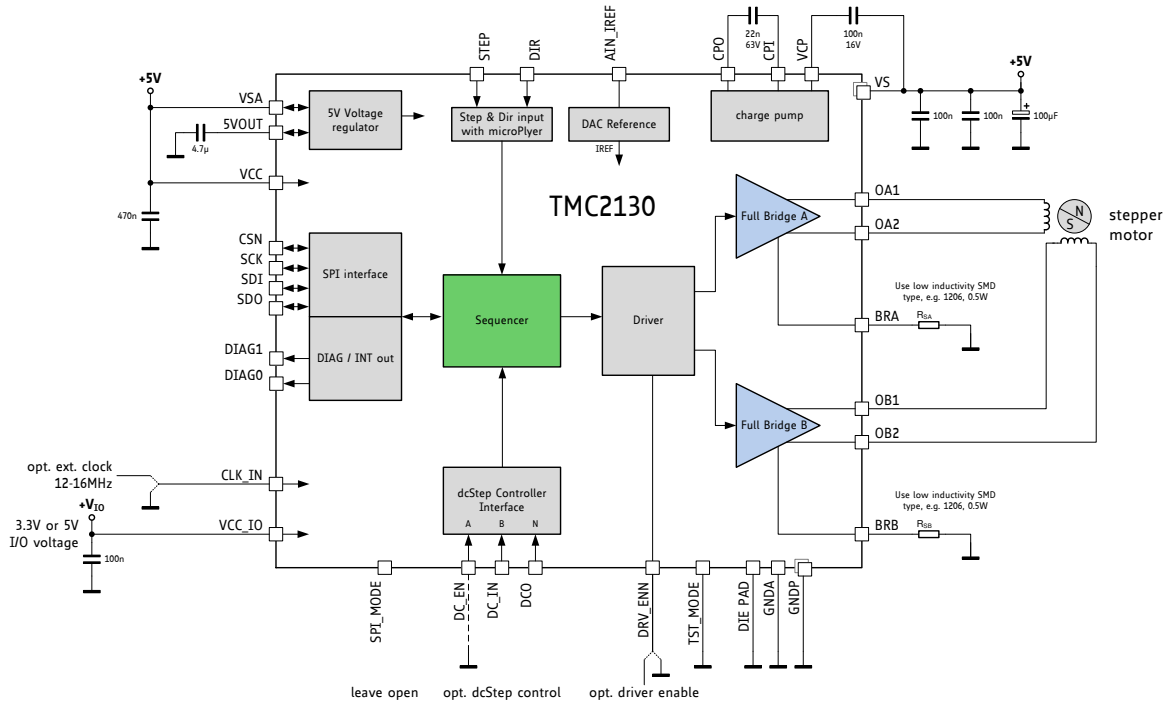


Figure 3.7 5V only operation

While the standard application circuit is limited to roughly 5.5 V lower supply voltage, a 5 V only application lets the IC run from a normal 5 V +/-5% supply. In this application, linear regulator drop must be minimized. Therefore, the major 5 V load is removed by supplying VCC directly from the external supply. In order to keep supply ripple away from the analog voltage reference, 5VOUT should have an own filtering capacity and the 5VOUT pin does not become bridged to the 5V supply.

3.7 High Motor Current

When operating at a high motor current, the driver power dissipation due to MOSFET switch on-resistance significantly heats up the driver. This power dissipation will heat up the PCB cooling infrastructure also, if operated at an increased duty cycle. This in turn leads to a further increase of driver temperature. An increase of temperature by about 100°C increases MOSFET resistance by roughly 50%. This is a typical behavior of MOSFET switches. Therefore, under high duty cycle, high load conditions, thermal characteristics have to be carefully taken into account, especially when increased environment temperatures are to be supported. Refer the thermal characteristics and the layout hints for more information. As a thumb rule, thermal properties of the PCB design become critical for the QFN-36 at or above about 1000mA RMS motor current for increased periods of time. Keep in mind that resistive power dissipation raises with the square of the motor current. On the other hand, this means that a small reduction of motor current significantly saves heat dissipation and energy.

An effect which might be perceived at medium motor velocities and motor sine wave peak currents above roughly 1.2A peak is a slight sine distortion of the current wave when using spreadCycle. It results from an increasing negative impact of parasitic internal diode conduction, which in turn negatively influences the duration of the fast decay cycle of the spreadCycle chopper. This is, because the current measurement does not see the full coil current during this phase of the sine wave, because an increasing part of the current flows directly from the power MOSFETs' drain to GND and does not flow through the sense resistor. This effect with most motors does not negatively influence the smoothness of operation, as it does not impact the critical current zero transition. The effect does not occur with stealthChop.

3.7.1 Reduce Linear Regulator Power Dissipation

When operating at high supply voltages, as a first step the power dissipation of the integrated 5V linear regulator can be reduced, e.g. by using an external 5V source for supply. This will reduce overall heating. It is advised to reduce motor stand still current in order to decrease overall power dissipation. If applicable, also use coolStep. A decreased clock frequency will reduce power dissipation of the internal logic. Further a decreased chopper frequency also can reduce power dissipation.

3.7.2 Operation near to / above 2A Peak Current

The driver can deliver up to 2.5A motor peak current. Considering thermal characteristics, this only is possible in duty cycle limited operation. When a peak current up to 2.5A is to be driven, the driver chip temperature is to be kept at a maximum of 105°C. Linearly derate the design peak temperature from 125°C to 105°C in the range 2A to 2.5A output current (see Figure 3.8). Exceeding this may lead to triggering the short circuit detection.

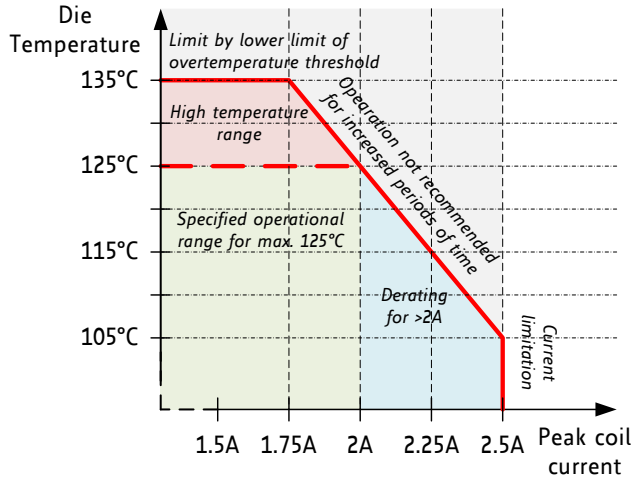


Figure 3.8 Derating of maximum sine wave peak current at increased die temperature

3.7.3 Reduction of Resistive Losses by Adding Schottky Diodes

Schottky Diodes can be added to the circuit to reduce driver power dissipation when driving high motor currents (see Figure 3.9). The Schottky diodes have a conduction voltage of about 0.5V and will take over more than half of the motor current during the negative half wave of each output in slow decay and fast decay phases, thus leading to a cooler motor driver. This effect starts from a few percent at 1.2A and increases with higher motor current rating up to roughly 20%. As a 30V Schottky diode has a lower forward voltage than a 50V or 60V diode, it makes sense to use a 30V diode when the supply voltage is below 30V. The diodes will have less effect when working with stealthChop due to lower times of diode conduction in the chopper cycle. At current levels below 1.2A coil current, the effect of the diodes is negligible.

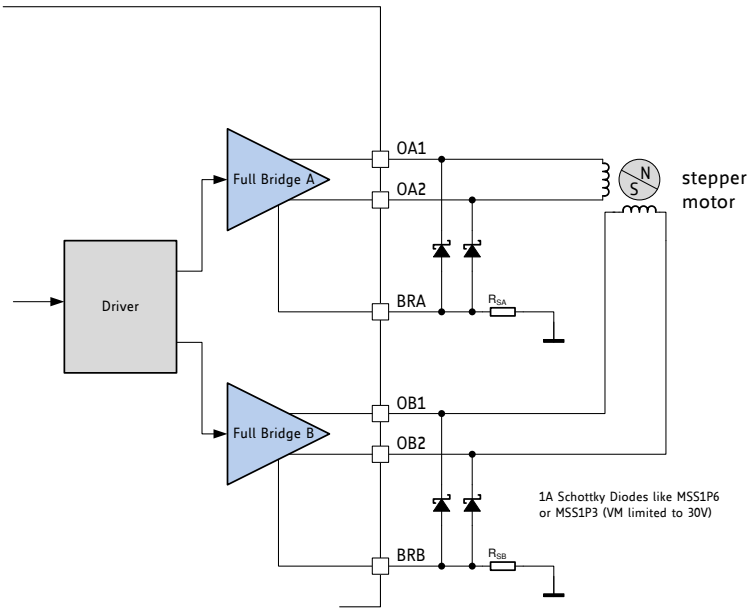


Figure 3.9 Schottky diodes reduce power dissipation at high peak currents up to 2A (2.5A)

3.8 Driver Protection and EME Circuitry

Some applications have to cope with ESD events caused by motor operation or external influence. Despite ESD circuitry within the driver chips, ESD events occurring during operation can cause a reset or even a destruction of the motor driver, depending on their energy. Especially plastic housings and belt drive systems tend to cause ESD events of several kV. It is best practice to avoid ESD events by attaching all conductive parts, especially the motors themselves to PCB ground, or to apply electrically conductive plastic parts. In addition, the driver can be protected up to a certain degree against ESD events or live plugging / pulling the motor, which also causes high voltages and high currents into the motor connector terminals. A simple scheme uses capacitors at the driver outputs to reduce the dV/dt caused by ESD events. Larger capacitors will bring more benefit concerning ESD suppression, but cause additional current flow in each chopper cycle, and thus increase driver power dissipation, especially at high supply voltages. The values shown are example values – they might be varied between 100pF and 1nF. The capacitors also dampen high frequency noise injected from digital parts of the application PCB circuitry and thus reduce electromagnetic emission. A more elaborate scheme uses LC filters to de-couple the driver outputs from the motor connector. Varistors in between of the coil terminals eliminate coil overvoltage caused by live plugging. Optionally protect all outputs by a varistor against ESD voltage.

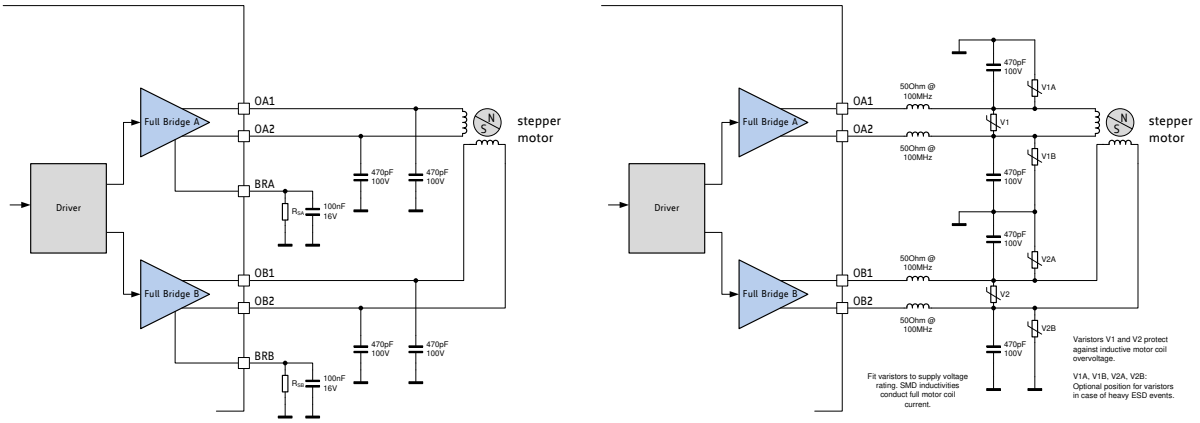


Figure 3.10 Simple ESD enhancement and more elaborate motor output protection

4 SPI Interface

4.1 SPI Datagram Structure

The TMC2130 uses 40 bit SPI™ (Serial Peripheral Interface, SPI is Trademark of Motorola) datagrams for communication with a microcontroller. Microcontrollers which are equipped with hardware SPI are typically able to communicate using integer multiples of 8 bit. The NCS line of the device must be handled in a way, that it stays active (low) for the complete duration of the datagram transmission.

Each datagram sent to the device is composed of an address byte followed by four data bytes. This allows direct 32 bit data word communication with the register set. Each register is accessed via 32 data bits even if it uses less than 32 data bits.

For simplification, each register is specified by a one byte address:

- For a read access the most significant bit of the address byte is 0.
- For a write access the most significant bit of the address byte is 1.

Most registers are write only registers, some can be read additionally, and there are also some read only registers.

SPI DATAGRAM STRUCTURE

MSB (transmitted first)	40 bit	LSB (transmitted last)
39 …		… 0
→ 8 bit address **← 8 bit SPI status**	**← → 32 bit data**	
39 … 32	31 … 0	
→ to TMC2130 RW + 7 bit address ← from TMC2130 8 bit SPI status	8 bit data	8 bit data	8 bit data	8 bit data
39 / 38 … 32	31 … 24	23 … 16	15 … 8	7 … 0

w	38…32							31…28				27…24				23…20				19…16				15…12				11…8				7…4				3…0			
39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

4.1.1 Selection of Write / Read (WRITE_notREAD)

The read and write selection is controlled by the MSB of the address byte (bit 39 of the SPI datagram). This bit is 0 for read access and 1 for write access. So, the bit named W is a WRITE_notREAD control bit. The active high write bit is the MSB of the address byte. So, 0x80 has to be added to the address for a write access. The SPI interface always delivers data back to the master, independent of the W bit. The data transferred back is the data read from the address which was transmitted with the *previous* datagram, if the previous access was a read access. If the previous access was a write access, then the data read back mirrors the previously received write data. So, the difference between a read and a write access is that the read access does not transfer data to the addressed register but it transfers the address only and its 32 data bits are dummies, and, further the following read or write access delivers back the data read from the address transmitted in the preceding read cycle.

A read access request datagram uses dummy write data. Read data is transferred back to the master with the subsequent read or write access. Hence, reading multiple registers can be done in a pipelined fashion.

Whenever data is read from or written to the TMC2130, the MSBs delivered back contain the SPI status, *SPI_STATUS*, a number of eight selected status bits.

Example:

For a read access to the register (*DRV_STATUS*) with the address 0x6F, the address byte has to be set to 0x6F in the access preceding the read access. For a write access to the register (*CHOPCONF*), the address byte has to be set to 0x80 + 0x6C = 0xEC. For read access, the data bit might have any value (-). So, one can set them to 0.

action	data sent to TMC2130	data received from TMC2130
read *DRV_STATUS*	→ 0x6F00000000	← 0xSS & unused data
read *DRV_STATUS*	→ 0x6F00000000	← 0xSS & DRV_STATUS
write *CHOPCONF*:= 0x00ABCDEF	→ 0xEC00ABCDEF	← 0xSS & DRV_STATUS
write *CHOPCONF*:= 0x00123456	→ 0xEC00123456	← 0xSS00ABCDEF

*)S: is a placeholder for the status bits *SPI_STATUS*

4.1.2 SPI Status Bits Transferred with Each Datagram Read Back

New status information becomes latched at the end of each access and is available with the next SPI transfer.

***SPI_STATUS* – status flags transmitted with each SPI access in bits 39 to 32**		
Bit	**Name**	**Comment**
7	-	*unused*
6	-	*unused*
5	-	*unused*
4	-	*unused*
3	*standstill*	*DRV_STATUS*[31] – 1: Signals motor stand still
2	*sg2*	*DRV_STATUS*[24] – 1: Signals stallguard flag active
1	*driver_error*	*GSTAT*[1] – 1: Signals driver 1 driver error (clear by reading *GSTAT*)
0	*reset_flag*	*GSTAT*[0] – 1: Signals, that a reset has occurred (clear by reading *GSTAT*)

4.1.3 Data Alignment

All data are right aligned. Some registers represent unsigned (positive) values, some represent integer values (signed) as two's complement numbers, single bits or groups of bits are represented as single bits respectively as integer groups.

4.2 SPI Signals

The SPI bus on the TMC2130 has four signals:

- SCK – bus clock input
- SDI – serial data input
- SDO – serial data output
- CSN – chip select input (active low)

The slave is enabled for an SPI transaction by a low on the chip select input CSN. Bit transfer is synchronous to the bus clock SCK, with the slave latching the data from SDI on the rising edge of SCK and driving data to SDO following the falling edge. The most significant bit is sent first. A minimum of 40 SCK clock cycles is required for a bus transaction with the TMC2130.

If more than 40 clocks are driven, the additional bits shifted into SDI are shifted out on SDO after a 40-clock delay through an internal shift register. This can be used for daisy chaining multiple chips.

CSN must be low during the whole bus transaction. When CSN goes high, the contents of the internal shift register are latched into the internal control register and recognized as a command from the master to the slave. If more than 40 bits are sent, only the last 40 bits received before the rising edge of CSN are recognized as the command.

4.3 Timing

The SPI interface is synchronized to the internal system clock, which limits the SPI bus clock SCK to half of the system clock frequency. If the system clock is based on the on-chip oscillator, an additional 10% safety margin must be used to ensure reliable data transmission. All SPI inputs as well as the ENN input are internally filtered to avoid triggering on pulses shorter than 20ns. Figure 4.1 shows the timing parameters of an SPI bus transaction, and the table below specifies their values.

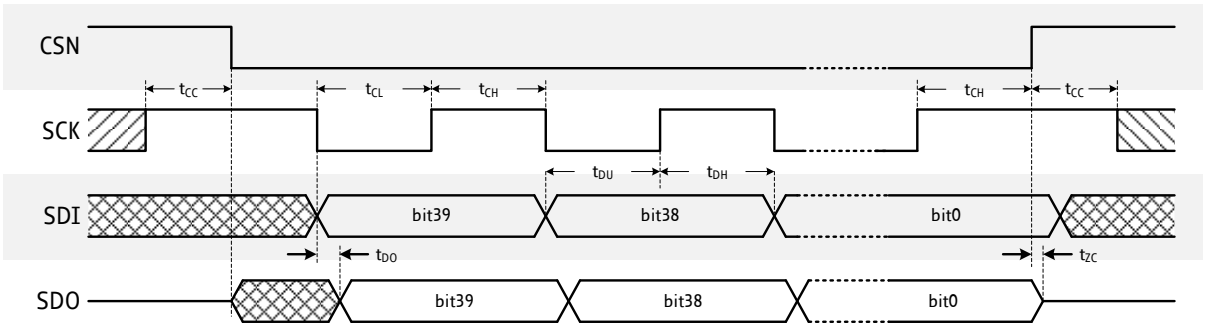


Figure 4.1 SPI timing

Hint
Usually this SPI timing is referred to as SPI MODE 3

SPI interface timing	**AC-Characteristics** clock period: t_{CLK}					
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
SCK valid before or after change of CSN	t_{CC}		10			ns
CSN high time	t_{CSH}	*) Min time is for synchronous CLK with SCK high one t_{CH} before CSN high only	t_{CLK}*)	>2t_{CLK}+10		ns
SCK low time	t_{CL}	*) Min time is for synchronous CLK only	t_{CLK}*)	>t_{CLK}+10		ns
SCK high time	t_{CH}	*) Min time is for synchronous CLK only	t_{CLK}*)	>t_{CLK}+10		ns
SCK frequency using internal clock	f_{SCK}	assumes minimum OSC frequency			4	MHz
SCK frequency using external 16MHz clock	f_{SCK}	assumes synchronous CLK			8	MHz
SDI setup time before rising edge of SCK	t_{DU}		10			ns
SDI hold time after rising edge of SCK	t_{DH}		10			ns
Data out valid time after falling SCK clock edge	t_{DO}	no capacitive load on SDO			t_{FILT}+5	ns
SDI, SCK and CSN filter delay time	t_{FILT}	rising and falling edge	12	20	30	ns

5 Register Mapping

This chapter gives an overview of the complete register set. Some of the registers bundling a number of single bits are detailed in extra tables. The functional practical application of the settings is detailed in dedicated chapters.

Note
- All registers become reset to 0 upon power up, unless otherwise noted.
- Add 0x80 to the address **Addr** for write accesses!

NOTATION OF HEXADECIMAL AND BINARY NUMBERS	
0x	precedes a hexadecimal number, e.g. 0x04
%	precedes a multi-bit binary number, e.g. %100

NOTATION OF R/W FIELD	
R	Read only
W	Write only
R/W	Read- and writable register
R+C	Clear upon read

OVERVIEW REGISTER MAPPING

REGISTER	**DESCRIPTION**
General Configuration Registers	These registers contain - global configuration - global status flags - interface configuration - and I/O signal configuration
Velocity Dependent Driver Feature Control Register Set	This register set offers registers for - driver current control - setting thresholds for coolStep operation - setting thresholds for different chopper modes - setting thresholds for dcStep operation
Motor Driver Register Set	This register set offers registers for - setting / reading out microstep table and counter - chopper and driver configuration - coolStep and stallGuard2 configuration - dcStep configuration - reading out stallGuard2 values and driver error flags
dcStep Minimum Velocity	Setting for minimum dcStep velocity

5.1 General Configuration Registers

GENERAL CONFIGURATION REGISTERS (0X00…0X0F)					
R/W	**Addr**	**n**	***Register***	**Description */ bit names***	
RW	0x00	17	*GCONF*	**Bit**	***GCONF* – Global configuration flags**
				0	*I_scale_analog* 0: Normal operation, use internal reference voltage 1: Use voltage supplied to AIN as current reference
				1	*internal_Rsense* 0: Normal operation 1: Internal sense resistors. Use current supplied into AIN as reference for internal sense resistor
				2	*en_pwm_mode* 1: stealthChop voltage PWM mode enabled (depending on velocity thresholds). Switch from off to on state while in stand still, only.
				3	*enc_commutation* 1: Enable commutation by full step encoder (DCIN_CFG5 = ENC_A, DCEN_CFG4 = ENC_B)
				4	*shaft* 1: Inverse motor direction
				5	*diag0_error* 1: Enable DIAG0 active on driver errors: Over temperature (*ot*), short to GND (*s2g*), undervoltage chargepump (*uv_cp*) DIAG0 always shows the reset-status, i.e. is active low during reset condition.
				6	*diag0_otpw* 1: Enable DIAG0 active on driver over temperature prewarning (*otpw*)
				7	*diag0_stall* 1: Enable DIAG0 active on motor stall (set *TCOOLTHRS* before using this feature)
				8	*diag1_stall* 1: Enable DIAG1 active on motor stall (set *TCOOLTHRS* before using this feature)
				9	*diag1_index* 1: Enable DIAG1 active on index position (microstep look up table position 0)
				10	*diag1_onstate* 1: Enable DIAG1 active when chopper is on (for the coil which is in the second half of the fullstep)
				11	*diag1_steps_skipped* 1: Enable output toggle when steps are skipped in dcStep mode (increment of *LOST_STEPS*). Do not enable in conjunction with other DIAG1 options.
				12	*diag0_int_pushpull* 0: DIAG0 is open collector output (active low) 1: Enable DIAG0 push pull output (active high)
				13	*diag1_pushpull* 0: DIAG1 is open collector output (active low) 1: Enable DIAG1 push pull output (active high)
				14	*small_hysteresis* 0: Hysteresis for step frequency comparison is 1/16 1: Hysteresis for step frequency comparison is 1/32