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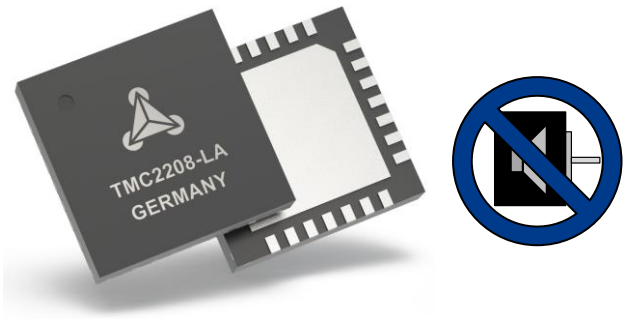
TMC2208/2 & TMC2224/0/5 family Datasheet

TMC2202, TMC2208, TMC2220, TMC2224, TMC2225 Step/Dir Drivers for Two-Phase Bipolar Stepper Motors up to 2A peak - stealthChop™ for Quiet Movement - UART Interface Option.



Applications

Compatible Design Upgrade
3D Printers
Printers, POS
Office and home automation
Textile, Sewing Machines
CCTV, Security
ATM, Cash recycler
HVAC

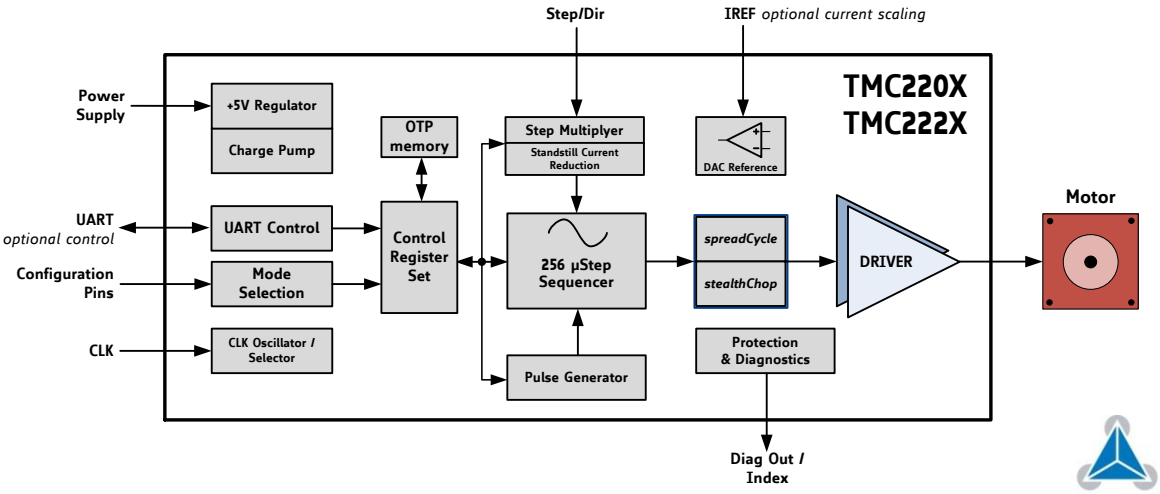
Features and Benefits

2-phase stepper motors up to 2A coil current (peak)
STEP/DIR Interface with 2, 4, 8, 16 or 32 microstep pin setting
Smooth Running 256 microsteps by **microPlyer™** interpolation
stealthChop2™ silent motor operation
spreadCycle™ highly dynamic motor control chopper
Low RDSon LS 280mΩ & HS 290mΩ (typ. at 25°C)
Voltage Range 4.75... 36V DC
Automatic Standby current reduction (option)
Internal Sense Resistor option (no sense resistors required)
Passive Braking and Freewheeling
Single Wire UART & OTP for advanced configuration options
Integrated Pulse Generator for standalone motion
Full Protection & Diagnostics
Choice of QFN, TQFP and HTSSOP packages for best fit

Description

The TMC2202, TMC2208, TMC2220, TMC2224 and TMC2225 are ultra-silent motor driver ICs for two phase stepper motors. Their pinning is compatible to a number of legacy drivers. TRINAMICs sophisticated stealthChop2 chopper ensures noiseless operation, maximum efficiency and best motor torque. Its fast current regulation and optional combination with spreadCycle allow for highly dynamic motion. Integrated power-MOSFETs handle motor current up to 1.4A RMS. Protection and diagnostic features support robust and reliable operation. A simple to use UART interface opens up more tuning and control options. Application specific tuning can be stored to OTP memory. Industries' most advanced STEP/DIR stepper motor driver family upgrades designs to noiseless and most precise operation for cost-effective and highly competitive solutions.

Block Diagram



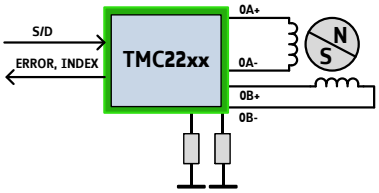
TRINAMIC Motion Control GmbH & Co. KG
Hamburg, Germany

TRINAMIC
MOTION CONTROL

APPLICATION EXAMPLES: SIMPLE SOLUTIONS – HIGHLY EFFECTIVE

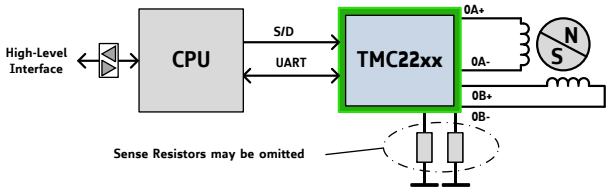
The TMC22xx family scores with power density, integrated power MOSFETs, smooth and quiet operation, and a congenial simplicity. The TMC22xx covers a wide spectrum of applications from battery systems to embedded applications with up to 2A motor current per coil. TRINAMICs unique chopper modes spreadCycle and stealthChop2 optimize drive performance. stealthChop reduces motor noise to the point of silence at low velocities. Standby current reduction keeps costs for power dissipation and cooling down. Extensive support enables rapid design cycles and fast time-to-market with competitive products.

STANDALONE REPLACEMENT FOR LEGACY STEPPER DRIVER



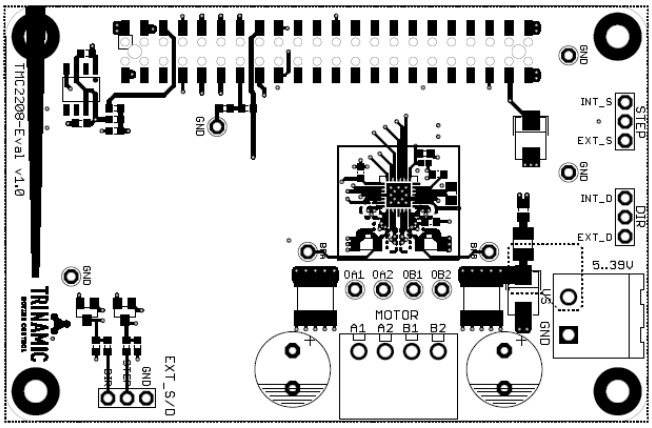
In this example, configuration is hard wired via pins. Software based motion control generates STEP and DIR (direction) signals, INDEX and ERROR signals report back status information.

UART INTERFACE FOR FULL DIAGNOSTICS AND CONTROL



A CPU operates the driver via step and direction signals. It accesses diagnostic information and configures the TMC22xx via the UART interface. The CPU manages motion control and the TMC22xx drives the motor and smoothens and optimizes drive performance.

TMC2208-EVAL EVALUATION BOARD



The TMC22xx-EVAL is part of TRINAMICs universal evaluation board system which provides a convenient handling of the hardware as well as a user-friendly software tool for evaluation. The TMC22xx evaluation board system consists of three parts: STARTRAMPE (base board), TMC2208-BRIDGE (connector board with several test points and stand-alone settings), and TMC22xx-EVAL.

ORDER CODES

Order code	Description	Size [mm²]
TMC2208-LA	stealthChop standalone driver; QFN28 (RoHS compliant)	5 x 5
TMC2224-LA	stealthChop standalone driver; QFN28 (RoHS compliant)	5 x 5
TMC2202-WA	stealthChop driver; wettable edge QFN32 (RoHS compliant)	5 x 5
TMC2220-TA	Option package: TQFP 48 – *please request for availability!*	9 x 9
TMC2225-SA	Option package: HTSSOP28 – *please request for availability!*	9.7 x 6.4
TMC2208-EVAL	Evaluation board for TMC2208 stepper motor driver	85 x 55
TMC2224-EVAL	Evaluation board for TMC2224 stepper motor driver	85 x 55
TMC22xx-Bridge	Connector and jumper board fitting to TMC22xx family	61 x 38
STARTRAMPE	Baseboard for TMC2208-EVAL and further evaluation boards	85 x 55

Table of Contents

1 Principles of Operation

The TMC22xx family of stepper drivers is intended as a drop-in upgrade for existing low cost stepper driver applications. Its silent drive technology stealthChop enables non-bugging motion control for home and office applications. A highly efficient power stage enables high current from a tiny package.

The TMC22xx requires just a few control pins on its tiny package. They allow selection of the most important setting: the desired microstep resolution. A choice of 2, 4, 8, 16 or 32 microsteps adapts the driver to the capabilities of the motion controller. Some package options also allow chopper mode selection by pin.

Even at low microstepping rate, the TMC22xx offers a number of unique enhancements over comparable products: TRINAMICs sophisticated stealthChop2 chopper plus the microstep enhancement microPlyer ensure noiseless operation, maximum efficiency and best motor torque. Its fast current regulation and optional combination with spreadCycle allow for highly dynamic motion. Protection and diagnostic features support robust and reliable operation. A simple-to-use 8 bit UART interface opens up more tuning and control options. Application specific tuning can be stored to on-chip OTP memory. Industries' most advanced step & direction stepper motor driver family upgrades designs to noiseless and most precise operation for cost-effective and highly competitive solutions.

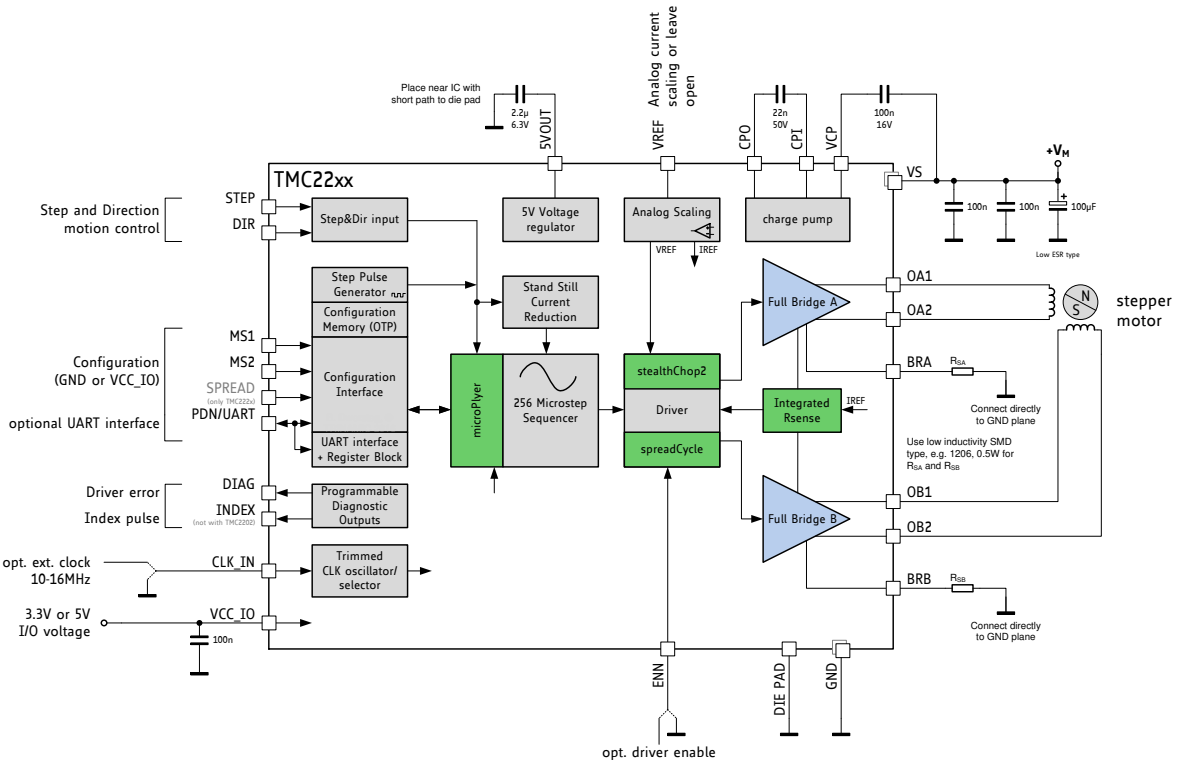


Figure 1.1 TMC22xx basic application block diagram

THREE MODES OF OPERATION:

OPTION 1: Standalone STEP/DIR Driver (Legacy Mode)

A CPU (µC) generates step & direction signals synchronized to additional motors and other components within the system. The TMC22xx operates the motor as commanded by the configuration pins and STEP/DIR signals. Motor run current either is fixed, or set by the CPU using the analog input VREF. The pin PDN_UART selects automatic standstill current reduction. Feedback from the driver to the CPU is granted by the INDEX and DIAG output signals. Enable or disable the motor using the ENN pin.

OPTION 2: Standalone STEP/DIR Driver with OTP pre-configuration

Additional options enabled by pre-programming OTP memory (label UART & OTP):

+ Tuning of the chopper to the application for application tailored performance
+ Cost reduction by switching the driver to internal sense resistor mode
+ Adapting the automatic power down level and timing for best application efficiency

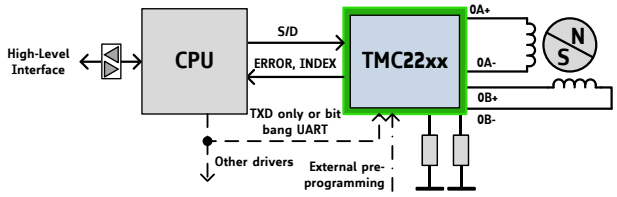


Figure 1.2 Stand-alone driver with pre-configuration

To enable the additional options, either one-time program the driver's OTP memory, or store configuration in the CPU and transfer it to the on-chip registers following each power-up. Operation uses the same signals as Option 1. Programming does not need to be done within the application - it can be executed during testing of the PCB! Alternatively, use bit-banging by CPU firmware to configure the driver. Multiple drivers can be programmed at the same time using a single TXD line.

OPTION 3: STEP/DIR Driver with Full Diagnostics and Control

Similar to Option 2, but pin PDN_UART is connected to the CPU UART interface.

Additional options (label UART):

+ Detailed diagnostics and thermal management
+ Passive braking and freewheeling for flexible, lowest power stop modes
+ More options for microstep resolution setting (fullstep to 256 microstep)
+ Software controlled motor current setting and more chopper options

This mode allows replacing all control lines like ENN, DIAG, INDEX, MS1, MS2, and analog current setting VREF by a single interface line. This way, only three signals are required for full control: STEP, DIR and PDN_UART. Even motion without external STEP pulses is provided by an internal programmable step pulse generator: Just set the desired motor velocity. However, no ramping is provided by the TMC22xx. Access to multiple driver ICs is possible using an analog multiplexer IC.

1.1 Key Concepts

The TMC22xx implements advanced features which are exclusive to TRINAMIC products. These features contribute toward greater precision, greater energy efficiency, higher reliability, smoother motion, and cooler operation in many stepper motor applications.

stealthChop2™ No-noise, high-precision chopper algorithm for inaudible motion and inaudible standstill of the motor. Allows faster motor acceleration and deceleration than stealthChop™ and extends stealthChop to low stand still motor currents.

spreadCycle™ High-precision cycle-by-cycle current control algorithm for highest dynamic movements.

microPlyer™ Microstep interpolator for obtaining full 256 microstep smoothness with lower resolution step inputs starting from fullstep

In addition to these performance enhancements, TRINAMIC motor drivers offer safeguards to detect and protect against shorted outputs, output open-circuit, overtemperature, and undervoltage conditions for enhancing safety and recovery from equipment malfunctions.

1.2 Control Interfaces

The TMC22xx supports both, discrete control lines for basic mode selection and a UART based single wire interface with CRC checking. The UART interface automatically becomes enabled when correct UART data is sent. When using UART, the pin selection may be disabled by control bits.

1.2.1 UART Interface

The single wire interface allows unidirectional operation (for parameter setting only), or bi-directional operation for full control and diagnostics. It can be driven by any standard microcontroller UART or even by bit banging in software. Baud rates from 9600 Baud to 500k Baud or even higher (when using an external clock) may be used. No baud rate configuration is required, as the TMC22xx automatically adapts to the masters' baud rate. The frame format is identical to the intelligent TRINAMIC controller & driver ICs TMC5130 and TMC5072. A CRC checksum allows data transmission over longer distance. For fixed initialization sequences, store the data including CRC into the µC, thus consuming only a few 100 bytes of code for a full initialization. CRC may be ignored during read access, if not desired. This makes CRC use an optional feature! The IC has a fixed address. Multiple drivers can be programmed in parallel by tying together all interface pins, in case no read access is required. An optional addressing can be provided by analog multiplexers, like 74HC4066.

From a software point of view the TMC22xx is a peripheral with a number of control and status registers. Most of them can either be written only or are read only. Some of the registers allow both, read and write access. In case read-modify-write access is desired for a write only register, a shadow register can be realized in master software.

1.3 Moving and Controlling the Motor

1.3.1 STEP/DIR Interface

The motor is controlled by a step and direction input. Active edges on the STEP input can be rising edges or both rising and falling edges as controlled by a special mode bit (DEDGE). Using both edges cuts the toggle rate of the STEP signal in half, which is useful for communication over slow interfaces such as optically isolated interfaces. The state sampled from the DIR input upon an active STEP edge determines whether to step forward or back. Each step can be a fullstep or a microstep, in which there are 2, 4, 8, 16, 32, 64, 128, or 256 microsteps per fullstep. A step impulse with a low state on DIR increases the microstep counter and a high decreases the counter by an amount controlled by the microstep resolution. An internal table translates the counter value into the sine and cosine values which control the motor current for microstepping.

1.3.2 Internal Step Pulse Generator

Some applications do not require a precisely co-ordinate motion – the motor just is required to move for a certain time and at a certain velocity. The TMC22xx comes with an internal pulse generator for these applications: Just provide the velocity via UART interface to move the motor. The velocity sign automatically controls the direction of the motion. However, the pulse generator does not integrate a ramping function. Motion at higher velocities will require ramping up and ramping down the velocity value via software.

STEP/DIR mode and internal pulse generator mode can be mixed in an application!

1.4 stealthChop2 & spreadCycle Driver

stealthChop is a voltage chopper based principle. It especially guarantees that the motor is absolutely quiet in standstill and in slow motion, except for noise generated by ball bearings. Unlike other voltage mode choppers, stealthChop2 does not require any configuration. It automatically learns the best settings during the first motion after power up and further optimizes the settings in subsequent motions. An initial homing sequence is sufficient for learning. Optionally, initial learning parameters can be stored to OTP. stealthChop2 allows high motor dynamics, by reacting at once to a change of motor velocity.

For highest velocity applications, spreadCycle is an option to stealthChop2. It can be enabled via input pin (TMC222x) or via UART and OTP. stealthChop2 and spreadCycle may even be used in a combined configuration for the best of both worlds: stealthChop2 for no-noise stand still, silent and smooth performance, spreadCycle at higher velocity for high dynamics and highest peak velocity at low vibration.

spreadCycle is an advanced cycle-by-cycle chopper mode. It offers smooth operation and good resonance dampening over a wide range of speed and load. The spreadCycle chopper scheme automatically integrates and tunes fast decay cycles to guarantee smooth zero crossing performance.

Benefits of using stealthChop2:

- Significantly improved microstepping with low cost motors
- Motor runs smooth and quiet
- Absolutely no standby noise
- Reduced mechanical resonance yields improved torque

1.5 Precise clock generator and CLK input

The TMC22xx provides a factory trimmed internal clock generator for precise chopper frequency and performance. However, an optional external clock input is available for cases, where quartz precision is desired, or where a lower or higher frequency is required. For safety, the clock input features timeout detection, and switches back to internal clock upon fail of the external source.

1.6 Automatic Standstill Power Down

An automatic current reduction drastically reduces application power dissipation and cooling requirements. Per default, the stand still current reduction is enabled by pulling PDN_UART input to GND. It reduces standstill power dissipation to less than 33% by going to slightly more than half of the run current.
Modify stand still current, delay time and decay via UART, or pre-programmed via internal OTP. Automatic freewheeling and passive motor braking are provided as an option for stand still. Passive braking reduces motor standstill power consumption to zero, while still providing effective dampening and braking!

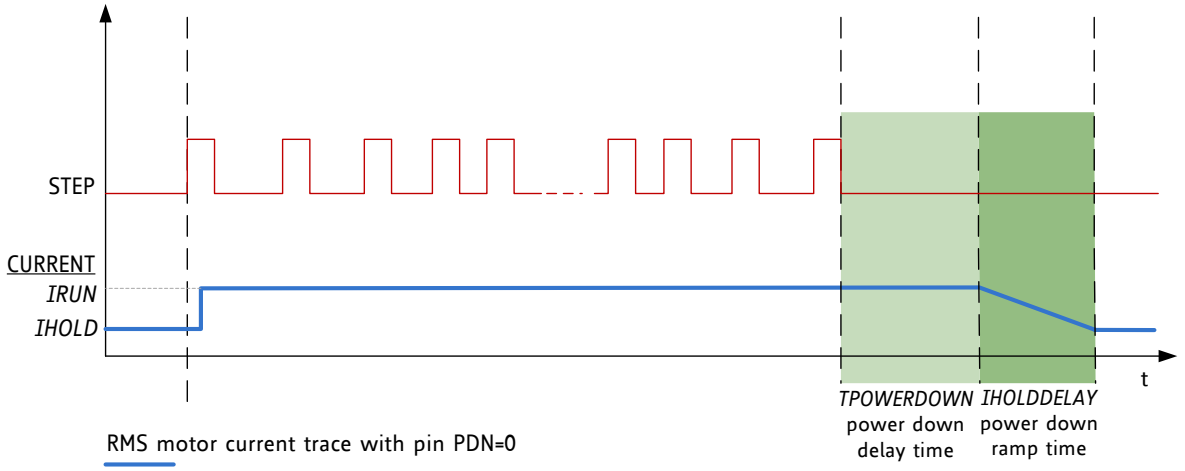


Figure 1.3 Automatic Motor Current Power Down

1.7 Index Output

The index output gives one pulse per electrical rotation, i.e. one pulse per each four fullsteps. It shows the internal sequencer microstep 0 position (*MSTEP* near 0). This is the power on position. In combination with a mechanical home switch, a more precise homing is enabled.

2 Pin Assignments

The TMC22xx family comes in a number of package variants in order to fit different footprints. Please check for availability.

2.1 Package Outline TMC2208

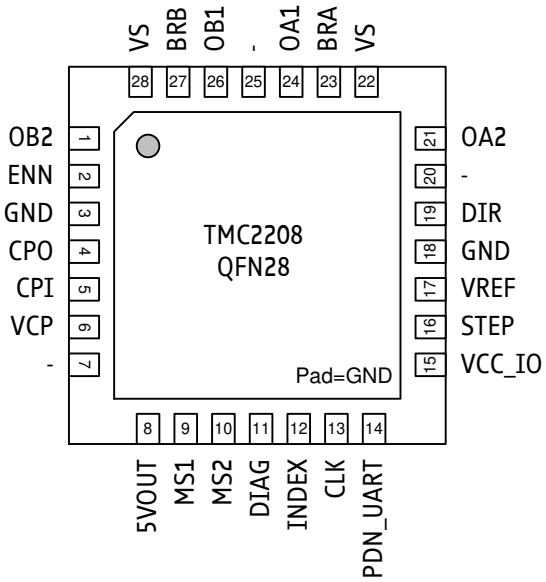


Figure 2.1 TMC2208 Pinning Top View – type: QFN28, 5x5mm², 0.5mm pitch

2.2 Signal Descriptions TMC2208

Pin	Number	Type	Function
OB2	1		Motor coil B output 2
ENN	2	DI	Enable not input. The power stage becomes switched off (all motor outputs floating) when this pin becomes driven to a high level.
GND	3, 18		GND. Connect to GND plane near pin.
CPO	4		Charge pump capacitor output.
CPI	5		Charge pump capacitor input. Tie to CPO using 22nF 50V capacitor.
VCP	6		Charge pump voltage. Tie to VS using 100nF capacitor.
N.C.	7, 20, 25		Unused pin, leave open or connect to GND for compatibility to future versions.
5VOUT	8		Output of internal 5V regulator. Attach 2.2µF to 4.7µF ceramic capacitor to GND near to pin for best performance. Provide the shortest possible loop to the GND pad.
MS1	9	DI (pd)	Microstep resolution configuration (internal pull down resistors)
MS2	10	DI (pd)	MS2, MS1: 00: 1/8, 01: 1/2, 10: 1/4 11: 1/16
DIAG	11	DO	Diagnostic output. Hi level upon driver error. Reset by ENN=high.
INDEX	12	DO	Configurable index output. Provides index pulse.
CLK	13	DI	CLK input. Tie to GND using short wire for internal clock or supply external clock.
PDN_UART	14	DIO	Power down not control input (low = automatic standstill current reduction). Optional UART Input/Output. Power down function can be disabled in UART mode.
VCC_IO	15		3.3V to 5V IO supply voltage for all digital pins.

Pin	Number	Type	Function
STEP	16	DI	STEP input
VREF	17	AI	Analog reference voltage for current scaling or reference current for use of internal sense resistors (optional mode)
DIR	19	DI (pd)	DIR input (internal pull down resistor)
VS	22, 28		Motor supply voltage. Provide filtering capacity near pin with shortest possible loop to GND pad.
OA2	21		Motor coil A output 2
BRA	23		Sense resistor connection for coil A. Place sense resistor to GND near pin. Tie to GND when using internal sense resistor.
OA1	24		Motor coil A output 1
OB1	26		Motor coil B output 1
BRB	27		Sense resistor connection for coil B. Place sense resistor to GND near pin. Tie to GND when using internal sense resistor.
Exposed die pad	-		Connect the exposed die pad to a GND plane. Provide as many as possible vias for heat transfer to GND plane. Serves as GND pin for power drivers and analogue circuitry.

2.3 Package Outline TMC2202

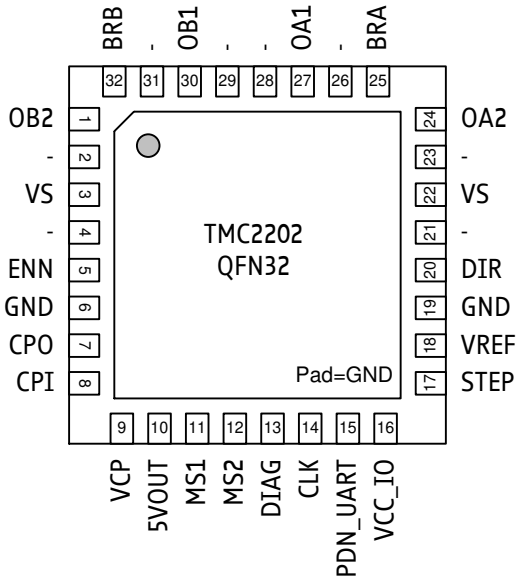


Figure 2.2 TMC2202 Pinning Top View – type: QFN32, 5x5mm², 0.5mm pitch

2.4 Signal Descriptions TMC2202

Pin	Number	Type	Function
OB2	1		Motor coil B output 2
N.C.	2, 4, 21, 23, 26, 28, 29, 31		Unused pin, leave open to provide for higher creeping voltage distances.
VS	3, 22		Motor supply voltage. Provide filtering capacity near pin with shortest possible loop to GND pad.
ENN	5	DI	Enable not input. The power stage becomes switched off (all motor outputs floating) when this pin becomes driven to a high level.

Pin	Number	Type	Function
GND	6, 19		GND. Connect to GND plane near pin.
CPO	7		Charge pump capacitor output.
CPI	8		Charge pump capacitor input. Tie to CPO using 22nF 50V capacitor.
VCP	9		Charge pump voltage. Tie to VS using 100nF capacitor.
5VOUT	10		Output of internal 5V regulator. Attach 2.2µF to 4.7µF ceramic capacitor to GND near to pin for best performance. Provide the shortest possible loop to the GND pad.
MS1	11	DI (pd)	Microstep resolution configuration (internal pull down resistors)
MS2	12	DI (pd)	MS2, MS1: 00: 1/8, 01: 1/2, 10: 1/4 11: 1/16
DIAG	13	DO	Diagnostic output. Hi level upon driver error. Reset by ENN=high.
CLK	14	DI	CLK input. Tie to GND using short wire for internal clock or supply external clock.
PDN_UART	15	DIO	Power down not control input (low = automatic standstill current reduction). Optional UART Input/Output. Power down function can be disabled in UART mode.
VCC_IO	16		3.3V to 5V IO supply voltage for all digital pins.
STEP	17	DI	STEP input
VREF	18	AI	Analog reference voltage for current scaling or reference current for use of internal sense resistors (optional mode)
DIR	20	DI (pd)	DIR input (internal pull down resistor)
OA2	24		Motor coil A output 2
BRA	25		Sense resistor connection for coil A. Place sense resistor to GND near pin. Tie to GND when using internal sense resistor.
OA1	27		Motor coil A output 1
OB1	30		Motor coil B output 1
BRB	32		Sense resistor connection for coil B. Place sense resistor to GND near pin. Tie to GND when using internal sense resistor.
Exposed die pad	-		Connect the exposed die pad to a GND plane. Provide as many as possible vias for heat transfer to GND plane. Serves as GND pin for power drivers and analogue circuitry.

2.5 Package Outline TMC2224

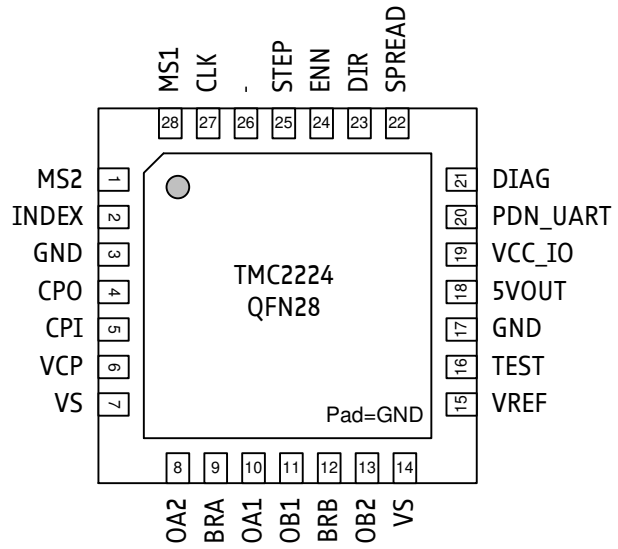


Figure 2.3 TMC2224 Pinning Top View – type: QFN28, 5x5mm², 0.5mm pitch

2.6 Signal Descriptions TMC2224

Pin	Number	Type	Function
MS1	28	DI (pd)	Microstep resolution configuration (internal pull down resistors) MS2, MS1: 00: 1/4, 01: 1/8, 10: 1/16, 11: 1/32
MS2	1	DI (pd)	
INDEX	2	DO	Configurable index output. Provides index pulse.
GND	3, 17		GND. Connect to GND plane near pin.
CPO	4		Charge pump capacitor output.
CPI	5		Charge pump capacitor input. Tie to CPO using 22nF 50V capacitor.
VCP	6		Charge pump voltage. Tie to VS using 100nF capacitor.
VS	7, 14		Motor supply voltage. Provide filtering capacity near pin with shortest possible loop to GND pad.
OA2	8		Motor coil A output 2
BRA	9		Sense resistor connection for coil A. Place sense resistor to GND near pin. Tie to GND when using internal sense resistor.
OA1	10		Motor coil A output 1
OB1	11		Motor coil B output 1
BRB	12		Sense resistor connection for coil B. Place sense resistor to GND near pin. Tie to GND when using internal sense resistor.
OB2	13		Motor coil B output 2
VREF	15	AI	Analog reference voltage for current scaling or reference current for use of internal sense resistors (optional mode)
TEST	16		Connect to GND. May alternatively be left open or connected to VREF.
5VOUT	18		Output of internal 5V regulator. Attach 2.2µF to 4.7µF ceramic capacitor to GND near to pin for best performance. Provide the shortest possible loop to the GND pad.
VCC_IO	19		3.3V to 5V IO supply voltage for all digital pins.
PDN_UART	20	DIO (pd)	Power down not control input (low = automatic standstill current reduction). (internal pull down resistor) Optional UART Input/Output. Power down function can be disabled in UART mode.
DIAG	21	DO	Diagnostic output. Hi level upon driver error. Reset by ENN=high.
SPREAD	22	DI (pd)	Chopper mode selection: Low=stealthChop, High=spreadCycle
DIR	23	DI (pd)	DIR input (internal pull down resistor)
ENN	24	DI	Enable not input. The power stage becomes switched off (all motor outputs floating) when this pin becomes driven to a high level.
STEP	25	DI (pd)	STEP input (internal pull down resistor)
N.C.	26		Unused pin, leave open or connect to GND for compatibility to future versions.
CLK	27	DI	CLK input. Tie to GND using short wire for internal clock or supply external clock.
Exposed die pad	-		Connect the exposed die pad to a GND plane. Provide as many as possible vias for heat transfer to GND plane. Serves as GND pin for power drivers and analogue circuitry.

2.7 Package Outline TMC2225

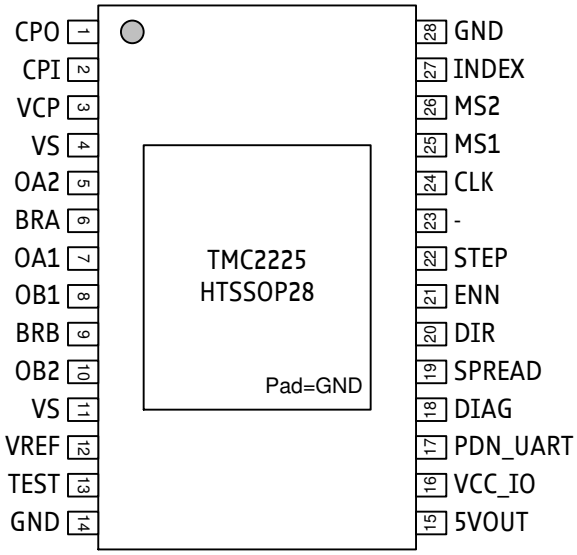


Figure 2.4 TMC2225 Pinning Top View – type: HTSSOP28, 9.7x6.4mm² over pins, 0.65mm pitch

2.8 Signal Descriptions TMC2225

Pin	Number	Type	Function
CPO	1		Charge pump capacitor output.
CPI	2		Charge pump capacitor input. Tie to CPO using 22nF 50V capacitor.
VCP	3		Charge pump voltage. Tie to VS using 100nF capacitor.
VS	4, 11		Motor supply voltage. Provide filtering capacity near pin with shortest possible loop to GND pad.
OA2	5		Motor coil A output 2
BRA	6		Sense resistor connection for coil A. Place sense resistor to GND near pin. Tie to GND when using internal sense resistor.
OA1	7		Motor coil A output 1
OB1	8		Motor coil B output 1
BRB	9		Sense resistor connection for coil B. Place sense resistor to GND near pin. Tie to GND when using internal sense resistor.
OB2	10		Motor coil B output 2
VREF	12	AI	Analog reference voltage for current scaling or reference current for use of internal sense resistors (optional mode)
TEST	13		Connect to GND. May alternatively be left open or connected to VREF.
GND	14, 28		GND. Connect to GND plane near pin.
5VOUT	15		Output of internal 5V regulator. Attach 2.2µF to 4.7µF ceramic capacitor to GND near to pin for best performance. Provide the shortest possible loop to the GND pad.
VCC_IO	16		3.3V to 5V IO supply voltage for all digital pins.
PDN_UART	17	DIO (pd)	Power down not control input (low = automatic standstill current reduction). (internal pull down resistor) Optional UART Input/Output. Power down function can be disabled in UART mode.
DIAG	18	DO	Diagnostic output. Hi level upon driver error. Reset by ENN=high.
SPREAD	19	DI (pd)	Chopper mode selection: Low=stealthChop, High=spreadCycle
DIR	20	DI (pd)	DIR input (internal pull down resistor)
ENN	21	DI	Enable not input. The power stage becomes switched off (all motor outputs floating) when this pin becomes driven to a high level.

Pin	Number	Type	Function
STEP	22	DI (pd)	STEP input (internal pull down resistor)
N.C.	23		Unused pin, leave open or connect to GND for compatibility to future versions.
CLK	24	DI	CLK input. Tie to GND using short wire for internal clock or supply external clock.
MS1	25	DI (pd)	Microstep resolution configuration (internal pull down resistors)
MS2	26	DI (pd)	MS2, MS1: 00: 1/4, 01: 1/8, 10: 1/16, 11: 1/32
INDEX	27	DO	Configurable index output. Provides index pulse.
Exposed die pad	-		Connect the exposed die pad to a GND plane. Provide as many as possible vias for heat transfer to GND plane. Serves as GND pin for power drivers and analogue circuitry.

2.9 Package Outline TMC2220

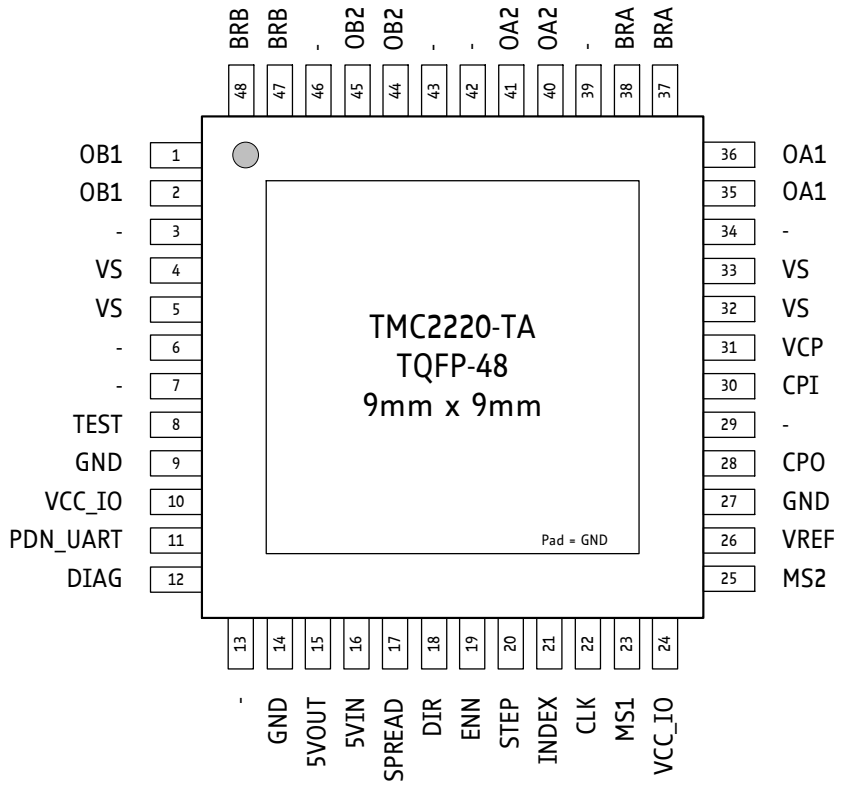


Figure 2.5 TMC2220 Pinning Top View – type: TQFP-EP 48, 9x9mm² over pins, 0.5mm pitch

2.10 Signal Descriptions TMC2220

Pin	Number	Type	Function
OB1	1, 2		Motor coil B output 1
VS	4, 5, 32, 33		Motor supply voltage. Provide filtering capacity near pin with shortest possible loop to GND pad.
TEST	8		Connect to GND. May alternatively be left open.
GND	9, 14, 27		GND. Connect to GND plane near pin.
VCC_IO	10, 24		3.3V to 5V IO supply voltage for all digital pins.

Pin	Number	Type	Function
PDN_UART	11	DIO (pd)	Power down not control input (low = automatic standstill current reduction). (internal pull down resistor) Optional UART Input/Output. Power down function can be disabled in UART mode.
5VOUT	15		Output of internal 5V regulator. Attach 2.2µF to 4.7µF ceramic capacitor to GND near to pin for best performance. Provide the shortest possible loop to the GND pad.
5VIN	16		Input of 5V supply. Directly connect to 5VOUT terminal.
DIAG	12	DO	Diagnostic output. Hi level upon driver error. Reset by ENN=high.
SPREAD	17	DI (pd)	Chopper mode selection: Low=stealthChop, High=spreadCycle
DIR	18	DI (pd)	DIR input (internal pull down resistor)
ENN	19	DI	Enable not input. The power stage becomes switched off (all motor outputs floating) when this pin becomes driven to a high level.
STEP	20	DI (pd)	STEP input (internal pull down resistor)
INDEX	21	DO	Configurable index output. Provides index pulse.
CLK	22	DI	CLK input. Tie to GND using short wire for internal clock or supply external clock.
MS1	23	DI (pd)	Microstep resolution configuration (internal pull down resistors)
MS2	25	DI (pd)	MS2, MS1: 00: 1/4, 01: 1/8, 10: 1/16, 11: 1/32
VREF	26	AI	Analog reference voltage for current scaling or reference current for use of internal sense resistors (optional mode)
CPO	28		Charge pump capacitor output.
CPI	30		Charge pump capacitor input. Tie to CPO using 22nF 50V capacitor.
VCP	31		Charge pump voltage. Tie to VS using 100nF capacitor.
OA1	35, 36		Motor coil A output 1
BRA	37, 38		Sense resistor connection for coil A. Place sense resistor to GND near pin. Tie to GND when using internal sense resistor.
OA2	40, 41		Motor coil A output 2
OB2	44, 45		Motor coil B output 2
BRB	47, 48		Sense resistor connection for coil B. Place sense resistor to GND near pin. Tie to GND when using internal sense resistor.
N.C.			Unused pin, leave open or connect to GND for compatibility to future versions.
Exposed die pad	-		Connect the exposed die pad to a GND plane. Provide as many as possible vias for heat transfer to GND plane. Serves as GND pin for power drivers and analogue circuitry.

3 Sample Circuits

The sample circuits show the connection of external components in different operation and supply modes. The connection of the bus interface and further digital signals is left out for clarity.

3.1 Standard Application Circuit

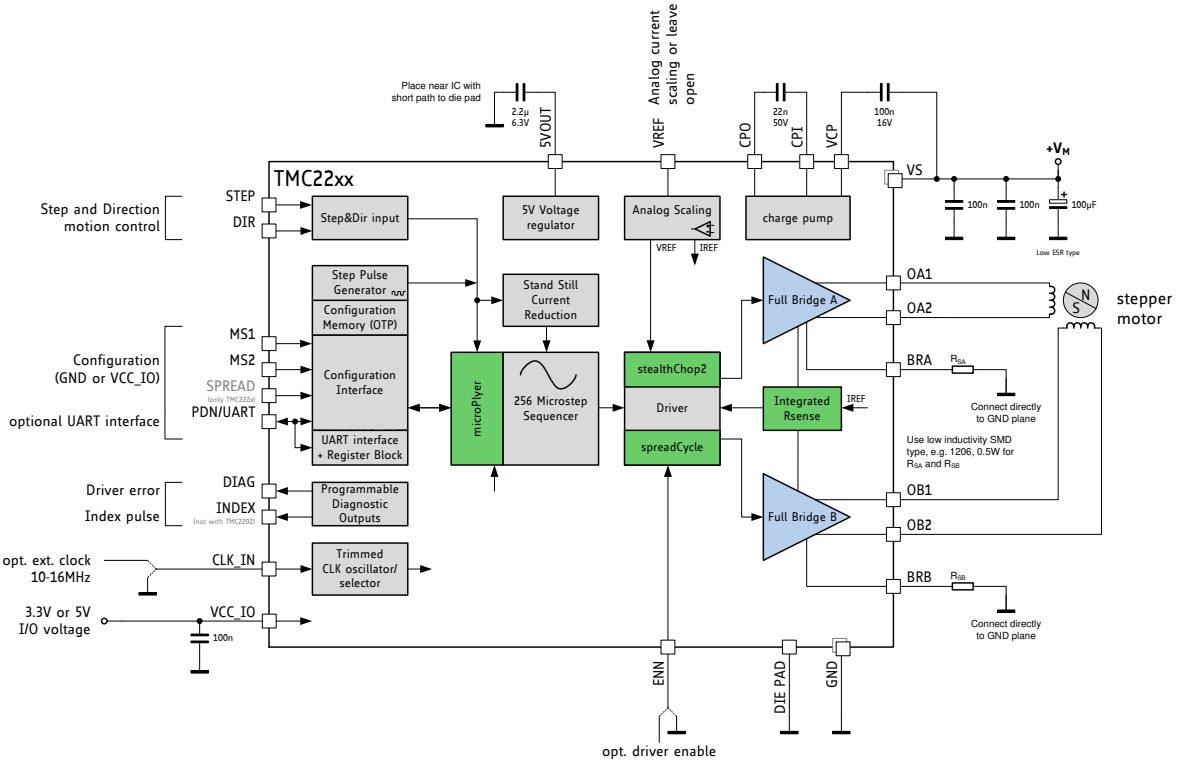


Figure 3.1 Standard application circuit

The standard application circuit uses a minimum set of additional components. Two sense resistors set the motor coil current. See chapter 8 to choose the right sense resistors. Use low ESR capacitors for filtering the power supply. The capacitors need to cope with the current ripple cause by chopper operation. A minimum capacity of 100µF near the driver is recommended for best performance. Current ripple in the supply capacitors also depends on the power supply internal resistance and cable length. VCC_IO can be supplied from 5VOUT, or from an external source, e.g. a 3.3V regulator.

Basic layout hints
Place sense resistors and all filter capacitors as close as possible to the related IC pins. Use a solid common GND for all GND connections, also for sense resistor GND. Connect 5VOUT filtering capacitor directly to 5VOUT and the die pad. See layout hints for more details. Low ESR electrolytic capacitors are recommended for VS filtering.

3.2 Internal RDSon Sensing

For cost critical or space limited applications, sense resistors can be omitted. For internal current sensing, a reference current set by a tiny external resistor programs the output current. For calculation of the reference resistor, refer chapter 9.1.

Attention
Be sure to switch the IC to RDSon mode, before enabling drivers: Set *otp_internalRsense* = 1.

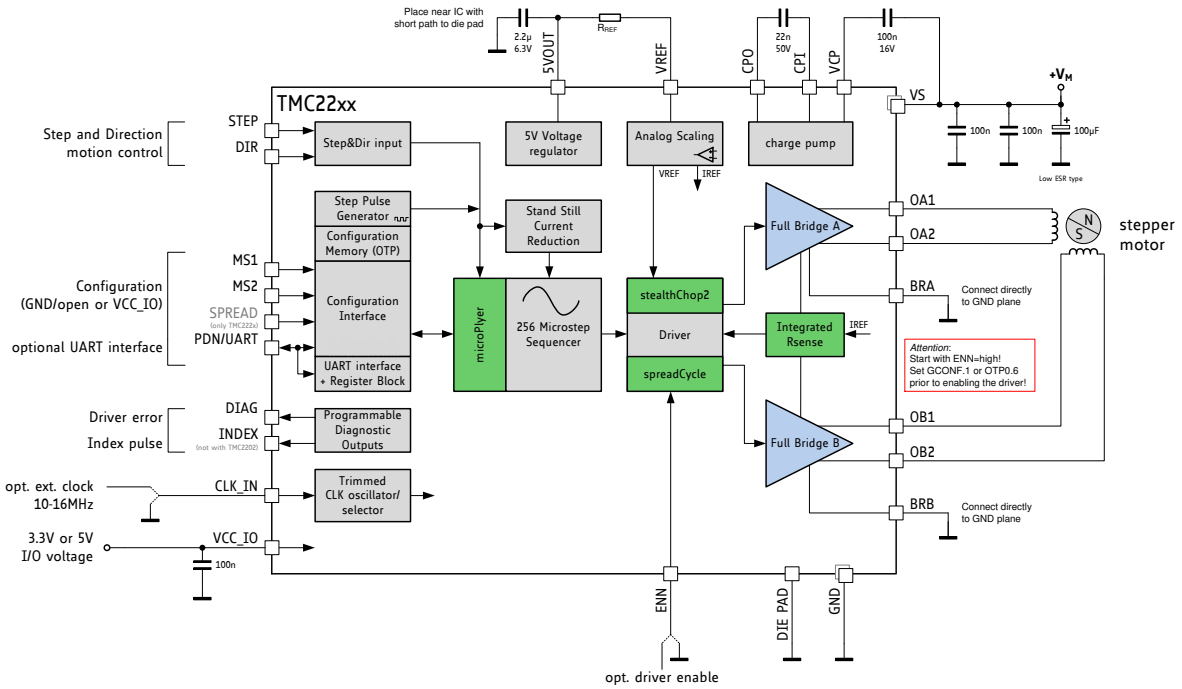


Figure 3.2 Application circuit using RDSon based sensing

3.3 5V Only Supply

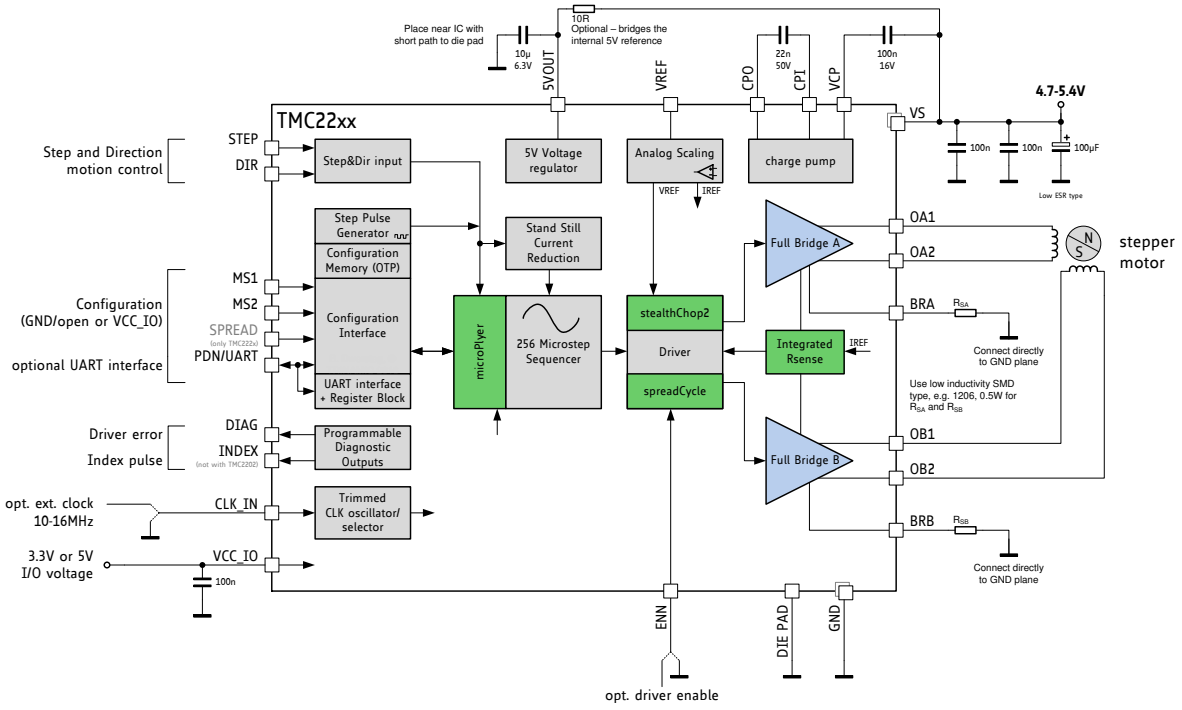


Figure 3.3 5V only operation

While the standard application circuit is limited to roughly 5.2V lower supply voltage, a 5V only application lets the IC run from a 5V +/-5% supply. In this application, linear regulator drop must be

minimized. Therefore, the internal 5V regulator is filtered with a higher capacitance. An optional resistor bridges the internal 5V regulator by connecting 5VOUT to the external power supply. This RC filter keeps chopper ripple away from 5VOUT. With this resistor, the external supply is the reference for the absolute motor current and must not exceed 5.5V.

3.4 Configuration Pins

The TMC22xx family members provide three or four configuration pins depending on the package option. These pins allow quick configuration for standalone operation. Several additional options can be set by OTP programming. In UART mode, the configuration pins can be disabled in order to set a different configuration via registers.

PDN_UART: Configuration of Standstill Power Down	
PDN_UART	**Current Setting**
GND	Enable automatic power down in standstill periods
VCC_IO	Disable
UART interface	When using the UART interface, the configuration pin should be disabled via *GCONF.pdn_disable* = 1. Program *IHOLD* as desired for standstill periods.

Options for TMC220x devices, only:

MS1/MS2: Configuration of Microstep Resolution for Step Input (TMC220x)		
MS2	**MS1**	**Microstep Setting**
GND	GND	8 microsteps
GND	VCC_IO	2 microsteps (half step)
VCC_IO	GND	4 microsteps (quarter step)
VCC_IO	VCC_IO	16 microsteps

Options for TMC222x devices, only:

SPREAD (only with TMC222x): Selection of Chopper Mode	
SPREAD	**Chopper Setting**
GND or Pin open / not available	stealthChop is selected. Automatic switching to spreadCycle in dependence of the step frequency can be programmed via OTP.
VCC_IO	spreadCycle operation.

MS1/MS2: Configuration of Microstep Resolution for Step Input (TMC222x)		
MS2	**MS1**	**Microstep Setting**
GND	GND	4 microsteps (quarter step)
GND	VCC_IO	8 microsteps
VCC_IO	GND	16 microsteps
VCC_IO	VCC_IO	32 microsteps

3.5 High Motor Current

When operating at a high motor current, the driver power dissipation due to MOSFET switch on-resistance significantly heats up the driver. This power dissipation will significantly heat up the PCB cooling infrastructure, if operated at an increased duty cycle. This in turn leads to a further increase of driver temperature. An increase of temperature by about 100°C increases MOSFET resistance by roughly 50%. This is a typical behavior of MOSFET switches. Therefore, under high duty cycle, high load conditions, thermal characteristics have to be carefully taken into account, especially when increased environment temperatures are to be supported. Refer the thermal characteristics and the layout hints for more information. As a thumb rule, thermal properties of the PCB design become

critical for the tiny QFN 5mm x 5mm package at or above 1A RMS motor current for increased periods of time. Keep in mind that resistive power dissipation raises with the square of the motor current. On the other hand, this means that a small reduction of motor current significantly saves heat dissipation and energy.

Pay special attention to good thermal properties of your PCB layout, when going for 1A RMS current or more.

An effect which might be perceived at medium motor velocities and motor sine wave peak currents above roughly 1.4A peak is a slight sine distortion of the current wave when using spreadCycle. It results from an increasing negative impact of parasitic internal diode conduction, which in turn negatively influences the duration of the fast decay cycle of the spreadCycle chopper. This is, because the current measurement does not see the full coil current during this phase of the sine wave, because an increasing part of the current flows directly from the power MOSFETs' drain to GND and does not flow through the sense resistor. This effect with most motors does not negatively influence the smoothness of operation, as it does not impact the critical current zero transition. The effect does not occur with stealthChop.

3.6 Driver Protection and EME Circuitry

Some applications have to cope with ESD events caused by motor operation or external influence. Despite ESD circuitry within the driver chips, ESD events occurring during operation can cause a reset or even a destruction of the motor driver, depending on their energy. Especially plastic housings and belt drive systems tend to cause ESD events of several kV. It is best practice to avoid ESD events by attaching all conductive parts, especially the motors themselves to PCB ground, or to apply electrically conductive plastic parts. In addition, the driver can be protected up to a certain degree against ESD events or live plugging / pulling the motor, which also causes high voltages and high currents into the motor connector terminals. A simple scheme uses capacitors at the driver outputs to reduce the dV/dt caused by ESD events. Larger capacitors will bring more benefit concerning ESD suppression, but cause additional current flow in each chopper cycle, and thus increase driver power dissipation, especially at high supply voltages. The values shown are example values – they may be varied between 100pF and 1nF. The capacitors also dampen high frequency noise injected from digital parts of the application PCB circuitry and thus reduce electromagnetic emission. A more elaborate scheme uses LC filters to de-couple the driver outputs from the motor connector. Varistors in between of the coil terminals eliminate coil overvoltage caused by live plugging. Optionally protect all outputs by a varistor to GND against ESD voltage.

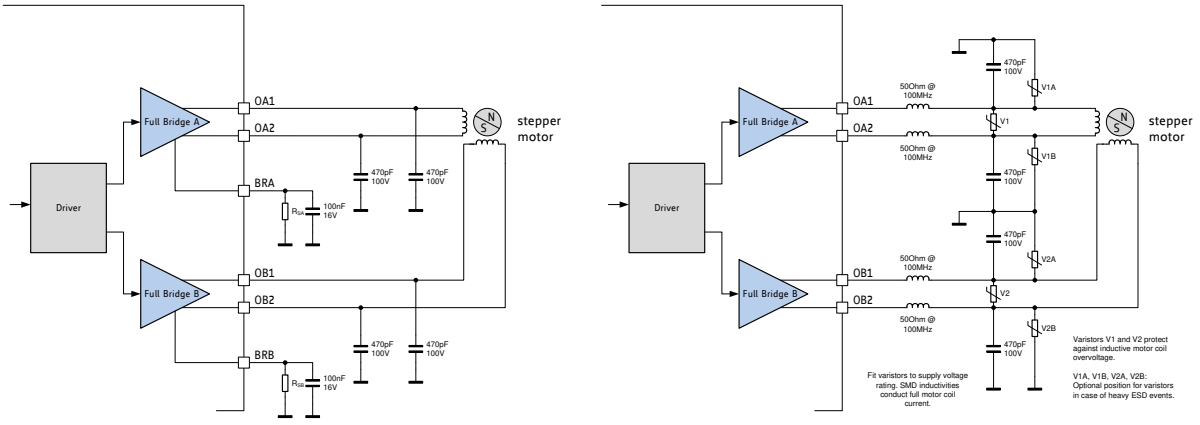


Figure 3.4 Simple ESD enhancement and more elaborate motor output protection

4 UART Single Wire Interface

The UART single wire interface allows control of the TMC22xx with any microcontroller UART. It shares transmit and receive line like an RS485 based interface. Data transmission is secured using a cyclic redundancy check, so that increased interface distances (e.g. over cables between two PCBs) can be bridged without danger of wrong or missed commands even in the event of electro-magnetic disturbance. The automatic baud rate detection makes this interface easy to use.

4.1 Datagram Structure

4.1.1 Write Access

UART WRITE ACCESS DATAGRAM STRUCTURE																			
each byte is LSB...MSB, highest byte transmitted first																			
0 ... 63																			
sync + reserved								**8 bit slave address**			**RW + 7 bit register addr.**			**32 bit data**			**CRC**		
0...7								8...15			16...23			24...55			56...63		
1	0	1	0	Reserved (don't cares but included in CRC)				*SLAVEADDR*=0			register address		1	data bytes 3, 2, 1, 0 (high to low byte)			CRC		
0	1	2	3	4	5	6	7	8	...	15	16	...	23	24	...	55	56	...	63

A sync nibble precedes each transmission to and from the TMC22xx and is embedded into the first transmitted byte, followed by an addressing byte (0 for TMC22xx). Each transmission allows a synchronization of the internal baud rate divider to the master clock. The actual baud rate is adapted and variations of the internal clock frequency are compensated. Thus, the baud rate can be freely chosen within the valid range. Each transmitted byte starts with a start bit (logic 0, low level on SWIOP) and ends with a stop bit (logic 1, high level on SWIOP). The bit time is calculated by measuring the time from the beginning of start bit (1 to 0 transition) to the end of the sync frame (1 to 0 transition from bit 2 to bit 3). All data is transmitted bytewise. The 32 bit data words are transmitted with the highest byte first.

A minimum baud rate of 9000 baud is permissible, assuming 20 MHz clock (worst case for low baud rate). Maximum baud rate is f_{CLK}/16 due to the required stability of the baud clock.

The slave address *SLAVEADDR* is always 0 for the TMC22xx.

The communication becomes reset if a pause time of longer than 63 bit times between the start bits of two successive bytes occurs. This timing is based on the last correctly received datagram. In this case, the transmission needs to be restarted after a failure recovery time of minimum 12 bit times of bus idle time. This scheme allows the master to reset communication in case of transmission errors. Any pulse on an idle data line below 16 clock cycles will be treated as a glitch and leads to a timeout of 12 bit times, for which the data line must be idle. Other errors like wrong CRC are also treated the same way. This allows a safe re-synchronization of the transmission after any error conditions. Remark, that due to this mechanism an abrupt reduction of the baud rate to less than 15 percent of the previous value is not possible.

Each accepted write datagram becomes acknowledged by the receiver by incrementing an internal cyclic datagram counter (8 bit). Reading out the datagram counter allows the master to check the success of an initialization sequence or single write accesses. Read accesses do not modify the counter.

The UART line must be logic high during idle state. Therefore, the power down function cannot be assigned by the pin PDN_UART in between of transmissions. In an application using the UART interface, set the desired power down function by register access and set *pdn_disable* in GCONF to disable the pin function.

4.1.2 Read Access

UART READ ACCESS REQUEST DATAGRAM STRUCTURE																							
each byte is LSB...MSB, highest byte transmitted first																							
sync + reserved								**8 bit slave address**				**RW + 7 bit register address**								**CRC**			
0...7								8...15				16...23								24...31			
1	0	1	0	Reserved (don't cares but included in CRC)				*SLAVEADDR*=0				register address							0	CRC			
0	1	2	3	4	5	6	7	8	...		15	16	...						23	24	...		31

The read access request datagram structure is identical to the write access datagram structure, but uses a lower number of user bits. Its function is the addressing of the slave and the transmission of the desired register address for the read access. The TMC22xx responds with the same baud rate as the master uses for the read request.

In order to ensure a clean bus transition from the master to the slave, the TMC22xx does not immediately send the reply to a read access, but it uses a programmable delay time after which the first reply byte becomes sent following a read request. This delay time can be set in multiples of eight bit times using *SENDDELAY* time setting (default=8 bit times) according to the needs of the master.

UART READ ACCESS REPLY DATAGRAM STRUCTURE																							
each byte is LSB...MSB, highest byte transmitted first																							
0 63																							
sync + reserved								**8 bit master address**				**RW + 7 bit register addr.**				**32 bit data**				**CRC**			
0...7								8...15				16...23				24...55				56...63			
1	0	1	0	reserved (0)				0xFF				register address			0	data bytes 3, 2, 1, 0 (high to low byte)				CRC			
0	1	2	3	4	5	6	7	8	...		15	16	...		23	24	...		55	56	...		63

The read response is sent to the master using address code %11111111. The transmitter becomes switched inactive four bit times after the last bit is sent.

Address %11111111 is reserved for read access replies going to the master.

4.2 CRC Calculation

An 8 bit CRC polynomial is used for checking both read and write access. It allows detection of up to eight single bit errors. The CRC8-ATM polynomial with an initial value of zero is applied LSB to MSB, including the sync- and addressing byte. The sync nibble is assumed to always be correct. The TMC22xx responds only to correctly transmitted datagrams containing its own slave address. It increases its datagram counter for each correctly received write access datagram.

$$CRC = x^8 + x^2 + x^1 + x^0$$

SERIAL CALCULATION EXAMPLE

```
CRC = (CRC << 1) OR (CRC.7 XOR CRC.1 XOR CRC.0 XOR [new incoming bit])
```

C-CODE EXAMPLE FOR CRC CALCULATION

```
void swuart_calcCRC(UCHAR* datagram, UCHAR datagramLength)
{
  int i,j;
  UCHAR* crc = datagram + (datagramLength-1); // CRC located in last byte of message
  UCHAR currentByte;

  *crc = 0;
  for (i=0; i<(datagramLength-1); i++) {      // Execute for all bytes of a message
    currentByte = datagram[i];                // Retrieve a byte to be sent from Array
    for (j=0; j<8; j++) {
      if ((*crc >> 7) ^ (currentByte&0x01))   // update CRC based result of XOR operation
      {
        *crc = (*crc << 1) ^ 0x07;
      }
      else
      {
        *crc = (*crc << 1);
      }
      currentByte = currentByte >> 1;
    } // for CRC bit
  } // for message byte
}
```

4.3 UART Signals

The UART interface on the TMC22xx uses a single bi-direction pin:

UART INTERFACE SIGNAL	
PDN_UART	Non-inverted data input and output. I/O with Schmitt Trigger and VCC_IO level.

The IC checks PDN_UART for correctly received datagrams with its own address continuously. It adapts to the baud rate based on the sync nibble, as described before. In case of a read access, it switches on its output drivers and sends its response using the same baud rate. The output becomes switched off four bit times after transfer of the last stop bit.

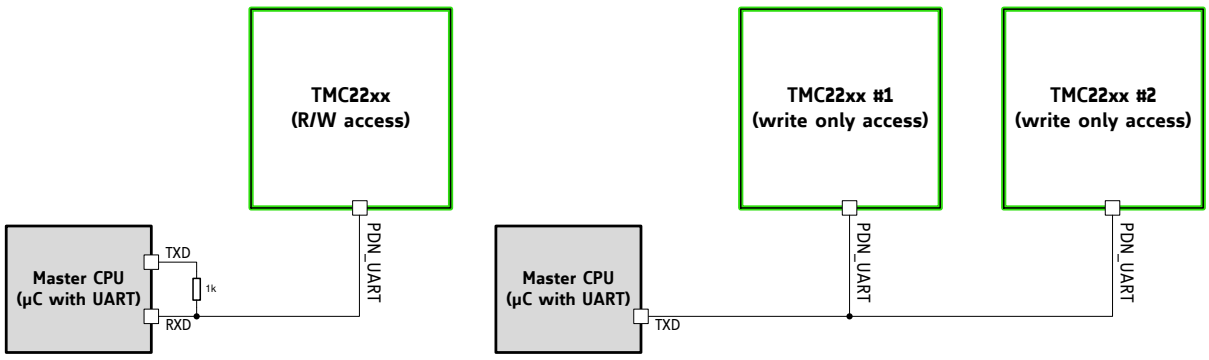


Figure 4.1 Attaching the TMC22xx to a microcontroller UART

4.4 Addressing Multiple Slaves

WRITE ONLY ACCESS

If read access is not used, and all slaves are to be programmed with the same initialization values, no addressing is required. All slaves can be programmed in parallel like a single device (Figure 4.1.).

ADDRESSING MULTIPLE SLAVES

As the TMC22xx uses a fixed UART address, in principle only one IC can be accessed per UART interface channel. Adding analog switches allows separated access to individual ICs. This scheme is similar to an SPI bus with individual slave select lines (Figure 4.2).

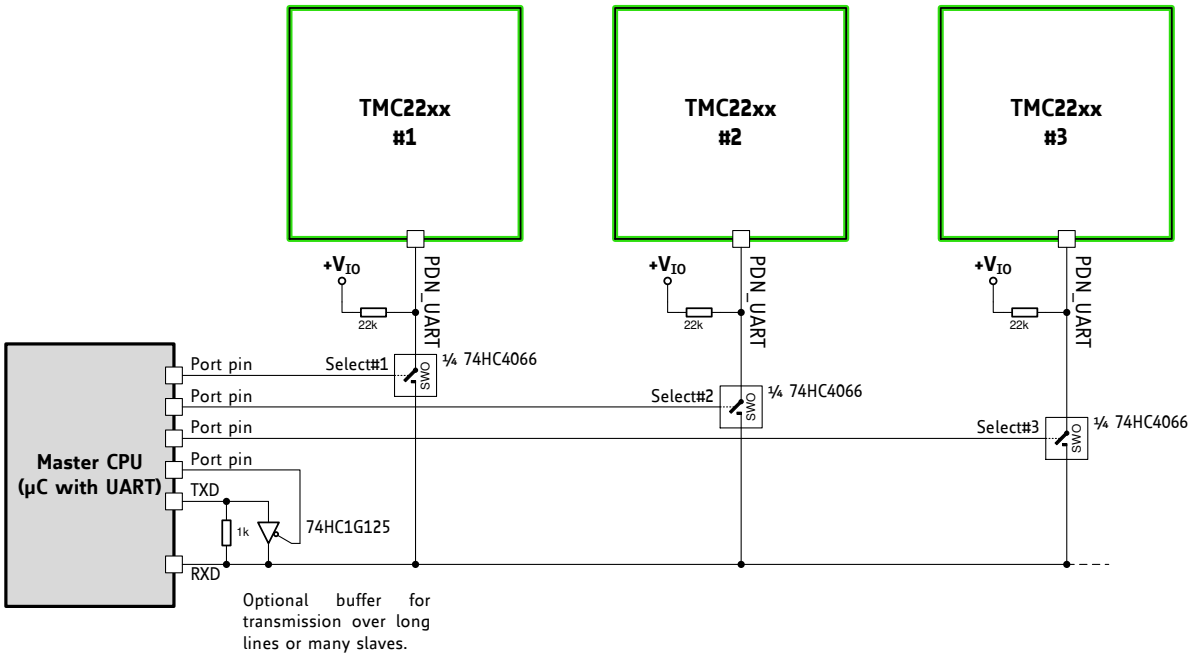


Figure 4.2 Addressing multiple TMC22xx via single wire interface using analog switches

PROCEED AS FOLLOWS TO CONTROL MULTIPLE SLAVES:

- Set the UART to 8 bits, no parity. Select a baud rate safely within the valid range. At 250kBaud, a write access transmission requires 320µs (=8 Bytes * (8+2) bits * 4µs).
- Before starting an access, activate the select pin going to the analog switch by setting it high. All other slaves select lines shall be off, unless a broadcast is desired.
- When using the optional buffer, set TMC22xx transmission send delay to an appropriate value allowing the µC to switch off the buffer before receiving reply data.
- To start a transmission, activate the TXD line buffer by setting the control pin low.
- When sending a read access request, switch off the buffer after transmission of the last stop bit is finished.
- Take into account, that all transmitted data also is received by the RXD input.

5 Register Map

This chapter gives an overview of the complete register set. Some of the registers bundling a number of single bits are detailed in extra tables. The functional practical application of the settings is detailed in dedicated chapters.

Note
- *Reset default*: All registers become reset to 0 upon power up, unless otherwise noted.
- Add 0x80 to the address **Addr** for write accesses!

NOTATION OF HEXADECIMAL AND BINARY NUMBERS	
0x	precedes a hexadecimal number, e.g. 0x04
%	precedes a multi-bit binary number, e.g. %100

NOTATION OF R/W FIELD	
R	Read only
W	Write only
R/W	Read- and writable register
R+C	Clear upon read

OVERVIEW REGISTER MAPPING

REGISTER	DESCRIPTION
General Configuration Registers	These registers contain - global configuration - global status flags - OTP read access and programming - interface configuration
Velocity Dependent Driver Feature Control Register Set	This register set offers registers for - driver current control, stand still reduction - setting thresholds for different chopper modes - internal pulse generator control
Chopper Register Set	This register set offers registers for - optimization of stealthChop2 and spreadCycle and read out of internal values - passive braking and freewheeling options - driver diagnostics - driver enable / disable

5.1 General Registers

GENERAL CONFIGURATION REGISTERS (0X00…0X0F)					
R/W	**Addr**	**n**	***Register***	**Description */ bit names***	
RW	0x00	10	*GCONF*	**Bit**	***GCONF* – Global configuration flags**
				0	*I_scale_analog* (*Reset default=1*) 0: Use internal reference derived from 5VOUT 1: Use voltage supplied to VREF as current reference
				1	*internal_Rsense* (*Reset default: OTP*) 0: Operation with external sense resistors 1: Internal sense resistors. Use current supplied into VREF as reference for internal sense resistor. VREF pin internally is driven to GND in this mode.
				2	*en_spreadCycle* (*Reset default: OTP*) 0: stealthChop PWM mode enabled (depending on velocity thresholds). Initially switch from off to on state while in stand still, only. 1: spreadCycle mode enabled A high level on the pin SPREAD (TMC222x, only) inverts this flag to switch between both chopper modes.
				3	*shaft* 1: Inverse motor direction
				4	*index_otpw* 0: INDEX shows the first microstep position of sequencer 1: INDEX pin outputs overtemperature prewarning flag (*otpw*) instead
				5	*index_step* 0: INDEX output as selected by *index_otpw* 1: INDEX output shows step pulses from internal pulse generator (toggle upon each step)
				6	*pdn_disable* 0: PDN_UART controls standstill current reduction 1: PDN_UART input function disabled. Set this bit, when using the UART interface!
				7	*mstep_reg_select* 0: Microstep resolution selected by pins MS1, MS2 1: Microstep resolution selected by MSTEP register
				8	*multistep_filt* (*Reset default=1*) 0: No filtering of STEP pulses 1: Software pulse generator optimization enabled when fullstep frequency > 750Hz (roughly). TSTEP shows filtered step time values when active.
				9	*test_mode* 0: Normal operation 1: Enable analog test output on pin ENN (pull down resistor off), ENN treated as enabled. *IHOLD*[1..0] selects the function of DCO: 0…2: T120, DAC, VDDH *Attention: Not for user, set to 0 for normal operation!*

GENERAL CONFIGURATION REGISTERS (0X00…0X0F)					
R/W	**Addr**	**n**	***Register***	**Description */ bit names***	
R+ WC	0x01	3	*GSTAT*	**Bit**	***GSTAT* – Global status flags** (Re-Write with '1' bit to clear respective flags)
				0	*reset* 1: Indicates that the IC has been reset since the last read access to *GSTAT*. All registers have been cleared to reset values.
				1	*drv_err* 1: Indicates, that the driver has been shut down due to overtemperature or short circuit detection since the last read access. Read DRV_STATUS for details. The flag can only be cleared when all error conditions are cleared.
				2	*uv_cp* 1: Indicates an undervoltage on the charge pump. The driver is disabled in this case. This flag is not latched and thus does not need to be cleared.
R	0x02	8	*IFCNT*		Interface transmission counter. This register becomes incremented with each successful UART interface write access. Read out to check the serial transmission for lost data. Read accesses do not change the content. The counter wraps around from 255 to 0.
W	0x03	4	*SLAVECONF*	**Bit**	***SLAVECONF***
				11..8	SENDDELAY for read access (time until reply is sent): 0, 1: 8 bit times 2, 3: 3*8 bit times 4, 5: 5*8 bit times 6, 7: 7*8 bit times 8, 9: 9*8 bit times 10, 11: 11*8 bit times 12, 13: 13*8 bit times 14, 15: 15*8 bit times
W	0x04	16	*OTP_PROG*	**Bit**	***OTP_PROGRAM* – OTP programming** Write access programs OTP memory (one bit at a time), Read access refreshes read data from OTP after a write
				2..0	*OTPBIT* Selection of OTP bit to be programmed to the selected byte location (n=0..7: programs bit n to a logic 1)
				5..4	*OTPBYTE* Selection of OTP programming location (0, 1 or 2)
				15..8	*OTPMAGIC* Set to *0xbd* to enable programming. A programming time of minimum 10ms per bit is recommended (check by reading *OTP_READ*).
R	0x05	24	*OTP_READ*	**Bit**	***OTP_READ*** (Access to OTP memory result and update) *See separate table!*
				7..0	*OTP0* byte 0 read data
				15..8	*OTP1* byte 1 read data
				23..16	*OTP2* byte 2 read data
R	0x06	10 + 8	*IOIN*	**Bit**	***INPUT*** (Reads the state of all input pins available)
				0	ENN (TMC220x)
				1	PDN_UART (TMC222x)
				2	MS1 (TMC220x), SPREAD (TMC222x)
				3	MS2 (TMC220x), DIR (TMC222x)