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We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

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# TMC262 DATASHEET

*Universal, cost-effective stepper driver for two-phase bipolar motors with state-of-the-art features. External MOSFETs fit different motor sizes. With Step/Dir Interface and SPI.*

coolStep™
stallGuard2™

## APPLICATIONS

Textile, Sewing Machines
Factory Automation
Lab Automation
Liquid Handling
Medical
Office Automation
Printer and Scanner
CCTV, Security
ATM, Cash recycler
POS
Pumps and Valves
Heliostat Controller
CNC Machines

## FEATURES AND BENEFITS

**High Current** up to 10A Motor current using external (N&P) MOSFETs.

**Highest Voltage** up to 60V DC operating voltage

**Highest Resolution** up to 256 microsteps per full step

**Smallest Size** 5x5mm QFN32 package

**Low Power Dissipation** synchronous rectification

**EMI-optimized** slope & current controlled gate drivers

**Protection & Diagnostics** overcurrent, short to GND, overtemperature & undervoltage

**stallGuard2™** high precision sensorless motor load detection

**coolStep™** load dependent current control for energy savings up to 75%

**microPlyer™** microstep interpolation for increased smoothness with coarse step inputs.

**spreadCycle™** high-precision chopper for best current sine wave form and zero crossing

## DESCRIPTION

The TMC262 driver for two-phase stepper motors offers an industry-leading feature set, including high-resolution micro-stepping, sensorless mechanical load measurement, load-adaptive power optimization, and low-resonance chopper operation. Standard SPI™ and STEP/DIR interfaces simplify communication. The TMC262 drives four external N- and P-channel dual MOSFETs for motor currents up to 8A and up to 60V. Integrated protection and diagnostic features support robust and reliable operation.

High integration, high energy efficiency and small form factor enable miniaturized designs with low external component count for cost-effective and highly competitive solutions.



TRINAMIC Motion Control GmbH & Co. KG
Hamburg, Germany

TRINAMIC
MOTION CONTROL
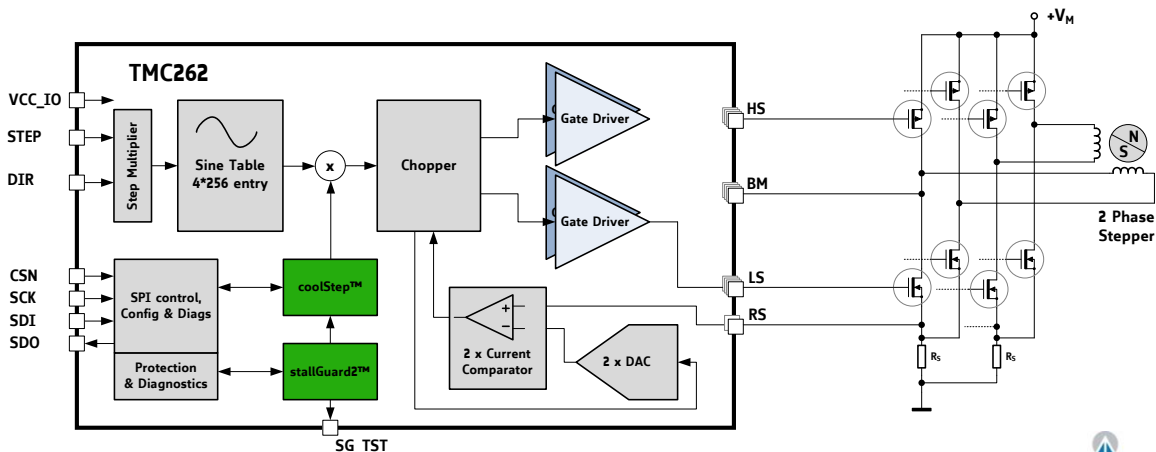
# APPLICATION EXAMPLES:  HIGH POWER – SMALL SIZE

The TMC262 scores with its high power density and a versatility that covers a wide spectrum of applications and motor sizes, all while keeping costs down. Extensive support at the chip, board, and software levels enables rapid design cycles and fast time-to-market with competitive products. High energy efficiency from TRINAMIC's coolStep technology delivers further cost savings in related systems such as power supplies and cooling.
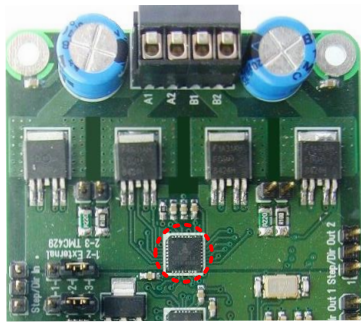


*Layout with 6A MOSFETs*

### STEPROCKER™

The driver stage shown uses 6A-capable dual MOSFETs. All cooling requirements are satisfied by passive convection cooling. The stepRocker is supported by the motioncontrol-community, with forum, applications, schematics, open source projects, demos etc.:





*Miniaturized Layout*

### TMCM-MODULE FOR NEMA 11 STEPPER MOTORS

This miniaturized power stage drives up to 1.2A RMS and mounts directly on a 28mm-size motor. Tiny TSOP6 dual MOSFETs enable an ultra-compact and flexible PCB layout.
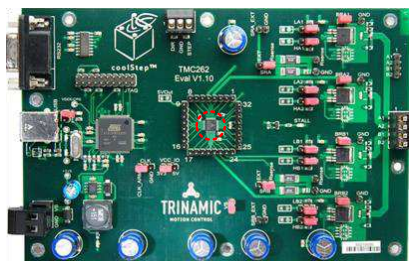


*Layout for Evaluation*

### TMC262-EVAL DEVELOPMENT PLATFORM

This evaluation board is a development platform for applications based on the TMC262.

The board features USB and RS232 interfaces for communication with control software running on a PC. External power MOSFETs support drive currents up to 6A at 40 V.

The control software provides a user-friendly GUI for setting control parameters and visualizing the dynamic response of the motor.

Motor movement can be controlled through the Step and Dir interface using inputs from an external source or signals generated by the onboard microcontroller acting as a step generator.

## ORDER CODES

| Order code | Description | Size |
|---|---|---|
| TMC262-LA | coolStep™ driver for external MOSFETs, QFN32 | 5 x 5 mm² |
| TMC262-EVAL | Evaluation board for TMC262 (RS232, USB) | 10 x 16 cm² |
| TMC429+26x-EVAL | Chipset evaluation board for TMC429, TMC260, TMC261, TMC262, and TMC424. | 10 x 16 cm² |

# TABLE OF CONTENTS
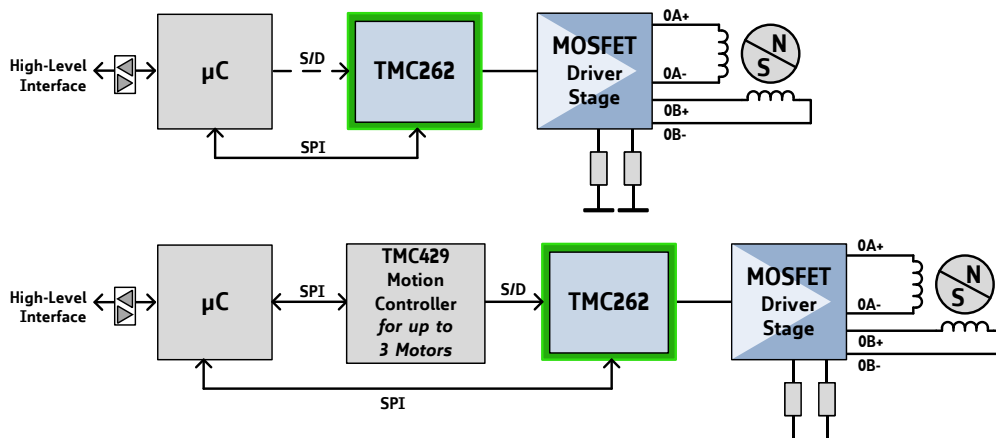
# 1 Principles of Operation



**Figure 1.1 Applications block diagrams**

The TMC262 motor driver is the intelligence between a motion controller and the power MOSFETs for driving a two-phase stepper motor, as shown in Figure 1.1 Following power-up, an embedded microcontroller initializes the driver by sending commands over an SPI bus to write control parameters and mode bits in the TMC262. The microcontroller may implement the motion-control function as shown in the upper part of the figure, or it may send commands to a dedicated motion controller chip such as TRINAMIC's TMC429 as shown in the lower part.

The motion controller can control the motor position by sending pulses on the STEP signal while indicating the direction on the DIR signal. The TMC262 has a microstep counter and sine table to convert these signals into the coil currents which control the position of the motor. If the microcontroller implements the motion-control function, it can write values for the coil currents directly to the TMC262 over the SPI interface, in which case the STEP/DIR interface may be disabled. This mode of operation requires software to track the motor position and reference a sine table to calculate the coil currents.

To optimize power consumption and heat dissipation, software may also adjust coolStep and stallGuard2 parameters in real-time, for example to implement different tradeoffs between speed and power consumption in different modes of operation.

The motion control function is a hard real-time task which may be a burden to implement reliably alongside other tasks on the embedded microcontroller. By offloading the motion-control function to the TMC429, up to three motors can be operated reliably with very little demand for service from the microcontroller. Software only needs to send target positions, and the TMC429 generates precisely timed step pulses. Software retains full control over both the TMC262 and TMC429 through the SPI bus.

## 1.1 Key Concepts

The TMC262 motor driver implements several advanced patented features which are exclusive to TRINAMIC products. These features contribute toward greater precision, greater energy efficiency, higher reliability, smoother motion, and cooler operation in many stepper motor applications.

*stallGuard2™*   High-precision load measurement using the back EMF on the coils

*coolStep™*   Load-adaptive current control which reduces energy consumption by as much as 75%

*spreadCycle™*   High-precision chopper algorithm available as an alternative to the traditional constant off-time algorithm

*microPlyer™*   Microstep interpolator for obtaining increased smoothness of microstepping over a STEP/DIR interface

In addition to these performance enhancements, TRINAMIC motor drivers also offer safeguards to detect and protect against shorted outputs, open-circuit output, overtemperature, and undervoltage conditions for enhancing safety and recovery from equipment malfunctions.

## 1.2   Control Interfaces

There are two control interfaces from the motion controller to the motor driver: the SPI serial interface and the STEP/DIR interface. The SPI interface is used to write control information to the chip and read back status information. This interface must be used to initialize parameters and modes necessary to enable driving the motor. This interface may also be used for directly setting the currents flowing through the motor coils, as an alternative to stepping the motor using the STEP and DIR signals, so the motor can be controlled through the SPI interface alone.

The STEP/DIR interface is a traditional motor control interface available for adapting existing designs to use TRINAMIC motor drivers. Using only the SPI interface requires slightly more CPU overhead to look up the sine tables and send out new current values for the coils.

### 1.2.1  SPI Interface

The SPI interface is a bit-serial interface synchronous to a bus clock. For every bit sent from the bus master to the bus slave, another bit is sent simultaneously from the slave to the master. Communication between an SPI master and the TMC262 slave always consists of sending one 20-bit command word and receiving one 20-bit status word.

The SPI command rate typically corresponds to the microstep rate at low velocities. At high velocities, the rate may be limited by CPU bandwidth to 10-100 thousand commands per second, so the application may need to change to fullstep resolution.

### 1.2.2  STEP/DIR Interface

The STEP/DIR interface is enabled by default. Active edges on the STEP input can be rising edges or both rising and falling edges, as controlled by another mode bit (DEDGE). Using both edges cuts the toggle rate of the STEP signal in half, which is useful for communication over slow interfaces such as optically isolated interfaces.

On each active edge, the state sampled from the DIR input determines whether to step forward or back. Each step can be a fullstep or a microstep, in which there are 2, 4, 8, 16, 32, 64, 128, or 256 microsteps per fullstep. During microstepping, a low state on DIR increases the microstep counter and a high decreases the counter by an amount controlled by the microstep resolution. An internal table translates the counter value into the sine and cosine values which control the motor current for microstepping.

## 1.3   Mechanical Load Sensing

The TMC262 provides stallGuard2 high-resolution load measurement for determining the mechanical load on the motor by measuring the back EMF. In addition to detecting when a motor stalls, this feature can be used for homing to a mechanical stop without a limit switch or proximity detector. The coolStep power-saving mechanism uses stallGuard2 to reduce the motor current to the minimum motor current required to meet the actual load placed on the motor.

## 1.4   Current Control

Current into the motor coils is controlled using a cycle-by-cycle chopper mode. Two chopper modes are available: a traditional constant off-time mode and the new spreadCycle mode. spreadCycle mode offers smoother operation and greater power efficiency over a wide range of speed and load.

# 2 Pin Assignments

## 2.1 Package Outline



Top view
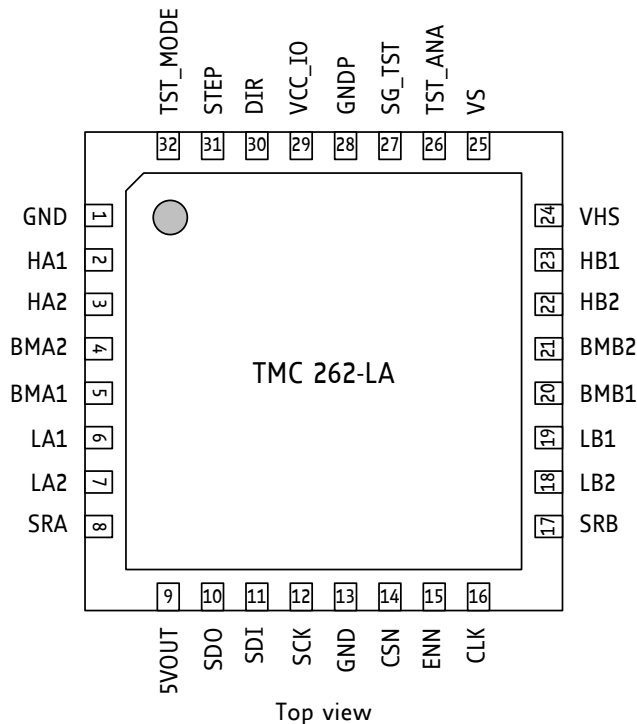
**Figure 2.1 TMC262 pin assignments**

## 2.2 Signal Descriptions

| Pin | Number | Type | Function |
|---|---|---|---|
| GND | 1 | | Digital and analog low power GND |
| | 13 | | |
| HA1 | 2 | O (VS) | High side P-channel driver output. Becomes driven to VHS to switch on MOSFET. |
| HA2 | 3 | | |
| HB1 | 23 | | |
| HB2 | 22 | | |
| BMA1 | 5 | I (VS) | Sensing input for bridge outputs. Used for short to GND protection. May be tied to VS if unused. |
| BMA2 | 4 | | |
| BMB1 | 20 | | |
| BMB2 | 21 | | |
| LA1 | 6 | O 5V | Low side MOSFET driver output. Becomes driven to 5VOUT to switch on MOSFET. |
| LA2 | 7 | | |
| LB1 | 19 | | |
| LB2 | 18 | | |
| SRA | 8 | AI | Sense resistor input of chopper driver. |
| SRB | 17 | | |
| 5VOUT | 9 | | Output of internal 5V linear regulator. This voltage is used to supply the low side drivers and internal analog circuitry. An external capacitor to GND close to the pin is required. Place the capacitor near to pin 9 and pin 13. 470nF ceramic are sufficient for most applications, an additional tantalum capacitor (10µF or more) improves performance with high gate charge MOSFETs. |
| SDO | 10 | DO VIO | Data output of SPI interface (Tristate) |

| Pin | Number | Type | Function |
|---|---|---|---|
| SDI | 11 | DI VIO | Data input of SPI interface<br>(Scan test input in test mode) |
| SCK | 12 | DI VIO | Serial clock input of SPI interface<br>(Scan test shift enable input in test mode) |
| CSN | 14 | DI VIO | Chip select input  of SPI interface |
| ENN | 15 | DI VIO | Enable not input for drivers. Switches off all MOSFETs. |
| CLK | 16 | DI VIO | Clock input for all internal operations. Tie low to use internal oscillator. A high signal disables the internal oscillator until power down. |
| VHS | 24 | | High side supply voltage (motor supply voltage VS - 10V) |
| VS | 25 | | Motor supply voltage |
| TST_ANA | 26 | AO VIO | Analog mode test output. Leave open for normal operation. |
| SG_TST | 27 | DO VIO | stallGuard2™ output. Signals motor stall (high active). |
| GNDP | 28 | | Power GND for MOSFET drivers. Connect directly to GND |
| VCC_IO | 29 | | Input / output supply voltage VIO for all digital pins. Tie to digital logic supply voltage. Allows operation in 3.3V and 5V systems. |
| DIR | 30 | DI VIO | Direction input. Is sampled upon detection of a step to determine stepping direction. An internal glitch filter for 60ns is provided. |
| STEP | 31 | DI VIO | Step input. An internal glitch filter for 60ns is provided. |
| TST_MODE | 32 | DI VIO | Test mode input. Puts IC into test mode. Tie to GND for normal operation using a short wire to GND plane. |

# 3  Internal Architecture

Figure 3.1 shows the internal architecture of the TMC262.
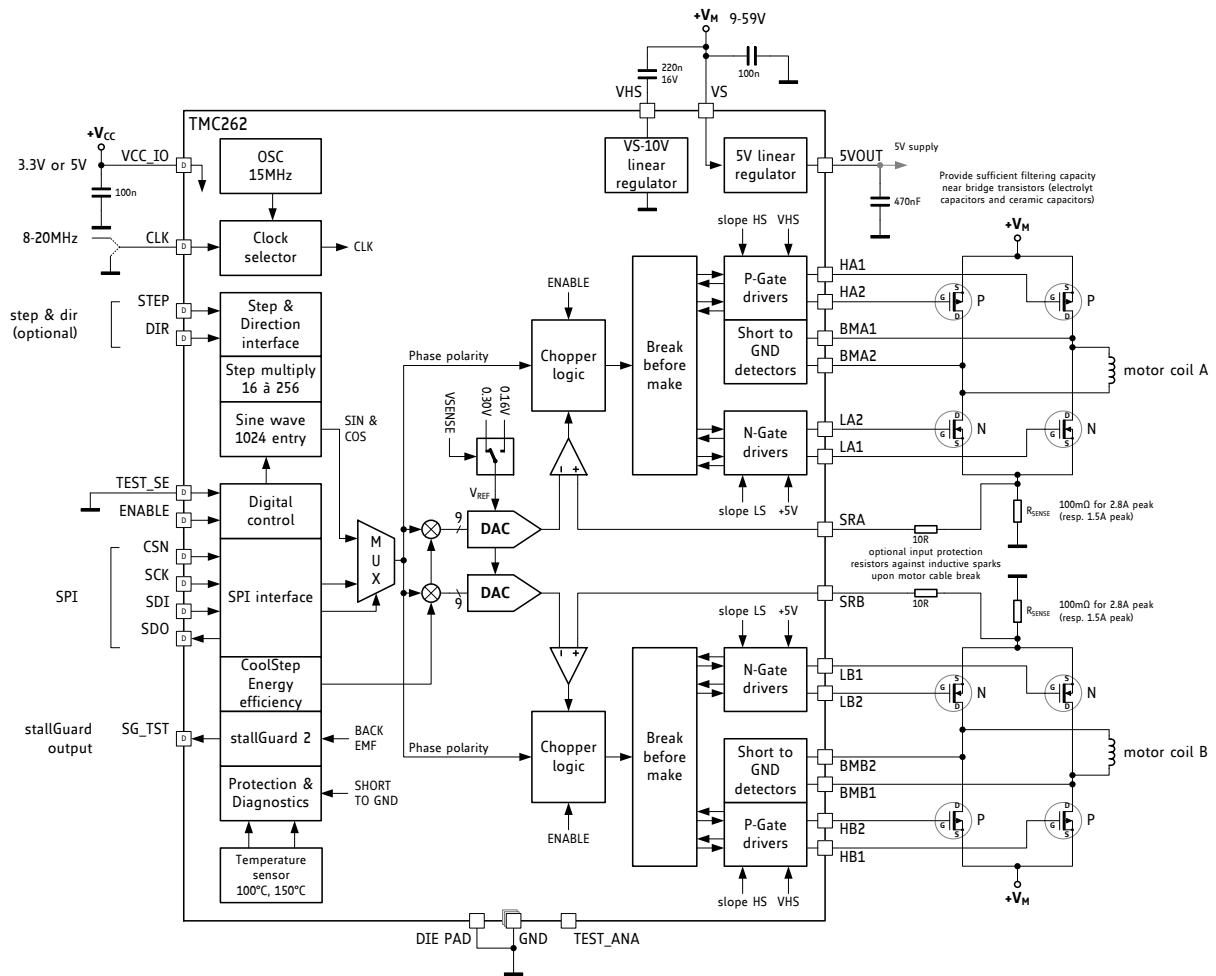


**Figure 3.1 TMC262 block diagram**

Prominent features include:

| | |
|---|---|
| *Oscillator and clock selector* | provides the system clock from the on-chip oscillator or an external source. |
| *Step and direction interface* | uses a microstep counter and sine table to generate target currents for the coils. |
| *SPI interface* | receives commands that directly set the coil current values. |
| *Multiplexer* | selects either the output of the sine table or the SPI interface for controlling the current into the motor coils. |
| *Multipliers* | scales down the currents to both coils when the currents are greater than those required by the load on the motor or as set by the CS current scale parameter. |
| *DACs and comparators* | converts the digital current values to analog signals that are compared with the voltages on the sense resistors. Comparator outputs terminate chopper drive phases when target currents are reached. |
| *Break-before-make and gate drivers* | ensure non-overlapping pulses, boost pulse voltage, and control pulse slope to the gates of the power MOSFETs. |
| *On-chip voltage regulators* | provide high-side voltage for P-channel MOSFET gate drivers and supply voltage for on-chip analog and digital circuits. |

# 4   stallGuard2 Load Measurement

stallGuard2 provides an accurate measurement of the load on the motor. It can be used for stall detection as well as other uses at loads below those which stall the motor, such as coolStep load-adaptive current reduction. (stallGuard2 is a more precise evolution of the earlier stallGuard technology.)

The stallGuard2 measurement value changes linearly over a wide range of load, velocity, and current settings, as shown in Figure 4.1. At maximum motor load, the value goes to zero or near to zero. This corresponds to a load angle of 90° between the magnetic field of the coils and magnets in the rotor. This also is the most energy-efficient point of operation for the motor.
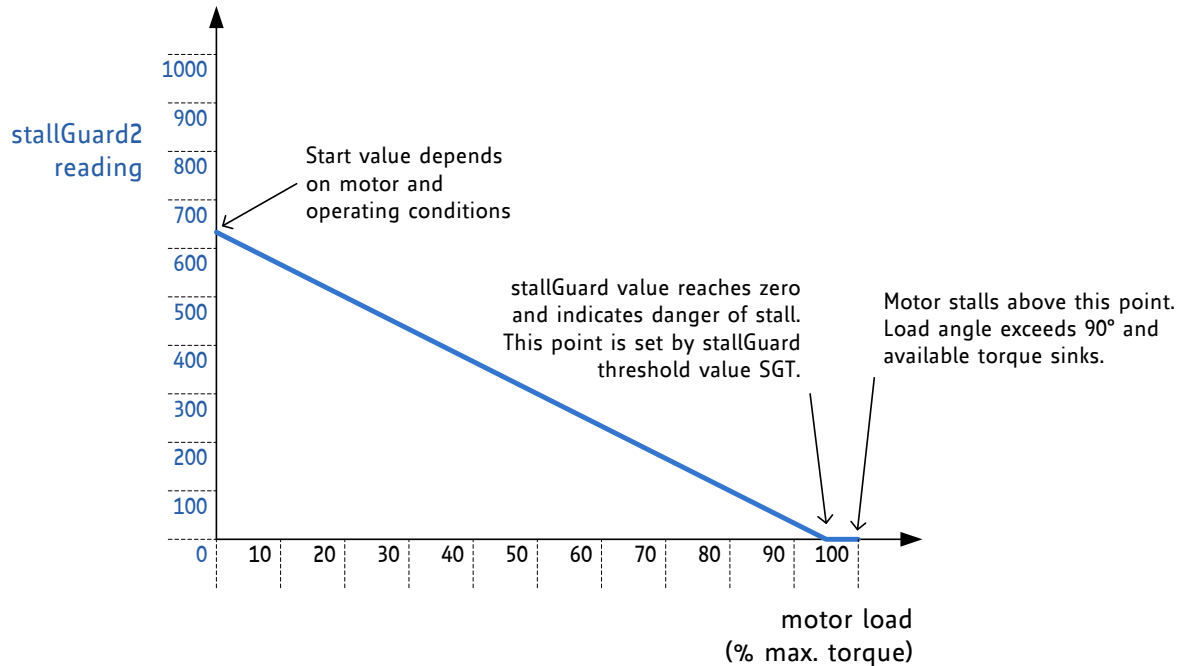


**Figure 4.1 stallGuard2 load measurement SG as a function of load**

Two parameters control stallGuard2 and one status value is returned.

| Parameter | Description | Setting | Comment |
|-----------|-------------|---------|---------|
| SGT | 7-bit signed integer that sets the stallGuard2 threshold level for asserting the SG_TST output and sets the optimum measurement range for readout. Negative values increase sensitivity, and positive values reduce sensitivity so more torque is required to indicate a stall. Zero is a good starting value. Operating at values below -10 is not recommended. | 0 | indifferent value |
|  |  | +1… +63 | less sensitivity |
|  |  | -1… -64 | higher sensitivity |
| SFILT | Mode bit which enables the stallGuard2 filter for more precision. If set, reduces the measurement frequency to one measurement per four fullsteps. If cleared, no filtering is performed. Filtering compensates for mechanical asymmetries in the construction of the motor, but at the expense of response time. Unfiltered operation is recommended for rapid stall detection. Filtered operation is recommended for more precise load measurement. | 0 | standard mode |
|  |  | 1 | filtered mode |

| Status word | Description | Range | Comment |
|---|---|---|---|
| SG | 10-bit unsigned integer stallGuard2 measurement value. A higher value indicates lower mechanical load. A lower value indicates a higher load and therefore a higher load angle. For stall detection, adjust SGT to return an SG value of 0 or slightly higher upon maximum motor load before stall. | 0… 1023 | 0: highest load low value: high load high value: less load |

# 4.1   Tuning the stallGuard2 Threshold

Due to the dependency of the stallGuard2 value SG from motor-specific characteristics and application-specific demands on load and velocity the easiest way to tune the stallGuard2 threshold *SGT* for a specific motor type and operating conditions is interactive tuning in the actual application.

The procedure is:

1. Operate the motor at a reasonable velocity for your application and monitor SG.
2. Apply slowly increasing mechanical load to the motor. If the motor stalls before SG reaches zero, decrease SGT. If SG reaches zero before the motor stalls, increase SGT. A good SGT starting value is zero. SGT is signed, so it can have negative or positive values.
3. The optimum setting is reached when SG is between 0 and 400 at increasing load shortly before the motor stalls, and SG increases by 100 or more without load. SGT in most cases can be tuned together with the motion velocity in a way that SG goes to zero when the motor stalls and the stall output SG_TST is asserted. This indicates that a step has been lost.

The system clock frequency affects SG. An external crystal-stabilized clock should be used for applications that demand the highest performance. The power supply voltage also affects SG, so tighter regulation results in more accurate values. SG measurement has a high resolution, and there are a few ways to enhance its accuracy, as described in the following sections.

## 4.1.1  Variable Velocity Operation

Across a range of velocities, on-the-fly adjustment of the stallGuard2 threshold SGT improves the accuracy of the load measurement SG. This also improves the power reduction provided by coolStep, which is driven by SG. Linear interpolation between two SGT values optimized at different velocities is a simple algorithm for obtaining most of the benefits of on-the-fly SGT adjustment, as shown in Figure 4.2. This figure shows an optimal SGT curve in black and a two-point interpolated SGT curve in red.
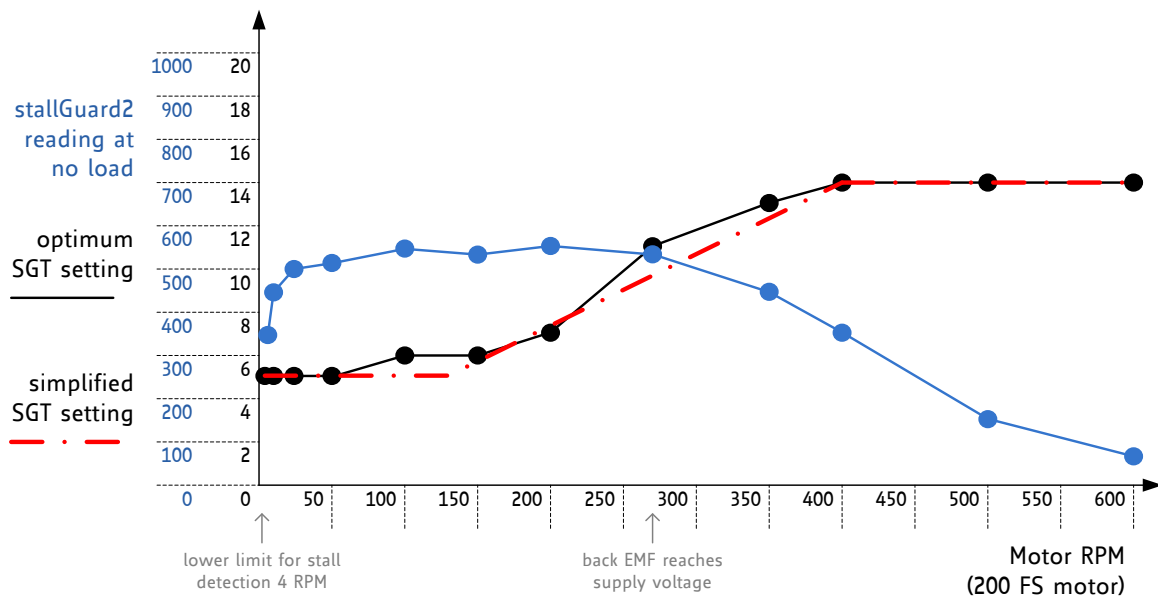
**Figure 4.2 Linear interpolation for optimizing SGT with changes in velocity**

## 4.1.2  Small Motors with High Torque Ripple and Resonance

Motors with a high detent torque show an increased variation of the stallGuard2 measurement value SG with varying motor currents, especially at low currents. For these motors, the current dependency might need correction in a similar manner to velocity correction for obtaining the highest accuracy.

## 4.1.3  Temperature Dependence of Motor Coil Resistance

Motors working over a wide temperature range may require temperature correction, because motor coil resistance increases with rising temperature. This can be corrected as a linear reduction of SG at increasing temperature, as motor efficiency is reduced.

## 4.1.4  Accuracy and Reproducibility of stallGuard2 Measurement

In a production environment, it may be desirable to use a fixed SGT value within an application for one motor type. Most of the unit-to-unit variation in stallGuard2 measurements results from manufacturing tolerances in motor construction. The measurement error of stallGuard2 – provided that all other parameters remain stable – can be as low as:

$$stallGuard\ measurement\ error = \pm max(1, |SGT|)$$

## 4.2    stallGuard2 Measurement Frequency and Filtering

The stallGuard2 measurement value SG is updated with each full step of the motor. This is enough to safely detect a stall, because a stall always means the loss of four full steps. In a practical application, especially when using coolStep, a more precise measurement might be more important than an update for each fullstep because the mechanical load never changes instantaneously from one step to the next. For these applications, the SFILT bit enables a filtering function over four load measurements. The filter should always be enabled when high-precision measurement is required. It compensates for variations in motor construction, for example due to misalignment of the phase A to phase B magnets. The filter should only be disabled when rapid response to increasing load is required, such as for stall detection at high velocity.

## 4.3   Detecting a Motor Stall

To safely detect a motor stall, a stall threshold must be determined using a specific SGT setting. Therefore, you need to determine the maximum load the motor can drive without stalling and to monitor the SG value at this load, for example some value within the range 0 to 400. The stall threshold should be a value safely within the operating limits, to allow for parameter stray. So, your microcontroller software should set a stall threshold which is slightly higher than the minimum value seen before an actual motor stall occurs. The response at an SGT setting at or near 0 gives some idea on the quality of the signal: Check the SG value without load and with maximum load. These values should show a difference of at least 100 or a few 100, which shall be large compared to the offset. If you set the SGT value so that a reading of 0 occurs at maximum motor load, an active high stall output signal will be available at SG_TST output.

## 4.4   Limits of stallGuard2 Operation

stallGuard2 does not operate reliably at extreme motor velocities: Very low motor velocities (for many motors, less than one revolution per second) generate a low back EMF and make the measurement unstable and dependent on environment conditions (temperature, etc.). Other conditions will also lead to extreme settings of SGT and poor response of the measurement value SG to the motor load.

Very high motor velocities, in which the full sinusoidal current is not driven into the motor coils also lead to poor response. These velocities are typically characterized by the motor back EMF reaching the supply voltage.

# 5   coolStep Load-Adaptive Current Control

coolStep allows substantial energy savings, especially for motors which see varying loads or operate at a high duty cycle. Because a stepper motor application needs to work with a torque reserve of 30% to 50%, even a constant-load application allows significant energy savings because coolStep automatically enables torque reserve when required. Reducing power consumption keeps the system cooler, increases motor life, and allows reducing cost in the power supply and cooling components.

*Reducing motor current by half results in reducing power by a factor of four.*

| | | |
|---|---|---|
| *Energy efficiency* | - | power consumption decreased up to 75%. |
| *Motor generates less heat* | - | improved mechanical precision. |
| *Less cooling infrastructure* | - | for motor and driver. |
| *Cheaper motor* | - | does the job. |
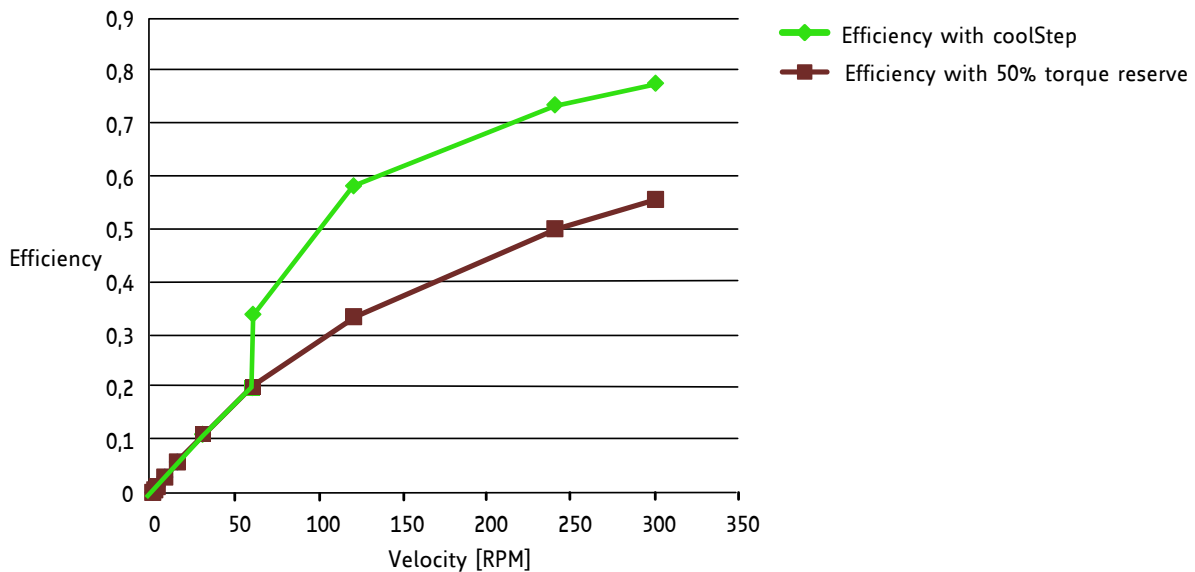


**Figure 5.1 Energy efficiency example with coolStep**

Figure 5.1 shows the efficiency gain of a 42mm stepper motor when using coolStep compared to standard operation with 50% of torque reserve. coolStep is enabled above 60rpm in the example.

coolStep is controlled by several parameters, but two are critical for understanding how it works:

| Parameter | Description | Range | Comment |
|---|---|---|---|
| SEMIN | 4-bit unsigned integer that sets a lower threshold. If SG goes below this threshold, coolStep increases the current to both coils. The 4-bit SEMIN value is scaled by 32 to cover the lower half of the range of the 10-bit SG value. (The name of this parameter is derived from smartEnergy, which is an earlier name for coolStep.) | 0… 15 | lower stallGuard threshold: SEMINx32 |
| SEMAX | 4-bit unsigned integer that controls an upper threshold. If SG is sampled equal to or above this threshold enough times, coolStep decreases the current to both coils. The upper threshold is (SEMIN + SEMAX + 1) x 32. | 0… 15 | upper stallGuard threshold: (SEMIN+SEMAX+1)x32 |

Figure 5.2 shows the operating regions of coolStep. The black line represents the SG measurement value, the blue line represents the mechanical load applied to the motor, and the red line represents the current into the motor coils. When the load increases, SG falls below SEMIN, and coolStep

increases the current. When the load decreases and SG rises above (SEMIN + SEMAX + 1) x 32 the current becomes reduced.
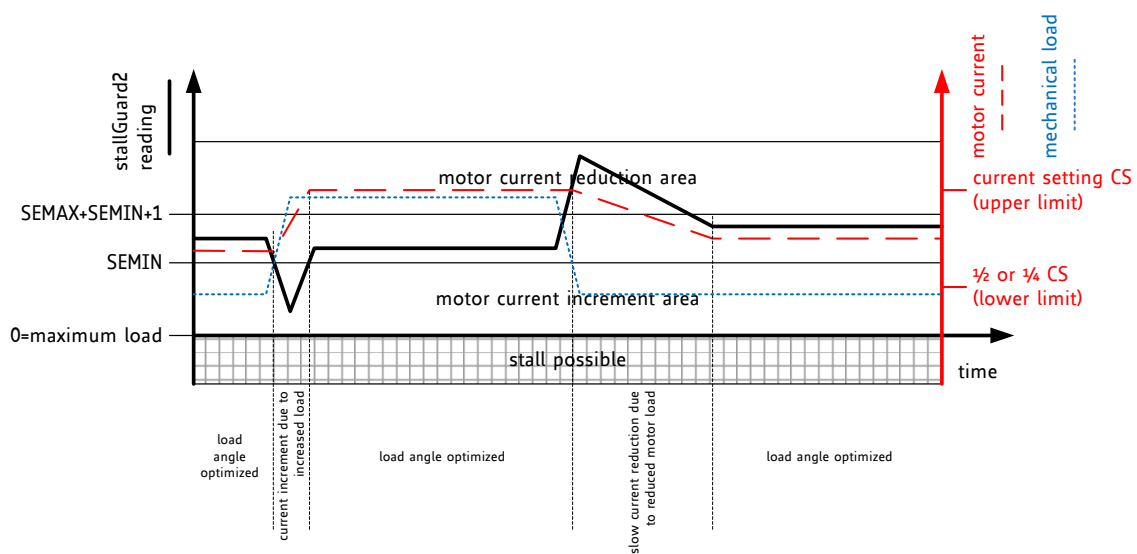


**Figure 5.2 coolStep adapts motor current to the load**

Four more parameters control coolStep and one status value is returned:

| Parameter | Description | Range | Comment |
|---|---|---|---|
| CS | *Current scale*. Scales both coil current values as taken from the internal sine wave table or from the SPI interface. For high precision motor operation, work with a current scaling factor in the range 16 to 31, because scaling down the current values reduces the effective microstep resolution by making microsteps coarser. This setting also controls the maximum current value set by coolStep™. | 0… 31 | scaling factor: 1/32, 2/32, … 32/32 |
| SEUP | Number of increments of the coil current for each occurrence of an SG measurement below the lower threshold. | 0… 3 | step width is: 1, 2, 4, 8 |
| SEDN | Number of occurrences of SG measurements above the upper threshold before the coil current is decremented. | 0… 3 | number of stallGuard measurements per decrement: 32, 8, 2, 1 |
| SEIMIN | Mode bit that controls the lower limit for scaling the coil current. If the bit is set, the limit is ¼ CS. If the bit is clear, the limit is ½ CS. | 0 | Minimum motor current: 1/2 of CS |
| | | 1 | 1/4 of CS |
| **Status word** | **Description** | **Range** | **Comment** |
| SE | 5-bit unsigned integer reporting the actual current scaling value determined by coolStep. This value is biased by 1 and divided by 32, so the range is 1/32 to 32/32. The value will not be greater than the value of CS or lower than either ¼ CS or ½ CS depending on the setting of SEIMIN. | 0… 31 | Actual motor current scaling factor set by coolStep: 1/32, 2/32, … 32/32 |

# 5.1   Tuning coolStep

Before tuning coolStep, first tune the stallGuard2 threshold level SGT, which affects the range of the load measurement value SG. coolStep uses SG to operate the motor near the optimum load angle of +90°.

The current increment speed is specified in SEUP, and the current decrement speed is specified in SEDN. They can be tuned separately because they are triggered by different events that may need different responses. The encodings for these parameters allow the coil currents to be increased much more quickly than decreased, because crossing the lower threshold is a more serious event that may require a faster response. If the response is too slow, the motor may stall. In contrast, a slow response to crossing the upper threshold does not risk anything more serious than missing an opportunity to save power.

> *coolStep operates between limits controlled by the current scale parameter CS and the SEIMIN bit.*

## 5.1.1  Response Time

For fast response to increasing motor load, use a high current increment step SEUP. If the motor load changes slowly, a lower current increment step can be used to avoid motor current oscillations. If the filter controlled by SFILT is enabled, the measurement rate and regulation speed are cut by a factor of four.

## 5.1.2  Low Velocity and Standby Operation

Because stallGuard2 is not able to measure the motor load in standstill and at very low RPM, the current at low velocities should be set to an application-specific default value and combined with standstill current reduction settings programmed through the SPI interface.

# 6   SPI Interface

The TMC262 requires setting configuration parameters and mode bits through the SPI interface before the motor can be driven. The SPI interface also allows reading back status values and bits.

## 6.1   Bus Signals

 The SPI bus on the TMC262 has four signals:

| | |
|---|---|
| SCK | bus clock input |
| SDI | serial data input |
| SDO | serial data output |
| CSN | chip select input (active low) |

The slave is enabled for an SPI transaction by a low on the chip select input CSN. Bit transfer is synchronous to the bus clock SCK, with the slave latching the data from SDI on the rising edge of SCK and driving data to SDO following the falling edge. The most significant bit is sent first. A minimum of 20 SCK clock cycles is required for a bus transaction with the TMC262.

If more than 20 clocks are driven, the additional bits shifted into SDI are shifted out on SDO after a 20-clock delay through an internal shift register. This can be used for daisy chaining multiple chips.

CSN must be low during the whole bus transaction. When CSN goes high, the contents of the internal shift register are latched into the internal control register and recognized as a command from the master to the slave. If more than 20 bits are sent, only the last 20 bits received before the rising edge of CSN are recognized as the command.

## 6.2   Bus Timing

SPI interface is synchronized to the internal system clock, which limits the SPI bus clock SCK to half of the system clock frequency. If the system clock is based on the on-chip oscillator, an additional 10% safety margin must be used to ensure reliable data transmission. All SPI inputs as well as the ENN input are internally filtered to avoid triggering on pulses shorter than 20ns. Figure 6.1 shows the timing parameters of an SPI bus transaction, and the table below specifies their values.
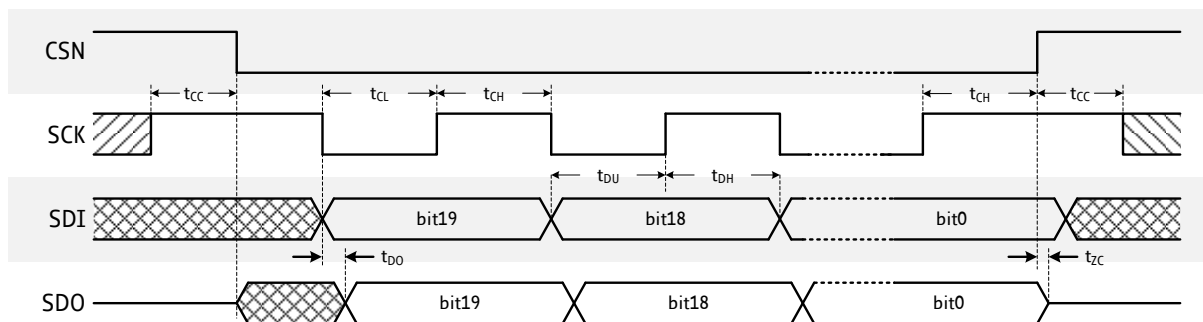


**Figure 6.1 SPI Timing**

| |
|---|
| *Hint* |
| Usually this SPI timing is referred to as SPI MODE 3 |

| SPI Interface Timing | AC-Characteristics<br>clock period is $t_{CLK}$ | | | | | |
|---|---|---|---|---|---|---|
| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
| SCK valid before or after change of CSN | $t_{CC}$ | | 10 | | | ns |
| CSN high time | $t_{CSH}$ | *)Min time is for synchronous CLK with SCK high one $t_{oi}$ before CSN high only | $t_{CLK}$ | >2$t_{CLK}$ +10 | | ns |
| SCK low time | $t_{CL}$ | *)Min time is for synchronous CLK only | $t_{CLK}$ | >$t_{CLK}$+10 | | ns |
| SCK high time | $t_{CH}$ | *)Min time is for synchronous CLK only | $t_{CLK}$ | >$t_{CLK}$+10 | | ns |
| SCK frequency using internal clock | $f_{SCK}$ | Assumes minimum OSC frequency | | | 4 | MHz |
| SCK frequency using external 16MHz clock | $f_{SCK}$ | Assumes synchronous CLK | | | 8 | MHz |
| SDI setup time before rising edge of SCK | $t_{DU}$ | | 10 | | | ns |
| SDI hold time after rising edge of SCK | $t_{DH}$ | | 10 | | | ns |
| Data out valid time after falling SCK clock edge | $t_{DO}$ | No capacitive load on SDO | | | $t_{FILT}$+5 | ns |
| SDI, SCK, and CSN filter delay time | $t_{FILT}$ | Rising and falling edge | 12 | 20 | 30 | ns |

## 6.3   Bus Architecture

SPI slaves can be chained and used with a single chip select line. If slaves are chained, they behave like a long shift register. For example, a chain of two motor drivers requires 40 bits to be sent. The last bits shifted to each register in the chain are loaded into an internal register on the rising edge of the CSN input. For example, 24 or 32 bits can be sent to a single motor driver, but it latches just the last 20 bits received before CSN goes high.
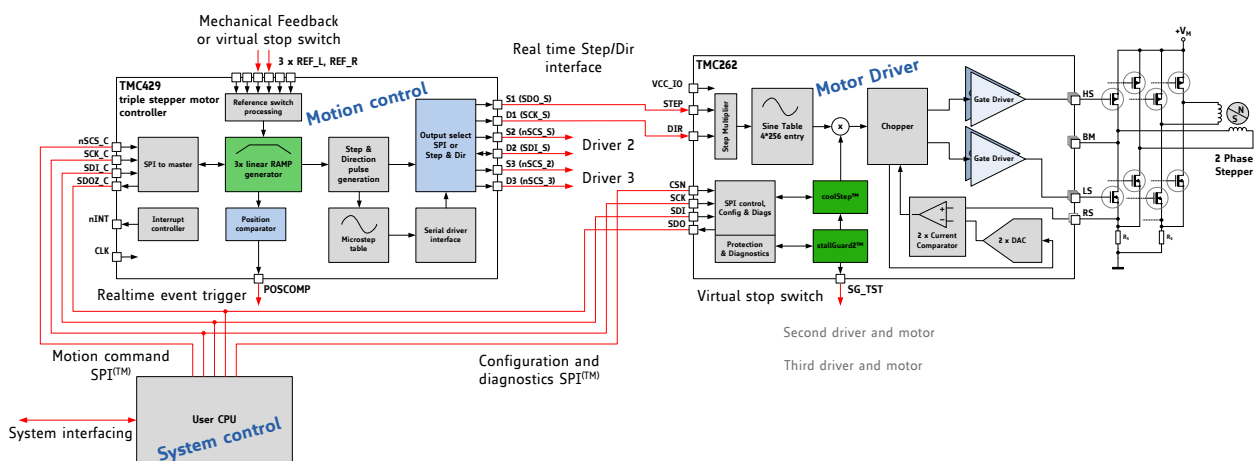


**Figure 6.2 Interfaces to a TMC429 motion controller chip and a TMC262 motor driver**

Figure 6.2 shows the interfaces in a typical application. The SPI bus is used by an embedded MCU to initialize the control registers of both a motion controller and one or more motor drivers. STEP/DIR interfaces are used between the motion controller and the motor drivers.

# 6.4   Register Write Commands

An SPI bus transaction to the TMC262 is a write command to one of the five write-only registers that hold configuration parameters and mode bits:

| Register | Description |
|---|---|
| Driver Control Register (DRVCTRL) | The DRVCTRL register has different formats for controlling the interface to the motion controller depending on whether or not the STEP/DIR interface is enabled. |
| Chopper Configuration Register (CHOPCONF) | The CHOPCONF register holds chopper parameters and mode bits. |
| coolStep Configuration Register (SMARTEN) | The SMARTEN register holds coolStep parameters and a mode bit. (smartEnergy is an earlier name for coolStep.) |
| stallGuard2 Configuration Register (SGCSCONF) | The SGCSCONF register holds stallGuard2 parameters and a mode bit. |
| Driver Configuration Register (DRVCONF) | The DRVCONF register holds parameters and mode bits used to control the power MOSFETs and the protection circuitry. It also holds the SDOFF bit which controls the STEP/DIR interface and the RDSEL parameter which controls the contents of the response returned in an SPI transaction |

*In the following sections, multibit binary values are prefixed with a % sign, for example %0111.*

## 6.4.1  Write Command Overview

The table below shows the formats for the five register write commands. Bits 19, 18, and sometimes 17 select the register being written, as shown in bold. The DRVCTRL register has two formats, as selected by the SDOFF bit. Bits shown as 0 must always be written as 0, and bits shown as 1 must always be written with 1. Detailed descriptions of each parameter and mode bit are given in the following sections.

| Register/ Bit | DRVCTRL (*SDOFF*=1) | DRVCTRL (*SDOFF*=0) | CHOPCONF | SMARTEN | SGCSCONF | DRVCONF |
|---|---|---|---|---|---|---|
| 19 | **0** | **0** | **1** | **1** | **1** | **1** |
| 18 | **0** | **0** | **0** | **0** | **1** | **1** |
| 17 | PHA | **0** | **0** | **1** | **0** | **1** |
| 16 | CA7 | 0 | TBL1 | 0 | SFILT | TST |
| 15 | CA6 | 0 | TBL0 | SEIMIN | 0 | SLPH1 |
| 14 | CA5 | 0 | CHM | SEDN1 | SGT6 | SLPH0 |
| 13 | CA4 | 0 | RNDTF | SEDN0 | SGT5 | SLPL1 |
| 12 | CA3 | 0 | HDEC1 | 0 | SGT4 | SLPL0 |
| 11 | CA2 | 0 | HDEC0 | SEMAX3 | SGT3 | 0 |
| 10 | CA1 | 0 | HEND3 | SEMAX2 | SGT2 | DISS2G |
| 9 | CA0 | INTPOL | HEND2 | SEMAX1 | SGT1 | TS2G1 |
| 8 | PHB | DEDGE | HEND1 | SEMAX0 | SGT0 | TS2G0 |
| 7 | CB7 | 0 | HEND0 | 0 | 0 | *SDOFF* |
| 6 | CB6 | 0 | HSTRT2 | SEUP1 | 0 | VSENSE |
| 5 | CB5 | 0 | HSTRT1 | SEUP0 | 0 | *RDSEL1* |
| 4 | CB4 | 0 | HSTRT0 | 0 | CS4 | *RDSEL0* |
| 3 | CB3 | MRES3 | TOFF3 | SEMIN3 | CS3 | 0 |
| 2 | CB2 | MRES2 | TOFF2 | SEMIN2 | CS2 | 0 |
| 1 | CB1 | MRES1 | TOFF1 | SEMIN1 | CS1 | 0 |
| 0 | CB0 | MRES0 | TOFF0 | SEMIN0 | CS0 | 0 |

### 6.4.2 Read Response Overview

The table below shows the formats for the read response. The RDSEL parameter in the DRVCONF register selects the format of the read response.

| Bit | RDSEL=%00 | RDSEL=%01 | RDSEL=%10 |
|-----|-----------|-----------|-----------|
| 19 | MSTEP9 | SG9 | SG9 |
| 18 | MSTEP8 | SG8 | SG8 |
| 17 | MSTEP7 | SG7 | SG7 |
| 16 | MSTEP6 | SG6 | SG6 |
| 15 | MSTEP5 | SG5 | SG5 |
| 14 | MSTEP4 | SG4 | SE4 |
| 13 | MSTEP3 | SG3 | SE3 |
| 12 | MSTEP2 | SG2 | SE2 |
| 11 | MSTEP1 | SG1 | SE1 |
| 10 | MSTEP0 | SG0 | SE0 |
| 9 | - | - | - |
| 8 | - | - | - |
| 7 | STST | | |
| 6 | OLB | | |
| 5 | OLA | | |
| 4 | S2GB | | |
| 3 | S2GA | | |
| 2 | OTPW | | |
| 1 | OT | | |
| 0 | SG | | |

## 6.5  Driver Control Register (DRVCTRL)

The format of the DRVCTRL register depends on the state of the SDOFF mode bit.

*SPI Mode*        SDOFF bit is set, the STEP/DIR interface is disabled, and DRVCTRL is the interface for specifying the currents through each coil.

*STEP/DIR Mode*   SDOFF bit is clear, the STEP/DIR interface is enabled, and DRVCTRL is a configuration register for the STEP/DIR interface.

### 6.5.1  DRVCTRL Register in SPI Mode

| DRVCTRL | | Driver Control in SPI Mode (SDOFF=1) | |
|---------|------|----------|---------|
| Bit | Name | Function | Comment |
| 19 | 0 | Register address bit | |
| 18 | 0 | Register address bit | |
| 17 | PHA | Polarity A | Sign of current flow through coil A:<br>0: Current flows from OA1 pins to OA2 pins.<br>1: Current flows from OA2 pins to OA1 pins. |
| 16 | CA7 | Current A MSB | Magnitude of current flow through coil A. The range is 0 to 248, if hysteresis or offset are used up to their full extent. The resulting value after applying hysteresis or offset must not exceed 255. |
| 15 | CA6 | | |
| 14 | CA5 | | |
| 13 | CA4 | | |
| 12 | CA3 | | |
| 11 | CA2 | | |
| 10 | CA1 | | |
| 9 | CA0 | Current A LSB | |

| DRVCTRL | | Driver Control in SPI Mode (SDOFF=1) | |
|---|---|---|---|
| Bit | Name | Function | Comment |
| 8 | PHB | Polarity B | Sign of current flow through coil B:<br>0: Current flows from OB1 pins to OB2 pins.<br>1: Current flows from OB2 pins to OB1 pins. |
| 7 | CB7 | Current B MSB | Magnitude of current flow through coil B. The range is 0 to 248, if hysteresis or offset are used up to their full extent. The resulting value after applying hysteresis or offset must not exceed 255. |
| 6 | CB6 | | |
| 5 | CB5 | | |
| 4 | CB4 | | |
| 3 | CB3 | | |
| 2 | CB2 | | |
| 1 | CB1 | | |
| 0 | CB0 | Current B LSB | |

## 6.5.2 DRVCTRL Register in STEP/DIR Mode

| DRVCTRL | | Driver Control in STEP/DIR Mode (SDOFF=0) | |
|---|---|---|---|
| Bit | Name | Function | Comment |
| 19 | 0 | Register address bit | |
| 18 | 0 | Register address bit | |
| 17 | 0 | Reserved | |
| 16 | 0 | Reserved | |
| 15 | 0 | Reserved | |
| 14 | 0 | Reserved | |
| 13 | 0 | Reserved | |
| 12 | 0 | Reserved | |
| 11 | 0 | Reserved | |
| 10 | 0 | Reserved | |
| 9 | INTPOL | Enable STEP interpolation | 0: Disable STEP pulse interpolation.<br>1: Enable STEP pulse multiplication by 16. |
| 8 | DEDGE | Enable double edge STEP pulses | 0: Rising STEP pulse edge is active, falling edge is inactive.<br>1: Both rising and falling STEP pulse edges are active. |
| 7 | 0 | Reserved | |
| 6 | 0 | Reserved | |
| 5 | 0 | Reserved | |
| 4 | 0 | Reserved | |
| 3 | MRES3 | Microstep resolution for STEP/DIR mode | Microsteps per 90°:<br>%0000: 256<br>%0001: 128<br>%0010: 64<br>%0011: 32<br>%0100: 16<br>%0101: 8<br>%0110: 4<br>%0111: 2 (halfstep)<br>%1000: 1 (fullstep) |
| 2 | MRES2 | | |
| 1 | MRES1 | | |
| 0 | MRES0 | | |

## 6.6 Chopper Control Register (CHOPCONF)

| CHOPCONF | | Chopper Configuration | | |
|---|---|---|---|---|
| **Bit** | **Name** | **Function** | **Comment** | |
| 19 | 1 | Register address bit | | |
| 18 | 0 | Register address bit | | |
| 17 | 0 | Register address bit | | |
| 16 | TBL1 | Blanking time | Blanking time interval, in system clock periods: %00: 16 %01: 24 %10: 36 %11: 54 | |
| 15 | TBL0 | | | |
| 14 | CHM | Chopper mode | This mode bit affects the interpretation of the HDEC, HEND, and HSTRT parameters shown below. | |
| | | | 0 | Standard mode (spreadCycle) |
| | | | 1 | Constant $t_{OFF}$ with fast decay time. Fast decay time is also terminated when the negative nominal current is reached. Fast decay is after on time. |
| 13 | RNDTF | Random TOFF time | Enable randomizing the slow decay phase duration: 0: Chopper off time is fixed as set by bits $t_{OFF}$ 1: Random mode, $t_{OFF}$ is random modulated by $dN_{CLK}$= -12 … +3 clocks. | |
| 12 | HDEC1 | Hysteresis decrement interval or Fast decay mode | CHM=0 | Hysteresis decrement period setting, in system clock periods: %00: 16 %01: 32 %10: 48 %11: 64 |
| 11 | HDEC0 | | | |
| | | | CHM=1 | HDEC1=0: current comparator can terminate the fast decay phase before timer expires. HDEC1=1: only the timer terminates the fast decay phase. HDEC0: MSB of fast decay time setting. |
| 10 | HEND3 | Hysteresis end (low) value or Sine wave offset | CHM=0 | %0000 … %1111: Hysteresis is -3, -2, -1, 0, 1, …, 12 (1/512 of this setting adds to current setting) This is the hysteresis value which becomes used for the hysteresis chopper. |
| 9 | HEND2 | | | |
| 8 | HEND1 | | CHM=1 | %0000 … %1111: Offset is -3, -2, -1, 0, 1, …, 12 This is the sine wave offset and 1/512 of the value becomes added to the absolute value of each sine wave entry. |
| 7 | HEND0 | | | |
| 6 | HSTRT2 | Hysteresis start value or Fast decay time setting | CHM=0 | Hysteresis start offset from HEND: %000: 1   %100: 5 %001: 2   %101: 6 %010: 3   %110: 7 %011: 4   %111: 8 *Effective: HEND+HSTRT must be ≤ 15* |
| 5 | HSTRT1 | | | |
| 4 | HSTRT0 | | CHM=1 | Three least-significant bits of the duration of the fast decay phase. The MSB is HDEC0. Fast decay time is a multiple of system clock periods: $N_{CLK}$= 32 x (*HDEC0+HSTRT*) |

| CHOPCONF | | Chopper Configuration | |
|---|---|---|---|
| Bit | Name | Function | Comment |
| 3 | TOFF3 | Off time/MOSFET disable | Duration of slow decay phase. If TOFF is 0, the MOSFETs are shut off. If TOFF is nonzero, slow decay time is a multiple of system clock periods: $N_{CLK}$= 12 + (32 x TOFF) (Minimum time is 64clocks.) %0000: Driver disable, all bridges off %0001: 1 (use with TBL of minimum 24 clocks) %0010 … %1111: 2 … 15 |
| 2 | TOFF2 | | |
| 1 | TOFF1 | | |
| 0 | TOFF0 | | |

# 6.7   coolStep Control Register (SMARTEN)

| SMARTEN | | coolStep Configuration | |
|---|---|---|---|
| Bit | Name | Function | Comment |
| 19 | 1 | Register address bit | |
| 18 | 0 | Register address bit | |
| 17 | 1 | Register address bit | |
| 16 | 0 | Reserved | |
| 15 | SEIMIN | Minimum coolStep current | 0: ½ CS current setting 1: ¼ CS current setting |
| 14 | SEDN1 | Current decrement speed | Number of times that the stallGuard2 value must be sampled equal to or above the upper threshold for each decrement of the coil current: %00: 32 %01: 8 %10: 2 %11: 1 |
| 13 | SEDN0 | | |
| 12 | 0 | Reserved | |
| 11 | SEMAX3 | Upper coolStep threshold as an offset from the lower threshold | If the stallGuard2 measurement value SG is sampled equal to or above (SEMIN+SEMAX+1) x 32 enough times, then the coil current scaling factor is decremented. |
| 10 | SEMAX2 | | |
| 9 | SEMAX1 | | |
| 8 | SEMAX0 | | |
| 7 | 0 | Reserved | |
| 6 | SEUP1 | Current increment size | Number of current increment steps for each time that the stallGuard2 value SG is sampled below the lower threshold: %00: 1 %01: 2 %10: 4 %11: 8 |
| 5 | SEUP0 | | |
| 4 | 0 | Reserved | |
| 3 | SEMIN3 | Lower coolStep threshold/coolStep disable | If SEMIN is 0, coolStep is disabled. If SEMIN is nonzero and the stallGuard2 value SG falls below SEMIN x 32, the coolStep current scaling factor is increased. |
| 2 | SEMIN2 | | |
| 1 | SEMIN1 | | |
| 0 | SEMIN0 | | |

## 6.8   stallGuard2 Control Register (SGCSCONF)

| SGCSCONF | | stallGuard2™ and Current Setting | |
|---|---|---|---|
| Bit | Name | Function | Comment |
| 19 | 1 | Register address bit | |
| 18 | 1 | Register address bit | |
| 17 | 0 | Register address bit | |
| 16 | SFILT | stallGuard2 filter enable | 0: Standard mode, fastest response time. 1: Filtered mode, updated once for each four fullsteps to compensate for variation in motor construction, highest accuracy. |
| 15 | 0 | Reserved | |
| 14 | SGT6 | stallGuard2 threshold value | The stallGuard2 threshold value controls the optimum measurement range for readout and stall indicator output (SG_TST). A lower value results in a higher sensitivity and less torque is required to indicate a stall. The value is a two's complement signed integer. Values below -10 are not recommended. Range: -64 to +63 |
| 13 | SGT5 | | |
| 12 | SGT4 | | |
| 11 | SGT3 | | |
| 10 | SGT2 | | |
| 9 | SGT1 | | |
| 8 | SGT0 | | |
| 7 | 0 | Reserved | |
| 6 | 0 | Reserved | |
| 5 | 0 | Reserved | |
| 4 | CS4 | Current scale (scales digital currents A and B) | Current scaling for SPI and STEP/DIR operation. %00000 … %11111: 1/32, 2/32, 3/32, … 32/32 This value is biased by 1 and divided by 32, so the range is 1/32 to 32/32. Example: CS=20 is 21/32 current. |
| 3 | CS3 | | |
| 2 | CS2 | | |
| 1 | CS1 | | |
| 0 | CS0 | | |

## 6.9   Driver Control Register (DRVCONF)

| DRVCONF | | Driver Configuration | |
|---|---|---|---|
| Bit | Name | Function | Comment |
| 19 | 1 | Register address bit | |
| 18 | 1 | Register address bit | |
| 17 | 1 | Register address bit | |
| 16 | TST | Reserved TEST mode | Must be cleared for normal operation. When set, the SG_TST output exposes digital test values, and the TEST_ANA output exposes analog test values. Test value selection is controlled by SGT1 and SGT0:<br>TEST_ANA:      %00: anatest_2vth,<br>                       %01: anatest_dac_out,<br>                       %10: anatest_vdd_half.<br>SG_TST:          %00: comp_A,<br>                       %01: comp_B,<br>                       %10: CLK,<br>                       %11: on_state_xy |
| 15 | SLPH1 | Slope control, high side | %00: Minimum<br>%01: Minimum temperature compensation mode.<br>%10: Medium temperature compensation mode.<br>%11: Maximum<br>In temperature compensated mode (tc), the MOSFET gate driver strength is increased if the overtemperature warning temperature is reached. This compensates for temperature dependency of high-side slope control. |
| 14 | SLPH0 | | |
| 13 | SLPL1 | Slope   control,   low side | %00: Minimum.<br>%01: Minimum.<br>%10: Medium.<br>%11: Maximum. |
| 12 | SLPL0 | | |
| 11 | 0 | Reserved | |
| 10 | DISS2G | Short to GND protection disable | 0: Short to GND protection is enabled.<br>1: Short to GND protection is disabled. |
| 9 | TS2G1 | Short to GND detection timer | %00: 3.2µs.<br>%01: 1.6µs.<br>%10: 1.2µs.<br>%11: 0.8µs. |
| 8 | TS2G0 | | |
| 7 | SDOFF | STEP/DIR interface disable | 0: Enable STEP/DIR operation.<br>1: Disable STEP/DIR operation. SPI interface is used to move motor. |
| 6 | VSENSE | Sense resistor voltage-based current scaling | 0: Full-scale sense resistor voltage is 305mV.<br>1: Full-scale sense resistor voltage is 165mV.<br>(Full-scale refers to a current setting of 31 and a DAC value of 255.) |
| 5 | RDSEL1 | Select value for read out (RD bits) | %00 | Microstep position read back |
| 4 | RDSEL0 | | %01 | stallGuard2 level read back |
| | | | %10 | stallGuard2 and coolStep current level read back |
| | | | %11 | Reserved, do not use |
| 3 | 0 | Reserved | |
| 2 | 0 | Reserved | |
| 1 | 0 | Reserved | |
| 0 | 0 | Reserved | |

## 6.10 Read Response

For every write command sent to the motor driver, a 20-bit response is returned to the motion controller. The response has one of three formats, as selected by the RDSEL parameter in the DRVCONF register. The table below shows these formats. Software must not depend on the value of any bit shown as reserved.

| DRVSTATUS | | | | Read Response | |
|---|---|---|---|---|---|
| Bit | Name | | | Function | Comment |
| | RDSEL=%00 | %01 | %10 | | |
| 19 | MSTEP9 | SG9 | SG9 | Microstep counter for coil A *or* stallGuard2 value SG9:0 *or* stallGuard2 value SG9:5 *and* coolStep value SE4:0 | Microstep position in sine table for coil A in STEP/DIR mode. MSTEP9 is the Polarity bit: 0:   Current flows from OA1 pins to OA2 pins. 1:   Current flows from OA2 pins to OA1 pins. |
| 18 | MSTEP8 | SG8 | SG8 | | |
| 17 | MSTEP7 | SG7 | SG7 | | |
| 16 | MSTEP6 | SG6 | SG6 | | |
| 15 | MSTEP5 | SG5 | SG5 | | stallGuard2 value SG9:0. |
| 14 | MSTEP4 | SG4 | SE4 | | |
| 13 | MSTEP3 | SG3 | SE3 | | |
| 12 | MSTEP2 | SG2 | SE2 | | stallGuard2 value SG9:5 and the actual coolStep scaling value SE4:0. |
| 11 | MSTEP1 | SG1 | SE1 | | |
| 10 | MSTEP0 | SG0 | SE0 | | |
| 9 | Reserved | | | | |
| 8 | Reserved | | | | |
| 7 | STST | | | Standstill indicator | 0:   No standstill condition detected. 1:   No active edge occurred on the STEP input during the last $2^{20}$ system clock cycles. |
| 6 | OLB | | | Open load indicator | 0:   No open load condition detected. 1:   No chopper event has happened during the last period with constant coil polarity. Only a current above 1/16 of the maximum setting can clear this bit! *Hint:* This bit is only a status indicator. The chip takes no other action when this bit is set. False indications may occur during fast motion and at standstill. Check this bit only during slow motion. |
| 5 | OLA | | | | |
| 4 | S2GB | | | Short to GND detection bits on high-side transistors | 0:   No short to ground shutdown condition. 1:   Short to ground shutdown condition. The short counter is incremented by each short circuit and the chopper cycle is suspended. The counter is decremented for each phase polarity change. The MOSFETs are shut off when the counter reaches 3 and remain shut off until the shutdown condition is cleared by disabling and re-enabling the driver. The shutdown condition becomes reset by deasserting the ENN input or clearing the TOFF parameter. |
| 3 | S2GA | | | | |
| 2 | OTPW | | | Overtemperature warning | 0:   No overtemperature warning condition. 1:   Warning threshold is active. |
| 1 | OT | | | Overtemperature shutdown | 0:   No overtemperature shutdown condition. 1:   Overtemperature shutdown has occurred. |
| 0 | SG | | | stallGuard2 status | 0:   No motor stall detected. 1:   stallGuard2 threshold has been reached, and the SG_TST output is driven high. |