imall

Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from, Europe, America and south Asia, supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of "Quality Parts, Customers Priority, Honest Operation, and Considerate Service", our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip, ALPS, ROHM, Xilinx, Pulse, ON, Everlight and Freescale. Main products comprise IC, Modules, Potentiometer, IC Socket, Relay, Connector. Our parts cover such applications as commercial, industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



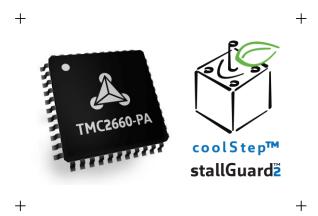
Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832 Email & Skype: info@chipsmall.com Web: www.chipsmall.com Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



TMC2660 DATASHEET

Universal, cost-effective stepper driver for two-phase bipolar motors with state-of-the-art features. Integrated MOSFETs for up to 4 A motor current per coil. With Step/Dir Interface and SPI.



FEATURES AND BENEFITS

Drive Capability up to 4A motor current

Voltage up to 30V DC

Highest Resolution up to 256 microsteps per full step

Compact Size 10x10mm QFP-44 package

Low Power Dissipation, very low RDSON & synchronous rectification

EMI-optimized programmable slope

Protection & Diagnostics overcurrent, short to GND, overtemperature & undervoltage

stallGuard2[™] high precision sensorless motor load detection

coolStep[™] load dependent current control for energy savings up to 75%

microPlyer™ microstep interpolation for increased smoothness with coarse step inputs.

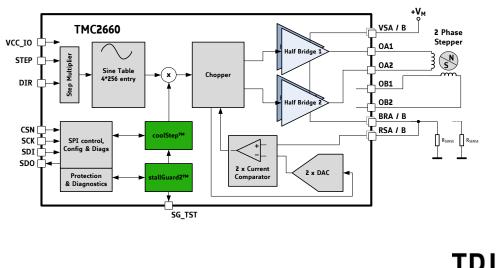
spreadCycle[™] high-precision chopper for best current sine wave form and zero crossing

1	A PPLICATIONS
	Textile, Sewing Machines Factory Automation Lab Automation Liquid Handling Medical Office Automation Printer and Scanner CCTV, Security ATM, Cash recycler POS
	Pumps and Valves Heliostat Controller CNC Machines
1.00	

DESCRIPTION

The TMC2660 driver for two-phase stepper motors offers an industry-leading feature set, including high-resolution microstepping, sensorless mechanical load measurement, load-adaptive power optimization, and low-resonance chopper operation. Standard SPI[™] and STEP/DIR interfaces simplify communication. Integrated power MOSFETs handle motor currents up to 2.2A RMS continuously or 2.8A RMS boost current per coil. Integrated protection and diagnostic features support robust and reliable operation. High integration, high energy efficiency and small form factor enable miniaturized designs with low external component count for cost-effective and highly competitive solutions.

AOTTON CONTROL



BLOCK DIAGRAM

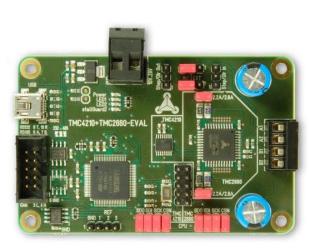
Hamburg, Germany

TRINAMIC Motion Control GmbH & Co. KG

APPLICATION EXAMPLES: SMALL SIZE – BEST PERFORMANCE

The TMC2660 scores with power density, integrated power MOSFETs, and a versatility that covers a wide spectrum of applications and motor sizes, all while keeping costs down. Extensive support at the chips, board, and software levels enables rapid design cycles and fast time-to-market with competitive products. High energy efficiency from TRINAMIC's coolStep technology delivers further cost savings in related systems such as power supplies and cooling.

TMC4210+TMC2660-EVAL EVALUATION-BOARD FOR 1 AXIS



Driver chain with TMC2660

This evaluation board is a development platform for applications based on the TMC2660. The board features USB and CAN interfaces for communication with control software running on a PC. The power MOSFETs of the TMC2660 support drive currents up to 2.8A RMS at 29V.

The control software provides a user-friendly GUI for setting control parameters and visualizing the dynamic response of the motor.

Motor movement can be controlled through the Step/Dir interface using inputs from an external source or signals generated by the onboard microcontroller acting as a step generator.

An external SPI motion controller can be connected if desired.

Order Codes

Order code	Description	Size
TMC2660-PA	coolStep™ driver with internal MOSFETs, up to 30V DC,	10 x 10 mm²
	QFP-44 with 12x12 pins	
TMC4210+2660-EVAL	Chipset evaluation board for TMC4210 and TMC2660.	55 x 85 mm ²

TABLE OF CONTENTS

1	PRINCIPLES OF OPERATION4
1.1 1.2 1.3 1.4	Key Concepts4 Control Interfaces5 Mechanical Load Sensing5 Current Control5
2	PIN ASSIGNMENTS6
2.1 2.2	Package Outline6 Signal Descriptions6
3	INTERNAL ARCHITECTURE8
4	STALLGUARD2 LOAD MEASUREMENT9
4.1 4.2 4.3	TUNING THE STALLGUARD2 THRESHOLD10 STALLGUARD2 MEASUREMENT FREQUENCY AND FILTERING
4.4	LIMITS OF STALLGUARD2 OPERATION11
5	COOLSTEP CURRENT CONTROL12
5.1	TUNING COOLSTEP14
6	SPI INTERFACE15
6.1 6.2 6.3 6.4 6.5 6.6	Bus Signals
	20
6.7 6.8 6.9 6.10 6.11	COOLSTEP CONTROL REGISTER (SMARTEN)21 STALLGUARD2 CONTROL REGISTER (SGCSCONF)
6.8 6.9 6.10	COOLSTEP CONTROL REGISTER (SMARTEN)21 STALLGUARD2 CONTROL REGISTER (SGCSCONF)
6.8 6.9 6.10 6.11	COOLSTEP CONTROL REGISTER (SMARTEN)21 STALLGUARD2 CONTROL REGISTER (SGCSCONF)
6.8 6.9 6.10 6.11 7 7 7.1 7.2 7.3 7.4	COOLSTEP CONTROL REGISTER (SMARTEN)21 STALLGUARD2 CONTROL REGISTER (SGCSCONF)
6.8 6.9 6.10 6.11 7 7 7.1 7.2 7.3 7.4 7.5	COOLSTEP CONTROL REGISTER (SMARTEN)21 STALLGUARD2 CONTROL REGISTER (SGCSCONF)
6.8 6.9 6.10 6.11 7 7 7.1 7.2 7.3 7.4 7.5 8	COOLSTEP CONTROL REGISTER (SMARTEN)21STALLGUARD2 CONTROL REGISTER(SGCSCONF)22DRIVER CONTROL REGISTER (DRVCONF)23READ RESPONSE24DEVICE INITIALIZATION25STEP/DIR INTERFACE26MICROSTEP TABLE27CHANGING RESOLUTION28MICROPLYER STEP INTERPOLATOR29CURRENT SETTING30
6.8 6.9 6.10 6.11 7 7 7.1 7.2 7.3 7.4 7.5 8 8 8.1	COOLSTEP CONTROL REGISTER (SMARTEN)21STALLGUARD2 CONTROL REGISTER(SGCSCONF)22DRIVER CONTROL REGISTER (DRVCONF)23READ RESPONSE24DEVICE INITIALIZATION25STEP/DIR INTERFACE26TIMING26MICROSTEP TABLE27CHANGING RESOLUTION28MICROPLYER STEP INTERPOLATOR29CURRENT SETTING30SENSE RESISTORS31CHOPPER OPERATION32SPREADCYCLE MODE33CONSTANT OFF-TIME MODE
6.8 6.9 6.10 6.11 7 7 7.1 7.2 7.3 7.4 7.5 8 8.1 9 9.1	COOLSTEP CONTROL REGISTER (SMARTEN)21STALLGUARD2 CONTROL REGISTER(SGCSCONF)22DRIVER CONTROL REGISTER (DRVCONF)23READ RESPONSE24DEVICE INITIALIZATION25STEP/DIR INTERFACE26TIMING27CHANGING RESOLUTION28MICROPLYER STEP INTERPOLATOR28STANDSTILL CURRENT REDUCTION29CURRENT SETTING30SENSE RESISTORS31CHOPPER OPERATION32SPREADCYCLE MODE33
6.8 6.9 6.10 6.11 7 7 7.1 7.2 7.3 7.4 7.5 8 8.1 9 9.1 9.2	COOLSTEP CONTROL REGISTER (SMARTEN)21STALLGUARD2 CONTROL REGISTER(SGCSCONF)22DRIVER CONTROL REGISTER (DRVCONF)23READ RESPONSE24DEVICE INITIALIZATION25STEP/DIR INTERFACE26TIMING26MICROSTEP TABLE27CHANGING RESOLUTION28MICROPLYER STEP INTERPOLATOR29CURRENT SETTING30SENSE RESISTORS31CHOPPER OPERATION32SPREADCYCLE MODE33CONSTANT OFF-TIME MODE
6.8 6.9 6.10 6.11 7 7 7.1 7.2 7.3 7.4 7.5 8 8.1 9 9.1 9.2 10 10.1	COOLSTEP CONTROL REGISTER (SMARTEN)21STALLGUARD2 CONTROL REGISTER(SGCSCONF)22DRIVER CONTROL REGISTER (DRVCONF)23READ RESPONSE24DEVICE INITIALIZATION25STEP/DIR INTERFACE26TIMINGMICROSTEP TABLE27CHANGING RESOLUTION28MICROPLYER STEP INTERPOLATOR28STANDSTILL CURRENT REDUCTION29CURRENT SETTING30SENSE RESISTORS31CHOPPER OPERATION32SPREADCYCLE MODE33CONSTANT OFF-TIME MODE37BREAK-BEFORE-MAKE LOGIC37

11.2	OPEN-LOAD DETECTION	39
11.3	OVERTEMPERATURE DETECTION	39
11.4	UNDERVOLTAGE DETECTION	40
12	POWER SUPPLY SEQUENCING	41
13	SYSTEM CLOCK	41
13.1	FREQUENCY SELECTION	42
14	LAYOUT CONSIDERATIONS	43
14.1	Sense Resistors	43
14.2	POWER MOSFET OUTPUTS	43
14.3	POWER SUPPLY PINS	43
14.4	Power Filtering	43
14.5	LAYOUT EXAMPLE	44
15	ABSOLUTE MAXIMUM RATINGS.	45
16	ELECTRICAL CHARACTERISTICS.	46
16 16.1	ELECTRICAL CHARACTERISTICS.	
		46
16.1	Operational Range	46 46
16.1 16.2	OPERATIONAL RANGE DC AND AC SPECIFICATIONS	46 46 49
16.1 16.2 16.3	OPERATIONAL RANGE DC and AC Specifications Thermal Characteristics	46 46 49 50
16.1 16.2 16.3 17	OPERATIONAL RANGE DC AND AC SPECIFICATIONS THERMAL CHARACTERISTICS PACKAGE MECHANICAL DATA	46 46 49 50
16.1 16.2 16.3 17 17.1	OPERATIONAL RANGE DC AND AC SPECIFICATIONS THERMAL CHARACTERISTICS PACKAGE MECHANICAL DATA DIMENSIONAL DRAWINGS	46 46 50 50 50
16.1 16.2 16.3 17 17.1 17.2	OPERATIONAL RANGE DC AND AC SPECIFICATIONS THERMAL CHARACTERISTICS PACKAGE MECHANICAL DATA DIMENSIONAL DRAWINGS PACKAGE CODE	46 46 50 50 50
16.1 16.2 16.3 17 17.1 17.2 18	OPERATIONAL RANGE DC AND AC SPECIFICATIONS THERMAL CHARACTERISTICS PACKAGE MECHANICAL DATA DIMENSIONAL DRAWINGS PACKAGE CODE DISCLAIMER	46 49 50 50 51 51

1 Principles of Operation

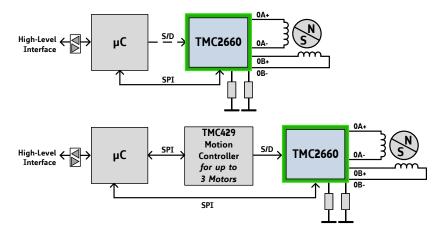


Figure 1.1 Block diagram: applications

The TMC2660 motor driver chip with included MOSFETs is the intelligence and power between a motion controller and the two phase stepper motor as shown in Figure 1.1. Following power-up, an embedded microcontroller initializes the driver by sending commands over an SPI bus to write control parameters and mode bits in the TMC2660. The microcontroller may implement the motion-control function as shown in the upper part of the figure, or it may send commands to a dedicated motion controller chip such as TRINAMIC's TMC429 as shown in the lower part.

The motion controller can control the motor position by sending pulses on the STEP signal while indicating the direction on the DIR signal. The TMC2660 has a microstep counter and sine table to convert these signals into the coil currents which control the position of the motor. If the microcontroller implements the motion-control function, it can write values for the coil currents directly to the TMC2660 over the SPI interface, in which case the STEP/DIR interface may be disabled. This mode of operation requires software to track the motor position and reference a sine table to calculate the coil currents.

To optimize power consumption and heat dissipation, software may also adjust coolStep and stallGuard2 parameters in real-time, for example to implement different tradeoffs between speed and power consumption in different modes of operation.

The motion control function is a hard real-time task which may be a burden to implement reliably alongside other tasks on the embedded microcontroller. By offloading the motion-control function to the TMC429, up to three motors can be operated reliably with very little demand for service from the microcontroller. Software only needs to send target positions, and the TMC429 generates precisely timed step pulses. Software retains full control over both the TMC2660 and TMC429 through the SPI bus.

1.1 Key Concepts

The TMC2660 motor driver implements several advanced features which are exclusive to TRINAMIC products. These features contribute toward greater precision, greater energy efficiency, higher reliability, smoother motion, and cooler operation in many stepper motor applications.

stallGuard2™	High-precision load measurement using the back EMF on the coils		
coolStep™	Load-adaptive current control which reduces energy consumption by as much as 75%		
spreadCycle™	High-precision chopper algorithm available as an alternative to the traditional constant off-time algorithm		
microPlyer™	Microstep interpolator for obtaining increased smoothness of microstepping over a STEP/DIR interface		

In addition to these performance enhancements, TRINAMIC motor drivers also offer safeguards to detect and protect against shorted outputs, open-circuit output, overtemperature, and undervoltage conditions for enhancing safety and recovery from equipment malfunctions.

1.2 Control Interfaces

There are two control interfaces from the motion controller to the motor driver: the SPI serial interface and the STEP/DIR interface. The SPI interface is used to write control information to the chip and read back status information. This interface must be used to initialize parameters and modes necessary to enable driving the motor. This interface may also be used for directly setting the currents flowing through the motor coils, as an alternative to stepping the motor using the STEP and DIR signals, so the motor can be controlled through the SPI interface alone.

The STEP/DIR interface is a traditional motor control interface available for adapting existing designs to use TRINAMIC motor drivers. Using only the SPI interface requires slightly more CPU overhead to look up the sine tables and send out new current values for the coils.

1.2.1 SPI Interface

The SPI interface is a bit-serial interface synchronous to a bus clock. For every bit sent from the bus master to the bus slave, another bit is sent simultaneously from the slave to the master. Communication between an SPI master and the TMC2660 slave always consists of sending one 20-bit command word and receiving one 20-bit status word.

The SPI command rate typically corresponds to the microstep rate at low velocities. At high velocities, the rate may be limited by CPU bandwidth to 10-100 thousand commands per second, so the application may need to change to fullstep resolution.

1.2.2 STEP/DIR Interface

The STEP/DIR interface is enabled by default. Active edges on the STEP input can be rising edges or both rising and falling edges, as controlled by another mode bit (DEDGE). Using both edges cuts the toggle rate of the STEP signal in half, which is useful for communication over slow interfaces such as optically isolated interfaces.

On each active edge, the state sampled from the DIR input determines whether to step forward or back. Each step can be a fullstep or a microstep, in which there are 2, 4, 8, 16, 32, 64, 128, or 256 microsteps per fullstep. During microstepping, a step impulse with a low state on DIR increases the microstep counter and a high decreases the counter by an amount controlled by the microstep resolution. An internal table translates the counter value into the sine and cosine values which control the motor current for microstepping.

1.3 Mechanical Load Sensing

The TMC2660 provides stallGuard2 high-resolution load measurement for determining the mechanical load on the motor by measuring the back EMF. In addition to detecting when a motor stalls, this feature can be used for homing to a mechanical stop without a limit switch or proximity detector. The coolStep power-saving mechanism uses stallGuard2 to reduce the motor current to the minimum motor current required to meet the actual load placed on the motor.

1.4 Current Control

Current into the motor coils is controlled using a cycle-by-cycle chopper mode. Two chopper modes are available: a traditional constant off-time mode and the new spreadCycle mode. spreadCycle mode offers smoother operation and greater power efficiency over a wide range of speed and load.

2 Pin Assignments

2.1 Package Outline

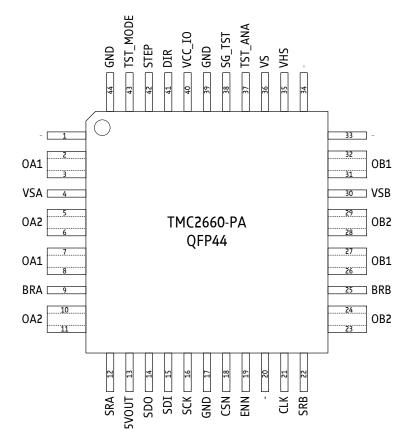


Figure 2.1 TMC2660 pin assignment

2.2 Signal Descriptions

Pin	Number	Туре	Function
0A1	2, 3	0 (VS)	Bridge A1 output. Interconnect all of these pins using thick traces
	7, 8		capable to carry the motor current and distribute heat into the PCB.
OA2	5, 6	0 (VS)	Bridge A2 output. Interconnect all of these pins using thick traces
	10, 11		capable to carry the motor current and distribute heat into the PCB.
OB1	26, 27	0 (VS)	Bridge B1 output. Interconnect all of these pins using thick traces
	31, 32		capable to carry the motor current and distribute heat into the PCB.
OB2	23, 24	0 (VS)	Bridge B2 output. Interconnect all of these pins using thick traces
	28, 29		capable to carry the motor current and distribute heat into the PCB.
VSA	4		Bridge A/B positive power supply. Connect to VS and provide
VSB	30		sufficient filtering capacity for chopper current ripple.
BRA	9	AI	Bridge A/B negative power supply via sense resistor in bridge foot
BRB	25		point.
SRA	12	AI	Sense resistor inputs for chopper current regulation.
SRB	22		
5VOUT	13		Output of the on-chip 5V linear regulator. This voltage is used to
			supply the low-side MOSFETs and internal analog circuitry. An
			external capacitor to GND close to the pin is required. Place the
			capacitor near pins 13 and 17. A 470nF ceramic capacitor is
			sufficient.
SDO	14	DO VIO	SPI serial data output.

Pin	Number	Туре	Function	
SDI	15	DI VIO	SPI serial data input.	
			(Scan test input in test mode.)	
SCK	16	DI VIO	Serial clock input of SPI interface.	
			(Scan test shift enable input in test mode.)	
GND	17, 39,		Digital and analog low power GND.	
	44			
CSN	18	DI VIO	Chip select input for the SPI interface. (Active low.)	
ENN	19	DI VIO	Power MOSFET enable input. All MOSFETs are switched off when disabled. (Active low.)	
CLK	21	DI VIO	System clock input for all internal operations. Tie low to use the on-chip oscillator. A high signal disables the on-chip oscillator until power down.	
VHS	35		High-side supply voltage (motor supply voltage - 10V)	
VS	36		Motor supply voltage	
TST_ANA	37	AO VIO	Reserved. Do not connect.	
SG_TST	38	DO VIO	stallGuard2 output. Signals a motor stall. (Active high.)	
VCC_IO	40		Input/output supply voltage VIO for all digital pins. Tie to digital logic supply voltage. Operation is allowed in 3.3V and 5V systems.	
DIR	41	DI VIO	Direction input. Sampled on an active edge of the STEP input to determine stepping direction. Sampling a low increases the microstep counter, while sampling a high decreases the counter. A 60-ns internal glitch filter rejects short pulses on this input.	
STEP	42	DI VIO	Step input. Active edges can be rising or both rising and falling, as controlled by the DEDGE mode bit. A 60-ns internal glitch filter rejects short pulses on this input.	
TST_MODE	43	DI VIO	Test mode input. Puts IC into test mode. Tie to GND for normal operation.	
n.c.	1, 33		No internal connection - can be tied to any net, e.g., in order to improve power routing to pins VSA and VSB.	

3 Internal Architecture

Figure 3.1 shows the internal architecture of TMC2660.

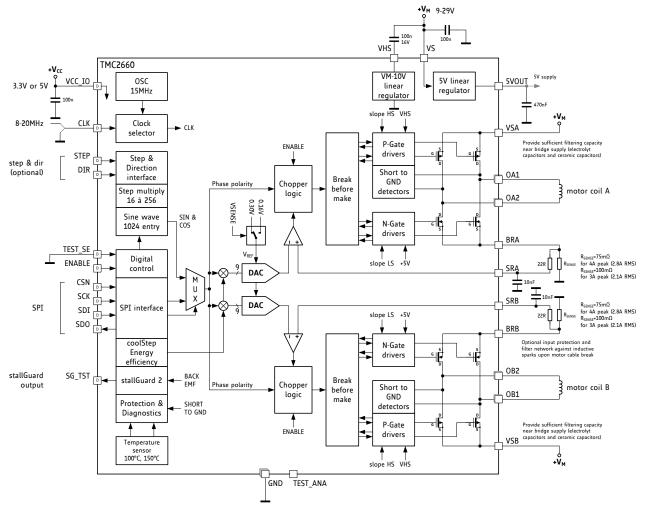


Figure 3.1 TMC2660 block diagram

PROMINENT FEATURES INCLUDE:

Oscillator and clock selector	provide the system clock from the on-chip oscillator or an external source.
Step and direction interface	uses a microstep counter and sine table to generate target currents for the coils.
SPI interface	receives commands that directly set the coil current values.
Multiplexer	selects either the output of the sine table or the SPI interface for controlling the current into the motor coils.
Multipliers	scale down the currents to both coils when the currents are greater than those required by the load on the motor or as set by the CS current scale parameter.
DACs and comparators	convert the digital current values to analog signals that are compared with the voltages on the sense resistors. Comparator outputs terminate chopper drive phases when target currents are reached.
Break-before-make and gate drivers	ensure non-overlapping pulses, boost pulse voltage, and control pulse slope to the gates of the power MOSFETs.
On-chip voltage regulators	provide high-side voltage for P-channel MOSFET gate drivers and supply voltage for on-chip analog and digital circuits.

4 stallGuard2 Load Measurement

stallGuard2 provides an accurate measurement of the load on the motor. It can be used for stall detection as well as other uses at loads below those which stall the motor, such as coolStep load-adaptive current reduction. (stallGuard2 is a more precise evolution of the earlier stallGuard technology.)

The stallGuard2 measurement value changes linearly over a wide range of load, velocity, and current settings, as shown in Figure 4.1. At maximum motor load, the value goes to zero or near to zero. This corresponds to a load angle of 90° between the magnetic field of the coils and magnets in the rotor. This also is the most energy-efficient point of operation for the motor.

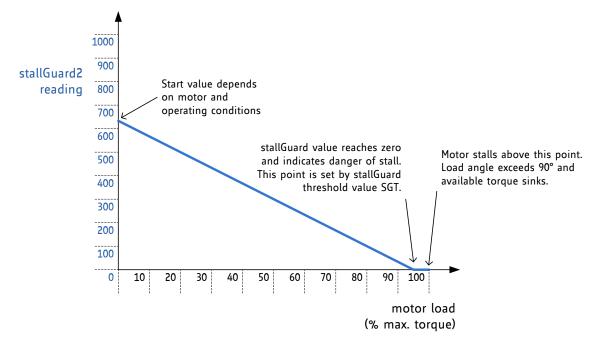


Figure 4.1 stallGuard2 load measurement SG as a function of load

Parameter	Description	Setting	Comment
SGT	7-bit signed integer that sets the stallGuard2 threshold level for asserting the SG_TST output and sets the optimum measurement range for	0	indifferent value
		+1 +63	less sensitivity
	readout. Negative values increase sensitivity, and positive values reduce sensitivity so more torque is required to indicate a stall. Zero is a good starting value. Operating at values below -10 is not recommended.	-164	higher sensitivity
SFILT	Mode bit which enables the stallGuard2 filter for	0	standard mode
	more precision. If set, reduces the measurement frequency to one measurement per four fullsteps. If cleared, no filtering is performed. Filtering compensates for mechanical asymmetries in the construction of the motor, but at the expense of response time. Unfiltered operation is recommended for rapid stall detection. Filtered operation is recommended for more precise load measurement.	1	filtered mode

Two parameters control stallGuard2 and one status value is returned.

Status word	Description	Range	Comment
SG	10-bit unsigned integer stallGuard2 measurement value. A higher value indicates lower mechanical load. A lower value indicates a higher load and therefore a higher load angle. For stall detection, adjust SGT to return an SG value of 0 or slightly higher upon maximum motor load before stall.	0 1023	0: highest load low value: high load high value: less load

4.1 Tuning the stallGuard2 Threshold

Due to the dependency of the stallGuard2 value SG from motor-specific characteristics and applicationspecific demands on load and velocity the easiest way to tune the stallGuard2 threshold *SGT* for a specific motor type and operating conditions is interactive tuning in the actual application.

The procedure is:

- 1. Operate the motor at a reasonable velocity for your application and monitor SG.
- 2. Apply slowly increasing mechanical load to the motor. If the motor stalls before SG reaches zero, decrease SGT. If SG reaches zero before the motor stalls, increase SGT. A good SGT starting value is zero. SGT is signed, so it can have negative or positive values.
- 3. The optimum setting is reached when SG is between 0 and 400 at increasing load shortly before the motor stalls, and SG increases by 100 or more without load. SGT in most cases can be tuned together with the motion velocity in a way that SG goes to zero when the motor stalls and the stall output SG_TST is asserted. This indicates that a step has been lost.

The system clock frequency affects SG. An external crystal-stabilized clock should be used for applications that demand the highest precision. The power supply voltage also affects SG, so tighter regulation results in more accurate values. SG measurement has a high resolution, and there are a few ways to enhance its accuracy, as described in the following sections.

4.1.1 Variable Velocity Operation

Across a range of velocities, on-the-fly adjustment of the stallGuard2 threshold SGT improves the accuracy of the load measurement SG. This also improves the power reduction provided by coolStep, which is driven by SG. Linear interpolation between two SGT values optimized at different velocities is a simple algorithm for obtaining most of the benefits of on-the-fly SGT adjustment, as shown in Figure 4.2. An optimal SGT curve in black and a two-point interpolated SGT curve in red are shown.

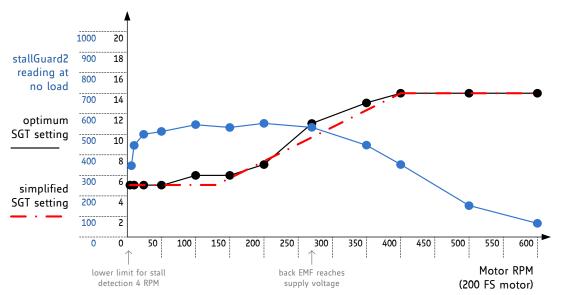


Figure 4.2 Linear interpolation for optimizing SGT with changes in velocity.

4.1.2 Small Motors with High Torque Ripple and Resonance

Motors with a high detent torque show an increased variation of the stallGuard2 measurement value SG with varying motor currents, especially at low currents. For these motors, the current dependency might need correction in a similar manner to velocity correction for obtaining the highest accuracy.

4.1.3 Temperature Dependence of Motor Coil Resistance

Motors working over a wide temperature range may require temperature correction, because motor coil resistance increases with rising temperature. This can be corrected as a linear reduction of SG at increasing temperature, as motor efficiency is reduced.

4.1.4 Accuracy and Reproducibility of stallGuard2 Measurement

In a production environment, it may be desirable to use a fixed SGT value within an application for one motor type. Most of the unit-to-unit variation in stallGuard2 measurements results from manufacturing tolerances in motor construction. The measurement error of stallGuard2 – provided that all other parameters remain stable – can be as low as:

stallGuard measurement error = $\pm max(1, |SGT|)$

4.2 stallGuard2 Measurement Frequency and Filtering

The stallGuard2 measurement value SG is updated with each full step of the motor. This is enough to safely detect a stall, because a stall always means the loss of four full steps. In a practical application, especially when using coolStep, a more precise measurement might be more important than an update for each fullstep because the mechanical load never changes instantaneously from one step to the next. For these applications, the SFILT bit enables a filtering function over four load measurements. The filter should always be enabled when high-precision measurement is required. It compensates for variations in motor construction, for example due to misalignment of the phase A to phase B magnets. The filter should only be disabled when rapid response to increasing load is required, such as for stall detection at high velocity.

4.3 Detecting a Motor Stall

To safely detect a motor stall, a stall threshold must be determined using a specific SGT setting. Therefore, you need to determine the maximum load the motor can drive without stalling and to monitor the SG value at this load, for example some value within the range 0 to 400. The stall threshold should be a value safely within the operating limits, to allow for parameter stray. So, your microcontroller software should set a stall threshold which is slightly higher than the minimum value seen before an actual motor stall occurs. The response at an SGT setting at or near 0 gives some idea on the quality of the signal: Check the SG value without load and with maximum load. These values should show a difference of at least 100 or a few 100, which shall be large compared to the offset. If you set the SGT value so that a reading of 0 occurs at maximum motor load, an active high stall output signal will be available at SG_TST output.

4.4 Limits of stallGuard2 Operation

stallGuard2 does not operate reliably at extreme motor velocities: Very low motor velocities (for many motors, less than one revolution per second) generate a low back EMF and make the measurement unstable and dependent on environment conditions (temperature, etc.). Other conditions will also lead to extreme settings of SGT and poor response of the measurement value SG to the motor load.

Very high motor velocities, in which the full sinusoidal current is not driven into the motor coils also lead to poor response. These velocities are typically characterized by the motor back EMF reaching the supply voltage.

5 coolStep Current Control

coolStep allows substantial energy savings, especially for motors which see varying loads or operate at a high duty cycle. Because a stepper motor application needs to work with a torque reserve of 30% to 50%, even a constant-load application allows significant energy savings because coolStep automatically enables torque reserve when required. Reducing power consumption keeps the system cooler, increases motor life, and allows reducing cost in the power supply and cooling components.

Reducing motor current by half results in reducing power by a factor of four.

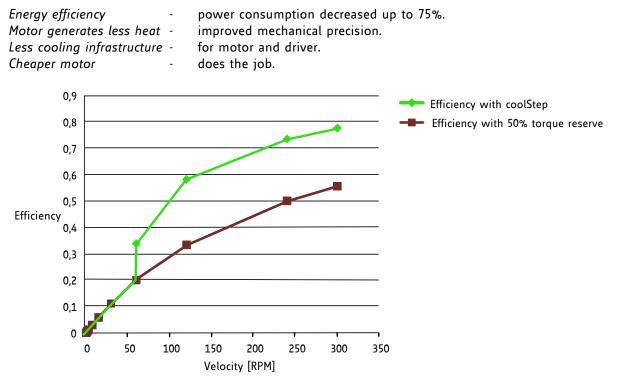


Figure 5.1 Energy efficiency example with coolStep

Figure 5.1 shows the efficiency gain of a 42mm stepper motor when using coolStep compared to standard operation with 50% of torque reserve. coolStep is enabled above 60rpm in the example.

coolStep is controlled by several parameters, but two are critical for understanding how it works:

Parameter	Description	Range	Comment
SEMIN	4-bit unsigned integer that sets a lower threshold. If SG goes below this threshold, coolStep increases the current to both coils. The 4-bit SEMIN value is scaled by 32 to cover the lower half of the range of the 10-bit SG value. (The name of this parameter is derived from smartEnergy, which is an earlier name for coolStep.)		lower coolStep threshold: SEMINx32
SEMAX	4-bit unsigned integer that controls an upper threshold. If SG is sampled equal to or above this threshold enough times, coolStep decreases the current to both coils. The upper threshold is (SEMIN + SEMAX + 1) x 32.	0 15	upper coolStep threshold: (SEMIN+SEMAX+1)x32

Figure 5.2 shows the operating regions of coolStep. The black line represents the SG measurement value, the blue line represents the mechanical load applied to the motor, and the red line represents the current into the motor coils. When the load increases, SG falls below SEMIN, and coolStep

increases the current. When the load decreases and SG rises above (SEMIN + SEMAX + 1) x 32 the current becomes reduced.

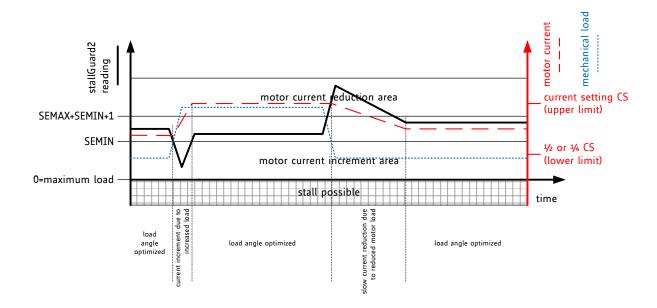


Figure 5.2 coolStep adapts motor current to the load.

Four more parameters control coolStep and one status value is returned:					
Parameter	Description	Range	Comment		
CS	Current scale. Scales both coil current values as taken from the internal sine wave table or from the SPI interface. For high precision motor operation, work with a current scaling factor in the range 16 to 31, because scaling down the current values reduces the effective microstep resolution by making microsteps coarser. This setting also controls the maximum current value set by coolStep [™] .		scaling factor: 1/32, 2/32, 32/32		
SEUP	Number of increments of the coil current for each occurrence of an SG measurement below the lower threshold.		step width is: 1, 2, 4, 8		
SEDN	Number of occurrences of SG measurements above the upper threshold before the coil current is decremented.	0 3	number of stallGuard measurements per decrement: 32, 8, 2, 1		
SEIMIN	Mode bit that controls the lower limit for scaling the coil current. If the bit is set, the limit is 1/4 CS. If the bit is clear, the limit is 1/2 CS.		Minimum motor current: 1/2 of CS		
Status word	Description	1 Range	1/4 of CS Comment		
SE	5-bit unsigned integer reporting the actual current scaling value determined by coolStep. This value is biased by 1 and divided by 32, so the range is 1/32 to 32/32. The value will not be greater than the value of CS or lower than either 1/4 CS or 1/2 CS depending on the setting of SEIMIN.	0 31	Actual motor current scaling factor set by coolStep: 1/32, 2/32, 32/32		

5.1 Tuning coolStep

Before tuning coolStep, first tune the stallGuard2 threshold level SGT, which affects the range of the load measurement value SG. coolStep uses SG to operate the motor near the optimum load angle of +90°.

The current increment speed is specified in SEUP, and the current decrement speed is specified in SEDN. They can be tuned separately because they are triggered by different events that may need different responses. The encodings for these parameters allow the coil currents to be increased much more quickly than decreased, because crossing the lower threshold is a more serious event that may require a faster response. If the response is too slow, the motor may stall. In contrast, a slow response to crossing the upper threshold does not risk anything more serious than missing an opportunity to save power.

coolStep operates between limits controlled by the current scale parameter CS and the SEIMIN bit.

5.1.1 Response Time

For fast response to increasing motor load, use a high current increment step SEUP. If the motor load changes slowly, a lower current increment step can be used to avoid motor current oscillations. If the filter controlled by SFILT is enabled, the measurement rate and regulation speed are cut by a factor of four.

5.1.2 Low Velocity and Standby Operation

Because stallGuard2 is not able to measure the motor load in standstill and at very low RPM, the current at low velocities should be set to an application-specific default value and combined with standstill current reduction settings programmed through the SPI interface.

6 SPI Interface

TMC2660 requires setting configuration parameters and mode bits through the SPI interface before the motor can be driven. The SPI interface also allows reading back status values and bits.

6.1 Bus Signals

The SPI bus on the TMC2660 has four signals:

SCK	bus clock input
SDI	serial data input
C D O	

- SDO serial data output
- CSN chip select input (active low)

The slave is enabled for an SPI transaction by a low on the chip select input CSN. Bit transfer is synchronous to the bus clock SCK, with the slave latching the data from SDI on the rising edge of SCK and driving data to SDO following the falling edge. The most significant bit is sent first. A minimum of 20 SCK clock cycles is required for a bus transaction with the TMC2660.

If more than 20 clocks are driven, the additional bits shifted into SDI are shifted out on SDO after a 20-clock delay through an internal shift register. This can be used for daisy chaining multiple chips.

CSN must be low during the whole bus transaction. When CSN goes high, the contents of the internal shift register are latched into the internal control register and recognized as a command from the master to the slave. If more than 20 bits are sent, only the last 20 bits received before the rising edge of CSN are recognized as the command.

6.2 Bus Timing

SPI interface is synchronized to the internal system clock, which limits the SPI bus clock SCK to half of the system clock frequency. If the system clock is based on the on-chip oscillator, an additional 10% safety margin must be used to ensure reliable data transmission. All SPI inputs as well as the ENN input are internally filtered to avoid triggering on pulses shorter than 20ns. Figure 6.1 shows the timing parameters of an SPI bus transaction, and the table below specifies their values.

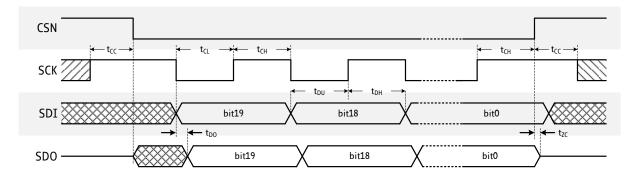


Figure 6.1 SPI Timing

SPI Interface Timing	AC-Characteristics							
SFI Interface finning	clock period is t _{CLK}							
Parameter	Symbol	Conditions	Min	Тур	Max	Unit		
SCK valid before or after change of CSN	t _{cc}		10			ns		
CSN high time	t _{csH}	^{*)} Min time is for synchronous CLK with SCK high one t __ before CSN high only	t _{clK}	>2t _{ськ} +10		ns		
SCK low time	t _{CL}	^{*)} Min time is for synchronous CLK only	t _{clk}	>t _{CLK} +10		ns		
SCK high time	t _{cH}	^{*)} Min time is for synchronous CLK only	t _{CLK}	>t _{CLK} +10		ns		
SCK frequency using internal clock	f _{sck}	Assumes minimum OSC frequency			4	MHz		
SCK frequency using external 16MHz clock	f _{scк}	Assumes synchronous CLK			8	MHz		
SDI setup time before rising edge of SCK	t _{DU}		10			ns		
SDI hold time after rising edge of SCK	t _{DH}		10			ns		
Data out valid time after falling SCK clock edge	t _{DO}	No capacitive load on SDO			t _{filt} +5	ns		
SDI, SCK, and CSN filter delay time	t _{FILT}	Rising and falling edge	12	20	30	ns		

6.3 Bus Architecture

SPI slaves can be chained and used with a single chip select line. If slaves are chained, they behave like a long shift register. For example, a chain of two motor drivers requires 40 bits to be sent. The last bits shifted to each register in the chain are loaded into an internal register on the rising edge of the CSN input. For example, 24 or 32 bits can be sent to a single motor driver, but it latches just the last 20 bits received before CSN goes high.

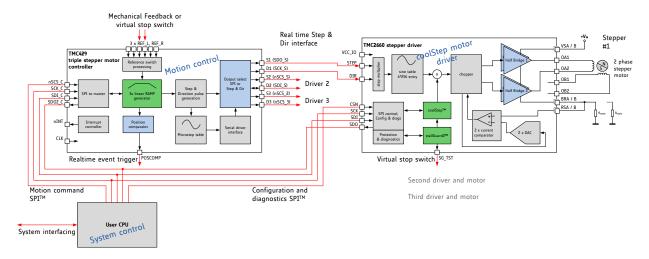


Figure 6.2 Interfaces to a TMC429 motion controller chip and a TMC2660 motor driver

Figure 6.2 shows the interfaces in a typical application. The SPI bus is used by an embedded MCU to initialize the control registers of both a motion controller and one or more motor drivers. STEP/DIR interfaces are used between the motion controller and the motor drivers.

6.4 Register Write Commands

An SPI bus transaction to the TMC2660 is a write command to one of the five write-only registers that hold configuration parameters and mode bits:

Register	Description
Driver Control Register (DRVCTRL)	The DRVCTRL register has different formats for controlling the interface to the motion controller depending on whether or not the STEP/DIR interface is enabled.
Chopper Configuration Register (CHOPCONF)	The CHOPCONF register holds chopper parameters and mode bits.
coolStep Configuration Register (SMARTEN)	The SMARTEN register holds coolStep parameters and a mode bit. (smartEnergy is an earlier name for coolStep.)
stallGuard2 Configuration Register (SGCSCONF)	The SGCSCONF register holds stallGuard2 parameters and a mode bit.
Driver Configuration Register (DRVCONF)	The DRVCONF register holds parameters and mode bits used to control the power MOSFETs and the protection circuitry. It also holds the SDOFF bit which controls the STEP/DIR interface and the RDSEL parameter which controls the contents of the response returned in an SPI transaction

In the following sections, multibit binary values are prefixed with a % sign, for example %0111.

6.4.1 Write Command Overview

The table below shows the formats for the five register write commands. Bits 19, 18, and sometimes 17 select the register being written, as shown in bold. The DRVCTRL register has two formats, as selected by the SDOFF bit. Bits shown as 0 must always be written as 0, and bits shown as 1 must always be written with 1. Detailed descriptions of each parameter and mode bit are given in the following sections.

Register/	DRVCTRL	DRVCTRL	CHOPCONF	SMARTEN	SGCSCONF	DRVCONF
Bit	(SDOFF=1)	(SDOFF=0)				
19	0	0	1	1	1	1
18	0	0	0	0	1	1
17	PHA	0	0	1	0	1
16	CA7	0	TBL1	0	SFILT	TST
15	CA6	0	TBL0	SEIMIN	0	SLPH1
14	CA5	0	СНМ	SEDN1	SGT6	SLPH0
13	CA4	0	RNDTF	SEDN0	SGT5	SLPL1
12	CA3	0	HDEC1	0	SGT4	SLPL0
11	CA2	0	HDEC0	SEMAX3	SGT3	0
10	CA1	0	HEND3	SEMAX2	SGT2	DISS2G
9	CA0	INTPOL	HEND2	SEMAX1	SGT1	TS2G1
8	PHB	DEDGE	HEND1	SEMAX0	SGT0	TS2G0
7	CB7	0	HEND0	0	0	SDOFF
6	CB6	0	HSTRT2	SEUP1	0	VSENSE
5	CB5	0	HSTRT1	SEUP0	0	RDSEL1
4	CB4	0	HSTRT0	0	CS4	RDSEL0
3	CB3	MRES3	TOFF3	SEMIN3	CS3	0
2	CB2	MRES2	TOFF2	SEMIN2	CS2	0
1	CB1	MRES1	TOFF1	SEMIN1	CS1	0
0	CB0	MRES0	TOFF0	SEMIN0	CS0	0

6.4.2 Read Response Overview

The table below shows the formats for the read response. The RDSEL parameter in the DRVCONF register selects the format of the read response.

Bit	RDSEL=%00	RDSEL=%01	RDSEL=%10		
19	MSTEP9	SG9	SG9		
18	MSTEP8	SG8	SG8		
17	MSTEP7	SG7	SG7		
16	MSTEP6	SG6	SG6		
15	MSTEP5	SG5	SG5		
14	MSTEP4	SG4	SE4		
13	MSTEP3	SG3	SE3		
12	MSTEP2	SG2	SE2		
11	MSTEP1	SG1	SE1		
10	MSTEP0	SG0	SE0		
9	-	-	-		
8	-	-	-		
7	STST				
6	OLB				
5	OLA				
4	S2GB				
3	S2GA				
2	OTPW				
1	OT				
0	SG				

6.5 Driver Control Register (DRVCTRL)

The format of the DRVCTRL register depends on the state of the SDOFF mode bit.

- *SPI Mode* SDOFF bit is set, the STEP/DIR interface is disabled, and DRVCTRL is the interface for specifying the currents through each coil.
- *STEP/DIR Mode* SDOFF bit is clear, the STEP/DIR interface is enabled, and DRVCTRL is a configuration register for the STEP/DIR interface.

DRVCTRL Driver Control in SPI M		Driver Control in SPI M	ode (SDOFF=1)
Bit	Name	Function	Comment
19	0	Register address bit	
18	0	Register address bit	
17	РНА	Polarity A	Sign of current flow through coil A: 0: Current flows from OA1 pins to OA2 pins. 1: Current flows from OA2 pins to OA1 pins.
16	CA7	Current A MSB	Magnitude of current flow through coil A. The range is
15	CA6		0 to 248, if hysteresis or offset are used up to their full
14	CA5		extent. The resulting value after applying hysteresis or
13	CA4		offset must not exceed 255.
12	CA3		
11	CA2		
10	CA1		
9	CA0	Current A LSB	

6.5.1 DRVCTRL Register in SPI Mode

DRVCTRL Driver Control in SPI Mode (SDOFF=1)			ode (SDOFF=1)
Bit	Name	Function	Comment
8	РНВ	Polarity B	Sign of current flow through coil B: 0: Current flows from OB1 pins to OB2 pins. 1: Current flows from OB2 pins to OB1 pins.
7	CB7	Current B MSB	Magnitude of current flow through coil B. The range is
6	CB6		0 to 248, if hysteresis or offset are used up to their full
5	CB5		extent. The resulting value after applying hysteresis or
4	CB4		offset must not exceed 255.
3	CB3		
2	CB2		
1	CB1		
0	CB0	Current B LSB	

6.5.2 DRVCTRL Register in STEP/DIR Mode

DRVCTRL		Driver Control in STEP/DIR Mode (SDOFF=0)		
Bit	Name	Function	Comment	
19	0	Register address bit		
18	0	Register address bit		
17	0	Reserved		
16	0	Reserved		
15	0	Reserved		
14	0	Reserved		
13	0	Reserved		
12	0	Reserved		
11	0	Reserved		
10	0	Reserved		
9	INTPOL	Enable STEP	0: Disable STEP pulse interpolation.	
		interpolation	1: Enable STEP pulse multiplication by 16.	
8	DEDGE	Enable double edge	0: Rising STEP pulse edge is active, falling edge is	
		STEP pulses	inactive.	
			1: Both rising and falling STEP pulse edges are active.	
7	0	Reserved		
6	0	Reserved		
5	0	Reserved		
4	0	Reserved		
3	MRES3	Microstep resolution	Microsteps per 90°:	
2	MRES2	for STEP/DIR mode	%0000: 256	
1	MRES1		%0001: 128	
0	MRES0		%0010: 64	
			%0011: 32	
			%0100: 16	
			%0101: 8	
			%0110: 4	
			%0111: 2 (halfstep)	
			%1000: 1 (fullstep)	

6.6 Chopper Control Register (CHOPCONF)

CHOR	PCONF	Chopper Configuration		
Bit	Name	Function	Commen	ıt
19	1	Register address bit		
18	0	Register address bit		
17	0	Register address bit		
16	TBL1	Blanking time	-	time interval, in system clock periods:
15	TBLO		%00:16	
			%01: 24	
			%10: 36 %11: 54	
14	СНМ	Chopper mode	This mod	de bit affects the interpretation of the HDEC, and HSTRT parameters shown below.
			0	Standard mode (spreadCycle)
			1	Constant t _{OFF} with fast decay time.
			-	Fast decay time is also terminated when the
				negative nominal current is reached. Fast
				decay is after on time.
13	RNDTF	Random TOFF time		andomizing the slow decay phase duration:
				er off time is fixed as set by bits $t_{\mbox{\scriptsize OFF}}$
				m mode, t _{OFF} is random modulated by 2 +3 clocks.
12	HDEC1	Hysteresis decrement	CHM=0	Hysteresis decrement period setting, in
11	HDECO	interval	CIII-0	system clock periods:
	HD LCO	or		%00: 16
		Fast decay mode		%01: 32
				%10: 48
				%11: 64
			CHM=1	HDEC1=0: current comparator can terminate
				the fast decay phase before timer expires.
				HDEC1=1: only the timer terminates the fast decay phase.
				HDECO: MSB of fast decay time setting.
10	HEND3	Hysteresis end (low)	CHM=0	%0000 %1111:
9	HEND2	value	••••••	Hysteresis is -3, -2, -1, 0, 1,, 12
		or		(1/512 of this setting adds to current setting)
		Sine wave offset		This is the hysteresis value which becomes
		-		used for the hysteresis chopper.
8	HEND1		CHM=1	%0000 %1111:
7	HEND0			Offset is -3, -2, -1, 0, 1,, 12 This is the sine ways offset and 1/512 of the
				This is the sine wave offset and 1/512 of the value becomes added to the absolute value
				of each sine wave entry.
6	HSTRT2	Hysteresis start value	CHM=0	Hysteresis start offset from HEND:
5	HSTRT1	or		%000: 1 %100: 5
4	HSTRT0	Fast decay time		%001: 2 %101: 6
		setting		%010: 3 %110: 7
				%011: 4 %111: 8 Effective: HEND: HSTRT must be < 15
			CHM=1	Effective: HEND+HSTRT must be ≤ 15 Three least-significant bits of the duration of
			CINIET	the fast decay phase. The MSB is HDECO.
				Fast decay time is a multiple of system clock
				periods: N _{CLK} = 32 x (<i>HDECO+HSTRT</i>)

СНО	PCONF	Chopper Configuration		
Bit	Name	Function	Comment	
3	TOFF3	Off time/MOSFET	Duration of slow decay phase. If TOFF is 0, the MOSFETs	
2	TOFF2	disable	are shut off. If TOFF is nonzero, slow decay time is a	
1	TOFF1		multiple of system clock periods:	
0	TOFF0		N _{CLK} = 12 + (32 x TOFF) (Minimum time is 64clocks.)	
			%0000: Driver disable, all bridges off	
			%0001: 1 (use with TBL of minimum 24 clocks)	
			%0010 %1111: 2 15	

6.7 coolStep Control Register (SMARTEN)

SMARTEN d		coolStep Configuration	
Bit	Name	Function	Comment
19	1	Register address bit	
18	0	Register address bit	
17	1	Register address bit	
16	0	Reserved	
15	SEIMIN	Minimum coolStep	0: ½ CS current setting
		current	1: 1/4 CS current setting
14	SEDN1	Current decrement	Number of times that the stallGuard2 value must be
13	SEDN0	speed	sampled equal to or above the upper threshold for each
			decrement of the coil current:
			%00: 32
			%01: 8
			%10: 2
			%11: 1
12	0	Reserved	
11	SEMAX3	Upper coolStep	If the stallGuard2 measurement value SG is sampled
10	SEMAX2	threshold as an offset	equal to or above (SEMIN+SEMAX+1) x 32 enough times,
9	SEMAX1	from the lower	then the coil current scaling factor is decremented.
8	SEMAX0	threshold	
7	0	Reserved	
6	SEUP1	Current increment	Number of current increment steps for each time that
5	SEUP0	size	the stallGuard2 value SG is sampled below the lower
			threshold:
			%00: 1
			%01: 2
			%10: 4
			%11: 8
4	0	Reserved	
3	SEMIN3	Lower coolStep	If SEMIN is 0, coolStep is disabled. If SEMIN is nonzero
2	SEMIN2	threshold/coolStep	and the stallGuard2 value SG falls below SEMIN x 32,
1	SEMIN1	disable	the coolStep current scaling factor is increased.
0	SEMIN0		

6.8 stallGuard2 Control Register (SGCSCONF)

SGCSCONF stallGuard2™ and Current S		stallGuard2™ and Cur	rent Setting
Bit	Name	Function	Comment
19	1	Register address bit	
18	1	Register address bit	
17	0	Register address bit	
16	SFILT	stallGuard2 filter enable	0: Standard mode, fastest response time.
		enable	1: Filtered mode, updated once for each four fullsteps to
			compensate for variation in motor construction, highest
15	0	Reserved	accuracy.
14	SGT6	stallGuard2 threshold	The stallGuard2 threshold value controls the optimum
13	SGT5	value	measurement range for readout. A lower value results in
12	SGT4	value	a higher sensitivity and requires less torque to indicate
			a stall. The value is a two's complement signed integer.
11	SGT3		Values below -10 are not recommended.
10	SGT2		
9	SGT1		Range: -64 to +63
8	SGT0		
7	0	Reserved	
6	0	Reserved	
5	0	Reserved	
4	CS4	Current scale	Current scaling for SPI and step/direction operation.
3	CS3	(scales digital	%00000 %11111: 1/32, 2/32, 3/32, 32/32
2	CS2	currents A and B)	This value is biased by 1 and divided by 32, so the
1	CS1		range is 1/32 to 32/32.
0	CS0		Example: CS=0 is 1/32 current

23	

DRVCONF		Driver Configuration		
Bit	Name	Function	Commen	t
19	1	Register address bit		
18	1	Register address bit		
17	1	Register address bit		
16	TST	Reserved TEST mode	SG_TST o TEST_AN/ selection TEST_AN/ SG_TST:	%01: anatest_dac_out, %10: anatest_vdd_half. %00: comp_A, %01: comp_B, %10: CLK, %11: on_state_xy
15	SLPH1	Slope control, high	%00: Min	imum
14	SLPHO	side	%10: Mea %11: Max In tempe driver str warning	imum temperature compensation mode. dium temperature compensation mode. dium temperature compensation mode. terature compensated mode (tc), the MOSFET gate rength is increased if the overtemperature temperature is reached. This compensates for ure dependency of high-side slope control.
13	SLPL1	Slope control, low	%00: Min	
12	SLPLO	side	%00: Min %01: Min %10: Mec %11: Max	imum. dium.
11	0	Reserved		
10	DISS2G	Short to GND	0: Short	to GND protection is enabled.
		protection disable	1: Short	to GND protection is disabled.
9	TS2G1	Short to GND	%00: 3.2µ	JS.
8	TS2G0 SD0FF	detection timer STEP/DIR interface	%01: 1.6µ %10: 1.2µ %11: 0.8µ	JS.
	SDOFF	disable		e STEP and DIR interface. SPI interface is used
6	VSENSE	Sense resistor voltage-based current scaling	0: Full-scale sense resistor voltage is 305mV. 1: Full-scale sense resistor voltage is 165mV. (Full-scale refers to a current setting of 31 and a DAC value of 255.)	
5	RDSEL1	Select value for read	%00	Microstep position read back
4	RDSELO	out (RD bits)	%01 %10 %11	stallGuard2 level read back stallGuard2 and coolStep current level read back Reserved, do not use
3	0	Reserved		
2	0	Reserved		
1	0	Reserved		
0	0	Reserved		
•	1 -		1	

6.9 Driver Control Register (DRVCONF)

6.10 Read Response

For every write command sent to the motor driver, a 20-bit response is returned to the motion controller. The response has one of three formats, as selected by the RDSEL parameter in the DRVCONF register. The table below shows these formats. Software must not depend on the value of any bit shown as reserved.

DRVSTATUS				Read Response	
Bit	Name		Function	Comment	
	RDSEL=%00	%01	%10		
19	MSTEP9	SG9	SG9	Microstep counter	Microstep position in sine table for coil A in
18	MSTEP8	SG8	SG8	for coil A	STEP/DIR mode. MSTEP9 is the Polarity bit:
17	MSTEP7	SG7	SG7	or	0: Current flows from OA1 pins to OA2 pins.
16	MSTEP6	SG6	SG6	stallGuard2 value	1: Current flows from OA2 pins to OA1 pins.
15	MSTEP5	SG5	SG5	SG9:0	
14	MSTEP4	SG4	SE4	or	stallGuard2 value SG9:0.
13	MSTEP3	SG3	SE3	stallGuard2 value SG9:5 and	
12	MSTEP2	SG2	SE2	coolStep value	stallGuard2 value SG9:5 and the actual
11	MSTEP1	SG1	SE1	SE4:0	coolStep scaling value SE4:0.
10	MSTEPO	SG0	SE0	524.0	
9	Reserved				
8	Reserved STST			Cham destill	0: No standstill condition detected.
/	5151			Standstill indicator	
				mulcator	1: No active edge occurred on the STEP input during the last 2 ²⁰ system clock cycles.
6	OLB			Open load	0: No open load condition detected.
5	OLA			indicator	1: No chopper event has happened during
	0LA			marcator	the last period with constant coil polarity.
					Only a current above 1/16 of the maximum
					setting can clear this bit!
					Hint: This bit is only a status indicator. The
					chip takes no other action when this bit is
					set. False indications may occur during fast
					motion and at standstill. Check this bit only
<u> </u>	6868				during slow motion.
4	S2GB			Short to GND	0: No short to ground shutdown condition.
3	S2GA			detection bits on	1: Short to ground shutdown condition. The
				high-side transistors	short counter is incremented by each short
				transistors	circuit and the chopper cycle is suspended. The counter is decremented for each phase
					polarity change. The MOSFETs are shut off
					when the counter reaches 3 and remain shut
					off until the shutdown condition is cleared by
					disabling and re-enabling the driver. The
					shutdown conditions reset by deasserting the
					ENN input or clearing the TOFF parameter.
2	OTPW			Overtemperature	0: No overtemperature warning condition.
				warning	1: Warning threshold is active.
1	OT			Overtemperature	0: No overtemperature shutdown condition.
				shutdown	1: Overtemperature shutdown has occurred.
0	SG			stallGuard2 status	0: No motor stall detected.
					1: stallGuard2 threshold has been reached,
					and the SG_TST output is driven high.

6.11 Device Initialization

The following sequence of SPI commands is an example of enabling the driver and initializing the chopper:

SPI = \$901B4;	// Hysteresis mode
SPI = \$94557;	// Constant t _{off} mode
SPI = \$D001F;	// Current setting: \$d001F (max. current)
SPI = \$E0010;	// low driver strength, stallGuard2 read, SDOFF=0
SPI = \$00000;	// 256 microstep setting

First test of coolStep current control:

or

SPI = \$A8202; // Enable coolStep with minimum current 1/4 CS

The configuration parameters should be tuned to the motor and application for optimum performance.