Chipsmall
深圳市津利帝科技有限公司
Geelead Technology Limited
Chipsmall
采购部

TMC5072 DATASHEET

Dual controller/driver for up to two 2-phase bipolar stepper motors. No-noise stepper operation. Integrated motion controller and encoder counter. SPI, UART (single wire) and Step/Dir.

Applications

CCTV, Security
Office Automation
Antenna Positioning
Heliostat Controller
Battery powered applications
ATM, Cash recycler, POS
Lab Automation
Liquid Handling
Medical
Printer and Scanner
Pumps and Valves

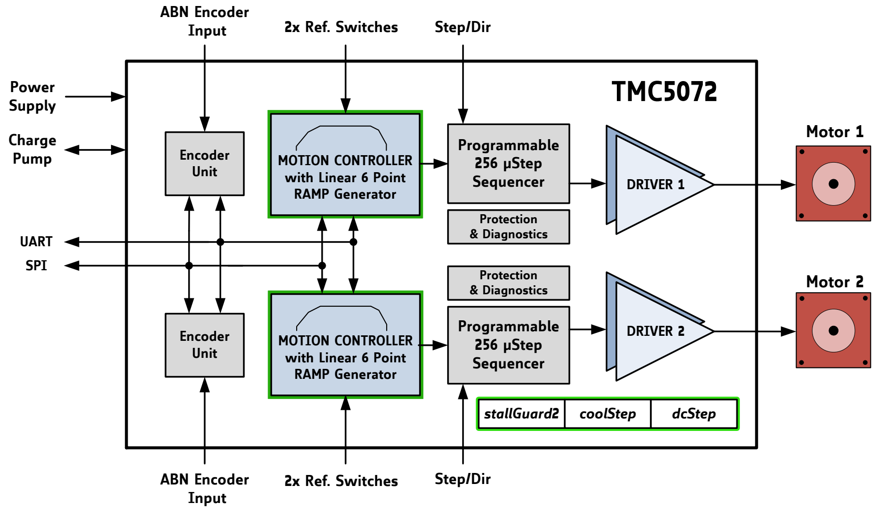
Features and Benefits

Two 2-phase stepper motors
Drive Capability up to 2x 1.1A coil current (2x 1.5A peak)
Parallel Option for one motor at 2.2A (3A peak)
Motion Controller with **sixPoint™** ramp
Voltage Range 4.75… 26V DC
SPI & Single Wire UART
Dual Encoder Interface and **2x Ref.-Switch input** per axis
Highest Resolution up to 256 microsteps per full step
stealthChop™ for extremely quiet operation and smooth motion
spreadCycle™ highly dynamic motor control chopper
dcStep™ load dependent speed control
stallGuard2™ high precision sensorless motor load detection
coolStep™ current control for energy savings up to 75%
Passive Breaking and freewheeling mode
Full Protection & Diagnostics
Compact Size 7x7mm^2 QFN48 package

Description

The TMC5072 is a dual high performance stepper motor controller and driver IC with serial communication interfaces. It combines flexible ramp generators for automatic target positioning with industries' most advanced stepper motor drivers. Based on TRINAMICs sophisticated stealthChop chopper, the driver ensures absolutely noiseless operation combined with maximum efficiency and best motor torque. High integration, high energy efficiency and a small form factor enable miniaturized and scalable systems for cost effective solutions. The complete solution reduces learning curve to a minimum while giving best performance in class.

Block Diagram



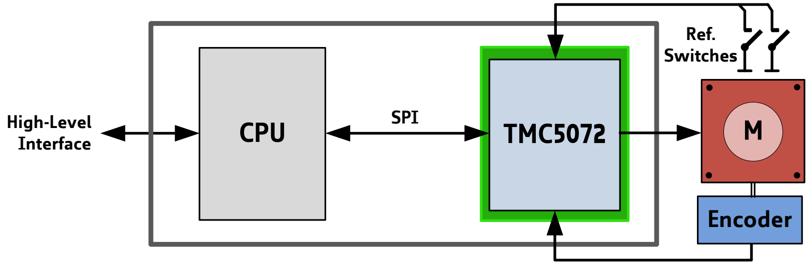
Hamburg, Germany

TRINAMIC
MOTION CONTROL

APPLICATION EXAMPLES: HIGH FLEXIBILITY – MULTIPURPOSE USE

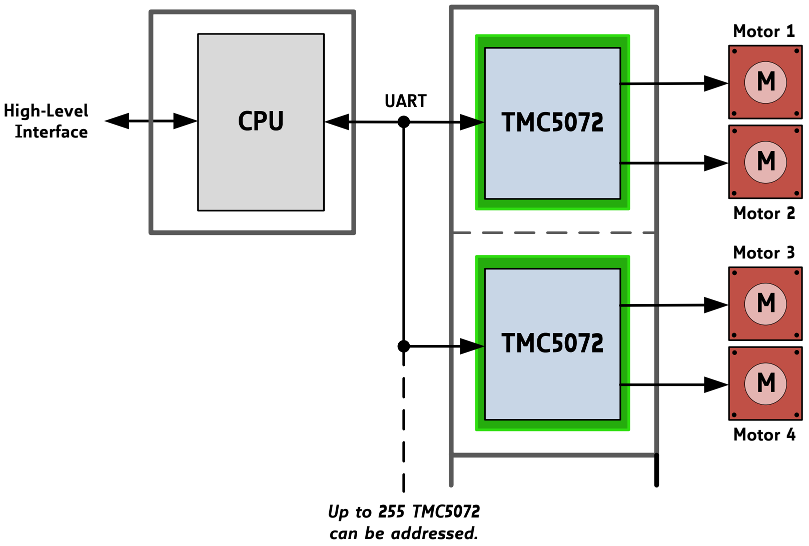
The TMC5072 scores with power density, complete motion controlling features and integrated power stages. It offers a versatility that covers a wide spectrum of applications from battery systems up to embedded applications with 1.5A motor current per coil. The small form factor keeps costs down and allows for miniaturized layouts. Extensive support at the chip, board, and software levels enables rapid design cycles and fast time-to-market with competitive products. High energy efficiency and reliability deliver cost savings in related systems such as power supplies and cooling.

MINIATURIZED DESIGN FOR ONE STEPPER MOTOR

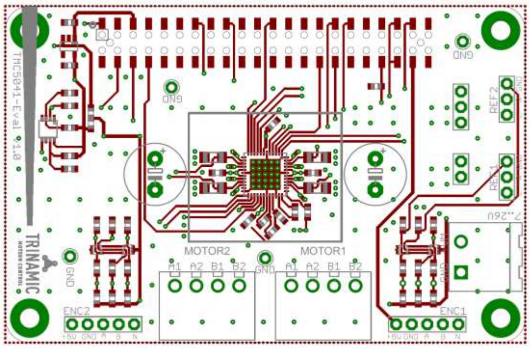


The stepper motor driver outputs are switched in parallel. A dual ABN encoder interface and two reference switch inputs are used.

COMPACT DESIGN FOR UP TO 510 STEPPER MOTORS



An application for up to 510 stepper motors is shown. The UART single wire differential interface allows for a decentralized distributed system with a minimized number of components. Additionally, an ABN encoder and up to two reference switches can be used for each motor. A single CPU can control the whole system. The CPU-board and controller / driver boards are highly economical and space saving.



TMC5072-EVAL EVALUATION BOARD

EVALUATION & DEVELOPMENT PLATFORM

The TMC5072-EVAL is part of TRINAMICs universal evaluation board system which provides a convenient handling of the hardware as well as a user-friendly software tool for evaluation. The TMC5072 evaluation board system consists of three parts: STARTRAMPE (base board), ESELSBRÜCKE (connector board including several test points), and TMC5072-EVAL.

ORDER CODES

Order code	Description	Size [mm^2]
TMC5072-LA	Dual axis stealthChop controller/driver, QFN-48	7 x 7
TMC5072-EVAL	Evaluation board for TMC5072	85 x 55
STARTRAMPE	Baseboard for TMC5072-EVAL and further evaluation boards	85 x 55
ESELSBRÜCKE	Connector board for plug-in evaluation board system	61 x 38

Table of Contents

1 Principles of Operation

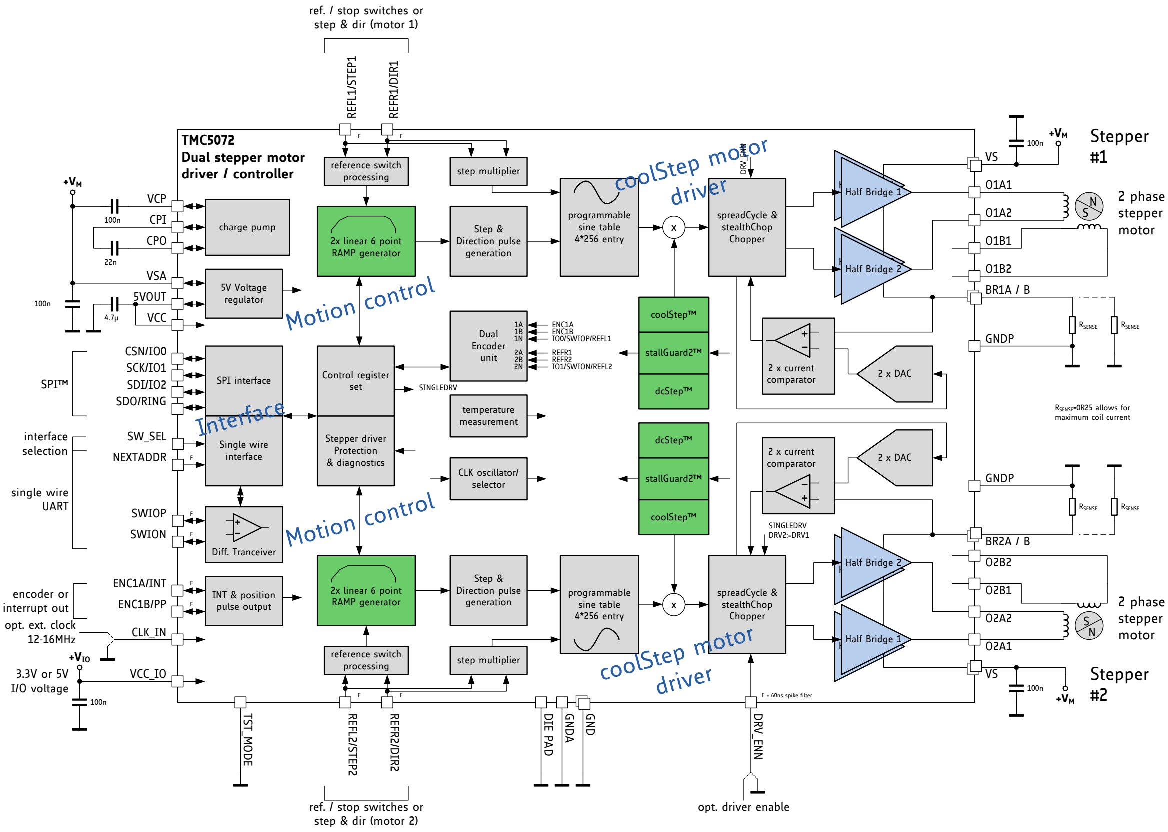


Figure 1.1 Basic application and block diagram

The TMC5072 motion controller and driver chip is an intelligent power component interfacing between the CPU and one or two stepper motors. All stepper motor logic is completely within the TMC5072. No software is required to control the motor – just provide target positions. The TMC5072 offers a number of unique enhancements which are enabled by the system-on-chip integration of driver and controller. The sixPoint ramp generator of the TMC5072 uses stealthChop, dcStep, coolStep, and stallGuard2 automatically to optimize every motor movement. The clear concept and the comprehensive solution save design time.

1.1 Key Concepts

The TMC5072 implements several advanced features which are exclusive to TRINAMIC products. These features contribute toward greater precision, greater energy efficiency, higher reliability, smoother motion, and cooler operation in many stepper motor applications.

stealthChop™ No-noise, high-precision chopper algorithm for inaudible motion and inaudible standstill of the motor.

dcStep™ Load dependent speed control. The motor moves as fast as possible and never loses a step.

stallGuard2™ High-precision load measurement using the back EMF on the motor coils.

coolStep™ Load-adaptive current control which reduces energy consumption by as much as 75%.

spreadCycle™ High-precision chopper algorithm available as an alternative to the traditional constant off-time algorithm.

sixPoint™ Fast and precise positioning using a hardware ramp generator with a set of four acceleration / deceleration settings. Quickest response due to dedicated hardware.

In addition to these performance enhancements, TRINAMIC motor drivers offer safeguards to detect and protect against shorted outputs, output open-circuit, overtemperature, and undervoltage conditions for enhancing safety and recovery from equipment malfunctions.

1.2 Control Interfaces

The TMC5072 supports both, an SPI and a UART based single wire interface with CRC checking. Selection of the actual interface is done via the configuration pin SW_SEL, which can be hardwired to GND or VCC_IO depending on the desired interface.

1.2.1 SPI Interface

The SPI interface is a bit-serial interface synchronous to a bus clock. For every bit sent from the bus master to the bus slave another bit is sent simultaneously from the slave to the master. Communication between an SPI master and the TMC5072 slave always consists of sending one 40-bit command word and receiving one 40-bit status word.

The SPI command rate typically is a few commands per complete motor motion.

1.2.2 UART Interface

The single wire interface allows differential operation similar to RS485 (using SWIOP and SWION) or single wire interfacing (leaving open SWION). It can be driven by any standard UART. No baud rate configuration is required. An optional ring mode allows chaining of slaves to optimize interfacing for applications with regularly distributed drives.

1.3 Software

From a software point of view the TMC5072 is a peripheral with a number of control and status registers. Most of them can either be written only or read only. Some of the registers allow both read and write access. In case read-modify-write access is desired for a write only register, a shadow register can be realized in master software.

1.4 Moving and Controlling the Motor

1.4.1 Integrated Motion Controller

The integrated 32 bit motion controller automatically drives the motor to target positions, or accelerates to target velocities. All motion parameters can be changed on the fly. The motion controller recalculates immediately. A minimum set of configuration data consists of acceleration and deceleration values and the maximum motion velocity. A start and stop velocity is supported as well as a second acceleration and deceleration setting. The integrated motion controller supports immediate reaction to mechanical reference switches and to the sensorless stall detection stallGuard2.

Benefits are:

- Flexible ramp programming
- Efficient use of motor torque for acceleration and deceleration allows higher machine throughput
- Immediate reaction to stop and stall conditions

1.4.2 STEP/DIR Interface

One or both motors can optionally be controlled by a step and direction input. In this case, the respective motion controller remains unused. Active edges on the STEP input can be rising edges or both rising and falling edges as controlled by another mode bit (DEDGE). Using both edges cuts the toggle rate of the STEP signal in half, which is useful for communication over slow interfaces such as optically isolated interfaces. On each active edge, the state sampled from the DIR input determines whether to step forward or back. Each step can be a fullstep or a microstep, in which there are 2, 4, 8, 16, 32, 64, 128, or 256 microsteps per fullstep. During microstepping, a step impulse with a low state on DIR increases the microstep counter and a high decreases the counter by an amount controlled by the microstep resolution. An internal table translates the counter value into the sine and cosine values which control the motor current for microstepping.

1.5 stealthChop Driver with Programmable Microstepping Wave

Current into the motor coils is controlled using a cycle-by-cycle chopper mode. Up to three chopper modes are available: a traditional constant off-time mode and the spreadCycle mode as well as the unique stealthChop. The constant off-time mode provides higher torque at highest velocity, while spreadCycle mode offers smoother operation and greater power efficiency over a wide range of speed and load. The spreadCycle chopper scheme automatically integrates a fast decay cycle and guarantees smooth zero crossing performance. In contrast to the other chopper modes, stealthChop is a voltage chopper based principle. It guarantees that the motor is absolutely quiet in standstill and in slow motion, except for noise generated by ball bearings. The extremely smooth motion is beneficial for many applications.

Programmable microstep shapes allow optimizing the motor performance.

Benefits of using stealthChop:

- Significantly improved microstepping with low cost motors
- Motor runs smooth and quiet
- Absolutely no standby noise
- Reduced mechanical resonances yields improved torque

1.6 stallGuard2 – Mechanical Load Sensing

stallGuard2 provides an accurate measurement of the load on the motor. It can be used for stall detection as well as other uses at loads below those which stall the motor, such as coolStep load-adaptive current reduction. This gives more information on the drive allowing functions like sensorless homing and diagnostics of the drive mechanics.

1.7 coolStep – Load Adaptive Current Control

coolStep drives the motor at the optimum current. It uses the stallGuard2 load measurement information to adjust the motor current to the minimum amount required in the actual load situation. This saves energy and keeps the components cool.

Benefits are:

- *Energy efficiency*	power consumption decreased up to 75%
- *Motor generates less heat*	improved mechanical precision
- *Less or no cooling*	improved reliability
- *Use of smaller motor*	less torque reserve required → cheaper motor does the job

Figure 1.2 shows the efficiency gain of a 42mm stepper motor when using coolStep compared to standard operation with 50% of torque reserve. coolStep is enabled above 60RPM in the example.

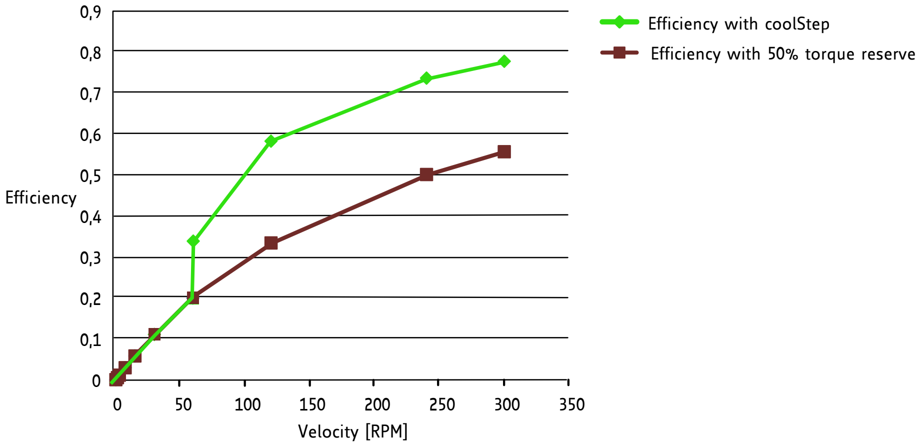


Figure 1.2 Energy efficiency with coolStep (example)

1.8 dcStep – Load Dependent Speed Control

dcStep allows the motor to run near its load limit and at its velocity limit without losing a step. If the mechanical load on the motor increases to the stalling load, the motor automatically decreases velocity so that it can still drive the load. With this feature, the motor will never stall. In addition to the increased torque at a lower velocity, dynamic inertia will allow the motor to overcome mechanical overloads by decelerating. dcStep directly integrates with the ramp generator, so that the target position will be reached, even if the motor velocity needs to be decreased due to increased mechanical load. A dynamic range of up to factor 10 or more can be covered by dcStep without any step loss. By optimizing the motion velocity in high load situations, this feature further enhances overall system efficiency.

Benefits are:

- Motor does not loose steps in overload conditions
- Application works as fast as possible
- Highest possible acceleration automatically
- Highest energy efficiency at speed limit
- Highest possible motor torque using fullstep drive
- Cheaper motor does the job

1.9 Encoder Interfaces

The TMC5072 provides two encoder interfaces for external incremental encoders. The encoders can be used for homing of the motion controllers (alternatively to reference switches) and for consistency checks on-the-fly between encoder position and ramp generator position. A programmable prescaler allows the adaptation of the encoder resolution to the motor resolution. 32 bit encoder counters are provided.

2 Pin Assignments

2.1 Package Outline

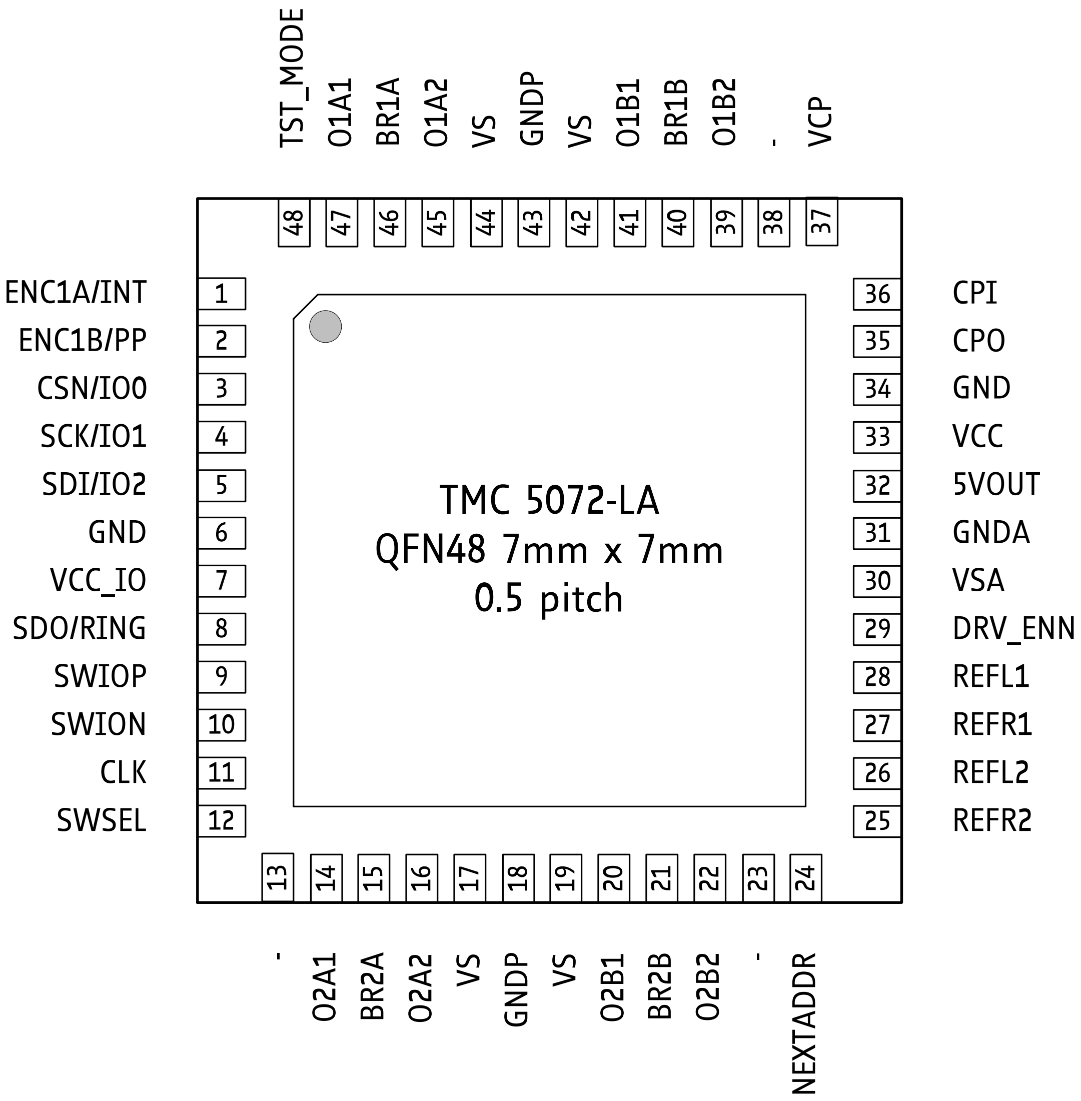


Figure 2.1 TMC5072 pin assignments.

2.2 Signal Descriptions

Pin	Number	Type	Function
GND	6, 34	GND	Digital ground pin for IO pins and digital circuitry.
VCC_IO	7		3.3V or 5V I/O supply voltage pin for all digital pins.
VSA	30		Analog supply voltage for 5V regulator – typically supplied with driver supply voltage. An additional 100nF capacitor to GND (GND plane) is recommended for best performance.
GNDA	31	GND	Analog GND. Tie to GND plane.
5VOUT	32		Output of internal 5V regulator. Attach 2.2 μ F or larger ceramic capacitor to GNDA near to pin for best performance. May be used to supply VCC of chip.

Pin	Number	Type	Function
VCC	33		5V supply input for digital circuitry within chip and charge pump. Attach 470nF capacitor to GND (GND plane). May be supplied by 5VOUT. A 2.2Ω resistor is recommended for decoupling noise from 5VOUT. When using an external supply, make sure, that VCC comes up before or in parallel to 5VOUT or VCC_IO, whichever comes up later!
DIE_PAD	-	GND	Connect the exposed die pad to a GND plane. Provide as many as possible vias for heat transfer to GND plane.

Table 2.1 Low voltage digital and analog power supply pins

Pin	Number	Type	Function
CPO	35	O(VCC)	Charge pump driver output. Outputs 5V (GND to VCC) square wave with 1/16 of internal oscillator frequency.
CPI	36	I(VCP)	Charge pump capacitor input: Provide external 22nF or 33nF / 50V capacitor to CPO.
VCP	37		Output of charge pump. Provide external 100nF capacitor to VS.

Table 2.2 Charge pump pins

Pin	Number	Type	Function
ENC1A/INT	1	I/O	Input A for incremental encoder 1. Can be programmed to provide interrupt output based on ramp generator flags *RAMP_STAT* bits 4, 5, 6 & 7 and encoder null event status *ENC_STATUS* bit 0 (*poscmp_enable*=1).
ENC1B/PP	2	I/O	Input B for incremental encoder 1. Can be programmed to provide position compare output for motor 1 (*poscmp_enable*=1).
CSN/IO0	3	I/O	Chip select input of SPI interface, programmable IO in UART mode
SCK/IO1	4	I/O	Serial clock input of SPI interface, programmable IO in UART mode
SDI/IO2	5	I/O	Data input of SPI interface, programmable IO in UART mode
SDO/RING	8	I/O	Data output of SPI interface (Tristate, enabled with CSN=0), mode configuration input in UART mode (0 = Normal mode, 1 = Single wire ring mode – SWIO_P is input, SWIO_N is output)
SWIOP	9	I/O	Single wire I/O (positive). Serial input in ring mode. Multi-purpose input in SPI mode or encoder 1 N input.
SWION	10	I/O	Single wire I/O (negative) for differential mode. Leave open in non-differential mode when operating at 5V IO voltage or tie to desired threshold voltage. Serial output in ring mode. Multi-purpose input in SPI mode or encoder 2 N input.
CLK	11	I	Clock input. Tie to GND using short wire for internal clock or supply external clock. The first high signal disables the internal oscillator until power down.
SWSEL	12	I	Interface selection input. Tie to GND for SPI mode, tie to VCC_IO for single wire (UART) interface mode.
NEXTADDR	24	I	Address increment (if tied high) for single wire (UART) mode. General purpose input in SPI mode
REFR2/DIR2	25	I	Right reference switch input for motor 2, optional DIR input for STEP/DIR operation of motor 2 or encoder 2 B input
REFL2/STEP2	26	I	Left reference switch input for motor 2, optional STEP input for STEP/DIR operation of motor 2
REFR1/DIR1	27	I	Right reference switch input for motor 1, optional DIR input for STEP/DIR operation of motor 1 or encoder 2 A input
REFL1/STEP1	28	I	Left reference switch input for motor 1, optional STEP input for STEP/DIR operation of motor 1
DRV_ENN	29	I	Enable input for motor drivers. The power stage becomes switched off (all motor outputs floating) when this pin becomes driven to a high level. Tie to GND for normal operation.
TST_MODE	48	I	Test mode input. Tie to GND using short wire.

Pin	Number	Type	Function
-	13, 23, 38	N.C.	Unused pins – no internal electrical connection. Leave open or tie to GND for compatibility with future devices.

Table 2.3 Digital I/O pins (all related to VCC_IO supply)

Pin	Number	Type	Function
O2A1	14	O (VS)	Motor 2 coil A output 1
BR2A	15		Sense resistor connection for motor 2 coil A. Place sense resistor to GND near pin.
O2A2	16	O (VS)	Motor 2 coil A output 2
VS	17, 19		Motor supply voltage. Provide filtering capacity near pin with shortest loop to nearest GNDP pin (respectively via GND plane).
GNDP	18	GND	Power GND. Connect to GND plane near pin.
O2B1	20	O (VS)	Motor 2 coil B output 1
BR2B	21		Sense resistor connection for motor 2 coil B. Place sense resistor to GND near pin.
O2B2	22	O (VS)	Motor 2 coil B output 2
O1B2	39	O (VS)	Motor 1 coil B output 2
BR1B	40		Sense resistor connection for motor 1 coil B. Place sense resistor to GND near pin.
O1B1	41	O (VS)	Motor 1 coil B output 1
VS	42, 44		Motor supply voltage. Provide filtering capacity near pin with shortest loop to nearest GNDP pin (respectively via GND plane).
GNDP	43	GND	Power GND. Connect to GND plane near pin.
O1A2	45	O (VS)	Motor 1 coil A output 2
BR1A	46		Sense resistor connection for motor 1 coil A. Place sense resistor to GND near pin.
O1A1	47	O (VS)	Motor 1 coil A output 1

Table 2.4 Power driver pins

3 Sample Circuits

The sample circuits show the connection of the external components in different operation and supply modes. The connection of the bus interface and further digital signals is left out for clarity.

3.1 Standard Application Circuit

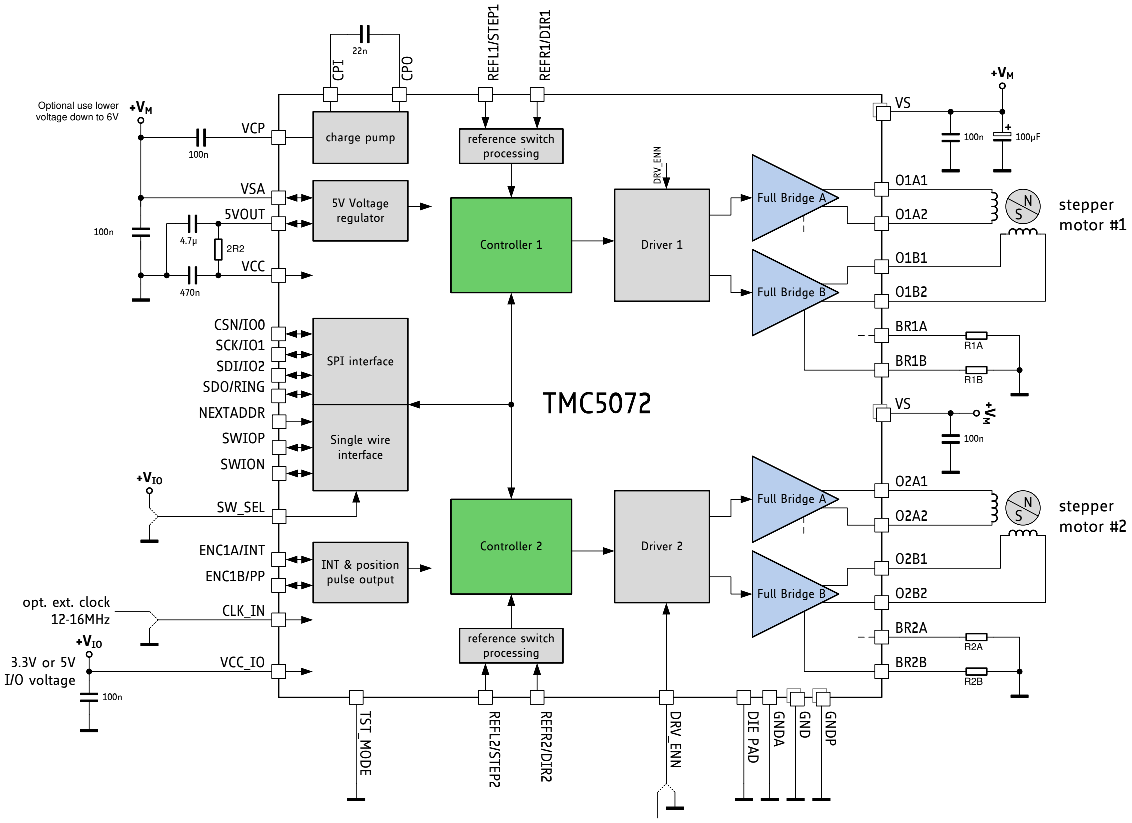


Figure 3.1 Standard application circuit

The standard application circuit uses a minimum set of additional components in order to operate the motor. Use low ESR capacitors for filtering the power supply which are capable to cope with the current ripple. The current ripple often depends on the power supply and cable length. The VCC_IO voltage can be supplied from 5VOUT, or from an external source, e.g. a low drop 3.3V regulator. In order to minimize linear voltage regulator power dissipation of the internal 5V voltage regulator in applications where VM is high, a different (lower) supply voltage can be used for VSA, if available. For example, many applications provide a 12V supply in addition to a higher supply voltage like 24V. Using the 12V supply for VSA will reduce the power dissipation of the internal 5V regulator to about 37% of the dissipation caused by supply with the full motor voltage. For best motor chopper performance, an optional R/C-filter de-couples 5VOUT from digital noise cause by power drawn from VCC.

Basic layout hints
Place sense resistors and all filter capacitors as close as possible to the related IC pins. Use a solid common GND for all GND connections, also for sense resistor GND. Connect 5VOUT filtering capacitor directly to 5VOUT and GNDA pin. See layout hints for more details. Low ESR electrolytic capacitors are recommended for VS filtering.

Attention
In case VSA is supplied by a different voltage source, make sure that VSA does not exceed VS by more than one diode drop upon power up or power down.

3.2 5 V Only Supply

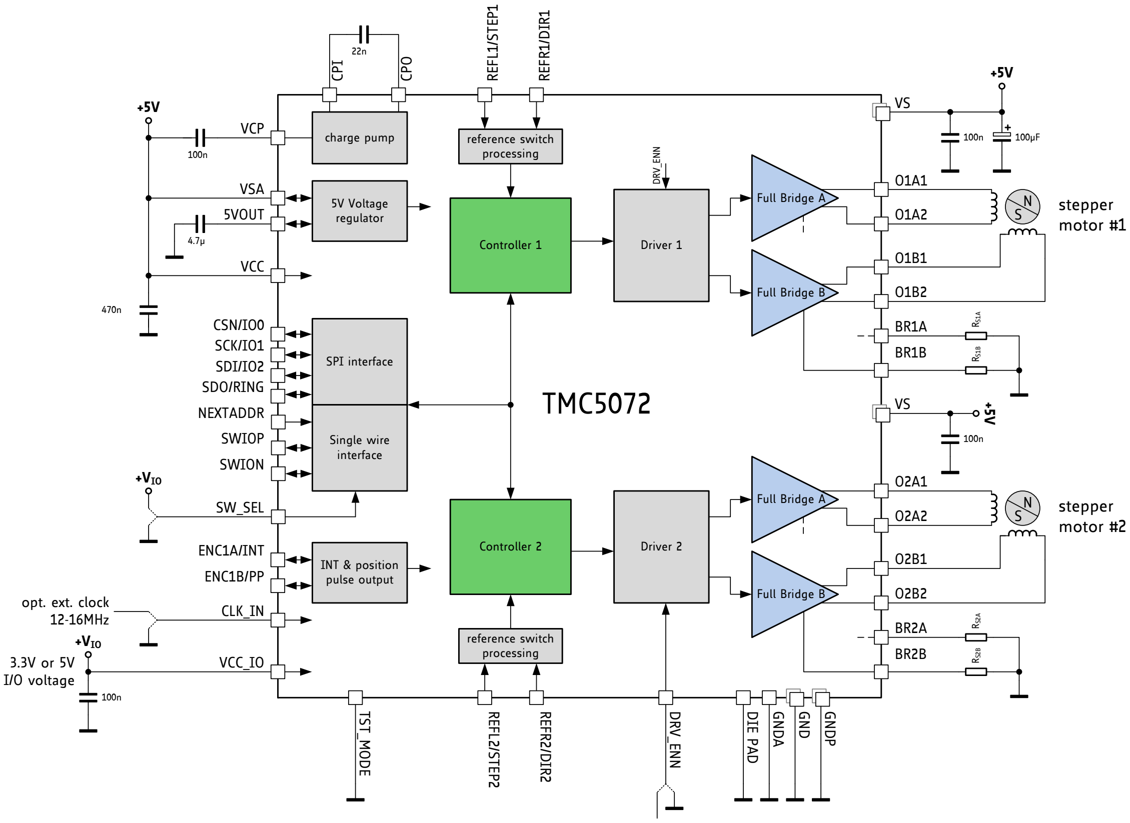


Figure 3.2 5V only operation

While the standard application circuit is limited to roughly 5.5V lower supply voltage, a 5V only application lets the IC run from a normal 5V +/-5% supply. In this application, linear regulator drop must be minimized. Therefore, the major 5V load is removed by supplying VCC directly from the external supply. In order to keep supply ripple away from the analog voltage reference, 5VOUT should have an own filtering capacity and the 5VOUT pin does not become bridged to the 5V supply.

3.3 One Motor with High Current

The TMC5072 supports double motor current for a single driver by paralleling both power stages. In order to operate in this mode, activate the flag *single_driver* in the global configuration register *GCONF*. This register can be locked for subsequent write access.

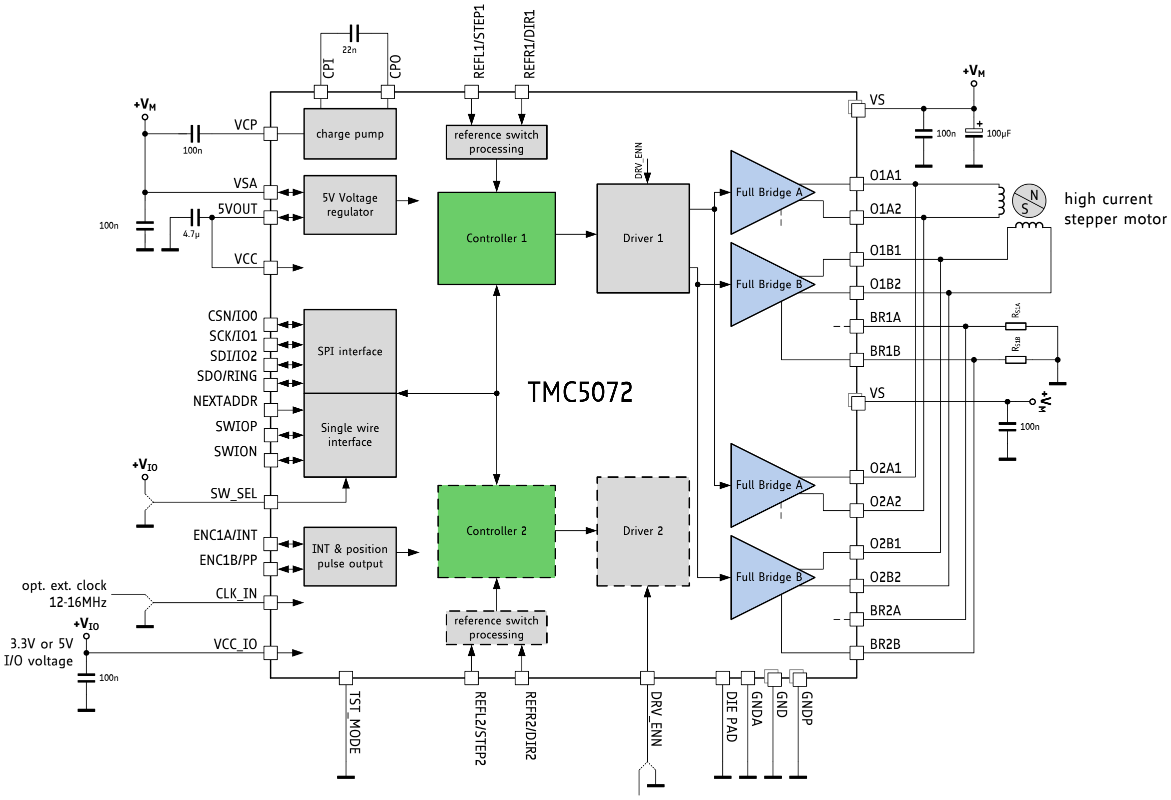


Figure 3.3 Driving a single motor with high current

3.4 External 5V Power Supply

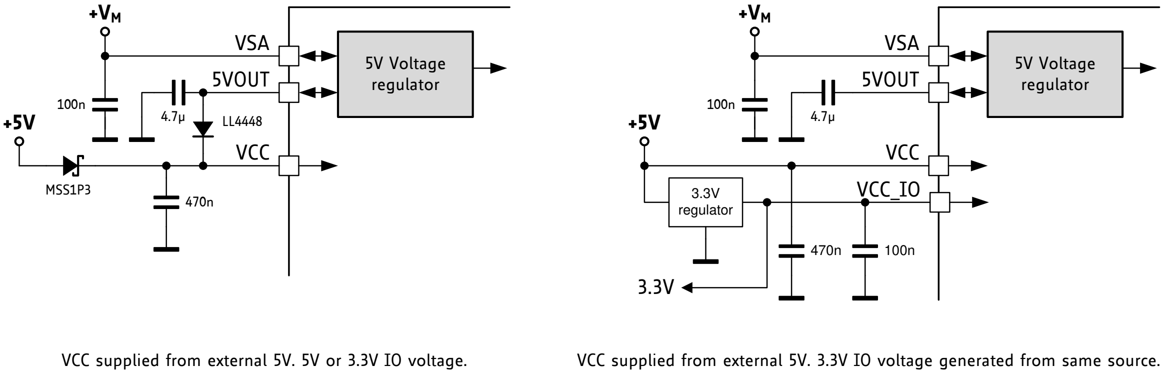
When an external 5V power supply is available, the power dissipation caused by the internal linear regulator can be eliminated. This especially is beneficial in high voltage applications, and when thermal conditions are critical. There are two options for using this external 5V source: either the external 5V source is used to support the digital supply of the driver by supplying the VCC pin, or the complete internal voltage regulator becomes bridged and is replaced by the external supply voltage.

3.4.1 Support for the VCC Supply

This scheme uses an external supply for all digital circuitry within the driver (Figure 3.4). As the digital circuitry makes up for most of the power dissipation, this way the internal 5V regulator sees only low remaining load. The precisely regulated voltage of the internal regulator is still used as the reference for the motor current regulation as well as for supplying internal analog circuitry.

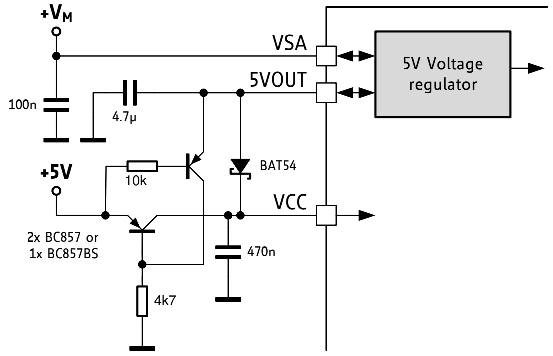
When cutting pin VCC from 5VOUT, make sure that the VCC supply comes up before or synchronously with the 5VOUT supply to ensure a correct power up reset of the internal logic. A simple schematic uses two diodes forming an OR of the internal and the external power supplies for VCC. In order to prevent the chip from drawing part of the power from its internal regulator, a low drop 1A Schottky diode is used for the external 5V supply path, while a silicon diode is used for the 5VOUT path. An enhanced solution uses a dual PNP transistor as an active switch. It minimizes voltage drop and thus gives best performance.

In certain setups, switching of VCC voltage can be eliminated. A third variant uses the VCC_IO supply to ensure power-on reset. This is possible, if VCC_IO comes up synchronously with or delayed to VCC. Use a linear regulator to generate a 3.3V VCC_IO from the external 5V VCC source. This 3.3V regulator will cause a certain voltage drop. A voltage drop in the regulator of 0.9V or more (e.g. LD1117-3.3) ensures that the 5V supply already has exceeded the lower limit of about 3.0V once the reset conditions ends. The reset condition ends earliest, when VCC_IO exceeds the undervoltage limit of minimum 2.1V. Make sure that the power-down sequence also is safe. Undefined states can result when VCC drops well below 4V without safely triggering a reset condition. Triggering a reset upon power-down can be ensured when VSA goes down synchronously with or before VCC.



VCC supplied from external 5V. 5V or 3.3V IO voltage.

VCC supplied from external 5V. 3.3V IO voltage generated from same source.



VCC supplied from external 5V using active switch. 5V or 3.3V IO voltage.

Figure 3.4 Using an external 5V supply for digital circuitry of driver (different options)

3.4.2 Internal Regulator Bridged

In case a clean external 5V supply is available, it can be used for complete supply of analog and digital part (Figure 3.5). The circuit will benefit from a well regulated supply, e.g. when using a +/-1% regulator. A precise supply guarantees increased motor current precision, because the voltage at 5VOUT directly is the reference voltage for all internal units of the driver, especially for motor current control. For best performance, the power supply should have low ripple to give a precise and stable supply at 5VOUT pin with remaining ripple well below 5mV. Some switching regulators have a higher remaining ripple, or different loads on the supply may cause lower frequency ripple. In this case, increase capacity attached to 5VOUT. In case the external supply voltage has poor stability or low frequency ripple, this would affect the precision of the motor current regulation as well as add chopper noise.

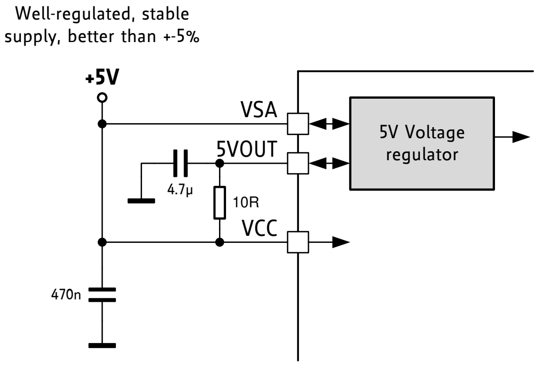


Figure 3.5 Using an external 5V supply to bypass internal regulator

3.5 Optimizing Analog Precision

The 5VOUT pin is used as an analog reference for operation of the TMC5072. Performance will degrade when there is voltage ripple on this pin. Most of the high frequency ripple in a TMC5072 design results from the operation of the internal digital logic. The digital logic switches with each edge of the clock signal. Further, ripple results from operation of the charge pump, which operates with roughly 1 MHz and draws current from the VCC pin. In order to keep this ripple as low as possible, an additional filtering capacitor can be put directly next to the VCC pin with vias to the GND plane giving a short connection to the digital GND pins (pin 6 and pin 34). Analog performance is best, when this ripple is kept away from the analog supply pin 5VOUT, using an additional series resistor of 2.2 Ω. The voltage drop on this resistor will be roughly 100 mV (I_{VCC} * R).

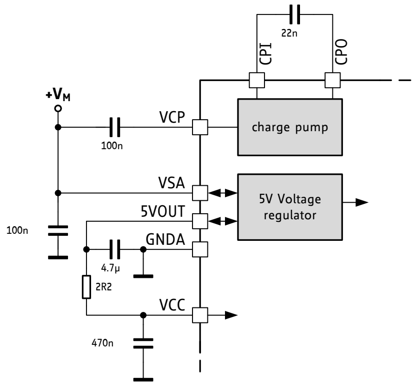
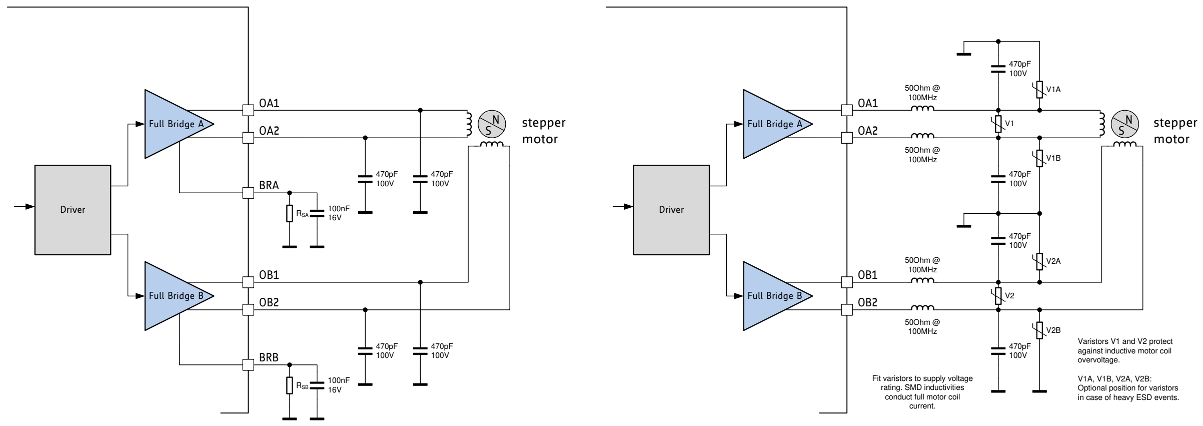


Figure 3.6 RC-Filter on VCC for reduced ripple

3.6 Driver Protection and EME Circuitry

Some applications have to cope with ESD events caused by motor operation or external influence. Despite ESD circuitry within the driver chips, ESD events occurring during operation can cause a reset or even a destruction of the motor driver, depending on their energy. Especially plastic housings and belt drive systems tend to cause ESD events. It is best practice to avoid ESD events by attaching all conductive parts, especially the motors themselves to PCB ground, or to apply electrically conductive plastic parts. In addition, the driver can be protected up to a certain degree against ESD events or live plugging / pulling the motor, which also causes high voltages and high currents into the motor connector terminals. A simple scheme uses capacitors at the driver outputs to reduce the dV/dt caused by ESD events. Larger capacitors will bring more benefit concerning ESD suppression, but cause additional current flow in each chopper cycle, and thus increase driver power dissipation, especially at high supply voltages. The values shown are example values – they might be varied between 100pF and 1nF. The capacitors also dampen high frequency noise injected from digital parts of the circuit and thus reduce electromagnetic emission. A more elaborate scheme uses LC filters to de-couple the driver outputs from the motor connector. Varistors in between of the coil terminals eliminate coil overvoltage caused by live plugging. Optionally protect all outputs by a varistor against ESD voltage.



Fit varistors to supply voltage rating. SMD inductivities conduct full motor coil current.

Varistors V1 and V2 protect against inductive motor coil overvoltage.

V1A, V1B, V2A, V2B: Optional position for varistors in case of heavy ESD events.

Figure 3.7 Simple ESD enhancement and more elaborate motor output protection

4 SPI Interface

4.1 SPI Datagram Structure

The TMC5072 uses 40 bit SPI™ (Serial Peripheral Interface, SPI is Trademark of Motorola) datagrams for communication with a microcontroller. Microcontrollers which are equipped with hardware SPI are typically able to communicate using integer multiples of 8 bit. The NCS line of the TMC5072 must be handled in a way, that it stays active (low) for the complete duration of the datagram transmission.

Each datagram sent to the device is composed of an address byte followed by four data bytes. This allows direct 32 bit data word communication with the register set. Each register is accessed via 32 data bits even if it uses less than 32 data bits.

For simplification, each register is specified by a one byte address:

- For a read access the most significant bit of the address byte is 0.
- For a write access the most significant bit of the address byte is 1.

Most registers are write only registers, some can be read additionally, and there are also some read only registers.

<table>
<tr><th colspan="40">SPI DATAGRAM STRUCTURE</th></tr>
<tr><td colspan="13">MSB (transmitted first)</td><td colspan="14">40 bit</td><td colspan="13">LSB (transmitted last)</td></tr>
<tr><td colspan="20">39 ...</td><td colspan="20">... 0</td></tr>
<tr><td colspan="8"><b>→ 8 bit address</b>
<b>← 8 bit SPI status</b></td><td colspan="32"><b>← → 32 bit data</b></td></tr>
<tr><td colspan="8">39 ... 32</td><td colspan="32">31 ... 0</td></tr>
<tr><td colspan="8">→ to TMC5072:
RW + 7 bit address
← from TMC5072:
8 bit SPI status</td><td colspan="8">8 bit data</td><td colspan="8">8 bit data</td><td colspan="8">8 bit data</td><td colspan="8">8 bit data</td></tr>
<tr><td colspan="8">39 / 38 ... 32</td><td colspan="8">31 ... 24</td><td colspan="8">23 ... 16</td><td colspan="8">15 ... 8</td><td colspan="8">7 ... 0</td></tr>
<tr><td>W</td><td colspan="7">38...32</td><td colspan="4">31...28</td><td colspan="4">27...24</td><td colspan="4">23...20</td><td colspan="4">19...16</td><td colspan="4">15...12</td><td colspan="4">11...8</td><td colspan="4">7...4</td><td colspan="4">3...0</td></tr>
<tr><td>39</td><td>38</td><td>37</td><td>36</td><td>35</td><td>34</td><td>33</td><td>32</td><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
</table>

4.1.1 Selection of Write / Read (WRITE_notREAD)

The read and write selection is controlled by the MSB of the address byte (bit 39 of the SPI datagram). This bit is 0 for read access and 1 for write access. So, the bit named W is a WRITE_notREAD control bit. The active high write bit is the MSB of the address byte. So, 0x80 has to be added to the address for a write access. The SPI interface always delivers data back to the master, independent of the W bit. The data transferred back is the data read from the address which was transmitted with the *previous* datagram, if the previous access was a read access. If the previous access was a write access, then the data read back mirrors the previously received write data. So, the difference between a read and a write access is that the read access does not transfer data to the addressed register but it transfers the address only and its 32 data bits are dummies, and, further the following read or write access delivers back the data read from the address transmitted in the preceding read cycle.

A read access request datagram uses dummy write data. Read data is transferred back to the master with the subsequent read or write access. Hence, reading multiple registers can be done in a pipelined fashion.

Whenever data is read from or written to the TMC5072, the MSBs delivered back contain the SPI status, *SPI_STATUS*, a number of eight selected status bits.

Example:

For a read access to the register (*XACTUAL*) with the address 0x21, the address byte has to be set to 0x21 in the access preceding the read access. For a write access to the register (*VACTUAL*), the address byte has to be set to 0x80 + 0x22 = 0xA2. For read access, the data bit might have any value (-). So, one can set them to 0.

action	data sent to TMC5072	data received from TMC5072
read *XACTUAL*	→ `0x2100000000`	← `0xSS & unused data`
read *XACTUAL*	→ `0x2100000000`	← `0xSS & XACTUAL`
write *VMAX*:= `0x00ABCDEF`	→ `0xA700ABCDEF`	← `0xSS & XACTUAL`
write *VMAX*:= `0x00123456`	→ `0xA700123456`	← `0xSS00ABCDEF`

`*)S:` is a placeholder for the status bits *SPI_STATUS*

4.1.2 SPI Status Bits Transferred with Each Datagram Read Back

New status information becomes latched at the end of each access and is available with the next SPI transfer.

***SPI_STATUS* – status flags transmitted with each SPI access in bits 39 to 32**		
Bit	**Name**	**Comment**
7	-	reserved (0)
6	*status_stop_l(2)*	*RAMP_STAT2*[0] – 1: Signals motor 2 stop left switch status
5	*status_stop_l(1)*	*RAMP_STAT1*[0] – 1: Signals motor 1 stop left switch status
4	*velocity_reached(2)*	*RAMP_STAT2*[8] – 1: Signals motor 2 has reached its target velocity
3	*velocity_reached(1)*	*RAMP_STAT1*[8] – 1: Signals motor 1 has reached its target velocity
2	*driver_error(2)*	*GSTAT*[2] – 1: Signals driver 2 driver error (clear by reading *GSTAT*)
1	*driver_error(1)*	*GSTAT*[1] – 1: Signals driver 1 driver error (clear by reading *GSTAT*)
0	*reset_flag*	*GSTAT*[0] – 1: Signals, that a reset has occurred (clear by reading *GSTAT*)

4.1.3 Data Alignment

All data are right aligned. Some registers represent unsigned (positive) values, some represent integer values (signed) as two's complement numbers, single bits or groups of bits are represented as single bits respectively as integer groups.

4.2 SPI Signals

The SPI bus on the TMC5072 has four signals:

- SCK – bus clock input
- SDI – serial data input
- SDO – serial data output
- CSN – chip select input (active low)

The slave is enabled for an SPI transaction by a low on the chip select input CSN. Bit transfer is synchronous to the bus clock SCK, with the slave latching the data from SDI on the rising edge of SCK and driving data to SDO following the falling edge. The most significant bit is sent first. A minimum of 40 SCK clock cycles is required for a bus transaction with the TMC5072.

If more than 40 clocks are driven, the additional bits shifted into SDI are shifted out on SDO after a 40-clock delay through an internal shift register. This can be used for daisy chaining multiple chips.

CSN must be low during the whole bus transaction. When CSN goes high, the contents of the internal shift register are latched into the internal control register and recognized as a command from the master to the slave. If more than 40 bits are sent, only the last 40 bits received before the rising edge of CSN are recognized as the command.

4.3 Timing

The SPI interface is synchronized to the internal system clock, which limits the SPI bus clock SCK to half of the system clock frequency. If the system clock is based on the on-chip oscillator, an additional 10% safety margin must be used to ensure reliable data transmission. All SPI inputs as well as the ENN input are internally filtered to avoid triggering on pulses shorter than 20ns. Figure 4.1 shows the timing parameters of an SPI bus transaction, and the table below specifies their values.

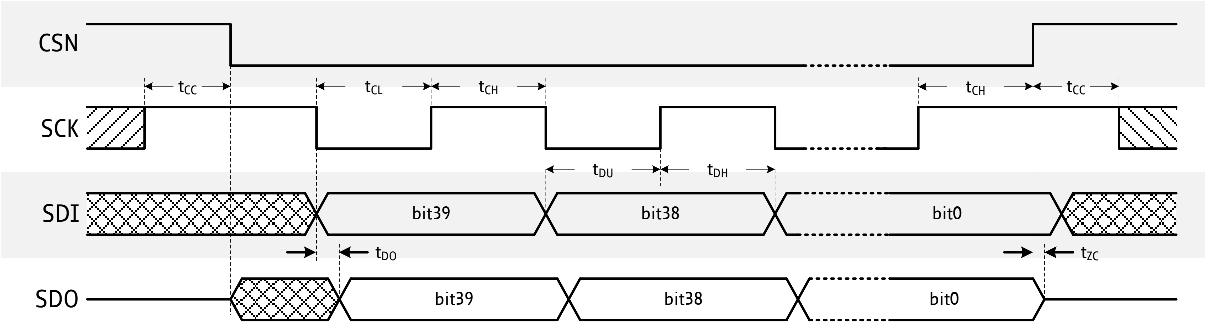


Figure 4.1 SPI timing

Hint
Usually this SPI timing is referred to as SPI MODE 3

SPI interface timing	**AC-Characteristics** clock period: t_{CLK}					
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
SCK valid before or after change of CSN	t_{CC}		10			ns
CSN high time	t_{CSH}	*) Min time is for synchronous CLK with SCK high one t_{CH} before CSN high only	t_{CLK} *)	>2t_{CLK}+10		ns
SCK low time	t_{CL}	*) Min time is for synchronous CLK only	t_{CLK} *)	>t_{CLK}+10		ns
SCK high time	t_{CH}	*) Min time is for synchronous CLK only	t_{CLK} *)	>t_{CLK}+10		ns
SCK frequency using internal clock	f_{SCK}	assumes minimum OSC frequency			4	MHz
SCK frequency using external 16MHz clock	f_{SCK}	assumes synchronous CLK			8	MHz
SDI setup time before rising edge of SCK	t_{DU}		10			ns
SDI hold time after rising edge of SCK	t_{DH}		10			ns
Data out valid time after falling SCK clock edge	t_{DO}	no capacitive load on SDO			t_{FILT}+5	ns
SDI, SCK and CSN filter delay time	t_{FILT}	rising and falling edge	12	20	30	ns

5 UART Single Wire Interface

The UART single wire interface allows the control of the TMC5072 with any microcontroller UART. It shares transmit and receive line like an RS485 based interface. Data transmission is secured using a cyclic redundancy check, so that increased interface distances (e.g. over cables between two PCBs) can be bridged without the danger of wrong or missed commands even in the event of electro-magnetic disturbance. The automatic baud rate detection and an advanced addressing scheme make this interface easy and flexible to use.

5.1 Datagram Structure

5.1.1 Write Access

<table>
<tr><th colspan="20">UART WRITE ACCESS DATAGRAM STRUCTURE</th></tr>
<tr><td colspan="20">each byte is LSB…MSB, highest byte transmitted first</td></tr>
<tr><td colspan="20">0 … 63</td></tr>
<tr><th colspan="8">sync + reserved</th><th colspan="3">8 bit slave address</th><th colspan="3">RW + 7 bit register addr.</th><th colspan="3">32 bit data</th><th colspan="3">CRC</th></tr>
<tr><td colspan="8">0…7</td><td colspan="3">8…15</td><td colspan="3">16…23</td><td colspan="3">24…55</td><td colspan="3">56…63</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td colspan="4">Reserved (don't cares but included in CRC)</td><td colspan="3"><i>SLAVEADDR</i></td><td colspan="2">register address</td><td>1</td><td colspan="3">data bytes 3, 2, 1, 0 (high to low byte)</td><td colspan="3">CRC</td></tr>
<tr><td>0</td><td>1</td><td>2</td><td>3</td><td>4</td><td>5</td><td>6</td><td>7</td><td>8</td><td>…</td><td>15</td><td>16</td><td>…</td><td>23</td><td>24</td><td>…</td><td>55</td><td>56</td><td>…</td><td>63</td></tr>
</table>

A sync nibble precedes each transmission to and from the TMC5072 and is embedded into the first transmitted byte, followed by an addressing byte. Each transmission allows a synchronization of the internal baud rate divider to the master clock. The actual baud rate is adapted and variations of the internal clock frequency are compensated. Thus, the baud rate can be freely chosen within the valid range. Each transmitted byte starts with a start bit (logic 0, low level on SWIOP) and ends with a stop bit (logic 1, high level on SWIOP). The bit time is calculated by measuring the time from the beginning of start bit (1 to 0 transition) to the end of the sync frame (1 to 0 transition from bit 2 to bit 3). All data is transmitted byte wise. The 32 bit data words are transmitted with the highest byte first.

A minimum baud rate of 9000 baud is permissible, assuming 20 MHz clock (worst case for low baud rate). Maximum baud rate is $f_{CLK}/16$ due to the required stability of the baud clock.

The slave address is determined by the register *SLAVEADDR*. If the external address pin NEXTADDR is set, the slave address becomes incremented by one.

The communication becomes reset if a pause time of longer than 63 bit times between the start bits of two successive bytes occurs. This timing is based on the last correctly received datagram. In this case, the transmission needs to be restarted after a failure recovery time of minimum 12 bit times of bus idle time. This scheme allows the master to reset communication in case of transmission errors. Any pulse on an idle data line below 16 clock cycles will be treated as a glitch and leads to a timeout of 12 bit times, for which the data line must be idle. Other errors like wrong CRC are also treated the same way. This allows a safe re-synchronization of the transmission after any error conditions. Remark, that due to this mechanism, an abrupt reduction of the baud rate to less than 15 percent of the previous value is not possible.

Each accepted write datagram becomes acknowledged by the receiver by incrementing an internal cyclic datagram counter (8 bit). Reading out the datagram counter allows the master to check the success of an initialization sequence or single write accesses. Read accesses do not modify the counter.

5.1.2 Read Access

UART READ ACCESS REQUEST DATAGRAM STRUCTURE																
each byte is LSB…MSB, highest byte transmitted first																
sync + reserved								**8 bit slave address**			**RW + 7 bit register address**			**CRC**		
0…7								8…15			16…23			24…31		
1	0	1	0	Reserved (don't cares but included in CRC)				*SLAVEADDR*			register address		0	CRC		
0	1	2	3	4	5	6	7	8	:	15	16	:	23	24	:	31

The read access request datagram structure is identical to the write access datagram structure, but uses a lower number of user bits. Its function is the addressing of the slave and the transmission of the desired register address for the read access. The TMC5072 responds with the same baud rate as the master uses for the read request.

In order to ensure a clean bus transition from the master to the slave, the TMC5072 does not immediately send the reply to a read access, but it uses a programmable delay time after which the first reply byte becomes sent following a read request. This delay time can be set in multiples of eight bit times using *SENDDELAY* time setting (default=8 bit times) according to the needs of the master.

UART READ ACCESS REPLY DATAGRAM STRUCTURE																			
each byte is LSB…MSB, highest byte transmitted first																			
0 …… 63																			
sync + reserved								**8 bit slave address**			**RW + 7 bit register addr.**			**32 bit data**			**CRC**		
0…7								8…15			16…23			24…55			56…63		
1	0	1	0	reserved (0)				0xFF			register address		0	data bytes 3, 2, 1, 0 (high to low byte)			CRC		
0	1	2	3	4	5	6	7	8	:	15	16	:	23	24	:	55	56	:	63

The read response is sent to the master using address code %1111. The transmitter becomes switched inactive four bit times after the last bit is sent.

> Address %11111111 is reserved for read accesses going to the master. A slave cannot use this address.

ERRATA IN READ ACCESS

A known bug in the UART interface implementation affects read access to registers that change during the access. While the SPI interface takes a snapshot of the read register before transmission, the UART interface transfers the register directly MSB to LSB without taking a snapshot. This may lead to inconsistent data when reading out a register that changes during the transmission. Further, the CRC sent from the driver may be incorrect in this case (but must not), which will lead to the master repeating the read access. As a workaround, it is advised not to read out quickly changing registers like *XACTUAL*, *MSCNT* or *X_ENC* during a motion, but instead first stop the motor or check the *position_reached* flag to become active, and read out these values afterwards. If possible, use *X_LATCH* and *ENC_LATCH* for a safe readout during motion (e.g. for homing). As the encoder cannot be guaranteed to stand still during motor stop, only a dual read access and check for identical result ensures correct *X_ENC* read data. Therefore it is advised to use the latching function instead. Use the *vzero* and *velocity_reached* flag rather than reading *VACTUAL*.

5.2 CRC Calculation

An 8 bit CRC polynomial is used for checking both read and write access. It allows detection of up to eight single bit errors. The CRC8-ATM polynomial with an initial value of zero is applied LSB to MSB, including the sync- and addressing byte. The sync nibble is assumed to always be correct. The TMC5072 responds only to correctly transmitted datagrams containing its own slave address. It increases its datagram counter for each correctly received write access datagram.

$$CRC = x^8 + x^2 + x^1 + x^0$$

Hint:

The CRC can be calculated within a CPU using a bit-wise cyclic XOR calculation of incoming and outgoing bits accumulated to an 8 bit CRC register. You find the algorithm in the TMC5072-EVAL evaluation board firmware.

```
CRC = (CRC << 1) OR (CRC.7 XOR CRC.1 XOR CRC.0 XOR [new incoming bit])
-- CRC.n is meant to extract bit n from the 8 bit CRC register
```

For a parallel 8 bit calculation of CRC in your CPU, you can use a look-up table. Additional algorithms can be found in literature.

5.3 UART Signals

The UART interface on the TMC5072 has following signals:

TMC5072 UART INTERFACE SIGNALS	
SWIOP	Non-inverted data input and output
SWION	Inverted data input and output for use in differential transmission. Can be left open in a 5V IO voltage system. Tie to the half IO level voltage for best performance in a 3.3V single wire non-differential application.
NEXTADDR	Address increment pin for sequential addressing scheme
SDO/RING	A low level on this input selects standard mode, a high level switches to ring mode

In UART mode (SW_SEL high) the slave checks the single wire SWIOP and SWION for correctly received datagrams with its own address continuously. Both signals are switched as input during this time. It adapts to the baud rate based on the sync nibble, as described before. In case of a read access, it switches on its output drivers on SWIOP and SWION and sends its response using the same baud rate.

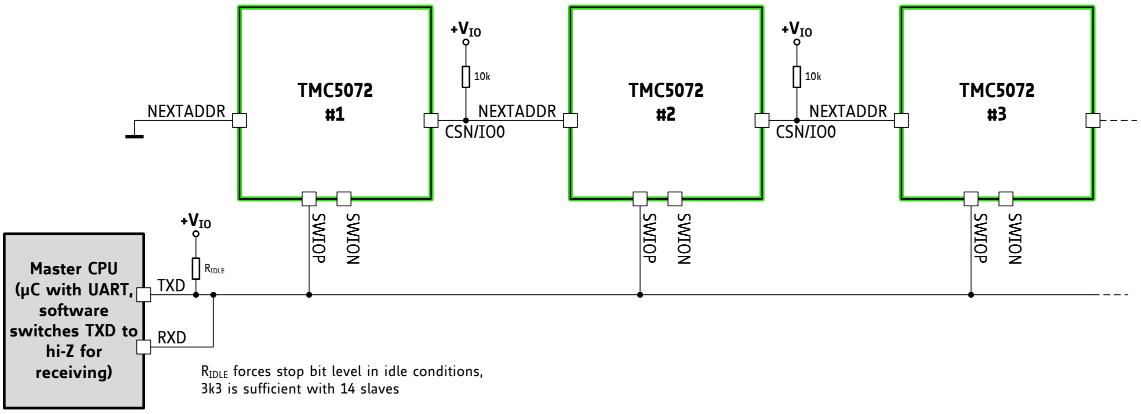
5.4 Addressing Multiple Slaves

Addressing one or two Slaves

If only one or two TMC5072 are addressed by a master using a single UART interface, a hardware address selection can be done by *setting the NEXTADDR pins to different levels*.

Addressing up to 255 Slaves

A different approach can address any number of devices by *using the input NEXTADDR as a selection pin*. Addressing up to 255 units is possible.



R_{IDLE} forces stop bit level in idle conditions, 3k3 is sufficient with 14 slaves

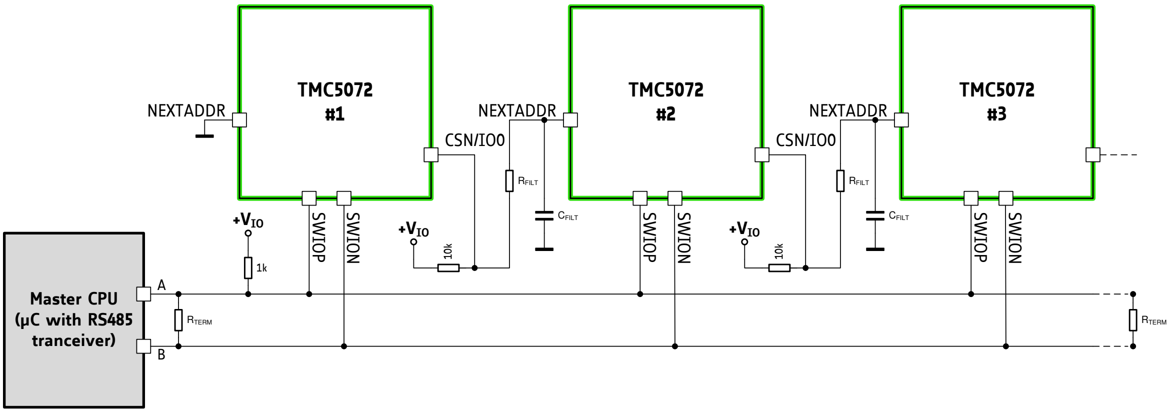
Example for addressing up to 255 TMC5072

Addressing phase 1:	address 0, IO0 is high-Z	address 1	address 1
Addressing phase 2:	program to address 254 & set IO0 low	address 0, IO0 is high-Z	address 1
Addressing phase 3:	address 254	program to address 253 & set IO0 low	address 0
Addressing phase 4:	address 254	address 253	program to address 252 & set IO0 low
Addressing phase *X*:	*continue procedure*		

Figure 5.1 Addressing multiple TMC5072 via single wire interface using chaining

Proceed as follows:

- Tie the NEXTADDR pin of your first TMC5072 to GND.
- Interconnect one of the general purpose IO-pins of the first TMC5072 to the next drivers NEXTADDR pin using an additional pull-up resistor. Connect further drivers in the same fashion.
- Now, the first driver responds to address 0. Following drivers are set to address 1.
- Program the first driver to its dedicated slave address. Note: once a driver is initialized with its slave address, its general purpose output, which is tied to the next drivers NEXTADDR has to be programmed as output and set to 0.
- Now, the second driver is accessible and can get its slave address. Further units can be programmed to their slave addresses sequentially.



Example for addressing up to 255 TMC5072

Addressing phase 1:	address 0, IO0 high	*address 1*	*address 1*
Addressing phase 2:	program to address 254 & set IO0 low	address 0, IO0 high	*address 1*
Addressing phase 3:	address 254	program to address 253 & set NAO low	address 0, IO0 high
Addressing phase 4:	address 254	address 253	program to address 252 & set IO0 low
Addressing phase *X*:	*continue procedure*		

Figure 5.2 Addressing multiple TMC5072 via differential interface, additional filtering for NEXTADDR

A different scheme (not shown) uses bus switches (like 74HC4066) to connect the bus to the next unit in the chain without using the NAI input. The bus switch can be controlled in the same fashion, using the NAO output to enable it (low level shall enable the bus switch). Once the bus switch is enabled it allows addressing the next bus segment. As bus switches add a certain resistance, the maximum number of nodes will be reduced.

It is possible to mix different styles of addressing in a system. For example a system using two boards with each two TMC5072 can have both devices on a board with a different level on NEXTADDR, while the next board is chained using analog switches separating the bus until the drivers on the first board have been programmed.