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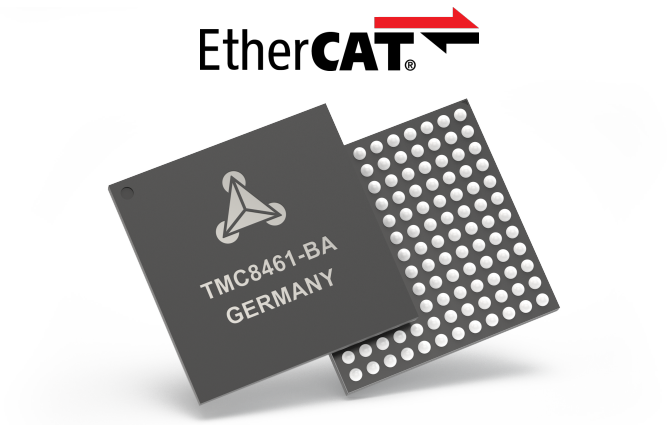
TMC8461 Datasheet

Document Revision V1.2 • 2018-Mar-16

The TMC8461 is a complete EtherCAT® Slave Controller optimized for real time. It comprises all blocks required for an EtherCAT slave including two switch regulator power supplies and 24V capable high voltage I/Os for industrial environments. Timer, watchdog, PWM and SPI/IIC master units allow for enhanced capabilities either in device emulation mode or in combination with an external CPU.



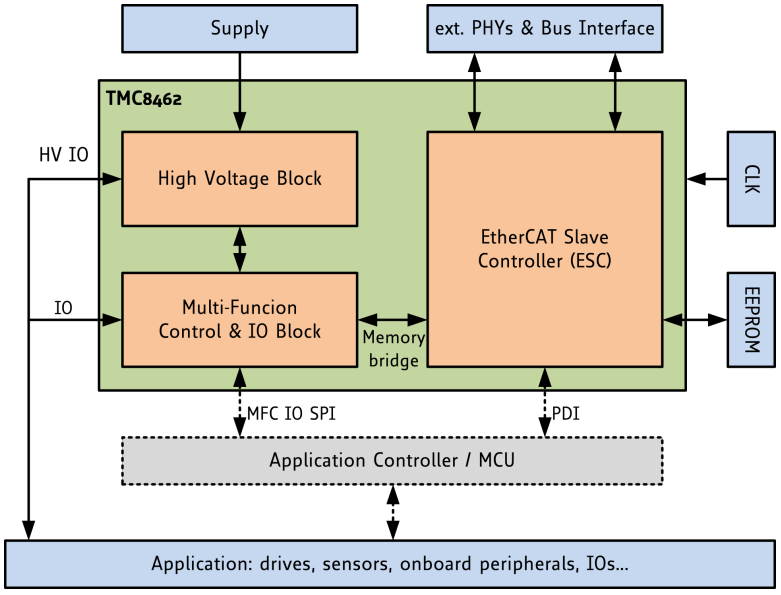
Features

- Standard compliant EtherCAT® Slave
- 2 MII Interfaces for external Ethernet PHY
- SPI Process Data Interface (PDI)
- IO Block with 24 Multi-Function I/Os
- Internal 3.3V plus free 5V-24V switch regulator
- 8 High Voltage I/Os (up to 35V, 100mA)
- Multifunction block comprises Watchdog, 4 PWM outputs and Step/Dir generator
- Direct EtherCAT access to external ADCs, stepper motor controllers, etc.
- EtherCAT-P compatible voltage range

Applications

- Factory Automation
- Process Automation
- Communication Modules
- Industrial IoT
- Industry 4.0
- Sensors & Encoders
- Robotics
- Industrial Motion Control
- Building Automation

Simplified Block Diagram



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TRINAMIC
MOTION CONTROL

Contents

1 Product Features 5

2 Order Codes 6

3 Principles of Operation / Key Concepts 7
3.1 General Device Architecture . . . 7
3.2 EtherCAT Slave Controller . . . 8
3.3 Multi-Function and Control IO Block . . . 8
3.4 Analog and High Voltage Block . . . 9
3.5 Interfaces . . . 10
3.6 Software- and Tool-Support . . . 10

4 Device Pin Definitions 15
4.1 Pinout and Pin Coordinates of TMC8461-BA . . . 15
4.2 Signal Descriptions . . . 15

5 Device Usage and Handling 23
5.1 Process Data Interface . . . 23
5.1.1 SPI protocol description . . . 24
5.1.2 Timing example . . . 26
5.2 MFC IO Control Interface . . . 27
5.2.1 SPI Protocol description . . . 27
5.2.2 Timing example . . . 28
5.2.3 Sharing Bus Lines with the PDI SPI . . . 28
5.3 Ethernet Interface . . . 30
5.3.1 Ethernet PHYs . . . 32
5.4 External Circuitry and Applications Examples . . . 33
5.4.1 Device Reset . . . 33
5.4.2 Supply Filtering for PLL Supply . . . 33
5.4.3 External Circuit for Fixed Switching Regulator 0 . . . 34
5.4.4 External Circuit for Adjustable Switching Regulator 1 . . . 35
5.4.5 Minimum External Supply Circuit for Single 3.3V Supply . . . 36
5.4.6 Minimum External Supply Circuit for Single 5V Supply . . . 37
5.4.7 Minimum External Supply Circuit for Single Supply >5V . . . 38
5.4.8 Typical Power Supply Chain Using Both Buck Converters . . . 39
5.4.9 Status LED Circuit . . . 39
5.4.10 SII EEPROM Circuit . . . 40

6 EtherCAT Slave Controller Description 41
6.1 General EtherCAT Information . . . 41
6.2 Overview of Available Chip Features . . . 42
6.3 EtherCAT Register Overview . . . 44
6.4 EtherCAT Register Set . . . 50
6.4.1 ESC Information . . . 50
6.4.2 Station Address . . . 54
6.4.3 Write Protection . . . 55
6.4.4 Data Link Layer . . . 57
6.4.5 Application Layer . . . 62
6.4.6 PDI . . . 65
6.4.7 Interrupts . . . 69
6.4.8 Error Counters . . . 72
6.4.9 Watchdogs . . . 75
6.4.10 SII EEPROM Interface . . . 78

6.4.11 ESC Parameter RAM . . . 82
6.4.12 MII Management Interface . . . 83
6.4.13 FMMUs . . . 87
6.4.14 SyncManagers . . . 90
6.4.15 Distributed Clocks Receive Times . . . 94
6.4.16 Distributed Clocks Time Loop Control Unit . . . 95
6.4.17 Distributed Clocks Cyclic Unit Control . . . 99
6.4.18 Distributed Clocks SYNC Out Unit . . . 100
6.4.19 Distributed Clocks LATCH In Unit . . . 104
6.4.20 Distributed Clocks SyncManager Event Times . . . 108
6.4.21 ESC Specific . . . 109
6.4.22 Process Data RAM . . . 110

7 MFC IO Block Description 111
7.1 General Information . . . 111
7.2 MFC IO Register Overview . . . 113
7.3 MFC IO Register Set . . . 116
7.3.1 Incremental Encoder Interface . . . 116
7.3.2 SPI Master Interface . . . 119
7.3.3 I2C Master Interface . . . 121
7.3.4 Step and Direction Signal Generator . . . 123
7.3.5 PWM Unit . . . 129
7.3.6 General Purpose I/Os . . . 133
7.3.7 DAC Unit . . . 134
7.3.8 IRQ Control Block . . . 135
7.3.9 Watchdog . . . 137
7.3.10 High Voltage Status and General Control . . . 140
7.3.11 Application Layer Control . . . 144
7.4 SII EEPROM MFC IO Block Parameter Map . . . 145
7.5 SII EEPROM MFC IO Crossbar Mapping . . . 149
7.6 SII EEPROM MFC IO High Voltage IO (HVIO) Configuration . . . 153
7.7 SII EEPROM MFC IO Switching Regulator Configuration . . . 154
7.8 SII EEPROM MFC IO Memory Block Mapping . . . 156
7.9 SII EEPROM MFC IO Register Configuration . . . 157
7.10 MFC IO ESI/XML Configuration Block . . . 158
7.11 MFC IO Incremental Encoder Block . . . 159
7.12 MFC IO SPI Master Block . . . 161
7.12.1 SPI Examples . . . 162
7.13 MFC IO I2C Master Block . . . 166
7.13.1 I2C Example . . . 168
7.14 MFC IO Step and Direction Block . . . 170
7.15 MFC IO PWM Block . . . 173
7.16 MFC IO DAC Block . . . 179
7.17 MFC IO General Purpose IO Block . . . 180
7.18 MFC IO IRQ Block . . . 181
7.19 MFC IO Watchdog Block . . . 182
7.20 MFC IO Emergency Switch Input . . . 186
7.21 MFC IO Analog and High Voltage Block . . . 187
7.21.1 Multi Voltage High Current I/O Lines . . . 187
7.21.2 Switching Regulators . . . 188
7.21.3 Analog Block Status Register . . . 189

8 Electrical Ratings **191**
8.1 Absolute Maximum Ratings . . . 191
8.2 Operational Ratings . . . 191
8.3 DC Characteristics and Timing Characteristics . . . 192
8.3.1 High Voltage I/O Block . . . 192
8.3.2 Switching Regulators . . . 193
8.3.3 Digital IOs . . . 194

9 Manufacturing Data **195**
9.1 Package Dimensions . . . 195
9.2 Marking . . . 197
9.3 Board and Layout Considerations . . . 197

10 Abbreviations **198**

11 Figures Index **200**

12 Tables Index **201**

13 Revision History **204**
13.1 IC Revision . . . 204
13.2 Document Revision . . . 204

1 Product Features

TMC8461 is an advanced EtherCAT Slave Controller device used for EtherCAT communication. It provides the interface for data exchange between EtherCAT master and the slave's local application controller. In addition, TMC8461 provides complex IO functions paired with high voltage features.

Advantages:

- Fully standard compliant and proven EtherCAT engine
- Highly integrated with highest feature count vs. package size
- License-free & royalty-free
- High Voltage & robust
- Saves board space & reduces BOM
- Long-term availability

Major Features:

- EtherCAT Slave Controller with 2 MII ports, 8 FMMU & 8 Sync Managers, Distributed clocks (64 bit), 16KByte ESC RAM size, external I2C EEPROM, SPI Process Data Interface (PDI), optional device emulation
- TRINAMIC Multi-Function Control and IO block with 24 configurable IO ports for complex real-time IO functions (GPIOs, PWM, Step/Direction, I2C, SPI, DAC, incremental encoder, and high voltage IOs)
- TRINAMIC high voltage block with 8 short circuit protected push-/pull or open drain high voltage IOs for up to 24V and 100mA drive current
- Two integrated 500mA step down switching voltage regulators with one being fixed at 3.3V and one being programmable between 5V and 24V
- Simple configuration of EtherCAT Slave Controller and Multi-Function Control and IO block via SII EEPROM
- Single supply voltage depending on application: 3.3V only or 5V to 35V (5V, 12V, or 24V typical)
- Industrial Temperature Range -40°C to +85°C
- Integrated temperature measurement and over-temperature shutdown
- Package: 10mm x10mm BGA packge with 144 pins and 0.8mm pitch

2 Order Codes

Order Code	Description	Size
TMC8461-BA	TMC8461 Advanced EtherCAT® Slave Controller in 144 pin BGA package with 0.8mm pitch	10mm x 10mm
TMC8461-EVAL	Evaluation Board for TMC8461-BA, RJ45 TPC interface, +5V...+24V	79mm x 85mm

Table 1: TMC8461 order codes

Trademark and Patents

EtherCAT® is a registered trademark and patented technology, licensed by Beckhoff Automation GmbH, Germany.

3 Principles of Operation / Key Concepts

TMC8461 is a highly integrated ASIC providing the interface between the Ethernet-based EtherCAT real-time field bus and the local application. Its extended digital and high voltage feature set provides additional functions to the EtherCAT slave.

3.1 General Device Architecture

Figure 1 shows the general device architecture and major connections of TMC8461. The three function blocks EtherCAT Slave Controller, Multi-Function Control and IO, and Analog and High Voltage are introduced in the following sub-sections.
For operation, a stable 100MHz clock source, an IIC EEPROM, and power supply for IO and high voltage operation are required (if the high voltage features are used). An application controller, which also runs the EtherCAT slave stack, connects to the SPI interfaces. The application and onboard peripherals can be controlled by the application controller or the Multi-Function Control and IO block.

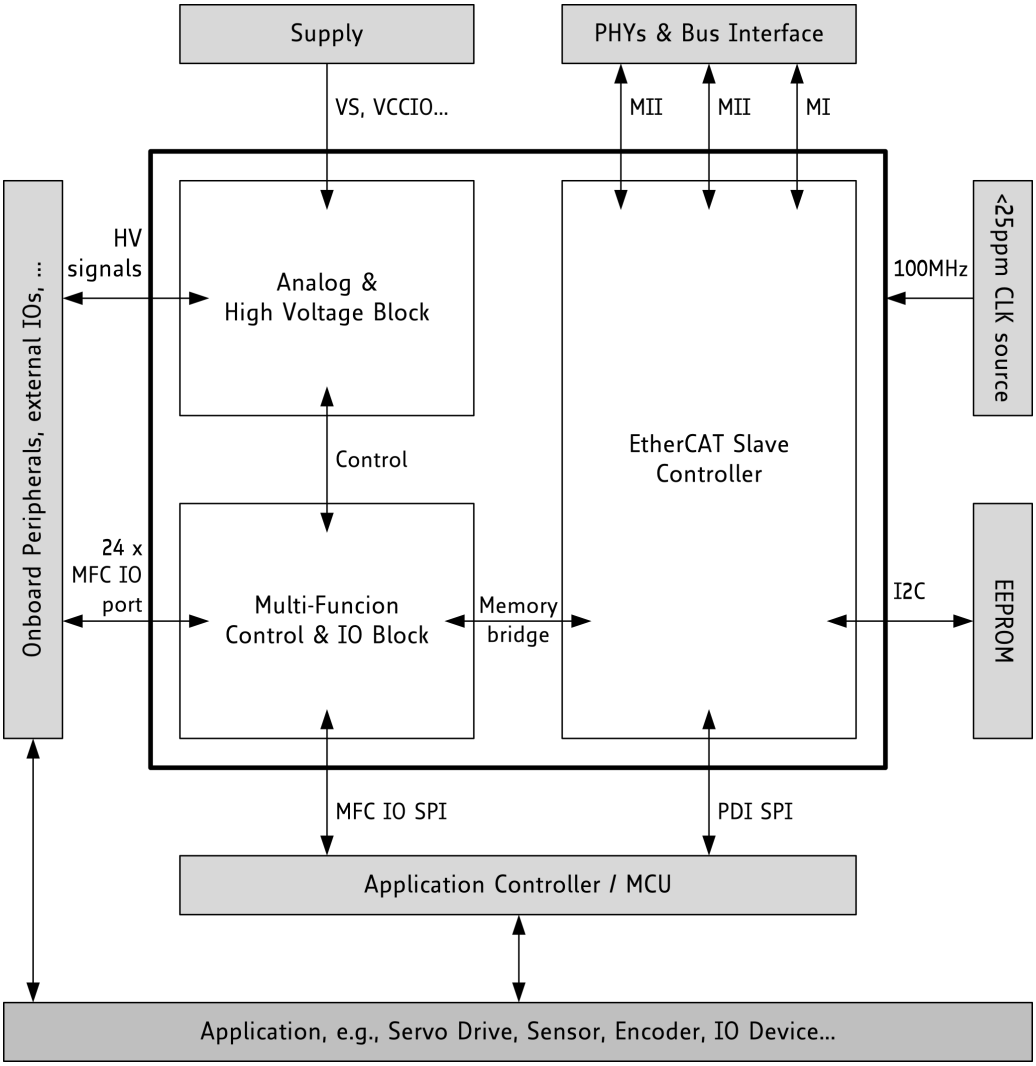

Figure 1: General device architecture

3.2 EtherCAT Slave Controller

TMC8461 contains a standard-conform EtherCAT Slave Controller (ESC) providing real-time EtherCAT MAC layer functionality to EtherCAT slaves. It connects via MII interface to standard Ethernet PHYs and provides a digital control interface to a local application controller while also providing the option for standalone operation.

The ESC part of TMC8461 provides the following EtherCAT-related features. More information is available in Section 6.

- Two Media Independent Interface (MII) to external Ethernet PHYs
- Eight Fieldbus Memory Management Units (FMMU)
- Eight Sync Managers (SM)
- 16 KByte of Process Data RAM (PDRAM)
- 64B bit Distributed Clocks support
- I2C interface for external EEPROM for ESC configuration
- SPI Process Data Interface (PDI) with 30Mbit/s
- Proven EtherCAT State Machine (ESM)
- Device Emulation Mode

3.3 Multi-Function and Control IO Block

In addition to the EtherCAT functionality, the TMC8461 comes with a dedicated function block providing a configurable set of complex real-time IO functionality for smart (embedded) EtherCAT slave systems. This IO functionality is called Multi-Function Control and IO block (MFC IO). Its special focus is on motor and motion control while it is not limited to this application area.
The MFC IO block combines various functional sub blocks that are helpful in an embedded design to reduce complexity, to simplify bill of materials (BOM), and to provide hardware acceleration to compute intensive or time critical tasks. More information is available in Section 7.

Configurable IO Ports The whole MFC IO block provides in total 24 IO ports that can be configured and assigned to any of the available functional units inside the MFC IO block. If not used, each IO port can be tristated.

General Purpose IOs Up to sixteen (16) general purpose IOs are available. Each IO can be configured either as input or as output. For the outputs, a safe state can be configured which is used in case of emergency event.

Incremental Encoder Interface Configurable incremental encoder interface with 32 bit position registers, single-ended or differential inputs, configurable counting constant for different resolutions, configurable polarity and N-signal behavior.

Step/Direction Generator Block The step and direction unit provides upt to 3 independent channels. Various configuration options and modes allow for example for continuous or one-shot mode, reading of the internal total step counters, pre-loading the next step frequency to be used at a certain counter value. The step and direction outputs signals can be single-ended or differential.

PWM Block The integrated PWM block provides up to 4 PWM channels. PWM frequency and duty cycle as well as polarities and dead times are configurable. The outputs can be configured for a safe state in case of emergency.

Generic SPI Master Interface The TMC8461 provides a generic SPI master interface to connect to on- or off-board SPI slave peripherals like ADCs, sensors, or motor drivers. The SPI master interface is fully configurable and offers 4 slave select lines.

Generic I2C Master Interface A generic I2C master interface is also available in TMC8461 to connect to I2C slaves. The I2C bus speed is configurable.

Digital DAC A simple digital 16 bit DAC channel is available which requires an external RC circuit for operation.

Safety Functions The following safety functions are available with the TMC8461

- Configurable watchdog functionality for the MFC IO block to monitor internal and external signals as well as EtherCAT activity. This block is fully configurable.
- A general emergency switch input can be activated. For critical outputs, a safe state can be configured which is used when the emergency switch triggers.
- A common IRQ signal is available at the MFC IO block which can be mapped to various events of the MFC IO block. The IRQ events can be processed by a local application controller.

3.4 Analog and High Voltage Block

TMC8461 has an integrated powerful high voltage sub block that provides analog functions and high voltage support to your EtherCAT slave. The integrated high voltage capabilities allow for BOM reduction and save board space. More information is available in Section 7.21.

High Voltage Ports 8 of the 24 configurable IO ports of the MFC IO block are high voltage IO ports. For pure digital systems operating at 3.3V or 5V these ports can simply be used as standard IO ports. When using a higher supply voltage at the VIOx inputs the high voltage ports can be used at up to 35V (5V, 12V, 24V typical). The 8 high voltage ports are grouped into 3 groups with 2, 3, and 3 ports. Each group can be used a different supply voltage level using VIO1, VIO2, and VIO3 inputs.
Each high voltage port has a short circuit protected push-/pull or open drain output stage with 100mA drive (ca. 200mA short time) and can be combined with any signal of the MFC IO block functions. The outputs' slope can be controlled. An optional input filter is selectable as well as pull downs or pull ups with $100\mu A$.
The high voltage ports have an over-temperature shutdown.

⚠ WARNING When driving inductive loads a freewheeling diode must be provided to the high voltage I/O pins to prevent from latch-up.

Switching Regulators Two switching regulators (buck regulators) are integrated into TMC8461 – SW0 and SW1. Both are capable of driving up to 500mA.
SW0 generates a fixed 3.3V rail for internal and external logic supply. SW1 is programmable between 3.3V and VS (up to 24V) and can be used for peripheral supply, e.g, to generate a 5V encoder supply.
Each switching regulator comes with a separate over-temperature shutdown.

Single Supply Operation TMC8461 is designed to work with a single external power supply rail. All required supply voltages are generated internally. The required external supply rail depends on the application scenario (between 3.3V and 24V).

3.5 Interfaces

ESC Process Data Interface The ESC part can be accessed via the so-called Process Data Interface (PDI). TMC8461 comes with an SPI PDI. Besides the standard SPI bus lines additional control signals belong to the SPI PDI, which are further described in Section 5.1..

MFC IO Control Interface The MFC IO block of TMC8461 can be accessed from EtherCAT master side or from the local application controller. For connection to the local application controller, a second SPI interface – the MFC IO SPI – is provided. The protocol used nearly identical to the SPI PDI interface. Additional information on the MFC IO SPI is given in Section 5.2.

Ethernet PHY Connection TMC8461 provides 2 communication ports and connects to 100Mbit Ethernet PHYs via MII running at 25MHz.
In addition, each PHY can be connected to the PHY Management Interface (MI) for functions like link state detection when not using dedicated LINK signals.

EEPROM Interface The EEPROM interface is intended to be a point-to-point interface between TMC8461 and EEPROM with TMC8461 being the master. If other I2C masters are required to access the I2C bus, TMC8461 must be held in reset state, for example for in-circuit-programming of the EEPROM. During operation, the application controller must tristate its I2C interface. Depending on the EEPROM size the addressing mode must be properly set using the PROM_SIZE configuration pin.

Configuration Inputs Hard-wired configuration pins are available at the TMC8461, which are used to configure various options related to the hardware configuration and application scenario and which will not change. These pins are PROM_SIZE, MII_TX_SHIFT[x], PHY_OFFSET, LINK_POLARITY, PDI_SHARED_SPI_BUS, and DEVICE_EMULATION.
More information on these configuration pins and signals is given in Section 4.2 and Section 5.

3.6 Software- and Tool-Support

TRINAMIC's EtherCAT Slave Controller family comes with extensive hardware and software tool support to get started quickly.

Evaluation Board An evaluation board is available for the TMC8461. The evaluation board comes with on-board 100-Mbit Ethernet PHYs and standard RJ45 connectors and transformers for interfacing twisted pair copper (TPC) media.

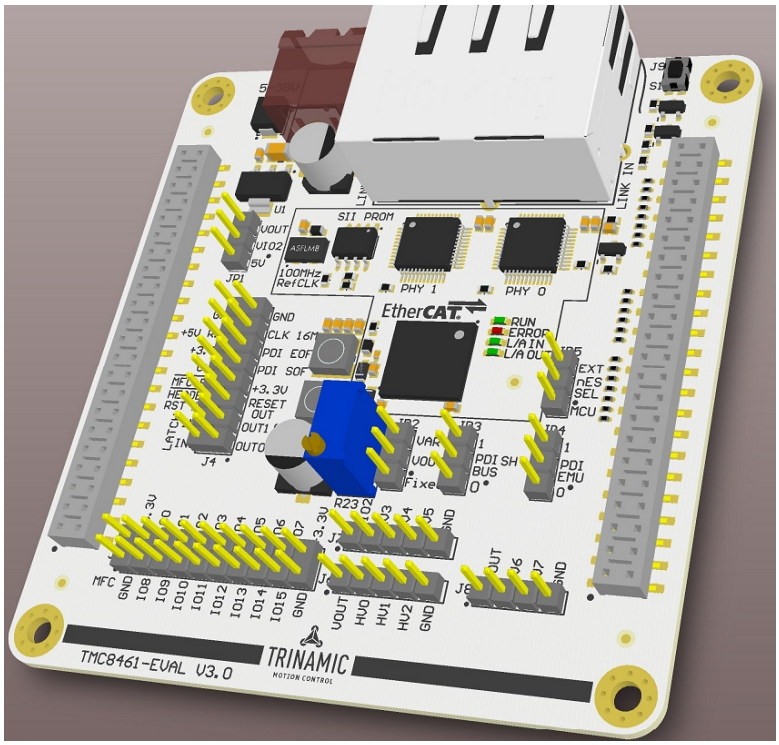

Figure 2: TMC8461 Evaluation Board

The complete board design files are available for download and can be used as reference. All information is available for download from the evaluation board section on TRINAMIC's website at https://www.trinamic.com/support/eval-kits/.

Breakout Board (BOB) Besides the Evaluation board another smaller breakout board is available. It allows for easy integration into own systems or connection to a prototyping platform. The breakout board provides the bus interface along with the ESC and requires an appropriate supply and controller connection. The BOB comes with standard RJ45 connectors to connect to TPC using the TMC8462 ESC with integrated Ethernet PHYs. TMC8462 is functionally equal to the TMC8461. The difference is in using external PHYs vs. integrated PHYs. The complete board design files are available for download and can be used as reference. All information is available for download from the evaluation board section on TRINAMIC's website at
https://www.trinamic.com/support/eval-kits/.

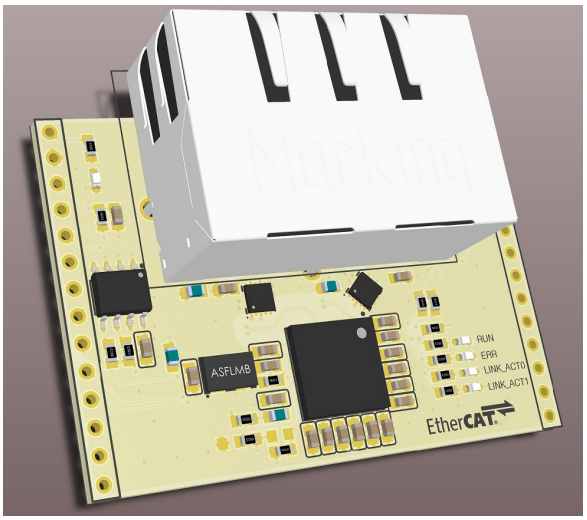

Figure 3: TMC8462 breakout board for RJ45 and TPC

TRINAMIC Technology Access Package In addition, a comprehensive source code and software package – TRINAMIC Technology Access Package (TTAP) – is available for download to get started quickly with own code.
The TTAP is available at `https://www.trinamic.com/support/software/access-package/`.

TMCL-IDE The TMCL-IDE is TRINAMIC's primary tool (for Windows PCs) to control TRINAMIC modules and evaluation boards. Besides, it provides feature like remote firmware updates, module monitoring options, and specific Wizard support. The TMCL-IDE can be used along with TRINAMICs modular evaluation board system.

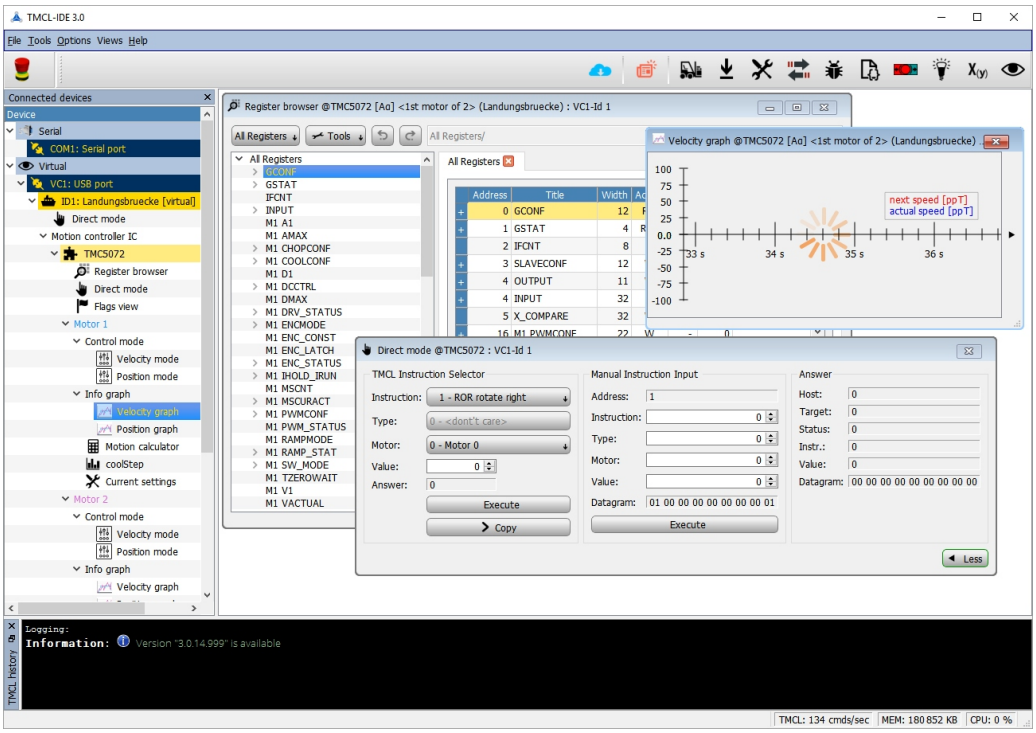

Figure 4: TMCL-IDE

The latest version and additional information is available for download from TRINAMIC's website at http://www.trinamic.com/software-tools/tmcl-ide.

EtherCAT Slave Configuration Configuration of the EtherCAT Slave Controller is done during boot time with configuration information read from the SII EEPROM after reset or power cycling. This information must be (pre)programmed into the SII EEPROM. This can be done via the EtherCAT master using a so-called EtherCAT Slave Information (ESI) file in standardized XML format. The SII EEPROM can also be (re)written using the local application controller.

Wizard The TMCL-IDE contains a wizard to assist users with the configuration of the TMC8461 various MFC IO functions. The wizard shows available and allowed options and provides XML code snippets for the ESI file for the SII EEPROM as well as generic C-Code blocks. These can be used as starting point for own firmware development for the application controller.

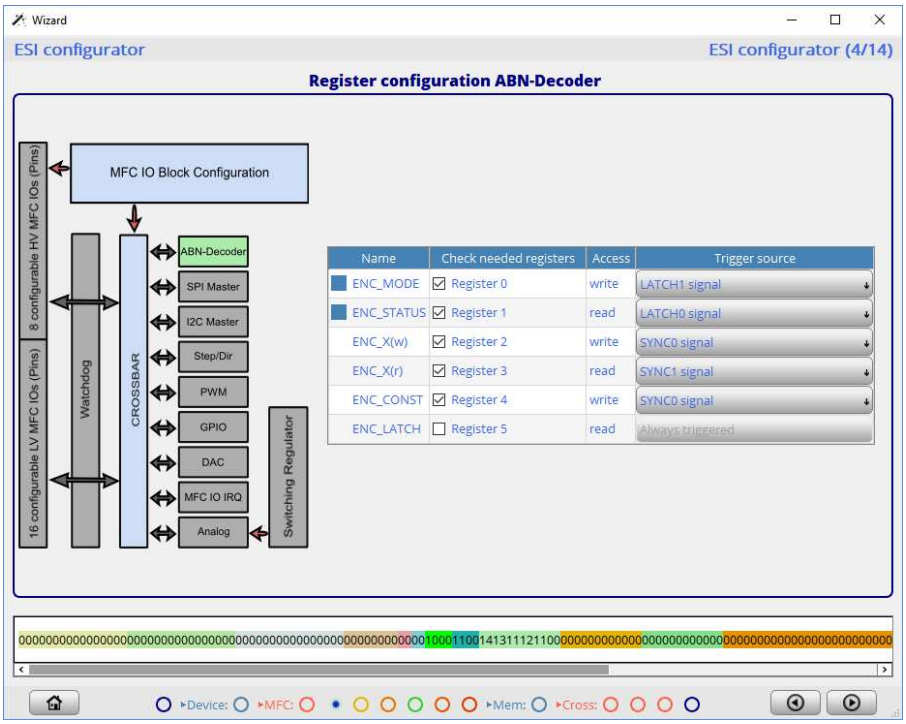

Figure 5: Configuration wizard example – MFC IO block configuration

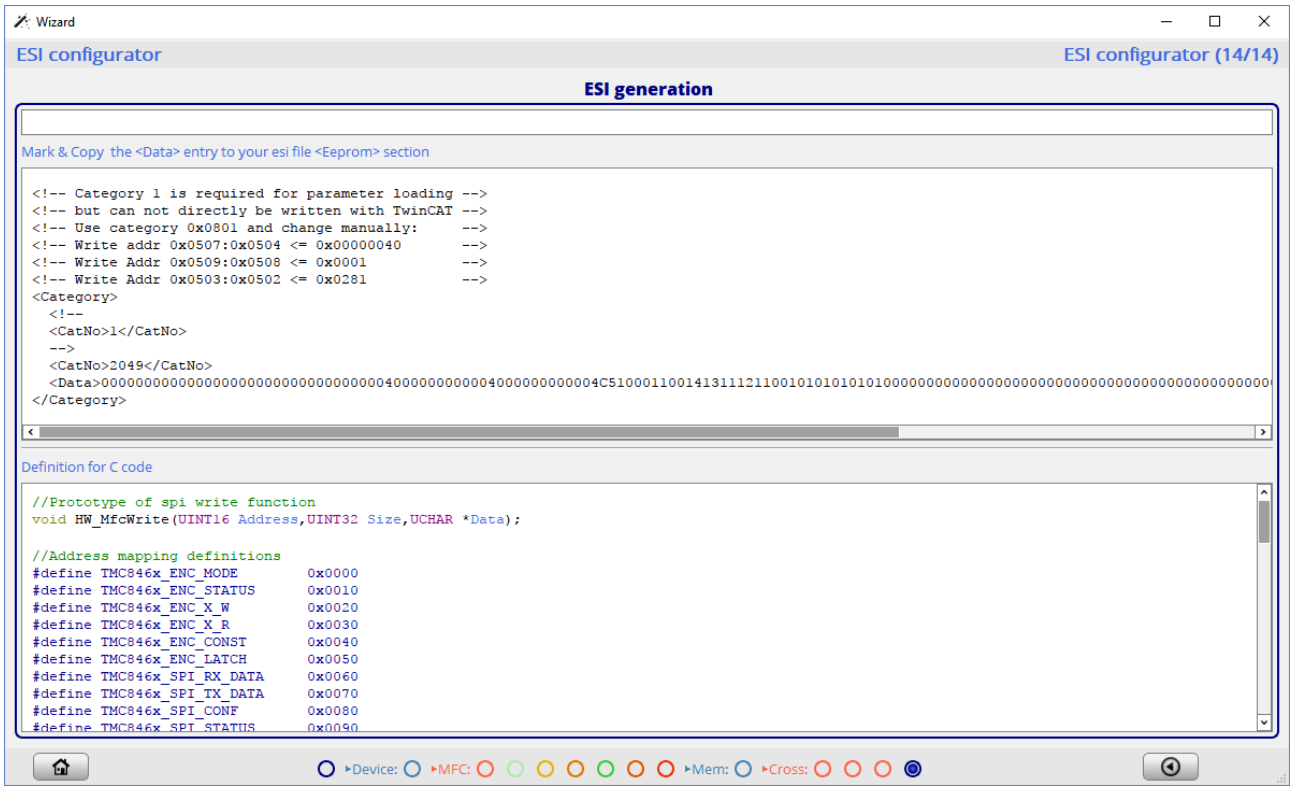

Figure 6: Configuration wizard example – SII EEPROM content and C-code output

4 Device Pin Definitions

4.1 Pinout and Pin Coordinates of TMC8461-BA

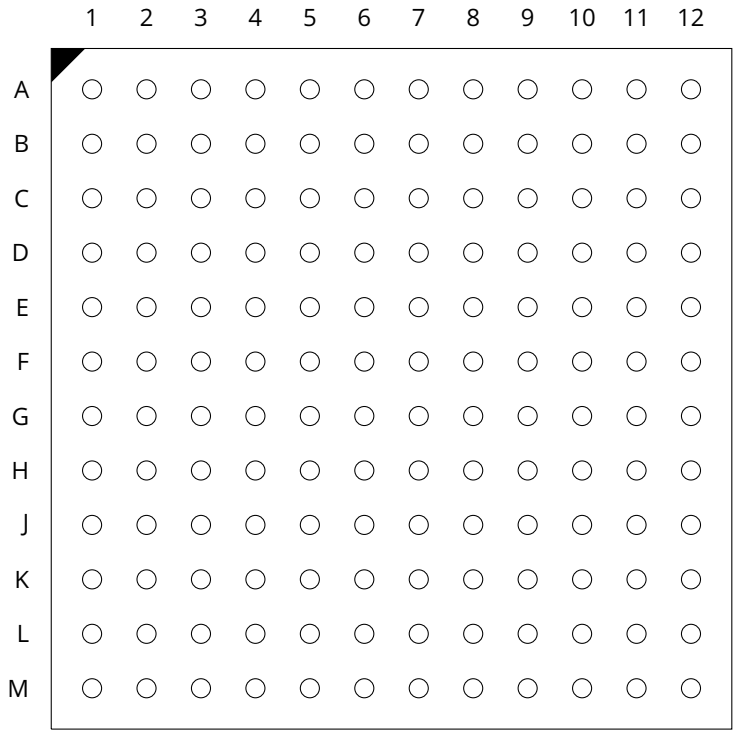

Figure 7: TMC8461-BA Pinout top view

4.2 Signal Descriptions

Name	Pin	Type (I,O,PU,PD)	Function
General Signals			
NRESET	J8	I/O	Low active system reset. NRESET is an I/O pin. Connected to VCCIO via a 10K resistor and to GND via a 10nF capacitor if no other reset source for proper power-on reset is used. For more information see Section **??**.
REF_CLK100_IN	M4	I	100MHz Reference clock input, connect to a clock source <25ppm.
CLK16_OUT	H8	O	16.6MHz auxiliary clock output. Not available during reset.
EN_CLK16_OUT	G10	I	Enable signal for CLK16_OUT: 0 = off, 1 = on
CLK25_OUT0	E3	O	25MHz clock output, e.g., for IN port PHY
CLK25_OUT1	H3	O	25MHz clock output, e.g., for OUT port PHY

Name	Pin	Type (I,O,PU,PD)	Function
RESET_OUT	K8	O	This high-active reset output is activated via EtherCAT register 0x0040), therefore RESET_OUT has to trigger the NRESET input, which clears RESET_OUT. This connection incl. changing the polarity has to be made externally .

EEPROM IOs			
PROM_INIT	J7	O	Signal indicating that EEPROM has been loaded, 0 = not ready, 1 = EEPROM loaded
PROM_CLK	J5	O	External I2C EEPROM clock signal, **use 1K pull up resistor to 3.3V**
PROM_DATA	J6	I/O	External I2C EEPROM data signal, **use 1K pull up resistor to 3.3V**
PROM_SIZE	E9	I	Selects between two different EEPROM sizes since the communication protocol for EEPROM access changes if a size > 16k is used (an additional address byte is required then). 0 = up to 16K EEPROM, 1 = 32 kbit-4Mbit EEPROM

DC Synchronization IOs			
SYNC_OUT0	D8	O	Distributed Clocks synchronization output 0, Typically connect to MCU
SYNC_OUT1	E8	O	Distributed Clocks synchronization output 1, typically connect to MCU
LATCH_IN0	C8	I	Latch input 0 for distributed clocks, connect to GND if not used.
LATCH_IN1	C7	I	Latch input 1 for distributed clocks, Connect to GND if not used.

LEDs			
LED_RUN	C5	O	Run Status LED, connect to green LED (Anode) 0 = LED off, 1 = LED on
LED_ERR	C4	O	Error Status LED, connect to red LED (Anode) 0 = LED off, 1 = LED on
LINK_ACT0	D4	O	Link In Port Activity, connect to green LED (Anode) 0 = LED off, 1 = LED on
LINK_ACT1	D5	O	Link Out Port Activity, connect to green LED (Anode) 0 = LED off, 1 = LED on

Name	Pin	Type (I,O,PU,PD)	Function
Process Data Interface IOs to/from MCU			
PDI_SOF	L4	O	Ethernet Start-of-Frame if 1
PDI_EOF	K4	O	Ethernet End-of-Frame if 1
PDI_SPI_CSN	M5	I	Chip select signal of the process data interface
PDI_SPI_SCK	L5	I	Serial clock signal of the process data interface
PDI_SPI_MOSI	M6	I	Serial data out signal of the process data interface
PDI_SPI_MISO	L6	O	Serial data in signal of the process data interface
PDI_SPI_IRQ	K5	O	Interrupt signal for primary process data interface, Connect to MCU
PDI_WDSTATE	H7	O	Watchdog state, 0: Expired, 1: Not expired
PDI_WDTRIGGER	H6	O	Watchdog trigger if 1
PDI_EMULATION	H9	I	Selects between PDI interface (SPI) or standalone operation with state machine emulation inside ESC. Has weak internal pull down. 0 = default, PDI interface active, 1 = standalone operation, state machine emulation

MFC IO Control Interface IOs			
MFC_CTRL_SPI_CSN	D6	I	Chip select signal of the MFC IO control interface
MFC_CTRL_SPI_SCK	E4	I	Serial clock signal of the MFC IO control interface
MFC_CTRL_SPI_MOSI	D7	I	Serial data out signal of the MFC IO control interface
MFC_CTRL_SPI_MISO	E5	O	Serial data in signal of the MFC IO control interface
MFC_IRQ	E6	O	MFCIO block IRQ for configurable events, connect to MCU, high active
MFC_NES	C6	I	low active (not) Emergency Stop/Switch/Halt (to bring PWM or other outputs into a safe state), the event must be cleared actively, has weak internal pull down, must be driven high for normal operation
PDI_SHARED_BUS	F10	I	Selects between separate SPI buses (MISO, MOSI, SCK) or one SPI bus with two CS lines for the PDI and MFC CTRL SPI interface: 0 = two separate SPI buses, 1 = one shared SPI bus using the PDI_SPI_x bus lines

Name	Pin	Type (I,O,PU,PD)	Function
MFC IOs			
MFCIO00	K9	I/O	MFCIO block low voltage I/O
MFCIO01	K10	I/O	MFCIO block low voltage I/O
MFCIO02	K11	I/O	MFCIO block low voltage I/O
MFCIO03	K12	I/O	MFCIO block low voltage I/O
MFCIO04	J9	I/O	MFCIO block low voltage I/O
MFCIO05	J10	I/O	MFCIO block low voltage I/O
MFCIO06	J11	I/O	MFCIO block low voltage I/O
MFCIO07	J12	I/O	MFCIO block low voltage I/O
MFCIO08	D9	I/O	MFCIO block low voltage I/O
MFCIO09	D10	I/O	MFCIO block low voltage I/O
MFCIO10	D11	I/O	MFCIO block low voltage I/O
MFCIO11	D12	I/O	MFCIO block low voltage I/O
MFCIO12	C9	I/O	MFCIO block low voltage I/O
MFCIO13	C10	I/O	MFCIO block low voltage I/O
MFCIO14	C11	I/O	MFCIO block low voltage I/O
MFCIO15	C12	I/O	MFCIO block low voltage I/O

MFC High Voltage IOs			
MFC_HV0 (MFCIO16)	A5	I/O	MFCIO block high voltage I/O
MFC_HV1 (MFCIO17)	A6	I/O	MFCIO block high voltage I/O
MFC_HV2 (MFCIO18)	A7	I/O	MFCIO block high voltage I/O
MFC_HV3 (MFCIO19)	A8	I/O	MFCIO block high voltage I/O
MFC_HV4 (MFCIO20)	A9	I/O	MFCIO block high voltage I/O
MFC_HV5 (MFCIO21)	A10	I/O	MFCIO block high voltage I/O
MFC_HV6 (MFCIO22)	A11	I/O	MFCIO block high voltage I/O
MFC_HV7 (MFCIO23)	A12	I/O	MFCIO block high voltage I/O

Name	Pin	Type (I,O,PU,PD)	Function
MFC High Voltage IO Supplies			
VIO1	B6	I	MFCHVIO block 1 supply voltage
VIO2	B8	I	MFCHVIO block 2 supply voltage
VIO3	B10	I	MFCHVIO block 3 supply voltage
GNDIO1	B7	I	MFCHVIO block 1 ground, **connect to GND**
GNDIO2	B9	I	MFCHVIO block 2 ground, **connect to GND**
GNDIO3	B11	I	MFCHVIO block 3 ground, **connect to GND**

MII Interface to external PHY (EtherCAT IN Port)			
MII_LINK0	C1	I	Link indication input
MII_RX_CLK0	C2	I	Receive clock
MII_RXD0[0]	A2	I	Receive data bit 0
MII_RXD0[1]	A1	I	Receive data bit 1
MII_RXD0[2]	B2	I	Receive data bit 2
MII_RXD0[3]	B1	I	Receive data bit 3
MII_RX_DV0	B3	I	Receive data valid signal
MII_RX_ERR0	A3	I	Receive error signal
MII_TX_CLK0	D2	I	Transmit clock
MII_TXD0[0]	D1	O	Transmit data bit 0
MII_TXD0[1]	E2	O	Transmit data bit 1
MII_TXD0[2]	E1	O	Transmit data bit 2
MII_TXD0[3]	F2	O	Transmit data bit 3
MII_TX_ENA0	F1	O	Transmit enable

Name	Pin	Type (I,O,PU,PD)	Function
MII Interface to external PHY (EtherCAT OUT Port)			
MII_LINK1	K2	I	Link indication input
MII_RX_CLK1	K1	I	Receive clock
MII_RXD1[0]	H1	I	Receive data bit 0
MII_RXD1[1]	H2	I	Receive data bit 1
MII_RXD1[2]	J1	I	Receive data bit 2
MII_RXD1[3]	J2	I	Receive data bit 3
MII_RX_DV1	G2	I	Receive data valid signal
MII_RX_ERR1	G1	I	Receive error signal
MII_TX_CLK1	L1	I	Transmit clock
MII_TXD1[0]	L2	O	Transmit data bit 0
MII_TXD1[1]	M1	O	Transmit data bit 1
MII_TXD1[2]	M2	O	Transmit data bit 2
MII_TXD1[3]	L3	O	Transmit data bit 3
MII_TX_ENA1	M3	O	Transmit enable

PHY Interface Configuration Pins and Management Interface			
LINK_POLARITY	H10	I	selects polarity of the PHYs link signal: 0 = low active, 1 = high active
MII_TX_SHIFT[0]	H12	I	Used for clock shift compensation on TX port, Weak internal pull down
MII_TX_SHIFT[1]	G12	I	Used for clock shift compensation on TX port, Weak internal pull down
PHY_OFFSET	E10	I	PHY Address Offset: 0 = Offset = 0, 1 = Offset = 1
MCLK	F3	O	PHY management clock, connect all PHYs to this bus
MDIO	G3	I/O	PHY management data, connect all PHYs to this bus if required, **use 4K7 pull up resistor to VCCIO (3.3V)**

Name	Pin	Type (I,O,PU,PD)	Function
Device Supply and Ground			
VS	B12	I	Supply voltage, **use a 100nF filter capacitor**
VCCIO	C3, D3, E11, F11, G11, H11, J3, K3	I	I/O supply voltage, **use a 100nF filter capacitor per pin**
VCC_CORE	E7, F6, F7, G6, G7	I	Core supply voltage, **connect to VDD1V8_OUT, use a 100nF filter capacitor per pin**
PLLCLK_VCCIO	L7	I	PLL supply voltage, **connect to VCCIO through a filter (R/L/C)**
TSTCLK_SELECT	K6	I	Test input, **always connect to VCCIO for normal operation**
GND	B4, F4, F5, F8, F9, G4, G5, G8, G9, J4	I	Supply Ground
PLLCLK_GND	K7	I	PLL supply ground, **connect to GND**

Voltage Regulator IOs			
VDD1V8_OUT	F12	O	Output of internal 1.8V regulator, **use a 100nF filter capacitor**
VDD5_OUT	E12	O	Output of internal 5V regulator, **use a 100nF filter capacitor if VS≥5V**

Name	Pin	Type (I,O,PU,PD)	Function
Switching Regulator 0 IOs			
VS0	M8	I	Switching regulator 0 supply voltage, Switching regulator 0 provides a fixed 3.3V output.
GND0	M10	I	Switching regulator 0 ground, **connect to GND**
SW0	M9	O	Switching regulator 0 output, fixed 3.3V
SW_DIODE	L8	I	Switching regulator 0 internal diode, **connect to SW0 only if VS0 is at or below 5V**
GND_DIODE	L9	I	Switching regulator 0 internal diode ground, **connect to GND**
Switching Regulator 1 IOs			
VS1	M12	I	Switching regulator 1 supply voltage, Switching regulator 1 provides an adjustable output voltage.
GND1	L10	I	Switching regulator 1 ground, **connect to GND**
SW1	M11	O	Switching regulator 1 output, adjustable
VOUT	L11	I	Switching regulator 1 inductor ringing suppression feedback
VOUT_FB	L12	I	Switching regulator 1 feedback voltage, 1.2V typically
Test Pins only			
TST_MODE	H4	I	Test mode enable, **connect to GND**
TST_ANA	H5	O	Analog Test output, **leave open**
CLKO_100	M7	O	100MHz clock output

Table 2: Pin and Signal description for TMC8461-BA

5 Device Usage and Handling

5.1 Process Data Interface

The Process Data Interface (PDI) is an SPI interface with a clock frequency of up to 30 MHz. The ESC registers and the process data RAM can be accessed from an external microcontroller using this interface. The interface can be configured via the EEPROM, however it is recommended to use the default configuration – SPI mode 3, low active chip select). For further details, see the ESC SPI slave configuration registers in Section 6.

Additionally some signals are available that can be evaluated by the application controller.

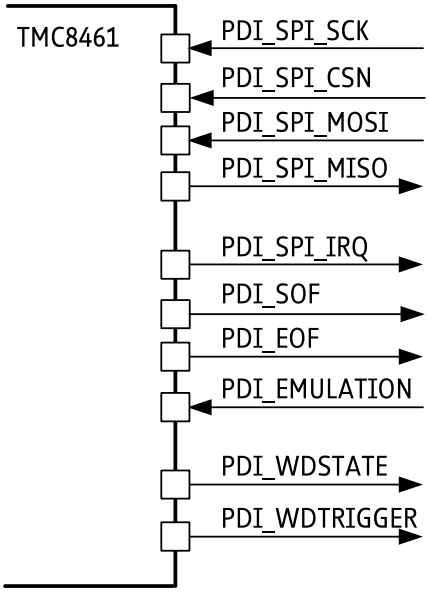

Figure 8: PDI control signals

TMC8461 pin	Description	Typical pin on a MCU
PDI_SPI_CSN	SPI chip select for the TMC8461 PDI	SSx
PDI_SPI_SCK	SPI master clock	SCK
PDI_SPI_MOSI	Master out slave in data	MOSI
PDI_SPI_MISO	Master in slave out data	MISO
PDI_SPI_IRQ	Configurable IRQ from PDI	General purpose Input
PDI_EMULATION	0: default mode for complex slaves, state machine changes processed in microcontroller firmware; 1: device emulation mode for, e.g., simple slaves, state machine changes directly handled in the ESC	General purpose Output or connected to either ground or 3.3V.
PDI_SOF	Indicates start of an Ethernet/EtherCAT frame	General purpose Input
PDI_EOF	Indicates end of an Ethernet/EtherCAT frame	General purpose Input

TMC8461 pin	Description	Typical pin on a MCU
PDI_WDSTATE	0: Watchdog expired; 1: Watchdog not expired	General purpose Input
PDI_WDTRIGGER	Watchdog triggered if '1'	General purpose Input

Table 3: PDI signal description

5.1.1 SPI protocol description

Each SPI datagram contains a 2- or 3-byte address/command part and a data part. For addresses below 0x2000, the 2-byte addressing mode can be used, the 3 byte addressing mode can be used for all addresses.

C2	C1	C0	Command
0	0	0	NOP (no operation, no following data bytes)
0	0	1	Reserved
0	1	0	Read
0	1	1	Read with wait state byte
1	0	0	Write
1	0	1	Reserved
1	1	0	Address extension, signaling 3 byte mode
1	1	1	Reserved

Table 4: PDI SPI commands

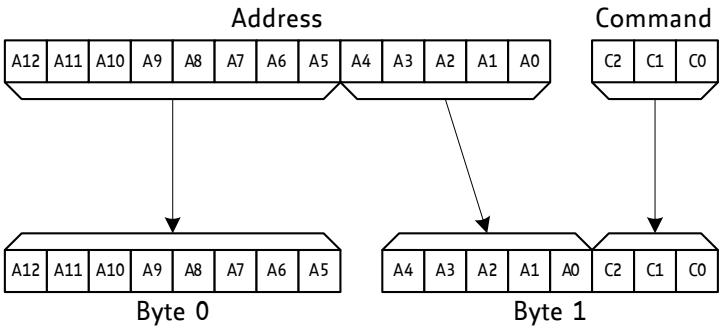

Figure 9: PDI SPI 2 byte addressing

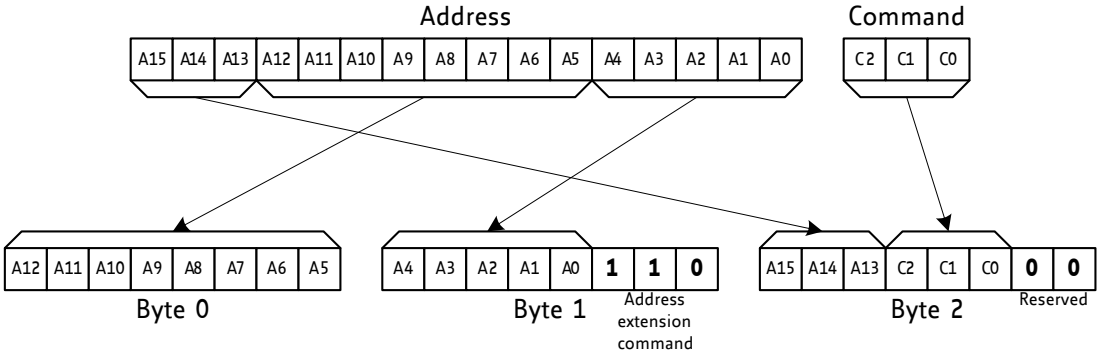

Figure 10: PDI SPI 3 byte addressing

Unless highest performance is required, using only the 3-byte addressing mode and the read with wait state command is recommended since it reduces the need for special cases in the software. During the address/command bytes, the ESC replies with the contents of the event request registers (0x0220, 0x0221 and in 3 byte addressing mode 0x0222).

Command 0 - NOP
This command can be used for checking the event request registers and resetting the PDI watchdog without a read or write access.

Example datagram: 0x00 0x00
Example reply (AL Control event bit is set): 0x01 0x00

Command 2 - READ
With the read command, an arbitrary amount of data can be read from the device. The first byte read is the data from the address given by the address/command bytes. With every read byte, the address is incremented. During the data transfer, the SPI master sends 0x00 except for the last byte where a 0xFF is sent.
When using this command, a pause of 240ns or more must be included between the address/command bytes and the data bytes for the ESC to fetch the requested data.

Example datagram (Read from address 0x0120 and 0x0121): 0x09 0x02 0x00 0xFF
Example reply (Operational State requested): 0x01 0x00 0x08 0x00

Command 3 - READ WITH WAIT STATE BYTE
This command is similar to the Read command with an added dummy byte between the address/command part and the data part of the datagram. This allows enough time to fetch the data in any case.

Example datagram (Read starting at address 0x3400): 0xA0 0x06 0x2C 0xFF 0x00 0x00 0x00 0xFF
Example reply (0xXX is undefined data): 0x00 0x00 0x00 0xXX 0x44 0x41 0x54 0x41

Command 4 - WRITE
The write command allows writing of an arbitrary number of bytes to writable ESC registers or the process data RAM. It requires no wait state byte or delay after the address/command bytes. After every transmitted byte, the address is incremented.

Example datagram (Write starting at address 0x4200): 0x10 0x06 0x50 0x4C 0x48
Example reply (0xXX is undefined data): 0x00 0x00 0x00 0xXX 0xXX
Address 0x4200 now contains 0x4C, Address 0x4201 contains 0x48