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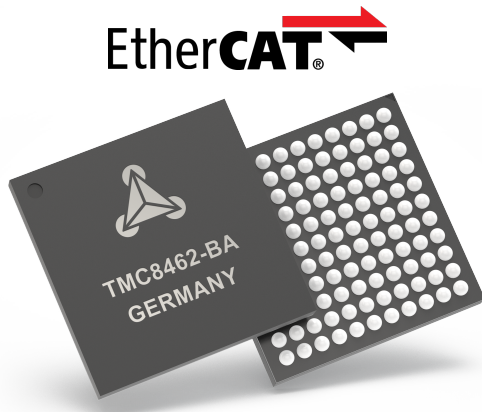
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TMC8462 Datasheet

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The TMC8462 is a complete EtherCAT® Slave Controller optimized for real time. It comprises all blocks required for an EtherCAT slave including two 100-Mbit PHYs, a dual switch regulator power supply and 24V capable high voltage I/Os for industrial environments. Timer, watchdog, PWM and SPI/IIC master units allow for enhanced capabilities either in device emulation mode or in combination with an external CPU.



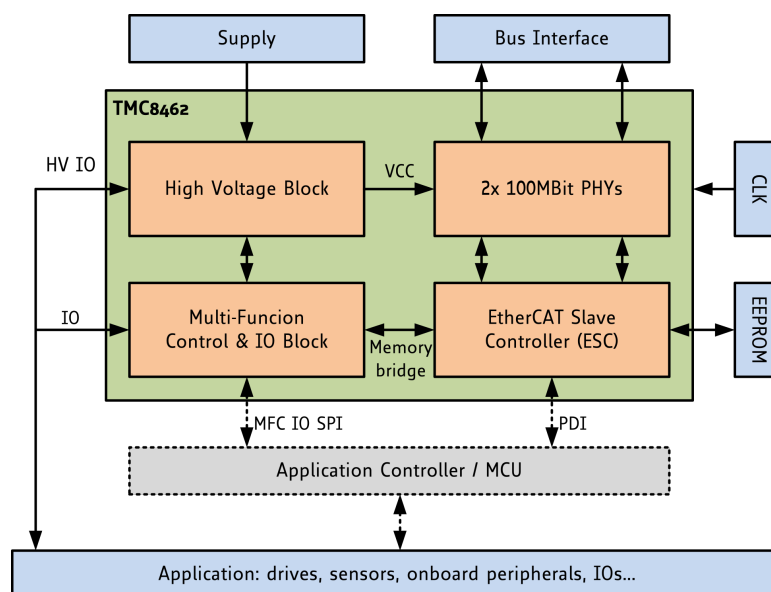
Features

- Standard compliant EtherCAT® Slave
- Dual Integrated 100-Mbit Ethernet PHY
- SPI Process Data Interface (PDI)
- IO Block with 24 Multi-Function I/Os
- Internal 3.3V plus free 5V-24V switch regulator
- 8 High Voltage I/Os (up to 35V, 100mA)
- Multifunction block comprises Watchdog, 4 PWM outputs and Step/Dir generator
- Direct EtherCAT access to external ADCs, stepper motor controllers, etc.
- EtherCAT-P compatible voltage range

Applications

- Factory Automation
- Process Automation
- Communication Modules
- Industrial IoT
- Industry 4.0
- Sensors & Encoders
- Robotics
- Industrial Motion Control
- Building Automation

Simplified Block Diagram



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1 Product Features

TMC8462 is an advanced EtherCAT Slave Controller device used for EtherCAT communication. It provides the interface for data exchange between EtherCAT master and the slave's local application controller. In addition, TMC8462 provides complex IO functions paired with high voltage features and integrated 100Bit Ethernet PHYs.

Advantages:

- Fully standard compliant and proven EtherCAT engine
- Highly integrated with highest feature count vs. package size
- License-free & royalty-free
- High Voltage & robust
- Saves board space & reduces BOM
- Long-term availability

Major Features:

- EtherCAT Slave Controller with 2 ports for bus interfacing, 8 FMMU & 8 Sync Managers, Distributed clocks with 64 bit, 16KByte of Process Data Memory, external I2C EEPROM, SPI Process Data Interface (PDI), optional device emulation
- TRINAMIC Multi-Function Control and IO block with 24 configurable IO ports for complex real-time IO functions (GPIOs, PWM, Step/Direction, I2C, SPI, DAC, incremental encoder) including 8 high voltage IOs
- TRINAMIC high voltage block with 8 short circuit protected push-/pull or open drain high voltage IOs for up to 24V and 100mA drive current
- Two integrated 500mA step down switching voltage regulators with one being fixed at 3.3V and one being programmable between 5V and 24V
- Internal 1.8V linear regulator for core voltage generation
- Two integrated 100-Mbit Ethernet PHYs to directly connect to twisted pair copper or back-to-back directly to another PHY
- Simple configuration of EtherCAT Slave Controller and Multi-Function Control and IO block via EEPROM
- 3.3V Digital IO Voltage
- Working with a single supply voltage depending on application: 3.3V only or 5V to 35V (5V, 12V, or 24V typical)
- Industrial Temperature Range -40°C to +125°C
- Additional clock output: 16.6 MHz CLK, 25 MHz PHY clock, 100 MHz
- Integrated temperature measurement and over-temperature shutdown
- Package: 9mm x 9mm BGA package with 121 pins and 0.75mm pitch



2 Order Codes

Order Code	Description	Size
TMC8462-BA	TMC8462 Advanced EtherCAT® Slave Controller in 121 pin BGA package with 0.75mm pitch	9mm x 9mm
TMC8462-EVAL	Evaluation Board for TMC8462-BA, compatible with the modular Landungsbruecke system, RJ45 twisted pair copper interface	79mm x 85mm
Landungsbruecke	MCU Board	85mm x 55mm
TMC8462-BOB-ETH	Breakout Board (BOB) for TMC8462-BA, with 0.1" header rows, reference clock source, SII-EEPROM, and RJ45 twisted pair copper transceiver interface	2.0" x 1.5"

Table 1: TMC8462 order codes

Trademark and Patents



EtherCAT® is a registered trademark and patented technology, licensed by Beckhoff Automation GmbH, Germany.



3 Principles of Operation / Key Concepts

TMC8462 is a highly integrated ASIC providing the interface between the Ethernet-based EtherCAT real-time field bus and the local application. Its extended digital and high voltage feature set provides additional functions to the EtherCAT slave.

3.1 General Device Architecture

Figure 1 shows the general device architecture and major connections of TMC8462. The four function blocks EtherCAT Slave Controller, Multi-Function Control and IO, Analog and High Voltage, and Ethernet PHYs are introduced in the following sub-sections.

For operation, a stable 100MHz clock source, an IIC EEPROM, and power supply for IO and high voltage operation are required (if the high voltage features are used). An application controller, which also runs the EtherCAT slave stack, connects to the SPI interfaces. The application and onboard peripherals can be controlled by the application controller or the Multi-Function Control and IO block.

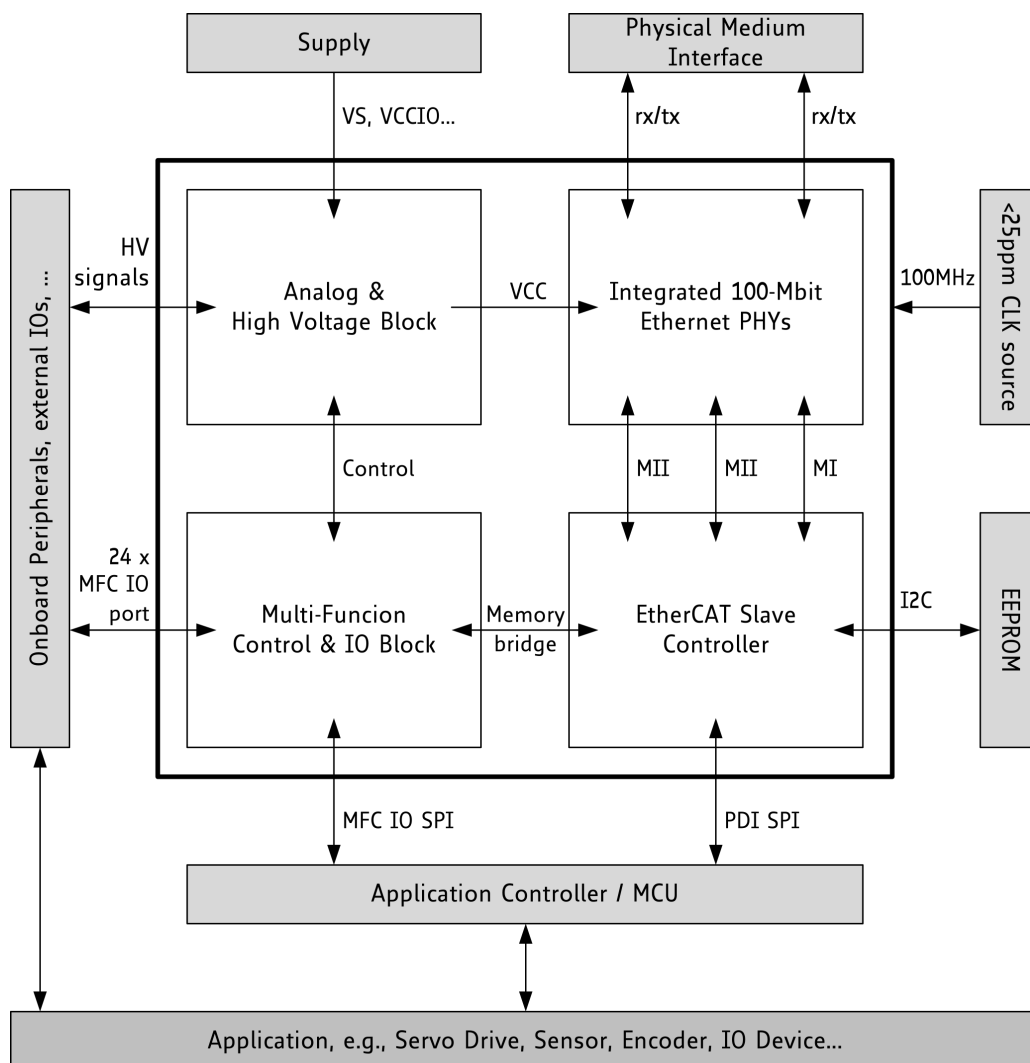


Figure 1: General device architecture



3.2 EtherCAT Slave Controller

TMC8462 contains a standard-conform EtherCAT Slave Controller (ESC) providing real-time EtherCAT MAC layer functionality to EtherCAT slaves. It connects via MII interface to standard Ethernet PHYs and provides a digital control interface to a local application controller while also providing the option for standalone operation.

The ESC part of TMC8462 provides the following EtherCAT-related features. More information is available in Section 6.

- Two internal 100Mbit Ethernet PHYs
- Eight Fieldbus Memory Management Units (FMMU)
- Eight Sync Managers (SM)
- 16 KByte of Process Data RAM (PDRAM)
- 64B bit Distributed Clocks support
- I2C interface for external EEPROM for ESC configuration
- SPI Process Data Interface (PDI) with 30Mbit/s
- Proven EtherCAT State Machine (ESM)
- Device Emulation Mode

3.3 Multi-Function and Control IO Block

In addition to the EtherCAT functionality, the TMC8462 comes with a dedicated function block providing a configurable set of complex real-time IO functionality for smart (embedded) EtherCAT slave systems. This IO functionality is called Multi-Function Control and IO block (MFC IO). Its special focus is on motor and motion control while it is not limited to this application area.

The MFC IO block combines various functional sub blocks that are helpful in an embedded design to reduce complexity, to simplify bill of materials (BOM), and to provide hardware acceleration to compute intensive or time critical tasks. More information is available in Section 7.

Configurable IO Ports The whole MFC IO block provides in total 24 IO ports that can be configured and assigned to any of the available functional units inside the MFC IO block. If not used, each IO port can be tristated.

General Purpose IOs Up to sixteen (16) general purpose IOs are available. Each IO can be configured either as input or as output. For the outputs, a safe state can be configured which is used in case of emergency event.

Incremental Encoder Interface Configurable incremental encoder interface with 32 bit position registers, single-ended or differential inputs, configurable counting constant for different resolutions, configurable polarity and N-signal behavior.

Step/Direction Generator Block The step and direction unit provides up to 3 independent channels. Various configuration options and modes allow for example for continuous or one-shot mode, reading of the internal total step counters, pre-loading the next step frequency to be used at a certain counter value. The step and direction outputs signals can be single-ended or differential.



PWM Block The integrated PWM block provides up to 4 PWM channels. PWM frequency and duty cycle as well as polarities and dead times are configurable. The outputs can be configured for a safe state in case of emergency.

Generic SPI Master Interface The TMC8462 provides a generic SPI master interface to connect to on- or off-board SPI slave peripherals like ADCs, sensors, or motor drivers. The SPI master interface is fully configurable and offers 4 slave select lines.

Generic I2C Master Interface A generic I2C master interface is also available in TMC8462 to connect to I2C slaves. The I2C bus speed is configurable.

Digital DAC A simple digital 16 bit DAC channel is available which requires an external RC circuit for operation.

Safety Functions The following safety functions are available with the TMC8462

- Configurable watchdog functionality for the MFC IO block to monitor internal and external signals as well as EtherCAT activity. This block is fully configurable.
- A general emergency switch input can be activated. For critical outputs, a safe state can be configured which is used when the emergency switch triggers.
- A common IRQ signal is available at the MFC IO block which can be mapped to various events of the MFC IO block. The IRQ events can be processed by a local application controller.

3.4 Analog and High Voltage Block

TMC8462 has an integrated powerful high voltage sub block that provides analog functions and high voltage support to your EtherCAT slave. The integrated high voltage capabilities allow for BOM reduction and save board space. More information is available in Section 7.21.

High Voltage Ports 8 of the 24 configurable IO ports of the MFC IO block are high voltage IO ports. For pure digital systems operating at 3.3V or 5V these ports can simply be used as standard IO ports. When using a higher supply voltage at the VIOx inputs the high voltage ports can be used at up to 35V (5V, 12V, 24V typical). The 8 high voltage ports are grouped into 3 groups with 2, 3, and 3 ports. Each group can be used a different supply voltage level using VIO1, VIO2, and VIO3 inputs.

Each high voltage port has a short circuit protected push-/pull or open drain output stage with 100mA drive current (ca. 200mA short time) and can be combined with any signal of the MFC IO block functions. The outputs' slope can be controlled. An optional input filter is selectable as well as pull downs or pull ups with 100 μ A.

The high voltage ports have an over-temperature shutdown.

Switching Regulators Two switching regulators (buck regulators) are integrated into TMC8462 – SW0 and SW1. Both are capable of driving up to 500mA.

SW0 generates a fixed 3.3V rail for internal and external logic supply. SW1 is programmable between 3.3V and VS (up to 24V) and can be used for peripheral supply, e.g. to generate a 5V encoder supply.

Each switching regulator comes with a separate over-temperature shutdown.

Single Supply Operation TMC8462 is designed to work with a single external power supply rail. All required supply voltages are generated internally. The required external supply rail depends on the application scenario (between 3.3V and 24V).



3.5 Interfaces

Field Bus Interface TMC8462 contains 2 integrated 100-Mbit Ethernet PHYs and directly connects to the field bus using an external transformer circuit. In addition, the PHY interfaces of two TMC8462 devices can also be connected directly to allow back-to-back connection with only low part count and a small circuit. This is useful when extending the EtherCAT bus on the board or to a another slave close by.

ESC Process Data Interface The ESC part can be accessed via the so-called Process Data Interface (PDI). TMC8462 comes with an SPI PDI. Besides the standard SPI bus lines additional control signals belong to the SPI PDI, which are further described in Section 5.1..

MFC IO Control Interface The MFC IO block of TMC8462 can be accessed from EtherCAT master side or from the local application controller. For connection to the local application controller, a second SPI interface – the MFC IO SPI – is provided. The protocol used nearly identical to the SPI PDI interface. Additional information on the MFC IO SPI is given in Section 5.2.

EEPROM Interface The EEPROM interface is intended to be a point-to-point interface between TMC8462 and EEPROM with TMC8462 being the master. If other I2C masters are required to access the I2C bus, TMC8462 must be held in reset state, for example for in-circuit-programming of the EEPROM. During operation, the application controller must tristate its I2C interface. Depending on the EEPROM size the addressing mode must be properly set using the PROM_SIZE configuration pin.

Configuration Inputs Hard-wired configuration pins are available at the TMC8462, which are used to configure various options related to the hardware configuration and application scenario and which will not change. These pins are PROM_SIZE, PDI_SHARED_SPI_BUS, and DEVICE_EMULATION. More information on these configuration pins and signals is given in Section 4.2 and Section 5.

3.6 Software- and Tool-Support

TRINAMIC's EtherCAT Slave Controller family comes with extensive hardware and software tool support to get started quickly.

Evaluation Board An evaluation board is available for the TMC8462 with standard RJ45 connectors and transformers for interfacing twisted pair copper (TPC) media.



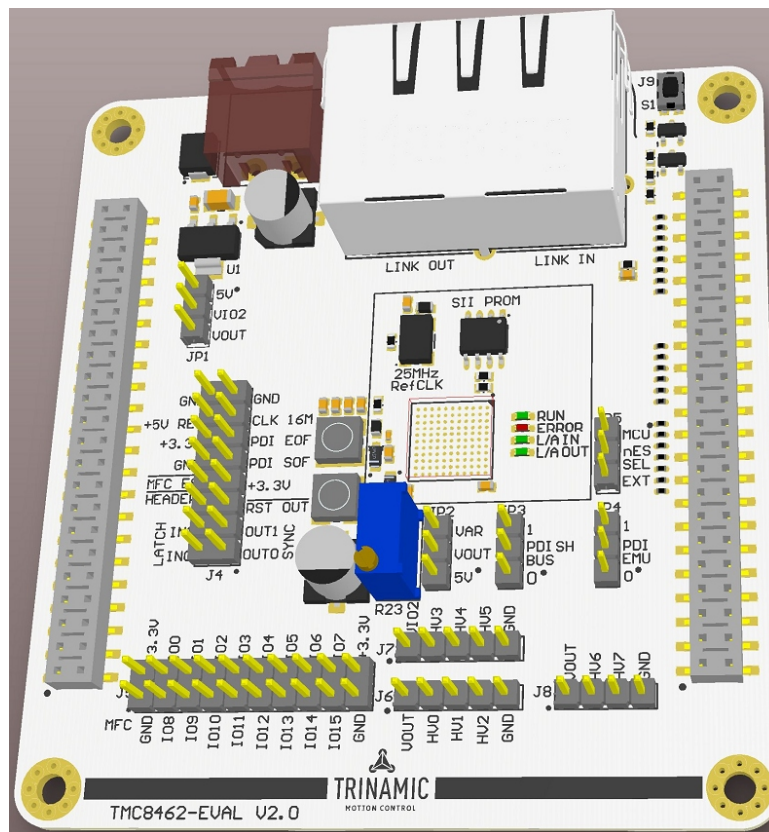


Figure 2: TMC8462 Evaluation Board

The complete board design files are available for download and can be used as reference. All information is available for download on the specific product page on TRINAMIC's website at <http://www.trinamic.com/products/integrated-circuits/evalboards>.

Breakout Board Two version of smaller breakout boards are available that allow for easy integration into own systems or connection to a prototyping platform. The breakout boards provide the bus interface along with the ESC and require an appropriate supply and controller connection. One breakout board version comes with standard RJ45 connectors to connect to TPC using the TMC8462 ESC with integrated Ethernet PHYs. A second version of the breakout board comes with on-board transceivers for Plastic/polymer Optical Fiber (POF) connections using the TMC8461 with external Ethernet PHYs. The complete board design files are available for download and can be used as reference. All information is available for download on the specific product page on TRINAMIC's website at <http://www.trinamic.com/products/integrated-circuits/>.



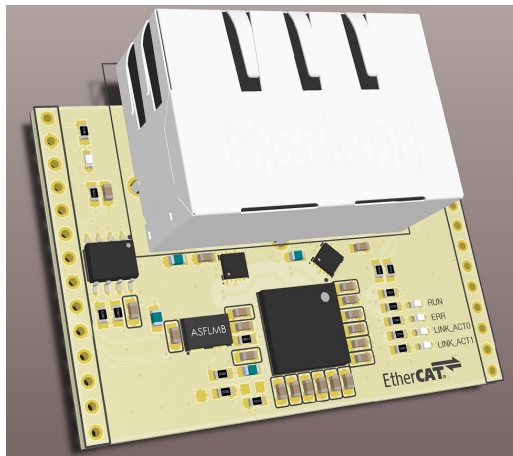


Figure 3: TMC8462 breakout board for RJ45 and TPC

TRINAMIC Technology Access Package In addition, a comprehensive source code and software package – TRINAMIC Technology Access Package (TTAP) – is available for download to get started quickly with own code.

The TTAP is available at <https://www.trinamic.com/support/software/access-package/>.

TMCL-IDE The TMCL-IDE is TRINAMIC's primary tool (for Windows PCs) to control TRINAMIC modules and evaluation boards. Besides, it provides feature like remote firmware updates, module monitoring options, and specific Wizard support. The TMCL-IDE can be used along with TRINAMICs modular evaluation board system.

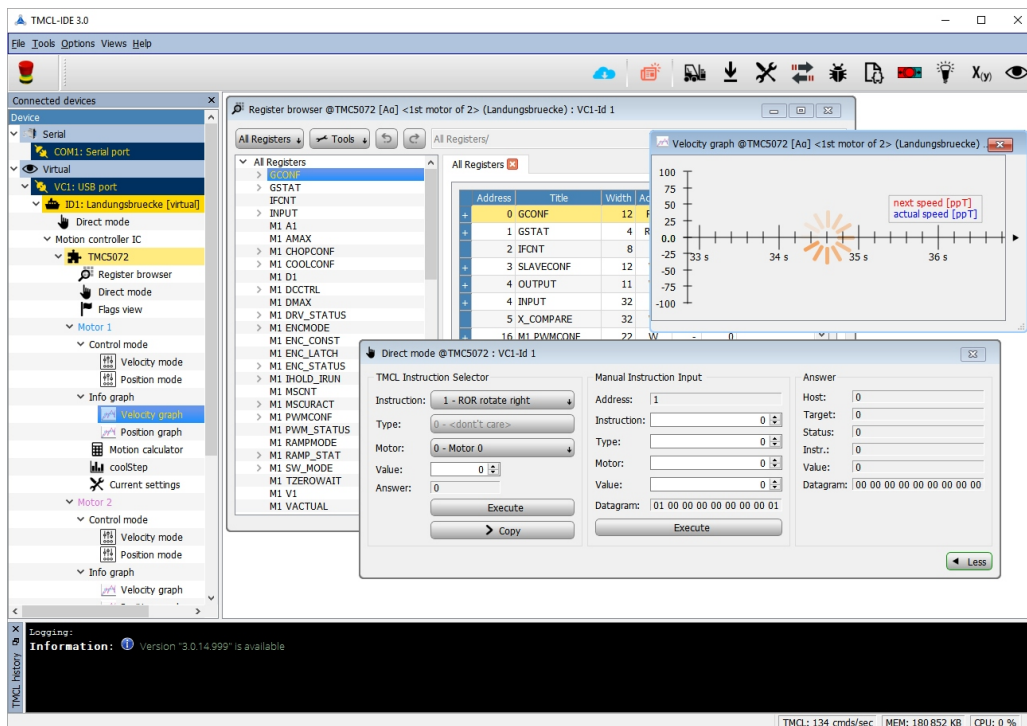


Figure 4: TMCL-IDE



The latest version and additional information is available for download from TRINAMIC’s website at <http://www.trinamic.com/software-tools/tmcl-ide>.

EtherCAT Slave Configuration Configuration of the EtherCAT Slave Controller is done during boot time with configuration information read from the SII EEPROM after reset or power cycling. This information must be (pre)programmed into the SII EEPROM. This can be done via the EtherCAT master using a so-called EtherCAT Slave Information (ESI) file in standardized XML format. The SII EEPROM can also be (re)written using the local application controller.

ESI Configuration Wizard The TMCL-IDE contains a wizard to assist users with the configuration of the TMC8462 various MFC IO functions. The wizard shows available and allowed options and provides XML code snippets for the ESI file for the SII EEPROM as well as generic C-Code blocks. These can be used as starting point for own firmware development for the application controller.

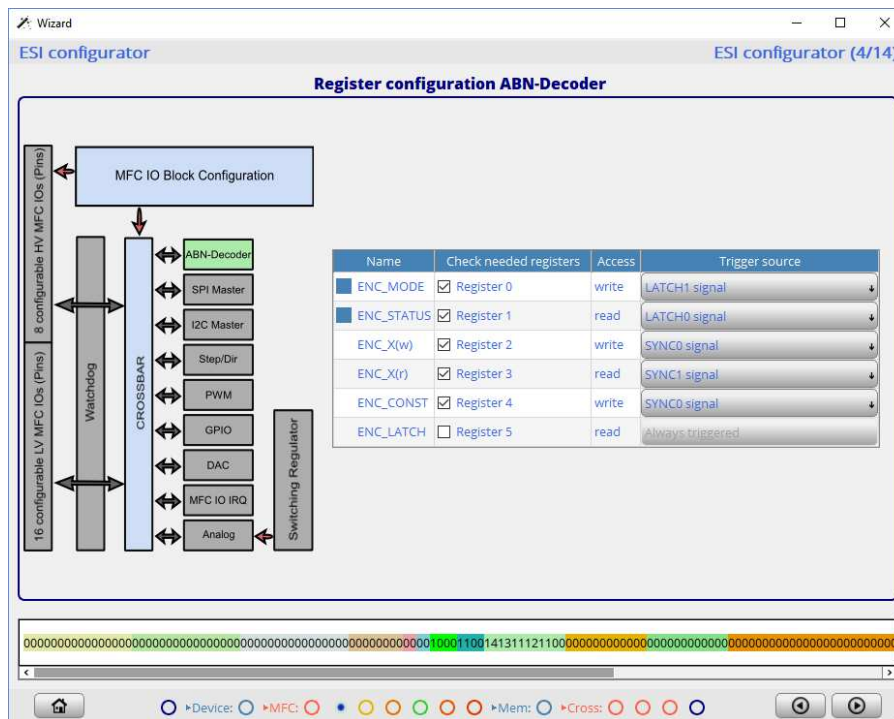


Figure 5: Configuration wizard example – MFC IO block configuration



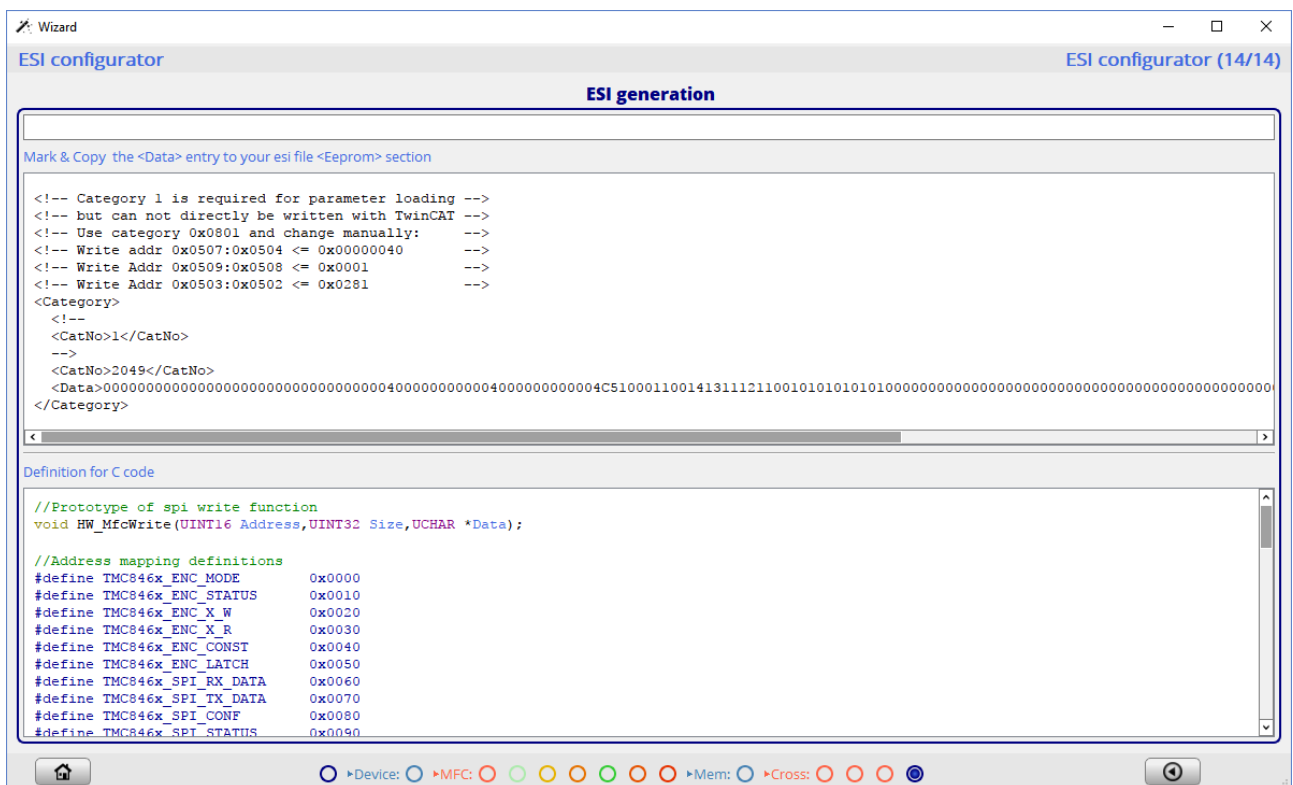


Figure 6: Configuration wizard example – SII EEPROM content and C-code output



4 Device Pin Definitions

4.1 Pinout and Pin Coordinates of TMC8462-BA

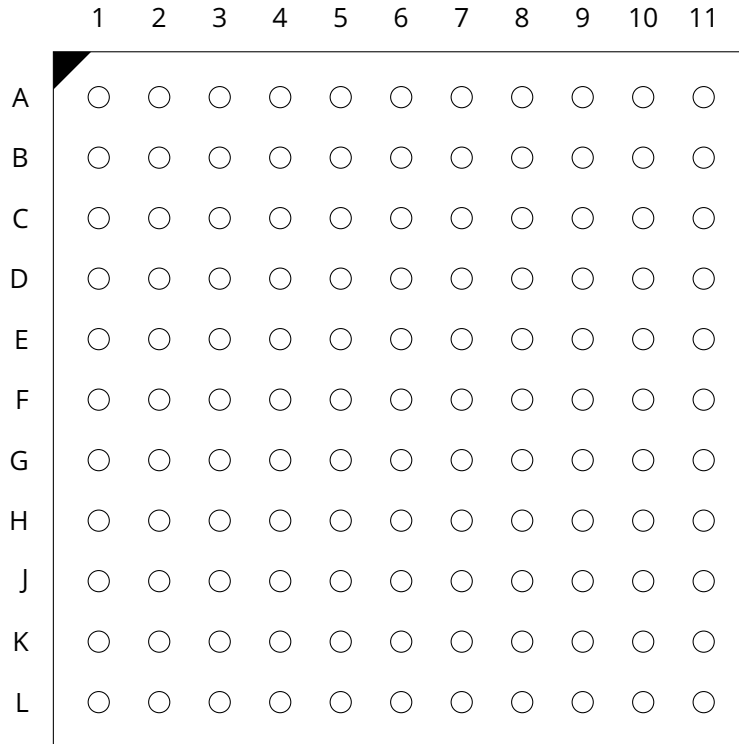


Figure 7: TMC8462-BA Pinout top view

4.2 Signal Descriptions

Name	Pin	Type (I,O,PU,PD)	Function
General Signals			
NRESET	K4	I/O	Low active system reset. NRESET is an I/O pin. Keep unconnected/open to use the internal reset only. For more information see Section 5.4.12.
REF_CLK100_IN	L3	I	100MHz Reference clock input, connect to a clock source <u>25ppm</u>.
CLK16_OUT	H7	O	16.6MHz auxiliary clock output. Not available during reset.
EN_CLK16_OUT	E9	I	Enable signal for CLK16_OUT: 0 = off, 1 = on
RESET_OUT	J4	O	This high-active reset output is activated via EtherCAT register 0x0040), therefore RESET_OUT has to trigger the NRESET input, which clears RESET_OUT. This connection incl. changing the polarity has to be made externally .



Name	Pin	Type (I,O,PU,PD)	Function
EEPROM IOs			
PROM_INIT	J5	O	Signal indicating that EEPROM has been loaded, 0 = not ready, 1 = EEPROM loaded
PROM_CLK	H4	O	External I2C EEPROM clock signal, use 1K pull up resistor to 3.3V
PROM_DATA	H5	I/O	External I2C EEPROM data signal, use 1k pull up resistor to 3V3
PROM_SIZE	G9	I	Selects between two different EEPROM sizes since the communication protocol for EEPROM access changes if a size > 16kBit is used (an additional address byte is required then). 0 = up to 16kBit EEPROM, 1 = 32 kBit-4Mbit EEPROM

DC Synchronization IOs			
SYNC_OUT0	D7	O	Distributed Clocks synchronization output 0, typically connect to MCU
SYNC_OUT1	D6	O	Distributed Clocks synchronization output 1, typically connect to MCU
LATCH_IN0	C7	I	Latch input 0 for Distributed Clocks, connect to GND if not used.
LATCH_IN1	C6	I	Latch input 1 for Distributed Clocks, connect to GND if not used.

LEDs			
LED_RUN	B3	O	Run Status LED, connect to green LED (Anode) 0 = LED off, 1 = LED on
LED_ERR	C3	O	Error Status LED, connect to red LED (Anode) 0 = LED off, 1 = LED on
LINK_ACT0	D3	O	Link In Port Status and Activity, connect to green LED (Anode) 0 = LED off, 1 = LED on
LINK_ACT1	E3	O	Link Out Port Status and Activity, connect to green LED (Anode) 0 = LED off, 1 = LED on



Name	Pin	Type (I,O,PU,PD)	Function
Process Data Interface IOs to/from MCU			
PDI_SOF	H3	O	Ethernet Start-of-Frame if 1
PDI_EOF	G3	O	Ethernet End-of-Frame if 1
PDI_SPI_CSN	L4	I	Chip select signal of the process data interface
PDI_SPI_SCK	K3	I	Serial clock signal of the process data interface
PDI_SPI_MOSI	L5	I	Serial data out signal of the process data interface
PDI_SPI_MISO	K5	O	Serial data in signal of the process data interface
PDI_SPI_IRQ	J3	O	Interrupt signal for primary process data interface, connect to MCU
PDI_WDSTATE	G4	O	EtherCAT Watchdog state, 0: Expired, 1: Not expired
PDI_WDTRIGGER	F4	O	EtherCAT Watchdog trigger if 1
PDI_EMULATION	J7	I	Selects between PDI interface (SPI) or standalone operation with state machine emulation inside ESC. Has weak internal pull down. 0 = default, PDI interface active, 1 = standalone operation, state machine emulation in Slave Controller

MFC IO Control Interface IOs			
MFC_CTRL_SPI_CSN	D4	I	Chip select signal of the MFC IO control interface
MFC_CTRL_SPI_SCK	E4	I	Serial clock signal of the MFC IO control interface
MFC_CTRL_SPI_MOSI	C4	I	Serial data out signal of the MFC IO control interface
MFC_CTRL_SPI_MISO	E7	O	Serial data in signal of the MFC IO control interface
MFC_IRQ	E6	O	MFCIO block IRQ for configurable events, connect to MCU, high active
MFC_NES	C5	I	low active (not) Emergency Stop/Switch/Halt (to bring PWM or other outputs into a safe state), the event must be cleared actively, has weak internal pull down, must be driven high for normal operation
PDI_SHARED_BUS	F9	I	Selects between separate SPI buses (MISO, MOSI, SCK) or one SPI bus with two CS lines for the PDI and MFC CTRL SPI interface: 0 = two separate SPI buses, 1 = one shared SPI bus using the PDI_SPI_x bus lines



Name	Pin	Type (I,O,PU,PD)	Function
MFC IOs			
MFCIO00	J8	I/O	MFCIO block low voltage I/O
MFCIO01	J9	I/O	MFCIO block low voltage I/O
MFCIO02	J10	I/O	MFCIO block low voltage I/O
MFCIO03	J11	I/O	MFCIO block low voltage I/O
MFCIO04	H8	I/O	MFCIO block low voltage I/O
MFCIO05	H9	I/O	MFCIO block low voltage I/O
MFCIO06	H10	I/O	MFCIO block low voltage I/O
MFCIO07	H11	I/O	MFCIO block low voltage I/O
MFCIO08	D8	I/O	MFCIO block low voltage I/O
MFCIO09	D9	I/O	MFCIO block low voltage I/O
MFCIO10	D10	I/O	MFCIO block low voltage I/O
MFCIO11	D11	I/O	MFCIO block low voltage I/O
MFCIO12	C8	I/O	MFCIO block low voltage I/O
MFCIO13	C9	I/O	MFCIO block low voltage I/O
MFCIO14	C10	I/O	MFCIO block low voltage I/O
MFCIO15	C11	I/O	MFCIO block low voltage I/O

MFC High Voltage IOs			
MFC_HV0 (MFCIO16)	A4	I/O	MFCIO block high voltage I/O
MFC_HV1 (MFCIO17)	A5	I/O	MFCIO block high voltage I/O
MFC_HV2 (MFCIO18)	A6	I/O	MFCIO block high voltage I/O
MFC_HV3 (MFCIO19)	A7	I/O	MFCIO block high voltage I/O
MFC_HV4 (MFCIO20)	A8	I/O	MFCIO block high voltage I/O
MFC_HV5 (MFCIO21)	A9	I/O	MFCIO block high voltage I/O
MFC_HV6 (MFCIO22)	A10	I/O	MFCIO block high voltage I/O
MFC_HV7 (MFCIO23)	A11	I/O	MFCIO block high voltage I/O



Name	Pin	Type (I,O,PU,PD)	Function
MFC High Voltage IO Supplies			
VIO1	B5	I	MFCHVIO block 1 supply voltage
VIO2	B7	I	MFCHVIO block 2 supply voltage
VIO3	B9	I	MFCHVIO block 3 supply voltage
GNDIO1	B6	I	MFCHVIO block 1 ground, connect to GND
GNDIO2	B8	I	MFCHVIO block 2 ground, connect to GND
GNDIO3	B10	I	MFCHVIO block 3 ground, connect to GND

Device Supply and Ground			
VS	B11	I	Supply voltage, use a 100nF filter capacitor
VCCIO	E10, F10, G10, F11	I	I/O supply voltage, use a 100nF filter capacitor per pin
VCC_CORE	F6, G6, F7, G7	I	Core supply voltage, connect to VDD1V8_OUT, use a 100nF filter capacitor per pin
PLLCLK_VCCIO	K6	I	PLL supply voltage, connect to VCCIO through a filter (R/L/C)
TSTCLK_SELECT	H6	I	Test input, always connect to VCCIO for normal operation
GND	C1, F1, J1, A3, B4, F5, G5, E8, F8, G8	I	Supply Ground
PLLCLK_GND	J6	I	PLL supply ground, connect to GND

Voltage Regulator IOs			
VDD1V8_OUT	G11	O	Output of internal 1.8V regulator, use a 100nF filter capacitor
VDD5_OUT	E11	O	Output of internal 5V regulator, use a 100nF filter capacitor if $V_S \geq 5V$



Name	Pin	Type (I,O,PU,PD)	Function
Switching Regulator 0 IOs			
VS0	L7	I	Switching regulator 0 supply voltage, Switching regulator 0 provides a fixed 3.3V output.
GND0	L9	I	Switching regulator 0 ground, connect to GND
SW0	L8	O	Switching regulator 0 output, fixed 3.3V
SW_DIODE	K7	I	Switching regulator 0 internal diode, connect to SW0 only if VS0 is at or below 5V
GND_DIODE	K8	I	Switching regulator 0 internal diode ground, connect to GND

Switching Regulator 1 IOs			
VS1	L11	I	Switching regulator 1 supply voltage, Switching regulator 1 provides an adjustable output voltage.
GND1	K9	I	Switching regulator 1 ground, connect to GND
SW1	L10	O	Switching regulator 1 output, adjustable
VOUT	K10	I	Switching regulator 1 inductor ringing suppression feedback
VOUT_FB	K11	I	Switching regulator 1 feedback voltage, 1.2V typically

Bus Interface 0 IOs (EtherCAT IN Port)			
TN0	D1	O	Negative pin of differential transmit output pair
TP0	E1	O	Positive pin of differential transmit output pair
RN0	A1	I	Negative pin of differential receive output pair
RP0	B1	I	Positive pin of differential receive output pair
REGOUT0	A2	O	Regulator power output, use a 10uF and 0.1uF for filtering power noise
MCLK	F2	O	PHY management clock, leave open if not needed
MDIO	F3	I/O, PU	PHY management data, use 4K7 pull up resistor to VCCIO (3.3V)



Name	Pin	Type (I,O,PU,PD)	Function
Bus Interface 1 IOs (EtherCAT OUT Port)			
TN1	K1	IO	Negative pin of differential transmit output pair
TP1	L1	IO	Positive pin of differential transmit output pair
RN1	G1	IO	Negative pin of differential receive output pair
RP1	H1	IO	Positive pin of differential receive output pair
REGOUT1	L2	O	Regulator power output, use a 10uF and 0.1uF for filtering power noise

Test Pins only			
TST_MODE	E5	I	Test mode enable, connect to GND
TST_ANA	D5	O	Analog test output, leave open
RXCLK0	D2	IO	Clock test pin, leave open
RXCLK1	G2	IO	Clock test pin, leave open
TXCLK0	E2	IO	Clock test pin, leave open
TXCLK1	H2	IO	Clock test pin, leave open
RXDV0	B2	I, PD	Test pin, leave open for normal operation
RXDV1	K2	I, PD	Test pin, leave open for normal operation
TXER0	C2	I, PD	Test pin, leave open for normal operation
TXER1	J2	I, PD	Test pin, leave open for normal operation
CLKO_100	L6	O	100MHz clock output

Table 2: Pin and Signal description for TMC8462-BA



5 Device Usage and Handling

5.1 Process Data Interface

The Process Data Interface (PDI) is an SPI interface with a clock frequency of up to 30 MHz. The ESC registers and the process data RAM can be accessed from an external microcontroller using this interface. The interface can be configured via the EEPROM, however it is recommended to use the default configuration (SPI mode 3 with low active chip select). For further details, see the ESC SPI slave configuration registers in Section 6.

Additionally, some signals are available that can be evaluated by the application controller.

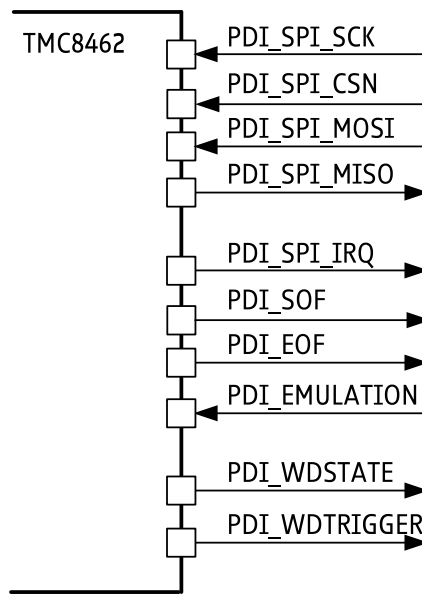


Figure 8: PDI control signals

TMC8462 pin	Description	Typical pin on a MCU
PDI_SPI_CSN	SPI chip select for the TMC8462 PDI	SSx
PDI_SPI_SCK	SPI master clock	SCK
PDI_SPI_MOSI	Master out slave in data	MOSI
PDI_SPI_MISO	Master in slave out data	MISO
PDI_SPI_IRQ	Configurable IRQ from PDI	General purpose Input
PDI_EMULATION	0: default mode for complex slaves, state machine changes processed in microcontroller firmware (SSC); 1: device emulation mode for, e.g., simple slaves, state machine changes directly handled in the ESC	General purpose Output or connected to either ground or 3.3V.
PDI_SOF	Indicates start of an Ethernet/EtherCAT frame (MII_RXDV = '1')	General purpose Input



TMC8462 pin	Description	Typical pin on a MCU
PDI_EOF	Indicates end of an Ethernet/EtherCAT frame	General purpose Input
PDI_WDSTATE	0: Watchdog expired; 1: Watchdog not expired	General purpose Input
PDI_WDTRIGGER	Watchdog triggered if '1'	General purpose Input

Table 3: PDI signal description

5.1.1 SPI protocol description

Each SPI datagram contains a 2- or 3-byte address/command part and a data part. For addresses below 0x2000, the 2-byte addressing mode can be used, the 3 byte addressing mode can be used for all addresses.

C2	C1	C0	Command
0	0	0	NOP (no operation, no following data bytes)
0	0	1	Reserved
0	1	0	Read
0	1	1	Read with wait state byte
1	0	0	Write
1	0	1	Reserved
1	1	0	Address extension, signaling 3 byte mode
1	1	1	Reserved

Table 4: PDI SPI commands

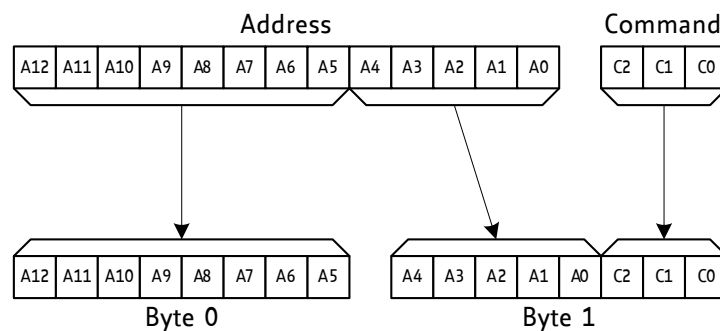


Figure 9: PDI SPI 2 byte addressing



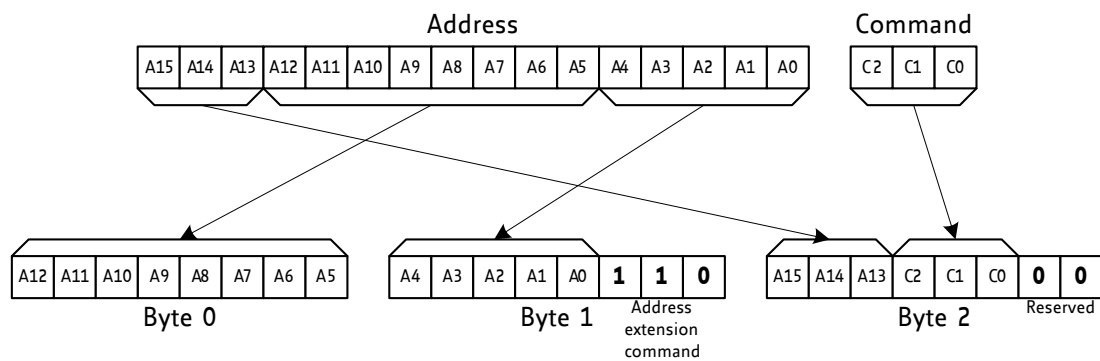


Figure 10: PDI SPI 3 byte addressing

Unless highest performance is required, using only the 3-byte addressing mode and the read with wait state command is recommended since it reduces the need for special cases in the software. During the address/command bytes, the ESC replies with the contents of the event request registers (0x0220, 0x0221 and in 3 byte addressing mode 0x0222).

Command 0 - NOP

This command can be used for checking the event request registers and resetting the PDI watchdog without a read or write access.

Example datagram: 0x00 0x00

Example reply (AL Control event bit is set): 0x01 0x00

Command 2 - READ

With the read command, an arbitrary amount of data can be read from the device. The first byte read is the data from the address given by the address/command bytes. With every read byte, the address is incremented. During the data transfer, the SPI master sends 0x00 except for the last byte where a 0xFF is sent.

When using this command, a pause of 240ns or more must be included between the address/command bytes and the data bytes for the ESC to fetch the requested data.

Example datagram (Read from address 0x0120 and 0x0121): 0x09 0x02 0x00 0xFF

Example reply (Operational State requested): 0x01 0x00 0x08 0x00

Command 3 - READ WITH WAIT STATE BYTE

This command is similar to the Read command with an added dummy byte between the address/command part and the data part of the datagram. This allows enough time to fetch the data in any case.

Example datagram (Read starting at address 0x3400): 0xA0 0x06 0x2C 0xFF 0x00 0x00 0x00 0xFF

Example reply (0xFF is undefined data): 0x00 0x00 0x00 0xFF 0x44 0x41 0x54 0x41

Command 4 - WRITE

The write command allows writing of an arbitrary number of bytes to writable ESC registers or the process data RAM. It requires no wait state byte or delay after the address/command bytes. After every transmitted byte, the address is incremented.

Example datagram (Write starting at address 0x4200): 0x10 0x06 0x50 0x4C 0x48

Example reply (0xFF is undefined data): 0x00 0x00 0x00 0xFF 0xFF

Address 0x4200 now contains 0x4C, Address 0x4201 contains 0x48



Command 6 - ADDRESS EXTENSION

The address extension command is mainly used for the 3-byte addressing mode as shown in Figure 10. For SPI masters that can only process datagrams with an even number of bytes, it might be necessary to pad the datagram to an even number of bytes. This can be achieved by duplicating the third byte of the 3-byte address/command part and using the address extension command in all but the last duplicate. For example, a SPI master that is only capable of transmitting a multiple of 4 bytes cannot use the example datagram for a write access above since it contains 5 bytes. With three added padding bytes, the master has to transmit two 4-byte groups.

Example datagram (Write starting at address 0x4200): 0x10 0x06 0x58 0x58 0x58 0x50 0x4C 0x48
 Example reply (0xXX is undefined data): 0x00 0x00 0x00 0xXX 0xXX 0xXX 0xXX 0xXX

5.1.2 Timing example

This example shows a generic read access with wait state and 2 byte addressing. All configurable options are shown. The delays between the transferred bytes are just to show the byte boundaries and are not required.

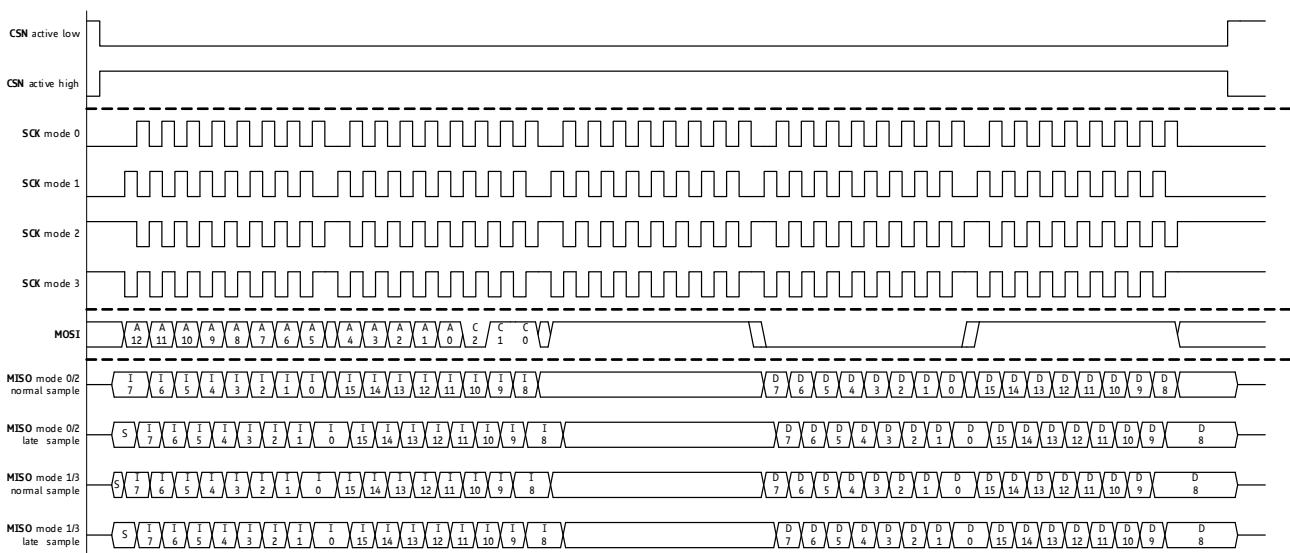


Figure 11: SPI timing example

