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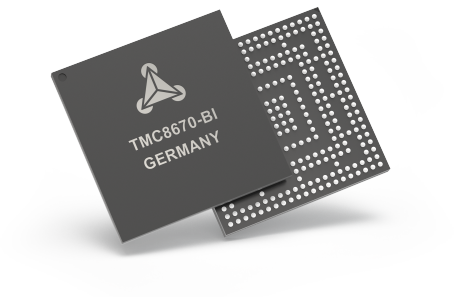
TMC8670 Datasheet

Hardware Version V1.0 | Document Revision V1.00 • 2018-June-11

The TMC8670 is a CANopen-over EtherCAT (CoE) field oriented control (FOC) servo controller for torque, velocity, and position control. It comes with a fully integrated EtherCAT Slave Controller (ESC), a flexible sensor engine for different position feedback and current sensing options, as well as a complete CANopen-over-EtherCAT firmware stack for the CiA DS402 device profile. TMC8670 is a building block that enables a servo controller with only a couple of components.



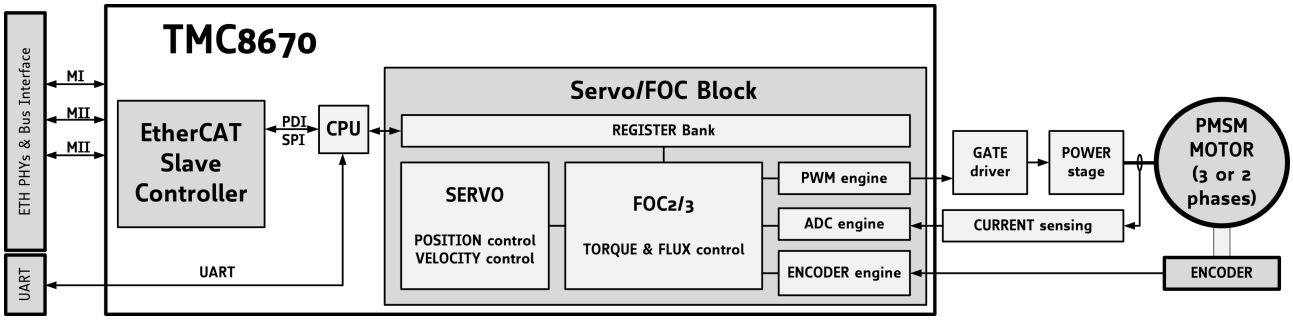
Features

- Field Oriented Control (FOC) Servo Controller
- Torque Control (FOC), Velocity Control, Position Control
- Sensor Engine (Hall analog/digital, Encoder analog/digital)
- Support for 3-Phase PMSM and 2-Phase Stepper Motors
- PWM Engine including SVPWM
- Integrated EtherCAT Slave Controller, CoE protocol CiA 402 drive profile
- UART interface

Applications

- Robotics
- Semiconductor Handling
- Factory Automation
- Laboratory Automation
- Manufacturing
- IIoT Applications

Simplified Block Diagram



Read entire documentation.

TRINAMIC
MOTION CONTROL

Contents

1 Product Features

TMC8670 is a highly integrated SoC providing the interface between an EtherCAT real-time field bus and the local drive application. It includes the real-time MAC layer for EtherCAT, the application software stack for the CiA DS402 CANopen device profile, and the complete servo control block in dedicated hardware with interfaces to ADCs and position feedback.
TMC8670 offers an extremely high function density in a small scale package.

Advantages:

- Fully standard compliant and proven EtherCAT Slave Controller and State Machine
- Highly integrated Servo Controller with rich feature set vs. package size
- Robust silicon technology
- Saves board space & reduces BOM
- Long-term availability

Major Features:

- Integrated EtherCAT Slave Controller with 2 MII ports for Ethernet bus interfacing
- Complete firmware stack with EtherCAT State Machine and CANopen over EtherCAT stack based on CiA DS402 device profile
- Firmware update via EtherCAT or via UART
- Fully integrated hardware servo controller with field-oriented control and rich interface support
- Two digital incremental encoder interfaces
- Analog SinCos encoder interface
- Digital hall sensor interface
- Analog hall sensor interface
- Flexible ADC interface to connect to external SPI ADCs or delta sigma modulators
- Industrial temperature range -40°C to +125°C
- Package: 325-pin BGA chip scale package with 0.5mm pitch, 11mm x 11mm

2 Order Codes

Order Code	Description	Size
TMC8670-BI	TMC8670 Advanced EtherCAT® Servo Controller in 325-pin BGA chip scale package with 0.5mm pitch	11mm x 11mm
TMC8670-EVAL	Evaluation Board for TMC8670-BI, compatible with the modular Landungsbruecke system, RJ45 twisted pair copper interface	79mm x 85mm

Table 1: TMC8670 order codes

Trademark and Patents

EtherCAT® is a registered trademark and patented technology, licensed by Beckhoff Automation GmbH, Germany.

3 Principles of Operation / Key Concepts

3.1 General Device Architecture

Figure 1 shows the general device architecture and major connections of TMC8670.
The EtherCAT Slave Controller (ESC) is realized in dedicated logic and provides two MII interfaces to external Ethernet PHYs suitable for EtherCAT.
The ESC connects to the integrated microcontroller, which executes the EtherCAT State Machine (ESM) and the CiA DS402 CANopen protocol stack. A debug UART interface connects to the MCU for debugging and firmware updates.
The firmware in the MCU controls the servo and field-oriented control (FOC) block, which is completely realized in dedicated logic. All PI-loops for position, velocity, and torque are fully configurable.
The FOC block drives external gate driver, which in turn are switching a power stage for 3-phase brushless motors or 2-phase stepper motors.
The FOC block provides a set of interfaces for different types of current sensing and position feedback. Current sensing and encoders are external components to the TMC8670.

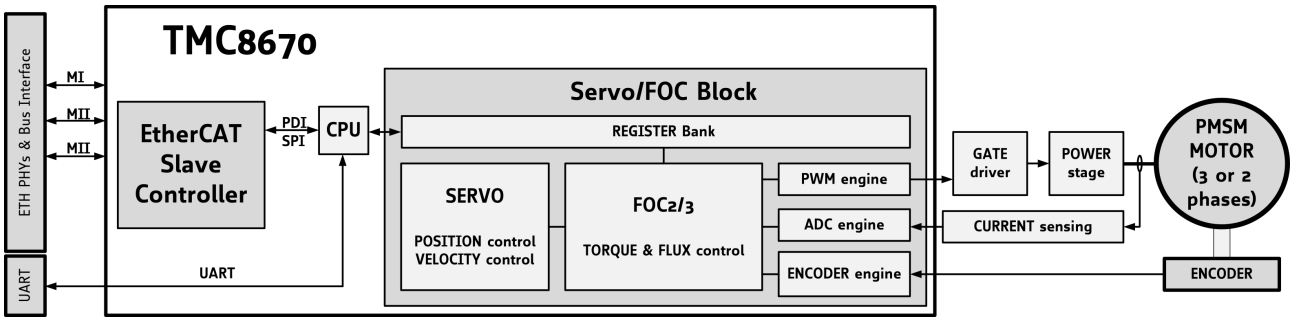


Figure 1: General device architecture

3.2 EtherCAT Slave Controller

TMC8670 contains a standard-conform and proven ESC engine providing real-time EtherCAT MAC layer functionality to EtherCAT slaves. It connects via MII interface to standard Ethernet PHYs and provides a digital control interface to a local application controller

The ESC part of TMC8670 provides the following EtherCAT-related features. More information is available in Section 7.

- Two MII interfaces to external Ethernet PHYs plus management interface
- Four Fieldbus Memory Management Units (FMMU)
- Four Sync Managers (SM)
- 4 KByte of Process Data RAM (PDRAM)
- 64 bit Distributed Clocks support
- IIC interface for an external SII-EEPROM for ESC configuration

3.3 Microcontroller and Firmware Stack

The integrated microcontroller system contains and controls the application layer of TMC8670. Thereby, the firmware is split up into a bootloader section and the application layer section. The bootloader allows

for future firmware updates. The application layer comprises the ESM to communicate with the ESC and the CANopen-over-EtherCAT (CoE) protocol stack. The CoE stack is based on the CiA DS402 device profile for drives. It controls the hardware servo/FOC controller block. The application layer also supports File-Transfer-over-EtherCAT (FoE), which is used for remote firmware updates via the EtherCAT master.

3.4 Servo/FOC Controller

The integrated servo/FOC controller is completely realized in dedicated logic. Its control registers are directly mapped into the microcontrollers address space. It offloads the microcontroller from the repetitive and time-consuming computation tasks of control loop processing, FOC Park and Clark transformations, PWM generation, and interfacing to ADCs and position feedback. The servo/FOC controller supports PWM frequencies and current loop frequencies of up to 100kHZ. It not only supports 3-phase brushless motors but also 2-phase stepper motors and single phase motors, for example DC motors.
More information is given the FOC Basics Section.

3.5 Flexible Sensor Engine

A versatile and flexible sensor engine is part of the servo/FOC controller block of TMC8670. The sensor engine handles digital hall sensors, digital incremental encoders, analog hall sensors, and analog sin-cos-sensors. Together with the relevant sensor parameters, it maps the measured sensor position to 16 bit signed values (s16) for the FOC engine.

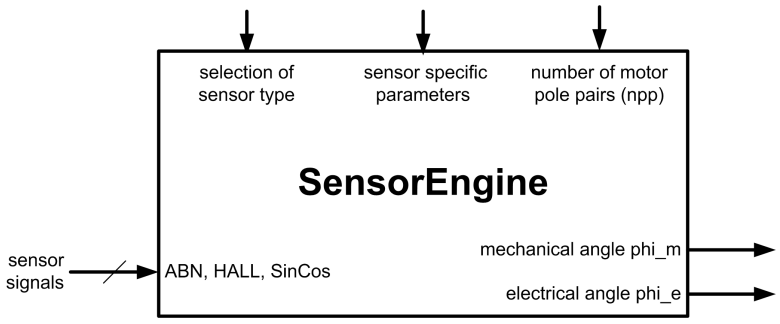


Figure 2: TMC8670 Sensor Engine maps position sensor signals to mechanical angels and electrical angels as direct input for the FOC engine.

ADC Interfaces The TMC8670 is a pure digital IC with interfaces for external ADCs. As ADC one can either select LTC2351 from Linear Technology or Delta Sigma Modulators (AD7401). As an alternative to Delta Sigma Modulators, the TMC8670 supports low cost comparators (e.g. LM339) together with some passive components to form delta sigma modulators.

Digital Encoder Interfaces The digital encoder interface support a wide range of encoders with different resolutions, signal polarities and zero pulses.

Analog Encoder Interfaces The analog encoder interface is for analog hall signals - two phase SinCos or three phase - and for analog (incremental) encoders. An interpollator for SinCos encoders is integrated.

Digital Hall Sensor Interface The digital hall signal interface enables digital hall signals for initialization of incremental encoders. The digital hall signal interface can be used directly for the FOC. For torque ripple reduction an interpolator for the digital hall signals is integrated.

Analog Hall Sensor Interface The interface for analog hall signals is the same interface as available for SinCos analog encoders.

3.6 Communication Interfaces

Field Bus Interface TMC8670 provides two MII ports to connect to 100-Mbit Ethernet PHYs that connect to the field bus. One port is the dedicated EtherCAT IN port. The second port is the dedicated EtherCAT OUT port. Depending on the physical medium (twisted pair copper or passive optical fiber) an external transformer circuit connects to the RX and TX lines.

IIC SII EEPROM Interface The IIC EEPROM interface is intended to be a point-to-point interface between TMC8670 and the SII EEPROM with TMC8670 being the master. Depending on the EEPROM's capacity the addressing mode must be properly set using the PROM_SIZE configuration pin.

Configuration of the EtherCAT Slave Controller is done during boot time with configuration information read from the SII EEPROM after reset or power cycling. This information must be (pre)programmed into the SII EEPROM. This can be done via the EtherCAT master using a so-called EtherCAT Slave Information (ESI) file in standardized XML format.

Debug UART Interfaces TMC8670 has two UART interfaces that allow for basic local debugging. The MCU UART directly connects to the microcontroller and can also be used for local firmware updates. The HW UART directly connects to the servo/FOC controller block and allows for direct control via register read/write of this function block alone. This is usable for local tuning, monitoring of the registers, and debugging.
More details on the two debug UART interfaces are given in the Debug UARTs' section

3.7 Software- and Tool-Support

Evaluation Board An evaluation board is available for the TMC8670 with standard RJ45 connectors and transformers for interfacing twisted pair copper media.

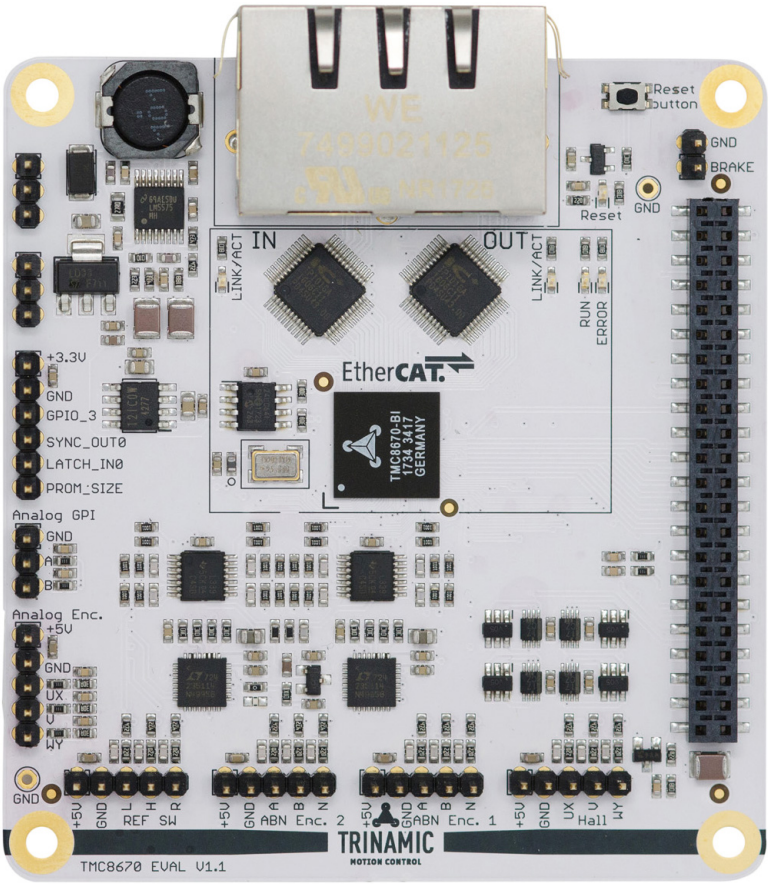


Figure 3: TMC8670 Evaluation Board

The complete board design files are available for download and can be used as reference. All information is available for download on the specific product page on TRINAMIC's website at https://www.trinamic.com/support/eval-kits/.

TMCL-IDE The TMCL-IDE is TRINAMIC's primary tool (for Windows PCs) to control TRINAMIC modules and evaluation boards. Besides, it provides feature like remote firmware updates, module monitoring options, and specific Wizard support. The TMCL-IDE can be used along with TRINAMIC's modular evaluation board system.

Info	The TMLC-IDE is not an EtherCAT master system!

The TMC8670-EVAL can be accessed via the UART interface of the evaluation board to try out the servo functions without using an EtherCAT master in the first place.

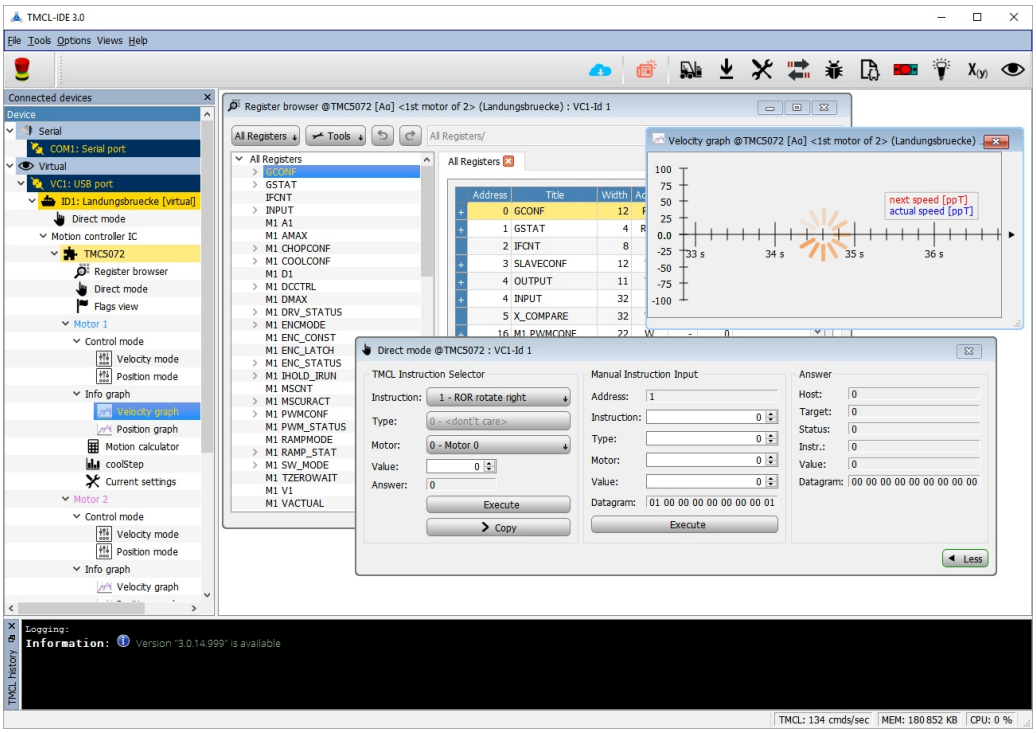


Figure 4: TMCL-IDE

The latest version and additional information is available for download from TRINAMIC's website at https://www.trinamic.com/support/software/tmcl-ide/.

4 Device Pin Definitions

4.1 Pinout and Pin Coordinates of TMC8670-BA

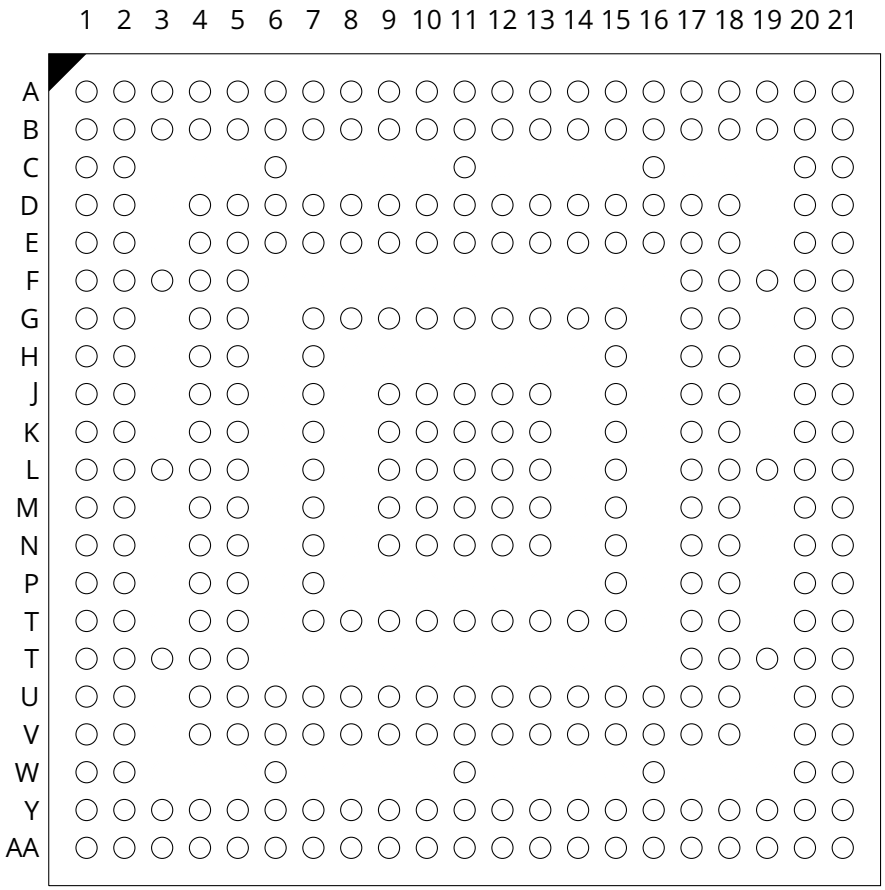


Figure 5: TMC8670-BI Pinout top view

4.2 Pin Numbers and Signal Descriptions

Pins not listed in the following table are N.C. (not connected).
Pin types are I = input, O = output, PU = has pull-up, PD = has pull-down.

Name	Pin	Type	Function
General Signals			
NRESET	M9	I	Low active system reset, pull up to VDD_3V3 with 10K
CLK_25MHZ	P1	I	25MHz Reference Clock Input, connect to clock source with <25ppm or better, typically same clock source as used for the ETH PHYs.
CLKOUT_25MHZ	H17	O	

Name	Pin	Type	Function
EtherCAT SII EEPROM IOs			
PROM_CLK	F1	O	External IIC SII EEPROM clock signal, **use 1K pull up resistor to VDD_3V3**
PROM_DATA	F2	I/O	External IIC SII EEPROM data signal, **use 1k pull up resistor to VDD_3V3**
PROM_SIZE	K1	I, PU	Selects between two different EEPROM sizes since the communication protocol for SII EEPROM access changes if a size > 16kBit is used (an additional address byte is required then). 0 = up to 16kBit EEPROM, 1 = 32 kBit-4Mbit EEPROM, has weak internal pull-up

EtherCAT Status LEDs			
LED_RUN	D1	O	ESM Run Status LED, connect to green LED (Anode) 0 = LED off, 1 = LED on
LED_ERR	D2	O	ESM Error Status LED, connect to red LED (Anode) 0 = LED off, 1 = LED on
LED_LINK_IN	E1	O	ETH Link In Port Status and Activity, connect to green LED (Anode) 0 = LED off, 1 = LED on
LED_LINK_OUT	F3	O	ETH Link Out Port Status and Activity, connect to green LED (Anode) 0 = LED off, 1 = LED on

Distributed Clocks Synchronization			
LATCH_IN0	K2	I, PD	Distributed Clocks Latch Input, has weak internal pull-down
SYNC_OUT0	K4	O	Distributed Clocks Synchronization Output

Name	Pin	Type	Function
MII Interface to external ETH PHY (EtherCAT IN Port)			
MII1_LINK	F18	I	Link indication input
MII1_RXCLK	G18	I	Receive clock
MII1_RXD[0]	F19	I	Receive data bit 0
MII1_RXD[1]	F20	I	Receive data bit 1
MII1_RXD[2]	E21	I	Receive data bit 2
MII1_RXD[3]	E20	I	Receive data bit 3
MII1_RXDV	G21	I	Receive data valid signal
MII1_RXER	G20	I	Receive error signal
MII1_TXCLK	E18	I	Transmit clock
MII1_TXD[0]	D21	O	Transmit data bit 0
MII1_TXD[1]	C21	O	Transmit data bit 1
MII1_TXD[2]	C20	O	Transmit data bit 2
MII1_TXD[3]	B21	O	Transmit data bit 3
MII1_TX_EN	E17	O	Transmit enable
MII Interface to external ETH PHY (EtherCAT OUT Port)			
MII2_LINK	K18	I	Link indication input
MII2_RXCLK	L18	I	Receive clock
MII2_RXD[0]	N21	I	Receive data bit 0
MII2_RXD[1]	M20	I	Receive data bit 1
MII2_RXD[2]	L20	I	Receive data bit 2
MII2_RXD[3]	L21	I	Receive data bit 3
MII2_RXDV	N20	I	Receive data valid signal
MII2_RXER	M18	I	Receive error signal
MII2_TXCLK	J17	I	Transmit clock
MII2_TXD[0]	L19	O	Transmit data bit 0
MII2_TXD[1]	K21	O	Transmit data bit 1
MII2_TXD[2]	J20	O	Transmit data bit 2
MII2_TXD[3]	J21	O	Transmit data bit 3
MII2_TX_EN	J18	O	Transmit enable

Name	Pin	Type	Function
ETH PHY Interface Configuration Pins and Management Interface			
LINK_POLARITY	R9	I, PD	selects polarity of the ETH PHYs link signal: 0 = low active, 1 = high active
MII1_TX_SHIFT[0]	K15	I	Used for clock shift compensation on TX port
MII1_TX_SHIFT[1]	K17	I	Used for clock shift compensation on TX port
MII2_TX_SHIFT[0]	L15	I	Used for clock shift compensation on TX port
MII2_TX_SHIFT[1]	L17	I	Used for clock shift compensation on TX port
MCLK	H20	O	PHY management clock, connect all ETH PHYs to this bus
MDIO	H21	I/O	PHY management data, connect all ETH PHYs to this bus if required, **use 4K7 pull up resistor to VDD_3V3**
Motor Position Feedback Signals			
ENC_A	N1	I, PU	incremental encoder signal A
ENC_B	N2	I, PU	incremental encoder signal B
ENC_N	P2	I, PU	incremental encoder null pulse N
ENC_2_A	V6	I, PU	2nd incremental encoder signal A
ENC_2_B	V7	I, PU	2nd incremental encoder signal B
ENC_2_N	W6	I, PU	2nd incremental encoder null pulse N
HALL_UX	M4	I, PU	digital Hall signal associated to U (H1)
HALL_V	N4	I, PU	digital Hall signal associated to V (H2)
HALL_WY	P4	I, PU	digital Hall signal associated to W (H1)
ENC_ADC_CSN	L3	O	analog encoder SPI ADC LTC2351 CONV
ENC_ADC_MISO	L1	I	analog encoder SPI ADC LTC2351 SDO
ENC_ADC_SCK	L2	O	analog encoder SPI ADC LTC2351 SCK

Reference Switch Signals			
REF_SW_H	H5	I, PU	Home Reference Switch
REF_SW_L	H4	I, PU	Left Reference Switch
REF_SW_R	J4	I, PU	Right Reference Switch

Name	Pin	Type	Function
Motor and Supply Current Measurement Signals			
SPI_ADC_CSN	U8	O	analog current measurement SPI ADC LTC2351 CONV
SPI_ADC_SCK	U9	O	analog current measurement SPI ADC LTC2351 SCK
SPI_ADC_MISO	U10	I, PU	analog current measurement SPI ADC LTC2351 SDO
ADC_PHASE_MISO_2ND	U11	I, PU	analog current measurement SPI ADC LTC2351 SDO
MCLK_AENC_UX	P5	IO	DS-Mod Clock analog encoder/analog Hall U or X
MCLK_AENC_VN	R4	IO	DS-Mod Clock analog encoder/analog Hall V or N
MCLK_AENC_WY	U4	IO	DS-Mod Clock analog encoder/analog Hall W or Y
MCLK_AGPI_A	T2	IO	DS-Mod Clock for Analog General Purpose Input AGPI_A
MCLK_AGPI_B	U2	IO	DS-Mod Clock for Analog General Purpose Input AGPI_B
MCLK_I_UX	V1	IO	DS-Mod Clock for Analog Current Sense Voltage of I_U or I_X
MCLK_I_WY	AA2	IO	DS-Mod Clock for Analog Current Sense Voltage of I_W or I_Y
MCLK_VM	T3	IO	DS-Mod Clock for (down-divided) motor supply voltage of V_M
MDAT_AENC_UX	R5	I	DS-Mod Data Stream for analog encoder/analog Hall U or X
MDAT_AENC_VN	T5	I	DS-Mod Data Stream for analog encoder/analog Hall V or N
MDAT_AENC_WY	U5	I	DS-Mod Data Stream for analog encoder/analog Hall W or Y
MDAT_AGPI_A	T1	I	DS-Mod Data Stream for Analog General Purpose Input AGPI_A
MDAT_AGPI_B	U1	I	DS-Mod Data Stream for Analog General Purpose Input AGPI_B
MDAT_I_UX	W1	I	DS-Mod Data Stream for Analog Current Sense Voltage of I_U or I_X
MDAT_I_WY	W2	I	DS-Mod Clock for Analog Current Sense Voltage of I_W or I_Y
MDAT_I_UX_2ND	Y1	I, PU	DS-Mod Data stream for Analog Current Sense Voltage of I_U or I_X
MDAT_I_WY_2ND	Y2	I, PU	DS-Mod Data stream for Analog Current Sense Voltage of I_W or I_Y
MDAT_VM	R2	I	DS-Mod Data stream for (down-divided) motor supply voltage of V_M

Name	Pin	Type	Function
PWM Signals			
PWM_UX1_H	Y7	O	Digital gate control signal for High Side of Phase U (FOC3) or X1 (FOC2)
PWM_UX1_L	AA7	O	Digital gate control signal for Low Side of Phase U (FOC3) or X1 (FOC2)
PWM_VX2_H	Y8	O	Digital gate control signal for High Side of Phase V (FOC3) or X2 (FOC2)
PWM_VX2_L	AA8	O	Digital gate control signal for Low Side of Phase V (FOC3) or X2 (FOC2)
PWM_WY1_H	Y10	O	Digital gate control signal for High Side of Phase W (FOC3) or Y1 (FOC2)
PWM_WY1_L	AA10	O	Digital gate control signal for Low Side of Phase W (FOC3) or Y1 (FOC2)
PWM_Y2_H	AA11	O	Digital gate control signal for High Side of Phase Y2 (FOC2)
PWM_Y2_L	Y11	O	Digital gate control signal for Low Side of Phase Y2 (FOC2)

Additional Control Signals			
ENABLE_OUT	W11	O	enable output
BRAKE_CHOPPER	Y9	O	brake chopper control signal

Debug UART Interfaces and Debug I/Os			
STATUS_OUT	M5	O	status signal output
RXD_HWI	G5	I, PU	HW debug UART, RxD input
TXD_HWO	G4	O	HW debug UART, TxD output
RXD_MCU	G2	I, PU	MCU debug UART, RxD input
TXD_MCU	G1	O	MCU debug UART, TxD output
MCU_GPO_15	V8	O	reserved, keep open
MCU_GPO_16	V10	O	reserved, keep open
MCU_GPO_17	V11	O	reserved, keep open
MCU_GPO_18	U12	O	reserved, keep open
PDI_IRQ	K5	O	reserved, keep open (GPIO_3 on TMC8670 EVAL V.1.1)

Name	Pin	Type	Function
Device Supply and Ground			
VDD_1V2	K10, K11, L10, L11, M12, M13, N12, N13, R12, R13, U14, V14, V16, W16		1.2V DC Core supply voltage, **use 100nF filter capacitors**
VDD_3V3	M7, U15, V12, K9, H7, G15, R14, E2, J5, M2, N5, V2, V5, AA9, R10, V9, D20, F17, J15, K20		3.3V supply voltage for I/Os, PLL, and NVM, **use 100nF filter capacitors**
GND	G7, H15, R15, A1, A11, A16, A21, A6, AA1, AA12, AA14, AA15, AA16, AA18, AA19, AA20, D12, D17, D7, F21, F4, G14, H1, H18, J10, J11, J7, K12, K13, L12, L13, L4, M10, M11, M17, M21, N10, N11, P15, P7, R1, T21, T4, U13, U16, U17, U6, U7, V13, V15, Y12, Y14, Y15, Y16, Y18, Y19, Y20, Y6, J9		Supply Ground

Explicitly Not Connected Pins		
N.C.	R11, Y4, V17, V18, Y13, Y17, Y5, D18, G12, G8, AA5, AA4, AA13, AA17, B13, B18, B3, B8, E14, E9, J12, J13, W20, N15, R18	not connected

Name	Pin	Type	Function
Test Pins only			
DUMMY_OUT	G17	O	reserved, keep open
JTAG_TCK	L9	I	JTAG test clock, pull up to VDD_3V3 with 1K
JTAG_TDI	N9	I	JTAG Test data, N.C.
JTAG_TDO	R7	O	JTAG Test data, N.C.
JTAG_TMS	AA3	I	JTAG Test mode select, N.C.
JTAG_TRSTB	Y3	I	JTAG Test reset, pull down to GND with 1K
JTAGSEL	V4	I	JTAG Select line, pull up to VDD_3V3 with 1K

Table 2: Pin and Signal description for TMC8670-BA

5 Device Usage and Handling

5.1 Reference Clock

TMC8670 and the external Ethernet PHYs must share the same clock source. For proper operation a stable and accurate 25MHz clock source is required. The recommended initial accuracy must be at least 25ppm or better.

TMC8670 has been successfully used with the following crystal oscillators so far (this list ist not limited to the mentioned parts):

- FOX Electronics FOX924B TCXO, 25.0MHz, 2.5ppm, 3.3V
- TXC 7M-25.000MAAJ-T XO 25.0MHz, 30ppm
- CTS 636L5C025M00000, 25MHz, 25ppm

5.2 Ethernet PHY Connection

For connection to the Ethernet physical medium and to the EtherCAT master, TMC8670 offers two MII ports (media independent interface) and connects to standard 100Mbit/s Ethernet PHYs or 1Gbit/s Ethernet PHYs running in 100Mbit/s mode.

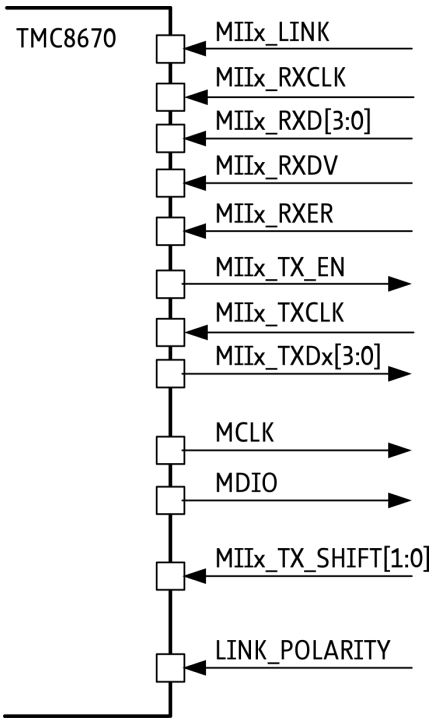


Figure 6: MII interface

TMC8670 pin	Description
MIIx_LINK	Active link input signal, active high/active low determined by LINK_POLARITY pin
MIIx_RXCLK	Receive clock input
MIIx_RXD[3:0]	Receive data inputs (4 bit wide)
MIIx_RXDV	Receive data valid input
MIIx_RXER	Receive error input
MIIx_TX_EN	Transmit enable output
MIIx_TXCLK	Transmit clock input, optional for automatic phase compensation
MIIx_TXD[3:0]	Transmit data output (4 bit wide)
MCLK	PHY MI configuration clock output
MDIO	PHY MI configuration data in-/output
MIIx_TX_SHIFT[1:0]	Phase compensation of MII TX signals, tie either to GND or VDD_3V3
LINK_POLARITY	Active level of MIIx_LINK signal, tie either to GND or VDD_3V3

Table 3: MII signal description

TMC8670 requires Ethernet PHYs with MII interface. The MII interface of TMC8670 is optimized for low additional delays by omitting a transmit FIFO. Additional requirements to Ethernet PHYs exist and not every Ethernet PHY is suited. Please see the Ethernet PHY Selection Guide provided by the ETG: http://download.beckhoff.com/download/Document/EtherCAT/Development_products/AN_PHY_Selection_GuideV2.6.pdf.

TMC8670 has been successfully tested in combination with the following Ethernet PHYs so far:

- IC+ IP101GA: http://www.icplus.com.tw
- Micrel KSZ8721BLI: http://www.micrel.com
- Micrel KSZ8081: http://www.micrel.com

The clock source of the Ethernet PHYs is the same as for the TMC8670.

LINK_POLARITY
This pin allows configuring the polarity of the link signal of the PHY. PHYs of different manufacturers may use different polarities at the PHY's pins.
In addition, some PHYs allow for bootstrap configuration with pull-up and pull-down resistors. This bootstrap information is used by the PHY at power-up/reset and also influences the polarity of the original pin function.

ETH PHY Addressing The TMC8670 addresses Ethernet PHYs using the logical port numbers 0 (LINK IN port) and 1 (LINK OUT port). Typically, the Ethernet PHY addresses should correspond with the logical port number, so PHY addresses have to be set to 0 and 1 accordingly using the ETH PHYs' bootstrap and configuration options.

MII_TX_SHIFT[1:0] TMC8670 and Ethernet PHYs share the same clock source. TX_CLK from the PHY has a fixed phase relation to the MII interface TX part of TMC8670Ṫhus, TX_CLK must not be connected and the delay of a TX FIFO inside the IP Core is saved. In order to fulfill the setup/hold requirements of the PHY, the phase shift between TX_CLK and MIIx_TX_EN and MIIx_TXD[3:0] has to be controlled.

- Manual TX Shift compensation with additional delays for MIIx_TX_EN/MIIx_TXD[3:0] of 10, 20, or 30 ns. Such delays can be added using the TX Shift feature and applying MIIx_TX_SHIFT[1:0]. MIIx_TX_SHIFT[1:0] determine the delay in multiples of 10 ns for each port. Set MIIx_TXCLK to zero if manual TX Shift compensation is used.
- Automatic TX Shift compensation if the TX Shift feature is selected: connect MIIx_TXCLK and the automatic TX Shift compensation will determine correct shift settings. Set MIIx_TX_SHIFT[1:0] to 0 in this case.

5.3 External Circuitry and Applications Examples

5.3.1 Supply and Filtering

There should be one 100nF cap for each two VDD_1V2 pins. There should be one 100nF cap for circa each two VDD_3V32 pins. They should be placed as near as possible to the pins.

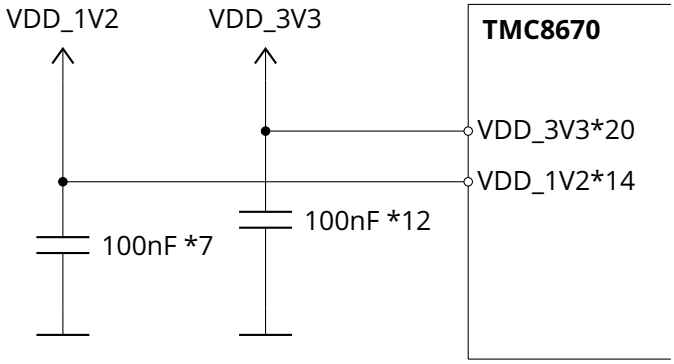


Figure 7: PLL supply filter

5.3.2 Status LED Circuit

The TMC8670 has 4 status LED outputs. All outputs are supplied from VDD_3V3, and drive a LED with current limiting resistor to GND. The use of low current LED is recommended to keep supply current low and to stay within the current limit of 10mA per pin. The appropriate resistor value must be chosen for the selected LED's forward voltage.
For a 2V forward voltage at 2mA, a value of ca. 680 Ohm is a reasonable value.
The LED colors are defined by **ETG.1300** (available on www.ethercat.org).

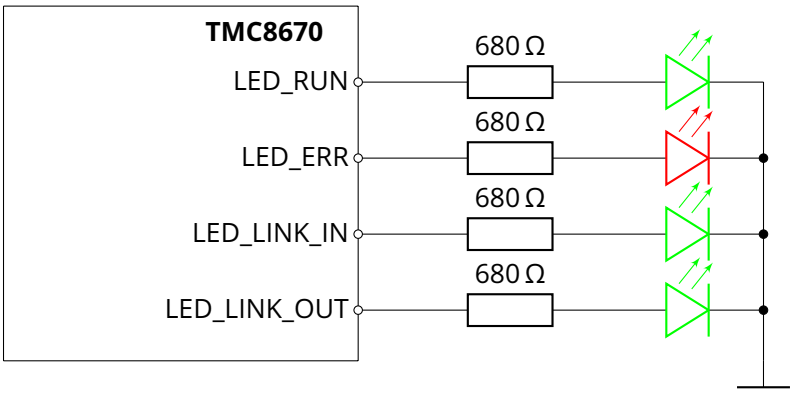


Figure 8: Status LED circuit

5.3.3 SII EEPROM Circuit

An IIC EEPROM is required for operation with the SII interface. Its size can be up to 4MBit. While the access protocol of the IIC EEPROMs is standardized, the addressing procedure changes from one address byte up to 16kBit to two address bytes from 32kBit.

Up to 16kBit the PROM_SIZE pin must be tied to GND, above that, it must be tied to VDD_3V3.

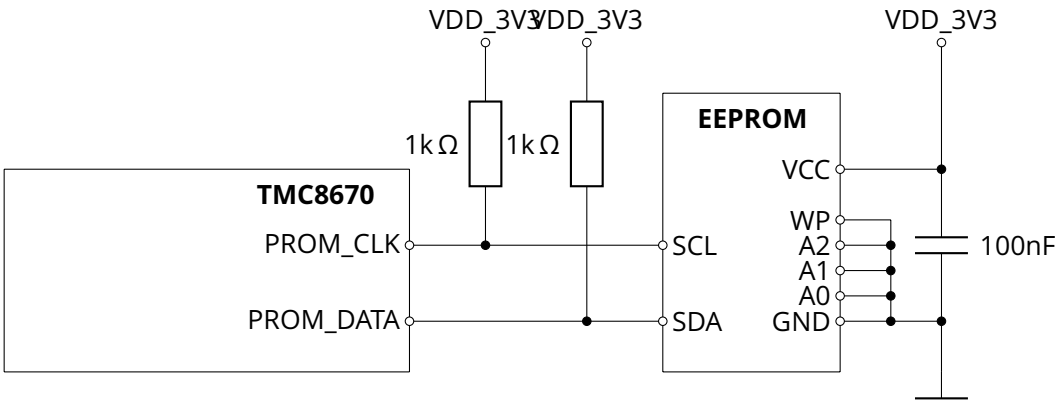


Figure 9: SII EEPROM circuit

5.4 Incremental Encoder Connection

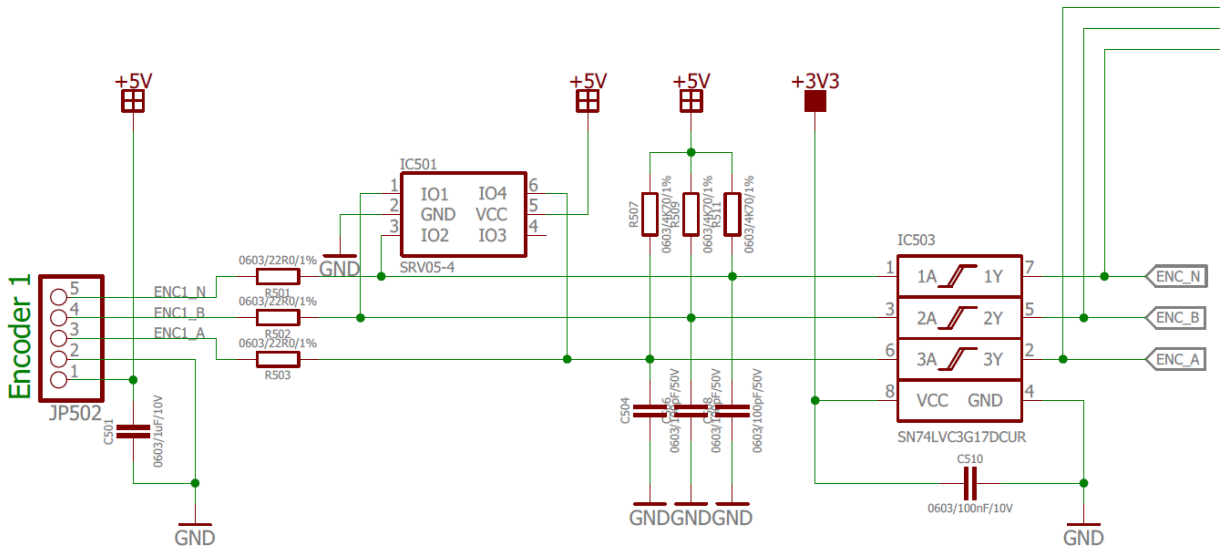


Figure 10: Example circuit for connecting an incremental encoder with level shifters from typically 5V to 3.3V

5.4.1 Incremental ABN Encoder

The incremental encoders give two phase shifted incremental pulse signals A and B. Some incremental encoders have an additional null position signal N or zero pulse signal Z. An incremental encoder (called ABN encoder or ABZ encoder) has an individual number of incremental pulses per revolution. The number of incremental pulses define the number of positions per revolution (PPR). The PPR might mean pulses per revolution or periods per revolution. Instead of positions per revolution some incremental encoder vendors call these CPR counts per revolution.

The PPR parameter is the most important parameter of the incremental encoder interface. With that, it forms a modulo (PPR) counter, counting from 0 to (PPR-1). Depending on the direction, it counts up or down. The modulo PPR counter is mapped into the register bank as a dual ported register. the user can over over write it with an initial position. The ABN encoder interface provides both, the electrical position and the multi-turn position are dual-ported read-write registers.

Note	The PPR parameter must be set exactly according to the used encoder.

The N pulse from an encoder triggers either sampling of the actual encoder count to fetch the position at the N pulse or it re-writes the fetched n position on an N pulse. The N pulse can either be uses as stand alone pulse or and-ed with NAB = N and A and B. It depends on the decoder what kind of N pulse has to be used, either N or NAB. For those encoder with precise N pulse within on AB quadrat, the N pulse must be used. For those encoders with N pulse over four AB quadrants one can enhance the precision of the N pulse position detection by using NAB instead of N.

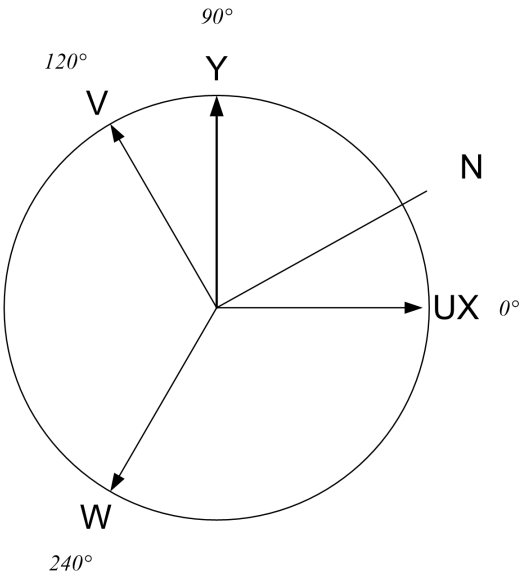


Figure 11: ABN Incremental Encoder N Pulse

The polarity of N pulse, A pulse and B pulse are programmable. The N pulse is for re-initialization with each turn of the motor. Once fetched, the ABN decoder can be configured to write back the fetched N pulse position with each N pulse.

Note	Incremental encoders are available with N pulse and without N pulse.

Note	The ABN encoder interface has a direction bit to set once the direction of motion for the application.

Logical ABN = A and B and N might be useful for incremental encoders with low resolution N pulse to enhance the resolution. On the other hand, for incremental encoders with high resolution n pulse a logical abn = a and b and n might totally suppress the resulting n pulse.