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TMD2620

Proximity Sensor Module

General Description

The device is an advanced proximity sensor. The slim module incorporates an IR LED and factory calibrated LED driver. The proximity detection feature provides object detection (e.g. mobile device screen to user's ear) by photodiode detection of reflected IR energy (sourced by the integrated LED).

Detect/release events are interrupt driven, and occur when proximity result crosses upper and/or lower threshold settings.

The proximity engine features offset adjustment registers to compensate for unwanted IR energy reflection at the sensor. Proximity results are further improved by automatic ambient light subtraction.

Ordering Information and *Content Guide* appear at end of datasheet.

Figure 1:
Added Value of Using TMD2620

| Benefits	Features
• Reduced board space requirements and enables low-profile system design	• Small footprint and low profile package • 3.10 x 2.00 x 1.00 mm
• Reduced power consumption	• 0.18µm process technology with 1.8V I²C bus

Applications

The TMD2620 is ideal for mobile phone touch screen disable.

Block Diagram

The functional blocks of this device are shown below:

Figure 2:
Functional Blocks of TMD2620
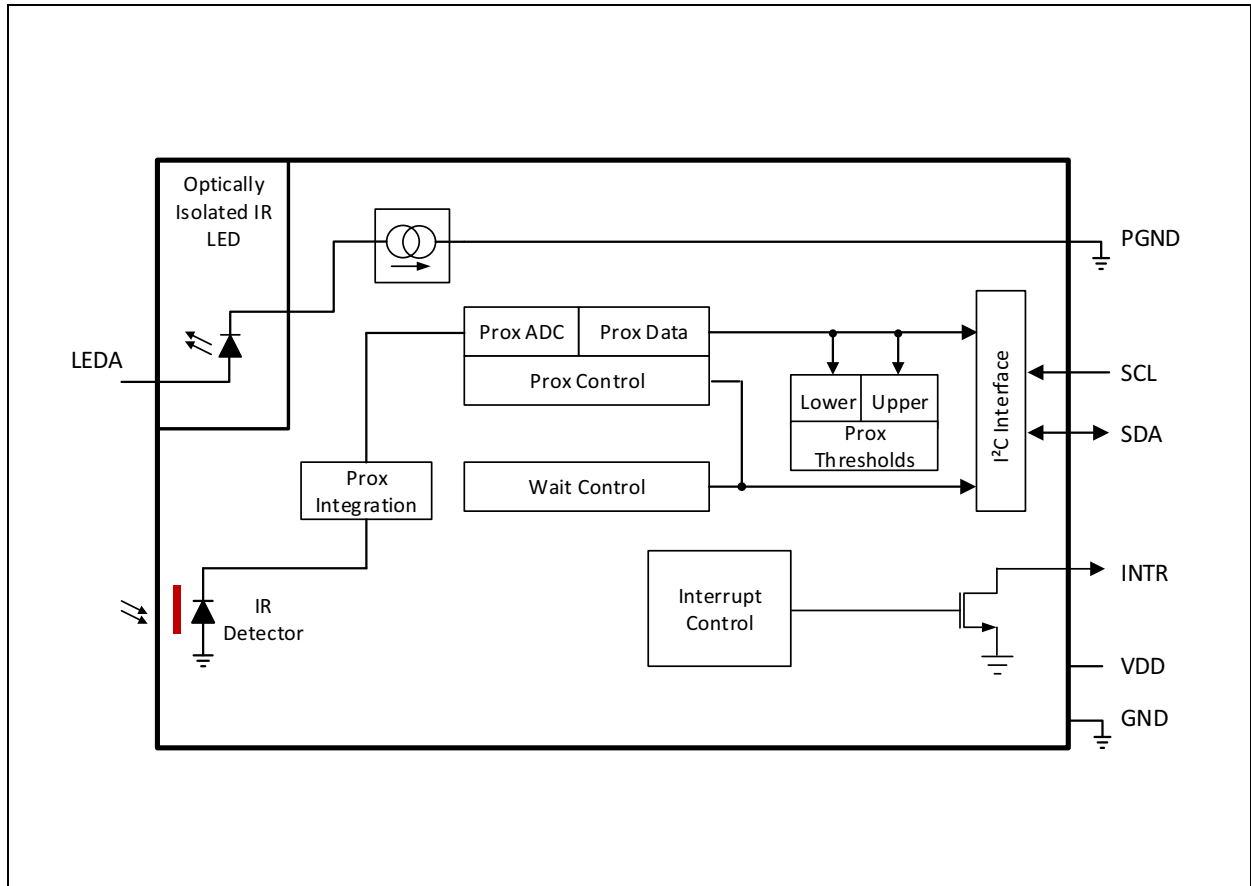
Pin Assignment
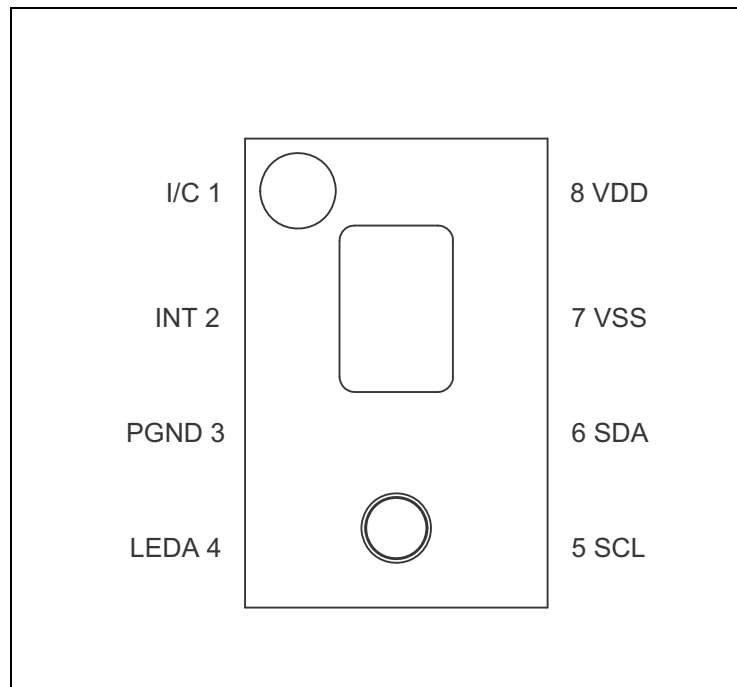
Figure 4:
Pin Description

Pin Number	Pin Name	Description
1	I/C	Internal connection. Connect to ground.
2	INT	Interrupt. Open drain output (active low)
3	PGND	Ground for LED current sink and I/O buffers
4	LEDA	LED anode
5	SCL	I^{2}C serial clock input
6	SDA	I^{2}C serial data I/O terminal
7	VSS	Ground. All voltages are referenced to GND
8	VDD	Supply voltage

Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 5:
Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
VDD	Supply voltage	-0.3	2.2	V
LEDA	Supply voltage	-0.3	3.6	V
V_{IO}	Digital I/O terminal voltage	-0.3	3.6	V
(SDA, INT)	Output terminal current	-1	20	mA
T_{STRG}	Storage temperature range	-40	85	ºC
I_{SCR}	Input current (latch up immunity) JEDEC JESD78D Nov 2011	CLASS 1		
ESD_{HBM}	Electrostatic discharge HBM S-001-2014	±2000		V
ESD_{CDM}	Electrostatic discharge CDM JEDEC JESD22-C101F Oct 2013	±500		V

Electrical Characteristics

Figure 6:
Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{DD}	Supply voltage	1.7	1.8	2.0	V
V_{LEDA}	Voltage supplied to LEDA pin		3.3		V
T_A	Operating free-air temperature [1]	-30		85	℃

Note(s):

1. While the device is operational across the temperature range, performance will vary with temperature. Operational characteristics are at 25°C, unless otherwise noted.

Figure 7:
Operating Characteristics, V_{DD} = 1.8 V, T_A = 25°C (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_{OSC}	Oscillator frequency			8.0		MHz
IDD	Supply current [1]	Idle state (PON=1, PEN=0) [2]		30		µA
		Sleep state [3]		0.7	5.0	µA
VOL	INT, SDA output low voltage	6 mA sink current			0.6	V
ILEAK	Leakage current, SDA, SCL, INT pins		-5		5	µA
VIH	SCL, SDA input high voltage		1.26			V
VIL	SCL, SDA input low voltage				0.54	V

Note(s):

1. Values are shown at the VDD pin and do not include current through the IR LED.

2. Idle state occurs when PON=1 and all functions are not enabled.

3. Sleep state occurs when PON = 0 and I²C bus is idle. If Sleep state has been entered as the result of operational flow, SAI = 1, PON will remain high.

Figure 8:
Proximity Optical Characteristics of TMD2620

Parameter	Conditions	Min	Typ	Max	Unit
Part to part variation [1]	Conditions: PGAIN = 2 (4x) PLDRIVE = 8 (54mA) PPULSE = 15 (16 pulses) PPULSE_LEN = 1 (16µs) d=23mm round target 30mm target distance	75	100	125	%
Response, absolute	Basic proximity measurement [2] Conditions: PGAIN = 2 (4x), PLDRIVE = 7(48mA) PPULSE = 15 (16 pulses) PPULSE_LEN = 2 (16µs) Target material: 90% reflective surface of Kodak gray card Target Size: 100mm x 100mm Target Distance: 60mm	82	103	123	Counts
Response, no target using offset values from 0xE6 and 0xE7	PGAIN = 2 (4x) ILEDDRIVE = 16 (102mA) PPULSE = 16 (17 Pulses) Pulse Length = 2 (16µS)	0		10	
Noise/Signal [3]	PGAIN = 2 (4x) IRLEDDRIVE = 8 (54mA) PPULSE = 15 (16 pulses) PPULSE_LEN = 1 (8µs) d=23mm round target 30mm target distance			1	%

Note(s):

1. Production tested result is the average of 5 readings expressed relative to a calibrated response.

2. Representative result by characterization.

3. Production tested result is the average of 20 readings divided by the average response.
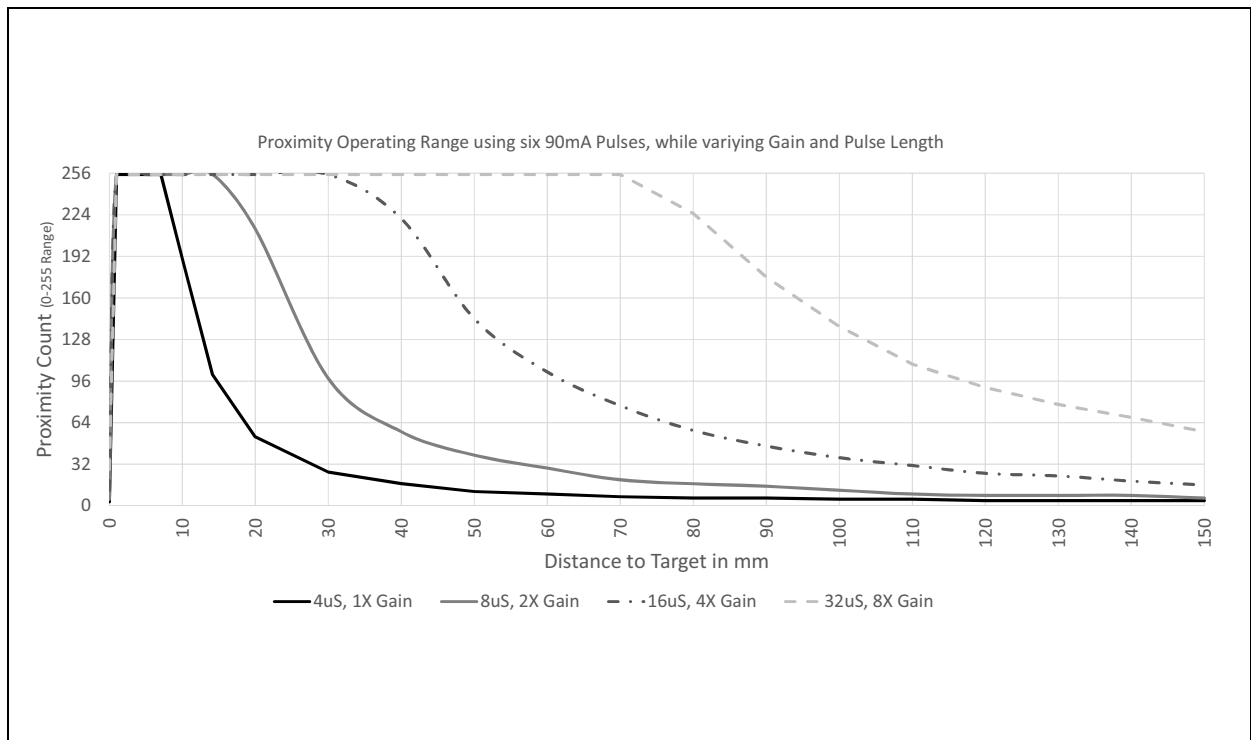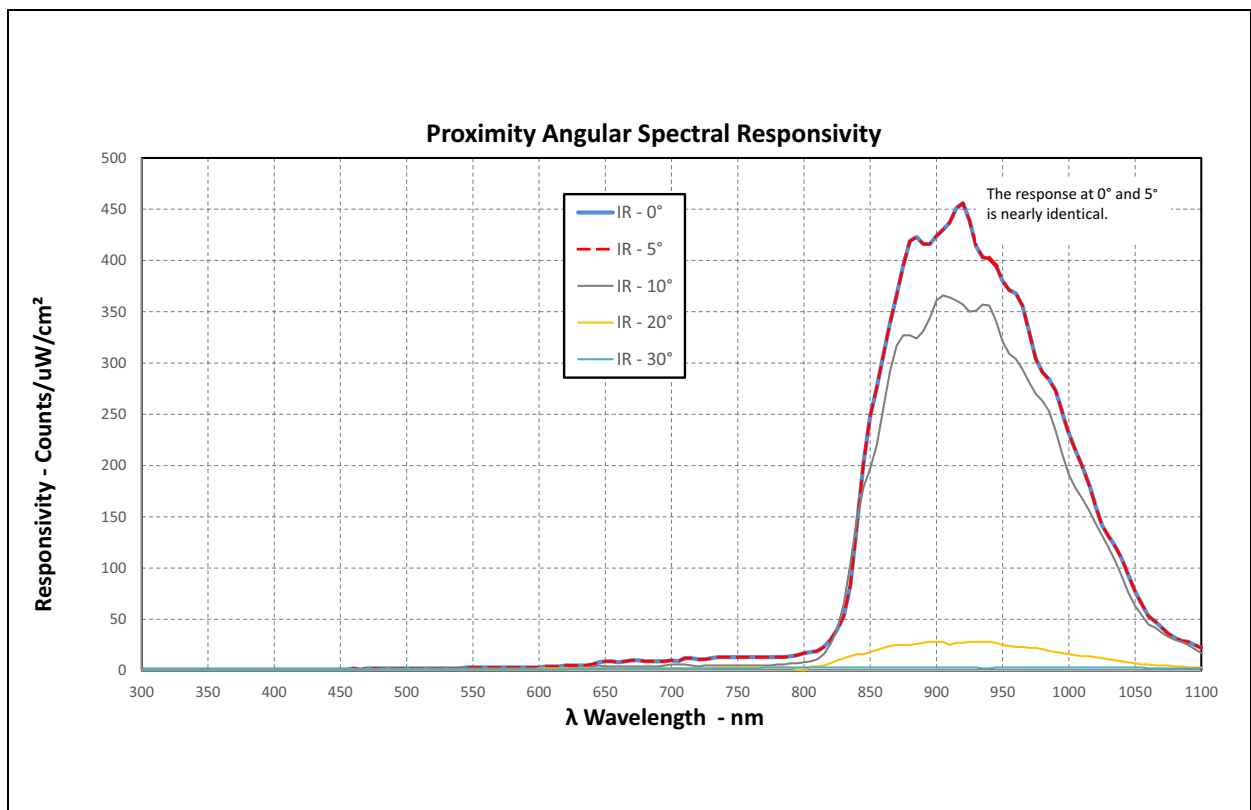
Figure 9:
Proximity Operation

Figure 10:
Proximity Angular Spectral Response

Register Description

Device address is 0x29.

Figure 11:
Register Overview

Address	Register Name	R/W	Register Function	Reset Value
0x80	ENABLE	R/W	Enables states and interrupts	0x00
0x82	PRATE	R/W	Proximity sample rate	0x1F
0x83	WTIME	R/W	Wait time	0x00
0x88	PILT	R/W	Proximity interrupt low threshold	0x00
0x8A	PIHT	R/W	Proximity interrupt high threshold	0x00
0x8C	PERS	R/W	Proximity interrupt persistence filters	0x00
0x8D	CFG0	R/W	WTIME configuration	0x80
0x8E	PCFG0	R/W	Proximity pulse width and count	0x4F
0x8F	PCFG1	R/W	Proximity gain and LED current	0x80
0x91	REVID	R	Revision ID	
0x92	ID	R	Device ID	0xD4
0x93	STATUS	R, SC	Device status register one	0x00
0x9C	PDATA	R	Proximity ADC data register MSBs	0x00
0x9E	REVID2	R	Reserved	0x00
0x9F	CFG2	R/W	Configuration register two	0x00
0xAB	CFG3	R/W	Configuration register three	0x0C
0xC0	POFFSET_L	R/W	Proximity offset value	0x00-0xFF
0xC1	POFFSET_H	R/W	Proximity offset sign	0x00-0xFF
0xD7	CALIB	R/W	Calibration control	0x00
0xD9	CALIBCFG	R/W	Calibration configuration	0x00
0xDC	CALIBSTAT	R/W	Calibration status bit	0x00
0xDD	INTENAB	R/W	Interrupt enables	0x00

Register Access:

- R = Read Only
- W = Write Only
- R/W = Read or Write
- SC = Self Clearing after access

ENABLE Register (0x80)

Figure 12:
ENABLE Register

	0x80: ENABLE			
Field	**Name**	**Reset**	**Type**	**Description**
7:4	Reserved	0	RW	Reserved
3	wen	0	RW	Wait Enable. This bit activates the wait feature. Writing a one actives the wait timer. Writing a zero disables the wait timer.
2	pen	0	RW	Proximity Detect Enable. This field activates the proximity detection.
1	Reserved	0	RW	Reserved
0	pon	0	RW	Power On. This field activates the internal oscillator to permit the timers and ADC channels to operate. Writing a one activates the oscillator. Writing a zero disables the oscillator.

The Mode/Parameter fields should be written before pen is asserted. The function pen require pon to be asserted for the respective function to operate correctly.

PRATE Register (0x82)

Figure 13:
PRATE Register

	0x82: PRATE			
Field	**Name**	**Reset**	**Type**	**Description**
7:0	prate	0x1F	RW	When averaging is turned on, this register defines the time between proximity measurements. The time will be 88µs times this register's value.

WTIME Register (0x83)

Figure 14:
WTIME Register

				0x83: WTIME		
Field	**Name**	**Reset**	**Type**	**Description**		
7:0	wtime	0x00	RW	Wait Time. Eight bit value that specifies the time		
				Value	**Wait Cycles**	**Wait Time**
				0x00	1	2.81ms/ 33.8ms
				0x01	2	5.6ms/ 67.6ms
				...	...	...
				0x3f	63	180ms/ 2.16s
				...	...	...
				0xff	255	721ms/ 8.65s

The wait timer is implemented with a down counter with 0x00 as the terminal count. Loading 0x00 will generate a 2.81ms wait time, loading 0x01 will generate a 5.6ms wait time, and so forth; by asserting wlong, in register 0x8D the wait time is given in multiples of 33.8ms (12x).

PILT Register (0x88)

Figure 15:
PILT Register

0x88: PILT				
Field	**Name**	**Reset**	**Type**	**Description**
7:0	pilt	0	RW	Proximity ADC Channel Low Threshold

This register provides the low interrupt threshold.
If the value generated by the proximity channel is below the low threshold specified and the PPERS value is reached, the pint bit is asserted which will assert the INT pin if pien is set.

PIHT Register (0x8A)

Figure 16:
PIHT Register

0x8A: PIHT				
Field	**Name**	**Reset**	**Type**	**Description**
7:0	piht	0	RW	Proximity ADC Channel High Threshold

This register provides the high interrupt threshold.
If the value generated by the proximity channel is above the high threshold specified and the PPERS value is reached, the pint bit is asserted which will assert the INT pin if pien is set.

PERS Register (0x8C)

This register controls the interrupt filtering capabilities of the device. Configurable filtering is provided to allow interrupts to be generated after a proximity cycle or if the integration cycle has produced a result that is outside of the values specified by threshold register for some specified number of times.

Figure 17:
PERS Register

0x8C: PERS				
Field	**Name**	**Reset**	**Type**	**Description**
7:4	ppers	0	RW	Proximity Persistence Filtering <table><tr><td>**Value**</td><td>**Interrupt generated when...**</td></tr><tr><td>0</td><td>Every proximity cycle</td></tr><tr><td>1</td><td>Any proximity value outside of threshold range</td></tr><tr><td>2</td><td>2 consecutive proximity values out of range</td></tr><tr><td>3</td><td>3 consecutive proximity values out of range</td></tr><tr><td>...</td><td>...</td></tr><tr><td>15</td><td>15 consecutive proximity values out of range</td></tr></table>
3:0	Reserved	0	RW	Reserved

CFG0 Register (0x8D)

Figure 18:
CFG0 Register

0x8D: CFG0				
Field	**Name**	**Reset**	**Type**	**Description**
7:3	Reserved	1 0 0 0 0	RW	Reserved. Must be set to 10000.
2	wlong	0	RW	Wait Long. When asserted, the wait cycle is increased by a factor 12x from that programmed in the WTIME register.
1:0	Reserved	0 0	RW	Reserved. Must be set to 00.

PCFG0 Register (0x8E)

Figure 19:
PCFG0 Register

0x8E: PCFG0				
Field	**Name**	**Reset**	**Type**	**Description**
7:6	ppulse_len	1	RW	Proximity Pulse Length <table><tr><td>**Value**</td><td>**Pulse Length**</td></tr><tr><td>0</td><td>4µs</td></tr><tr><td>1</td><td>8µs</td></tr><tr><td>2</td><td>16µs</td></tr><tr><td>3</td><td>32µs</td></tr></table>
5:0	ppulse	15	RW	Maximum Number of Pulses in Proximity <table><tr><td>**Value**</td><td>**Number of Pulses**</td></tr><tr><td>0</td><td>1</td></tr><tr><td>1</td><td>2</td></tr><tr><td>2</td><td>3</td></tr><tr><td>...</td><td>...</td></tr><tr><td>63</td><td>64</td></tr></table>

PCFG1 Register (0x8F)

Figure 20:
PCFG1 Register

0x8F: PCFG1				
Field	**Name**	**Reset**	**Type**	**Description**
7:6	pgain	2	RW	Proximity Gain Control. Sets the gain of the proximity receiver. **Value** / **Gain Value** 0 / 1x 1 / 2x 2 / 4x 3 / 8x
5	Reserved	0	RW	Reserved
4:0	pldrive	0	RW	Proximity LED Drive Strength. This is configured linearly in steps of 6mA, this is the nominal value. The actual value depends on the trim procedure. **Value** / **LED Current** 0 / 6mA 1 / 12mA … / … 31 / 192mA

REVID Register (0x91)

Figure 21:
REVID Register

0x91: REVID				
Field	**Name**	**Reset**	**Type**	**Description**
7:3	Reserved	0	RO	Reserved
2:0	rev_id		RO	Revision Number Identification

ID Register (0x92)

Figure 22:
ID Register

0x92: ID						
Field	**Name**	**Reset**	**Type**	**Description**		
7:2	ID	0x35	RO	Part Number Identification		
				Value		**Meaning**
				110101		TMD2620
1:0	Reserved	00	RO	Reserved		

STATUS Register (0x93)

Figure 23:
STATUS Register

				0x93: STATUS	
Field	**Name**	**Reset**	**Type**	**Description**	
7	Reserved	0	R, SC	Reserved	
6	psat	0	R, SC	Proximity Saturation. Indicates that an ambient- or reflective-saturation event occurred during a previous proximity cycle. Writing a 1 will clear this status flag; to enable clear-by-read function, the register CFG3.int_read_clear must be set 1	
5	pint	0	R, SC	Proximity Interrupt. Indicates that the device is asserting a proximity interrupt. Writing a 1 will clear this status flag; to enable clear-by-read function, the register CFG3.int_read_clear must be set 1	
4	Reserved	0	R, SC	Reserved	
3	cint	0	R, SC	Calibration Interrupt. Writing a 1 will clear this status flag; to enable clear-by-read function, the register CFG3.int_read_clear must be set 1	
2	zint	0	R, SC	Zero Detection Interrupt. Writing a 1 will clear this status flag. Enable clear-byread with CFG3	
1	psat_reflective	0	R, SC	psat interrupt is from reflective light saturation writing a 1 to psat or psat_reflective will clear this status flag; to enable clear-by-read function, the register CFG3.int_read_clear must be set 1	
0	psat_ambient	0	R, SC	psat interrupt is from ambient light or idac threshold saturation writing a 1 to psat or psat_ambient will clear this status flag; to enable clear-by-read function, the register CFG3.int_read_clear must be set 1	

STATUS flags are reset with reading from STATUS address, or with writing 1 to dedicated bits of STATUS address.

PDATA Register (0x9C)

Figure 24:
PDATA Register

				0x9C: PDATA
Field	**Name**	**Reset**	**Type**	**Description**
7:0	pdata	0	RO	This register contains the 8-bit proximity data.

REVID2 Register (0x9E)

Figure 25:
REVID2 Register

				0x9E: REVID2
Field	**Name**	**Reset**	**Type**	**Description**
7:4	Reserved	0	RO	Reserved
3:0	aux_id	0	RO	TBD

CFG3 Register (0xAB)

Figure 26:
CFG3 Register

<table>
<tr><td colspan="5">0xAB: CFG3</td></tr>
<tr><td>Field</td><td>Name</td><td>Reset</td><td>Type</td><td>Description</td></tr>
<tr><td>7</td><td>int_read_clear</td><td>0</td><td>RW</td><td>If set to 1, interrupt flags in STATUS register (0x93) are reset after I²C reads to the STATUS register; otherwise the interrupt flags will not be reset.</td></tr>
<tr><td>6:5</td><td>Reserved</td><td>0</td><td>R, SC</td><td>Reserved. Set to 0.</td></tr>
<tr><td>4</td><td>sai</td><td>0</td><td>RW</td><td>Sleep After Interrupt: Power down the device at the end of the proximity cycle if an interrupt has been generated.[1]

PON	**SAI**	**INT (low active)**	**Oscillator**
0	x	x	OFF
1	0	x	ON
1	1	1	ON
1	1	0	OFF (SAI induced sleep)

The way to "wake up" the device from SAI-sleep is by clearing the interrupt register 0x93.</td></tr>
<tr><td>3:0</td><td>Reserved</td><td>1100</td><td>RW</td><td>Reserved. Set to 0.</td></tr>
</table>

Note(s):

1. SAI does not modify any register bits directly, it rather uses the interrupt signal to turn OFF the oscillator.

POFFSET_L Register (0xC0)

Figure 27:
POFFSET_L Register

0xC0: POFFSET_L				
Field	**Name**	**Reset**	**Type**	**Description**
7:0	poffset_l	0x00-0xFF	R, SC	Offset compensation for proximity channel (magnitude)

POFFSET_H Register (0xC1)

Figure 28:
POFFSET_H Register

0xC1: POFFSET_H				
Field	**Name**	**Reset**	**Type**	**Description**
0	poffset_h	0x00-0xFF	R, SC	Offset compensation for proximity channel (sign)

CALIB Register (0xD7)

Figure 29:
CALIB Register

0xD7: CALIB				
Field	**Name**	**Reset**	**Type**	**Description**
7:6	Reserved	0	RO	Reserved. Set to 0.
5	electrical_calibration	0	RW_SM	If set, do electrical offset calibration (diodes disabled) instead of optical. Otherwise, do optical calibration. In either case, the result is stored in the POFFSET_L/H registers. This flag is cleared after calibration is completed. This flag is redundant, software could just: set gdiode_disab=0xf set concap_intinn=1 start calibration. However, since electrical calibration is done automatically at the first time PON gets asserted, the function is there anyway, so it's made available to the user here.
4:1	Reserved	0	WS_SC	Reserved. Set to 0.
0	start_offset_calib	0	RW_SM	Start Offset Calibration. The result is stored in the POFFSET registers. The calib_finished flag is asserted afterwards. Calibration can be stopped by writing a 0 to this bit.

CALIBCFG Register (0xD9)

Figure 30:
CALIBCFG Register

0xD9: CALIBCFG				
Field	**Name**	**Reset**	**Type**	**Description**
7:5	binsrch_target	0x2	RW	ADC target during binary search | **Value**	**Target** | |---|---| | 0 | 0 | | 1 | 1 | | 2 | 3 | | 3 | 7 | | 4 | 15 | | 5 | 31 | | 6 | 63 | | 7 | 127 | **Note:** This target is relative to 8-bit ADC values. In the circuit, a 10-bit target is used (x4) of which the lowest 2 bits are always ignored when checking for zero during binary search and zero detection. In hardware, this defines a mask of which bits to ignore when comparing to zero. e.g. binsrch_target=4 (target=15) means that values from the ADC are AND'ed with 0xffc0 before comparing to zero. Only values 16 or larger are taken as positive ADC values.
4	Reserved	0	RW	Reserved. Set to 0.
3	prox_auto_offset_adjust	0	SC	This bit enables an automatic adjustment of the offset used in proximity measurements. If this bit is set, when a measurement returns zero, the value of 0xC0 will be decremented and offset_adjusted flag will be set, bit 2 in 0xDC.

0xD9: CALIBCFG				
Field	**Name**	**Reset**	**Type**	**Description**
2:0	prx_data_avg	0	R_PUSH	Prox data calculation is done by averaging consecutive windows of constant size. At the end of the window, PDATA is updated. Typical use case is HRM measurement **Value** / **Window Size**: 0 — disable 1 — 2 2 — 4 3 — 8 4 — 16 5 — 32 6 — 64 7 — 128

CALIBSTAT Register (0xDC)

Figure 31:
CALIBSTAT Register

0xDC: CALIBSTAT				
Field	**Name**	**Reset**	**Type**	**Description**
7:3	Reserved	0		Reserved
2	offset_adjusted	0	SC	This bit is a flag that the automatic proximity offset adjustment has changed the offset in register 0xDC. See 0xD9 for "prox_auto_offset_adjust".
1	Reserved	0		Reserved
0	calib_finished	0	R/W	Offset calibration has finished. Clear bit by writing '1' to it. Bit generates interrupt if cien is asserted.

INTENAB Register (0xDD)

Figure 32:
INTENAB Register

				0xDD: INTENAB
Field	**Name**	**Reset**	**Type**	**Description**
6	psien	0	RW	Writing '1' to this bit enables psat.
5	pien	0	RW	Writing '1' to this bit enables prox interrupt.
3	cien	0	RW	Writing '1' to this bit enables calibration interrupt.
2	zien	0	RW	Writing '1' to this bit enables zero_detection/offset_adjustment.

Application Information

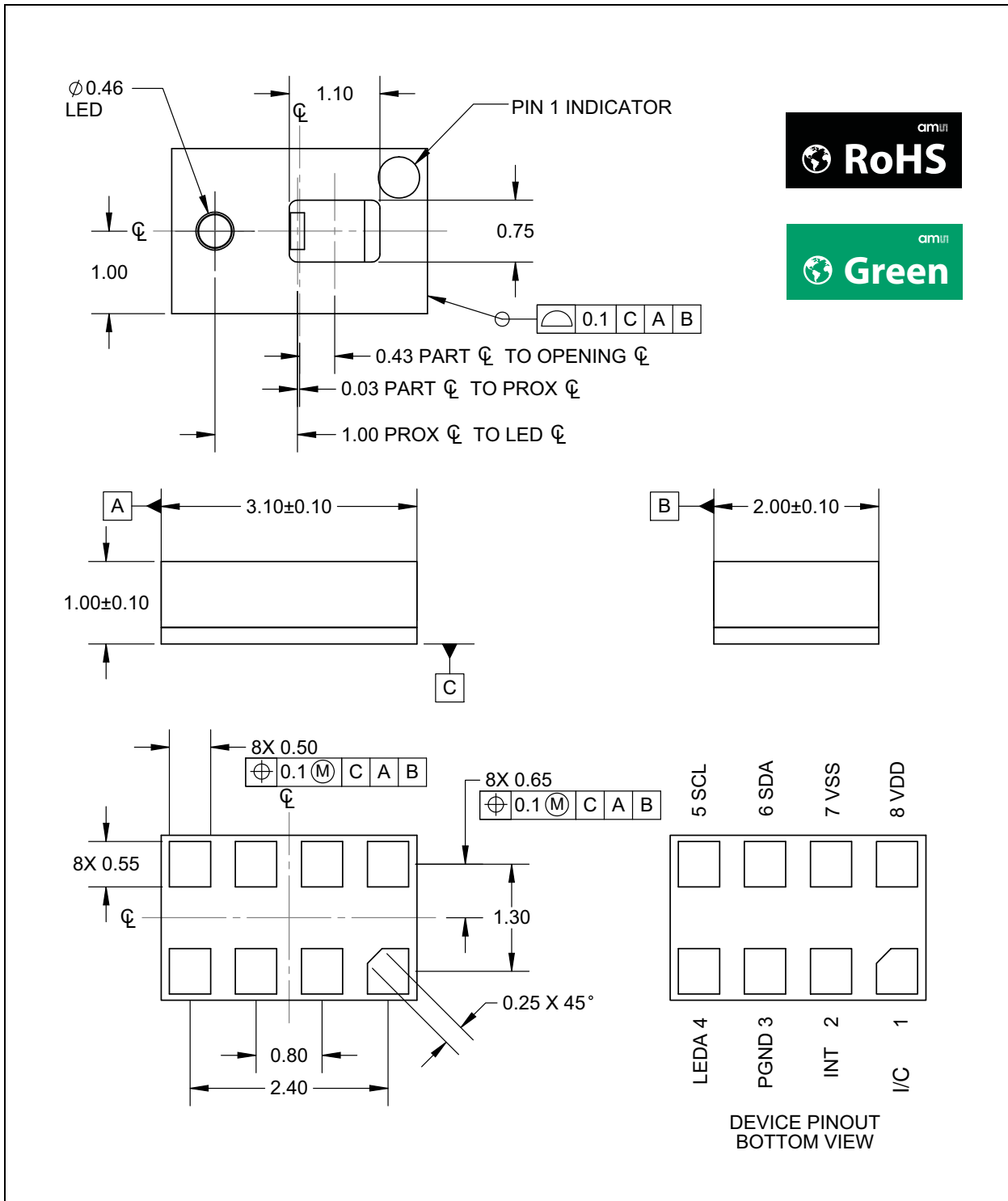**Figure 33:**
Typical Application Hardware Circuit
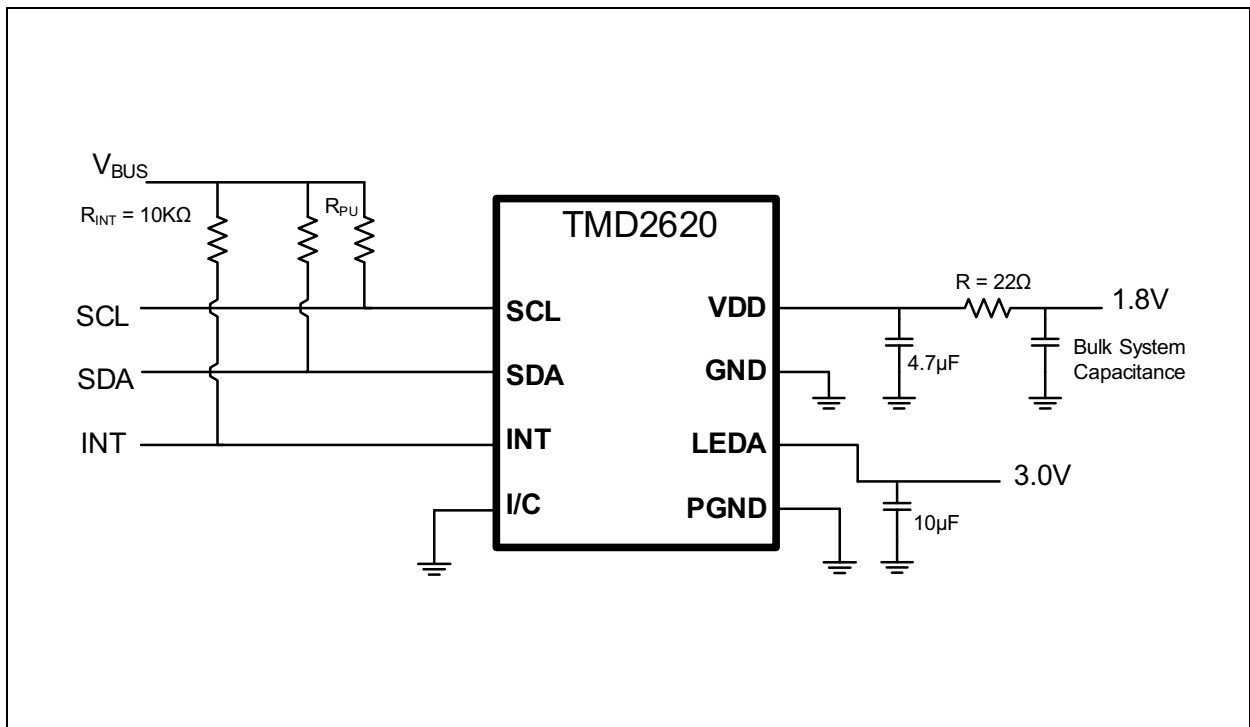
Note(s):

1. Place the 4.7µF and 10µF capacitors within 5mm of the module.

2. The value of the I²C pull up resistors RPU should be based on the 1.8V bus voltage, system bus speed and trace capacitance.

3. The bulk capacitor can affect the stability of a regulated supply output and should be chosen with the regulator characteristics in mind.

4. GND and PGND should be connected to the same solid ground plane as close to the device as possible.

PCB Pad Layout

Figure 34:
Recommended PCB Pad Layout

Note(s):

1. All linear dimensions are in millimeters.

2. Dimension tolerances are 0.05mm unless otherwise noted.

3. This drawing is subject to change without notice.

Packaging Mechanical Data
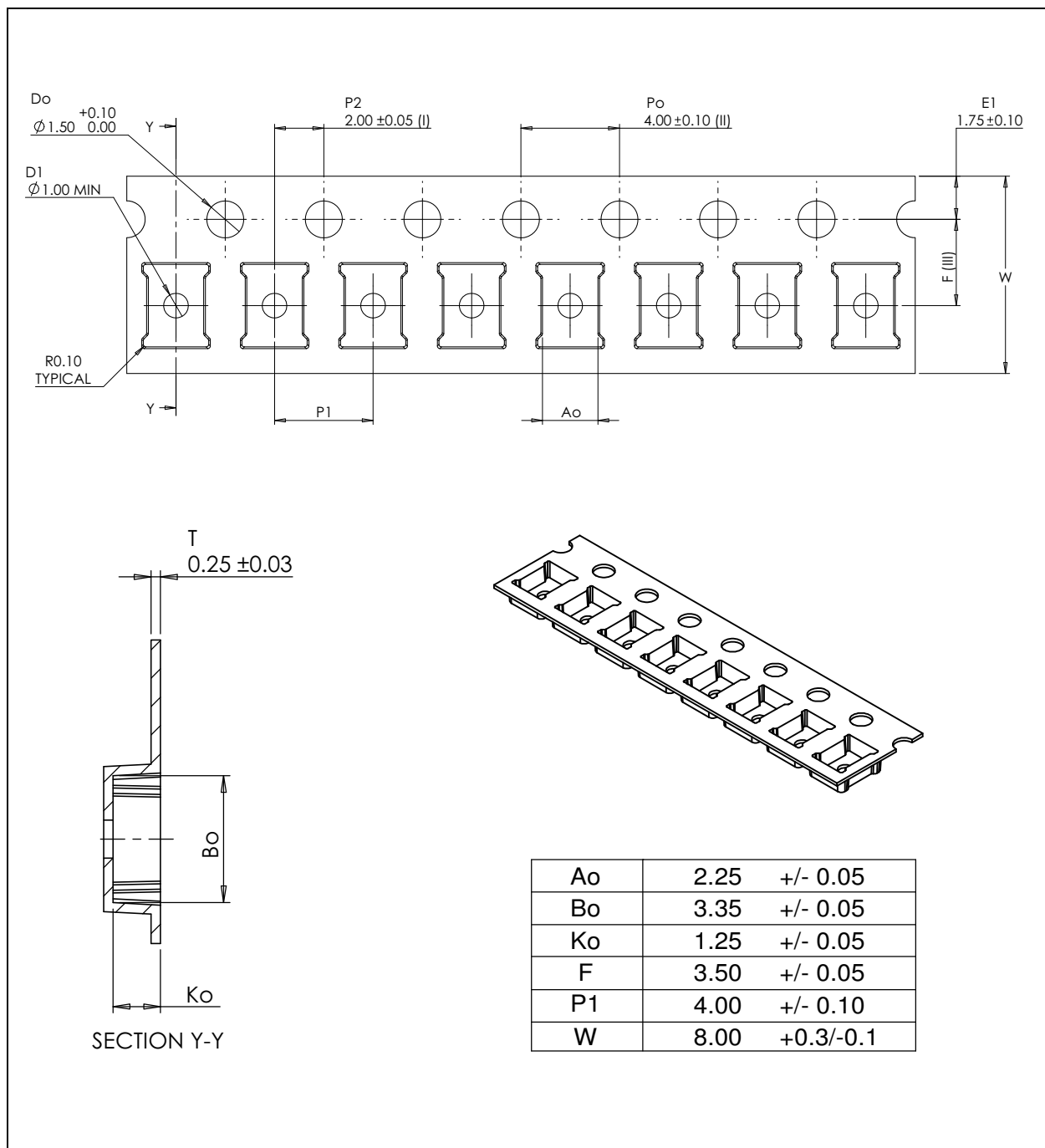
Figure 35:
Package Drawing

Note(s):

1. All linear dimensions are in millimeters.

2. Dimension tolerances are 0.05mm unless otherwise noted.

3. Contact finish is Au.

4. This package contains no lead (Pb).

5. This drawing is subject to change without notice.

Tape & Reel Information

Figure 36:
Tape & Reel Information

Ao	2.25	+/- 0.05
Bo	3.35	+/- 0.05
Ko	1.25	+/- 0.05
F	3.50	+/- 0.05
P1	4.00	+/- 0.10
W	8.00	+0.3/-0.1

Note(s):

1. Measured from centreline of sprocket hole to centreline of pocket.

2. Cumulative tolerance of 10 sprocket holes is ± 0.20.

3. Measured from centreline of sprocket hole to centreline of pocket.

4. Other material available.