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TMD2671

Digital Proximity Detector

General Description

The TMD2671 family of devices provides a complete proximity detection system and digital interface logic in a single 8-pin package. The proximity detector includes a digital proximity sensor with integrated LED driver, and IR LED. The proximity function is calibrated to 100mm (without cover glass), thus eliminating the need for end-equipment or sub-assembly factory calibration. The proximity detection feature operates from sunlight to dark rooms. The wide dynamic range also allows for operation in short distance detection behind dark glass such as with a cell phone. An internal state machine provides the ability to put the device into a low-power mode providing very low average power consumption. The addition of the micro-optics lenses within the module provide highly efficient transmission and reception of infrared energy, which lowers overall power dissipation for the detection function.

The proximity function specifically targets near-field proximity applications. In cell phones, the proximity detection can detect when the user positions the phone close to their ear. The device is fast enough to provide proximity information at a high repetition rate needed when answering a phone call. This provides both improved *green* power saving capability and the added security to lock the screen when the user may accidentally deploy a touch.

Communication with the device is accomplished with a simple 2-wire I^2C interface with data rates up to 400kHz. An interrupt output pin is provided for connection to the host processor. This interrupt pin can be used to eliminate the need to poll the device on a repetitive basis. There is also a digital filter that compares the proximity ADC results to programmed values so that an interrupt is only generated upon a proximity event.

The TMD2671 is packaged in a very small form factor 8-pin optical package. The PCB board area required is only 9.36mm^2, which is far smaller than discrete solutions. Also, the package height is only 1.35mm, which makes the TMD2671 device suitable for very thin mechanical applications.

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits & Features

The benefits and features of the TMD2671, Digital Proximity Detector are listed below:

Figure 1:
Added Value of Using TMD2671

Benefits	Features
• Module reduces board space and design effort	• Integrated proximity detection sensor and IR LED
• Enables operation in IR light environments	• Patented dual-diode architecture
• Pre-calibration eliminates need for customer to end-product calibrate	• Proximity detection calibrated and trimmed to 100mm detection
• Allows multiple power-level selection without external passives	• Programmable LED drive current

- Digital Proximity Detector, LED Driver, and IR LED in a Single Optical Module
- Proximity Detection
  - Calibrated to 100mm Detection
  - Integrated IR LED and Synchronous LED Driver
  - Programmable Number of IR Pulses
  - Programmable Current Sink for the IR LED - No Limiting Resistor Needed
  - Programmable Interrupt Function with Upper and Lower Threshold
- Programmable Wait Timer
  - Wait State - 65µA Typical Current
  - Programmable from 2.72ms to > 8s
- I^2C Interface Compatible
  - Up to 400kHz (I^2C Fast Mode)
- Sleep Mode - 2.5µA Typical
- Dedicated Interrupt Pin
- 3.94mm × 2.36mm × 1.35mm Package

Applications

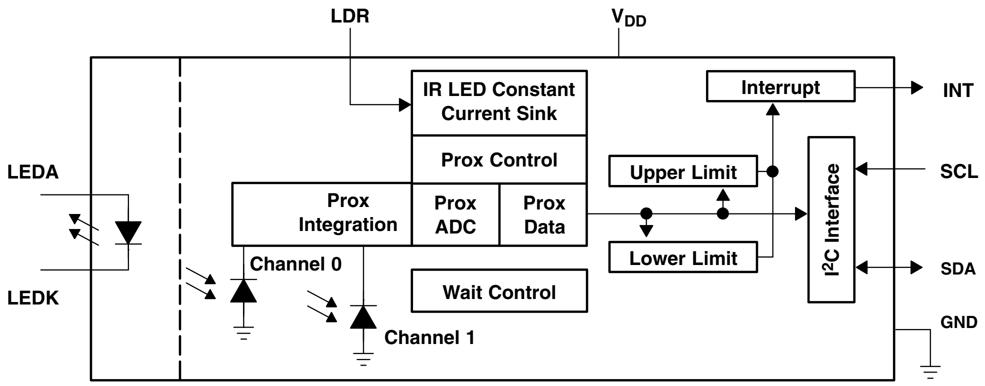
The applications of this device include:

- Cell Phone Touch Screen Disable
- Automatic Speakerphone Enable
- Automatic Menu Popup

Block Diagram

The functional blocks of this device are shown below:

Figure 2:
TMD2671 Block Diagram



Detailed Description

A fully integrated proximity detection solution is provided with an 850nm IR LED, LED driver circuit, and proximity detection engine. An internal LED driver (LDR) pin, is connected to the LED cathode (LEDK) to provide a factory calibrated proximity of 100mm, ±20mm. This is accomplished with a proprietary current calibration technique that accounts for all variances in silicon, optics, package, and most important, IR LED output power. This eliminates or greatly reduces the need for factory calibration that is required for most discrete proximity sensor solutions. While the *device* is factory calibrated at a given pulse count, the number of proximity LED pulses can be programmed from 1 to 255 pulses, which allows different proximity distances to be achieved. Each pulse has a 16µs period, with a 7.2µs on time.

The device provides a separate pin for level-style interrupts. When interrupts are enabled and a pre-set value is exceeded, the interrupt pin is asserted and remains asserted until cleared by the controlling firmware. The interrupt feature simplifies and improves system efficiency by eliminating the need to poll a sensor for a proximity value. An interrupt is generated when the value of a proximity conversion exceeds either an upper or lower threshold. In addition, a programmable interrupt persistence feature allows the user to determine how many consecutive exceeded thresholds are necessary to trigger an interrupt.

Pin Assignment

The TMD2671 pin assignment is described below:

Figure 3:
Pin Diagram of Package Module-8 (Top View)

Note: Package drawing is not to scale

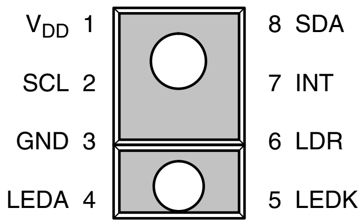


Figure 4:
Terminal Functions

Terminal		Type	Description
Name	No.		
V_{DD}	1		Supply voltage
SCL	2	I	I^2C serial clock input terminal - clock signal for I^2C serial data
GND	3		Power supply ground. All voltages are referenced to GND.
LEDA	4	I	LED anode
LEDK	5	O	LED cathode. Connect to LDR pin when using internal LED driver circuit.
LDR	6	I	LED driver input for proximity IR LED, constant current source LED driver
INT	7	O	Interrupt - open drain
SDA	8	I/O	I^2C serial data I/O terminal - serial data I/O for I^2C

Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 5:
Absolute Maximum Ratings over Operating Free-Air Temperature Range (unless otherwise noted)

Symbol	Parameter	Min	Max	Unit
V_{DD}	Supply voltage [(1)]		3.8	V
V_O	Digital output voltage range	-0.5	3.8	V
I_O	Digital output current	-1	20	mA
LDR	Analog voltage range	-0.5	3.8	V
T_{strg}	Storage temperature range	-40	85	°C
ESD_{HBM}	ESD tolerance, human body model	±2000		V

Note(s):

1. All voltages are with respect to GND.

Electrical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Figure 6:
Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Unit
V_{DD}	Supply voltage	2.5	3	3.6	V
	Supply voltage accuracy, V_{DD} total error including transients	-3		3	%
T_A	Operating free-air temperature range [1]	-30		85	°C

Note(s):

1. While the device is operational across the temperature range, functionality will vary with temperature. Specifications are stated only at 25°C unless otherwise noted.

Figure 7:
Operating Characteristics, V_{DD} = 3V, T_A = 25°C (unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{DD}	Supply current	Active: proximity and wait delay states		175	250	µA
		Wait state		65		
		Sleep state		2.5	4	
V_{OL}	INT, SDA output low voltage	3mA sink current	0		0.4	V
		6mA sink current	0		0.6	
I_{LEAK}	Leakage current, SDA, SCL, INT pins		-5		5	µA
I_{LEAK}	Leakage current, LDR pin				10	µA
V_{IH}	SCL, SDA input high voltage	TMD26711	0.7 V_{DD}			V
		TMD26713	1.25			
V_{IL}	SCL, SDA input low voltage	TMD26711			0.3 V_{DD}	V
		TMD26713			0.54	

Figure 8:
Proximity Characteristics, V_{DD} = V_{LEDA} = 3V, T_A = 25°C, PEN = 1 (unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{DD}	Supply current - LDR pulse on			3		mA
	ADC conversion time step size	PTIME = 0xFF		2.72		ms
	ADC number of integration steps		1		256	steps
	ADC counts per step	PTIME = 0xFF	0		1023	counts
	Proximity IR LED pulse count		0		255	pulses
	Proximity pulse period			16.3		µs
I_{LEDA}	LED current @ V 600mV LDR pin sink (1)	PDRIVE = 0 (100% current)		100		mA
		PDRIVE = 1 (50% current)		50		
		PDRIVE = 2 (25% current)		25		
		PDRIVE = 3 (12.5% current)		12.5		
T_{LDR}	On time per pulse	PDRIVE = 1		7.2		µs
	Proximity response, no target (offset)	PDRIVE = 0, PPULSE = 8 (2)		100		counts
	Prox count, 100mm target (3)	73mm × 83mm, 90% reflective Kodak Gray Card, PPULSE = 8, PDRIVE = 0, PTIME = 0xFF	414	520	624	counts

Note(s):

1. Value is factory-adjusted to meet the Prox count specification. Considerable variation (relative to the typical value) is possible after adjustment.
2. No reflective surface above the module. Proximity offset varies with power supply characteristics and noise.
3. I_{LEDA} is factory calibrated to achieve this specification. Offset and crosstalk directly sum with this value and is system dependent.
4. No glass or aperture above the module. Tested value is the average of 5 consecutive readings.
5. These parameters are ensured by design and characterization and are not 100% tested.
6. Proximity test was done using the following circuit. See Application Information: Hardware section for recommended application circuit.

Figure 9:
Proximity Test Circuit

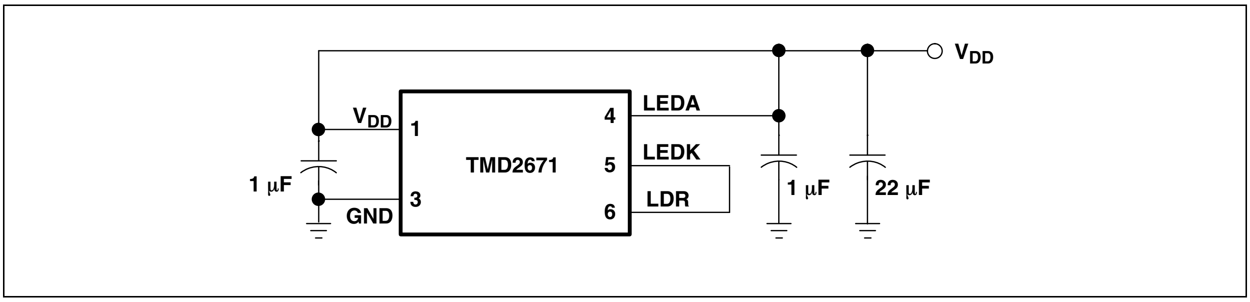


Figure 10:
IR LED Characteristics, V_{DD} = 3V, T_A = 25°C

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_F	Forward voltage	I_F = 20mA		1.4	1.5	V
V_R	Reverse voltage	I_R = 10µA	5			V
P_O	Radiant power	I_F = 20mA	4.5			mW
λ_p	Peak wavelength	I_F = 20mA		850		nm
Δ_λ	Spectral radiation bandwidth	I_F = 20mA		40		nm
T_R	Optical rise time	I_F = 100mA, T_W = 125ns, duty cycle = 25%		20	40	ns
T_F	Optical fall time	I_F = 100mA, T_W = 125ns, duty cycle = 25%		20	40	ns

Figure 11:
Wait Characteristics, V_{DD} = 3V, T_A = 25°C, WEN = 1 (unless otherwise noted)

Parameter	Test Conditions	Min	Typ	Max	Unit
Wait step size	WTIME = 0xFF		2.72	2.9	ms
Wait number of integration steps		1		256	steps

Figure 12:
AC Electrical Characteristics, V_{DD} = 3V, T_A = 25°C (unless otherwise noted)

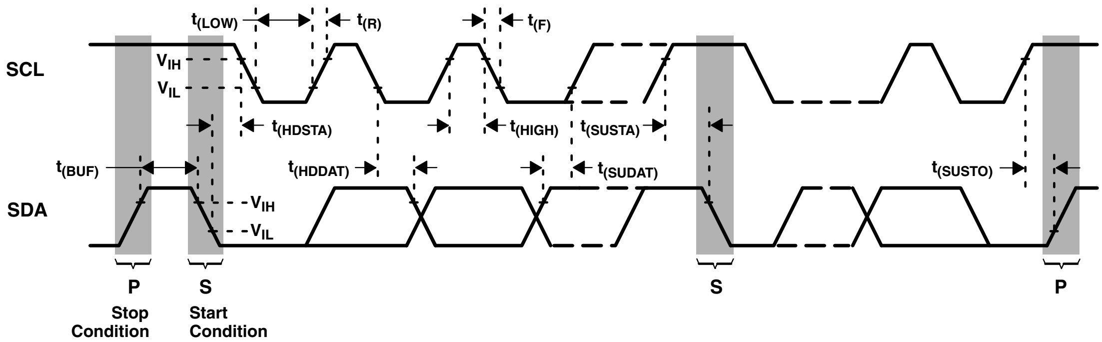
Symbol	Parameter (1)	Test Conditions	Min	Typ	Max	Unit
$f_{(SCL)}$	Clock frequency (I^2C only)		0		400	kHz
$t_{(BUF)}$	Bus free time between start and stop condition		1.3			µs
$t_{(HDSTA)}$	Hold time after (repeated) start condition. After this period, the first clock is generated.		0.6			µs
$t_{(SUSTA)}$	Repeated start condition setup time		0.6			µs
$t_{(SUSTO)}$	Stop condition setup time		0.6			µs
$t_{(HDDAT)}$	Data hold time		0			µs
$t_{(SUDAT)}$	Data setup time		100			ns
$t_{(LOW)}$	SCL clock low period		1.3			µs
$t_{(HIGH)}$	SCL clock high period		0.6			µs
t_F	Clock/data fall time				300	ns
t_R	Clock/data rise time				300	ns
C_i	Input pin capacitance				10	pF

Note(s):

1. Specified by design and characterization; not production tested.

Parameter Measurement Information

Figure 13:
Timing Diagrams



Typical Operating Characteristics

Figure 14:
Spectral Responsivity

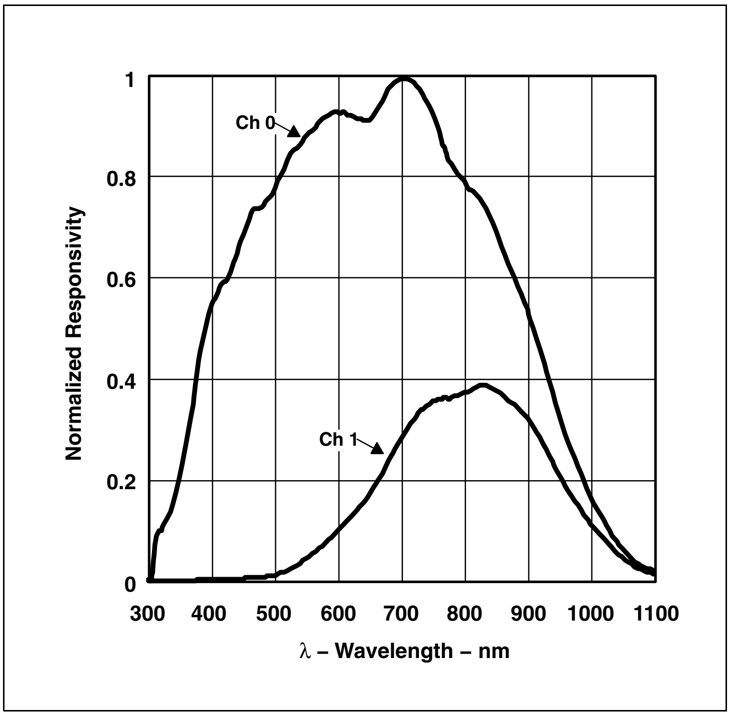


Figure 15:
LDR Output Compliance

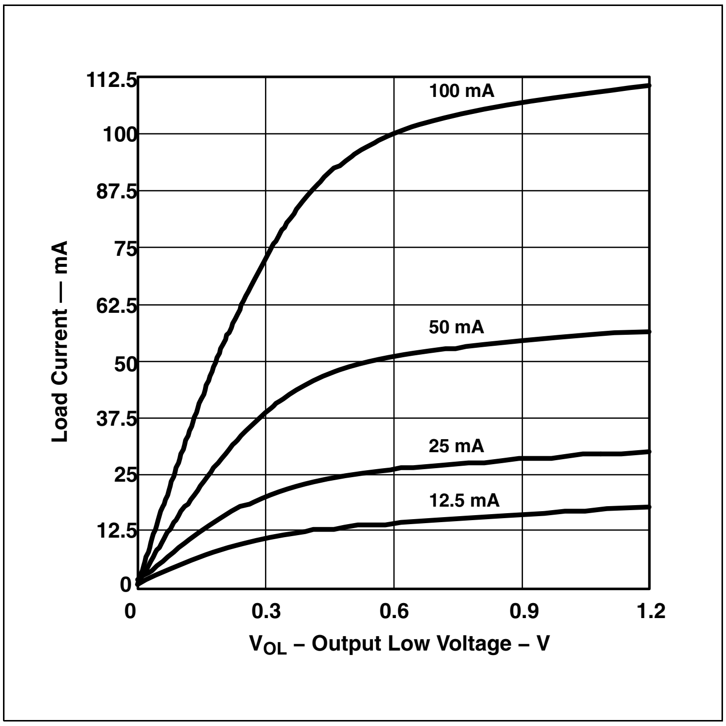
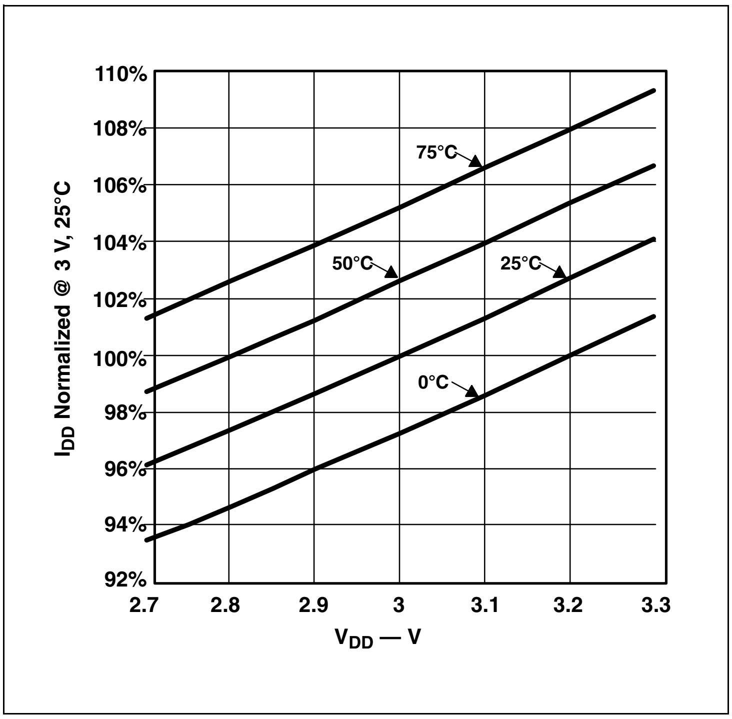


Figure 16:
Normalized I_{DD} vs. V_{DD} and Temperature

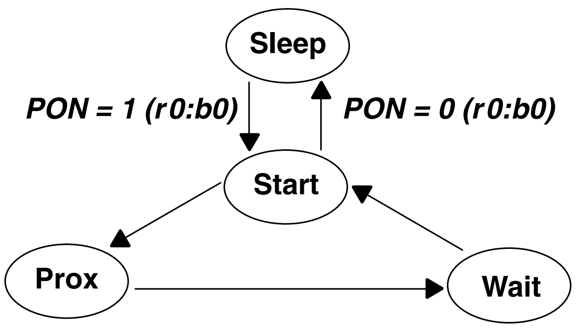


Principles of Operation

System State Machine

The device provides control of proximity detection and power management functionality through an internal state machine. After a power-on-reset, the device is in the sleep mode. As soon as the PON bit is set, the device will move to the start state. It will then cycle through the Proximity and Wait states. If these states are enabled, the device will execute each function. If the PON bit is set to a 0, the state machine will continue until the current conversion is complete and then go into a low-power sleep mode.

Figure 17:
Simplified State Diagram

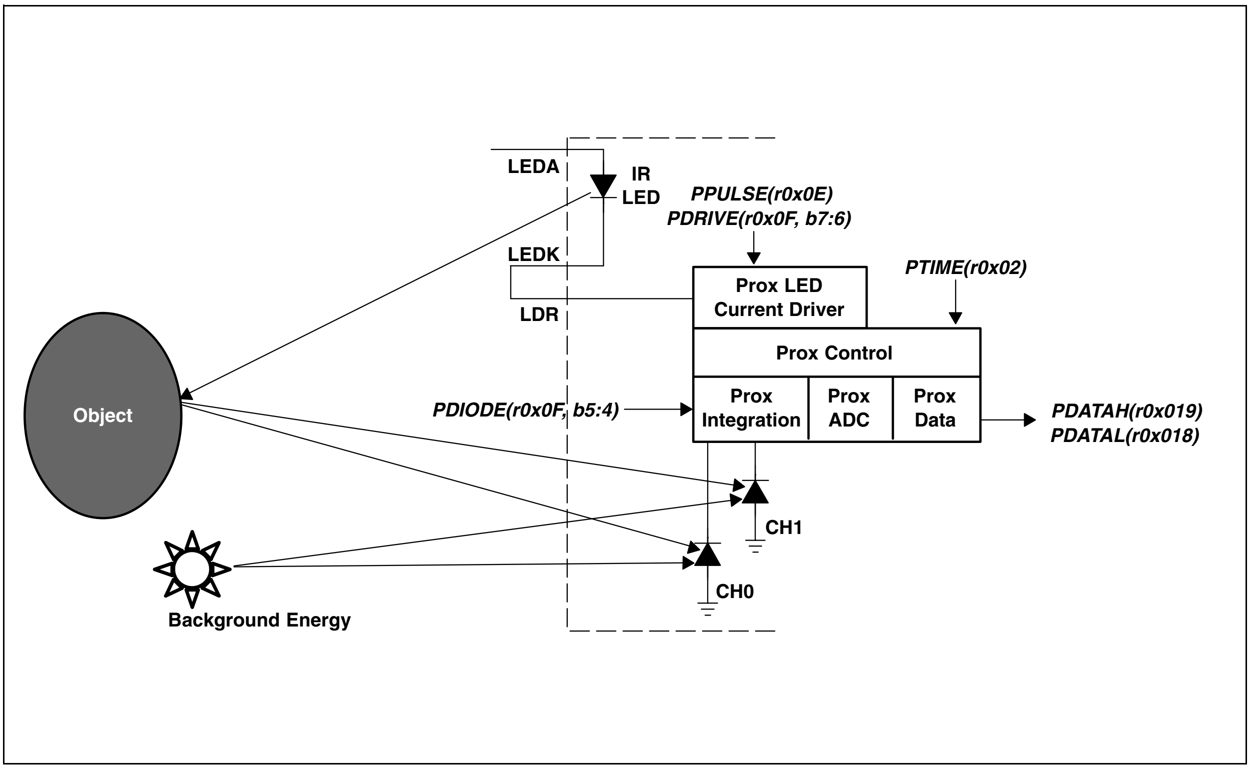


Note: In this document, the nomenclature uses the bit field name in italics followed by the register number and bit number to allow the user to easily identify the register and bit that controls the function. For example, the power on (PON) is in register 0, bit 0. This is represented as *PON (r0:b0)*.

Proximity Detection

Proximity detection is accomplished by measuring the amount of IR energy, from the internal IR LED, reflected off an object to determine its distance. The internal proximity IR LED is driven by the integrated proximity LED current driver as shown in Figure 18.

Figure 18:
Proximity Detection



The LED current driver provides a regulated current sink on the LDR terminal that eliminates the need for an external current limiting resistor. The PDRIVE register setting sets the sink current to 100%, 50%, 25%, or 12.5% of the factory trimmed full scale current.

Referring to the Detailed State Machine figure, the LED current driver pulses the IR LED as shown in Figure 19 during the Prox Accum state. Figure 19 also illustrates that the LED On pulse has a fixed width of 7.3µs and period of 16.0µs. So, in addition to setting the proximity drive current, 1 to 255 proximity pulses (PPULSE) can be programmed. When deciding on the number of proximity pulses, keep in mind that the signal increases proportionally to PPULSE, while noise increases by the square root of PPULSE.

Figure 19:
Proximity LED Current Driver Waveform

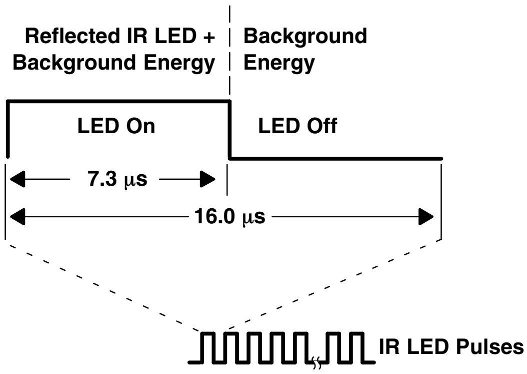


Figure 18 illustrates light rays emitting from the internal IR LED, reflecting off an object, and being absorbed by the CH0 and CH1 photodiodes. The proximity diode selector (PDIODE) determines which of the two photodiodes is used for a given proximity measurement. Note that neither photodiode is selected when the device first powers up, so PDIODE must be set for proximity detection to work.

Referring again to Figure 19, the reflected IR LED and the background energy is integrated during the LED On time, then during the LED Off time, the integrated background energy is subtracted from the LED On time energy, leaving the IR LED energy to accumulate from pulse to pulse.

After the programmed number of proximity pulses have been generated, the proximity ADC converts and scales the proximity measurement to a 16-bit value, then stores the result in two 8-bit proximity data (PDATAx) registers. ADC scaling is controlled by the proximity ADC conversion time (PTIME) which is programmable from 1 to 256 2.73ms time units. However, depending on the application, scaling the proximity data will equally scale any accumulated noise. Therefore, in general, it is recommended to leave PTIME at the default value of one 2.73ms ADC conversion time (0xFF).

For additional information on using the proximity detection function behind glass and for optical system design guidance, please see available **ams** application notes.

Optical Design Considerations

The TMD2671 device simplifies the optical system design by integrating an IR LED into the package, and also by providing an effective barrier between the LED and proximity sensor. In addition the package contains integrated lenses and apertures over both the LED and the sensor, which significantly extends the maximum proximity detection distance and helps to reduce optical crosstalk.

Although the package integrates an optical barrier between the IR LED and detector, placing the device behind a cover glass potentially provides another significant path for IR light to reach the detector, via reflection from the inside and outside faces of the cover glass. Because it is cost prohibitive to use anti-reflection coatings on the glass, the faces of the glass will reflect significantly (typically on the order of 4% of the light), and it is crucial that the system be designed so that this reflected light cannot find an efficient path back to the optical detector. See **ams** Application Note DN28: *Proximity Detection Behind Glass* for a detailed discussion of optical design considerations.

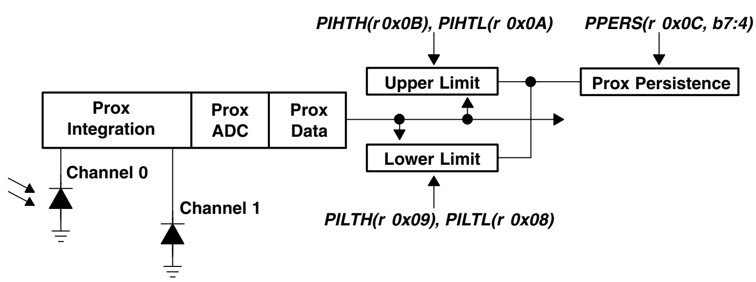
Interrupts

The interrupt feature simplifies and improves system efficiency by eliminating the need to poll the sensor for a proximity value. The interrupt mode is determined by the state of the PIEN field in the ENABLE register.

Two 16-bit-wide interrupt threshold registers allow the user to define upper and lower threshold limits. An interrupt can be generated when the proximity data (PDATA) exceeds the upper threshold value (PIHTx) or falls below the lower threshold (PILTx).

To further control when an interrupt occurs, the device provides an interrupt persistence feature. This feature allows the user to specify a number of conversion cycles for which an event exceeding the proximity interrupt threshold must persist (PPERS) before actually generating an interrupt. See the register descriptions for details on the length of the persistence.

Figure 20:
Programmable Interrupt

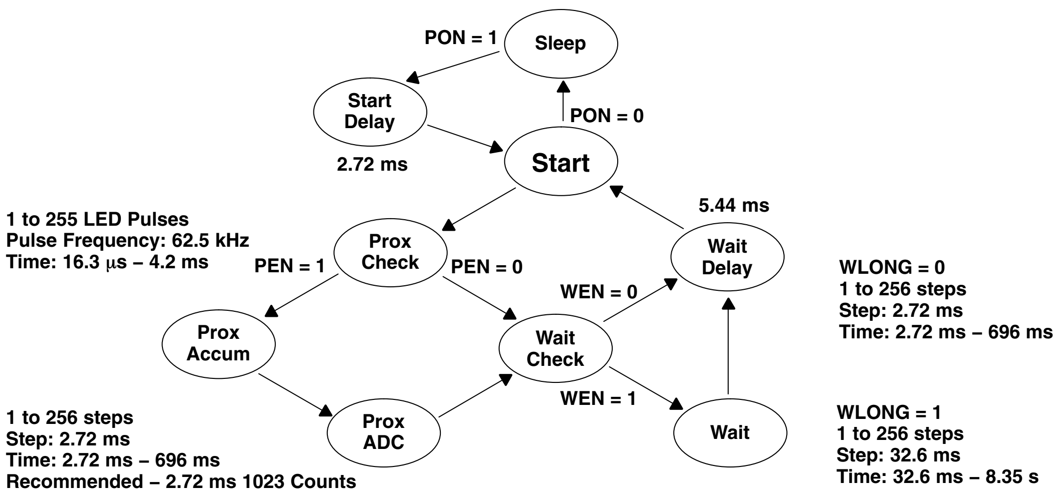


State Diagram

The following state diagram shows a more detailed flow for the state machine. The device starts in the sleep mode. The PON bit is written to enable the device. A 2.72ms Start Delay will occur before entering the start state. If the PEN bit is set, the state machine will step through the proximity accumulate, then proximity ADC conversion states. As soon as the conversion is complete, the state machine will move to the Wait Check state.

If the WEN bit is set, the state machine will then cycle through the wait state. If the WLONG bit is set, the wait cycles are extended by 12× over normal operation. When the wait counter terminates, the state machine will move to the 2.72ms Wait Delay state before returning to the Start state.

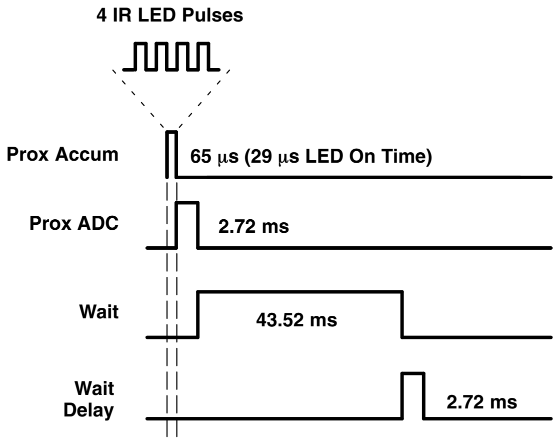
Figure 21:
Expanded State Diagram



Power Management

Power consumption can be controlled through the use of the wait state timing because the wait state consumes only 65µA of power. Figure 22 shows an example of using the power management feature to achieve an average power consumption of 136µA current with four 100mA pulses of proximity detection.

Figure 22:
Power Consumption Calculations



Example: ~49 ms Cycle TIme

State	Duration (ms)	Current (mA)
Prox Accum	0.065 (Note 1)	
LED On	0.029 (Note 2)	100.0
Prox ADC	2.72	0.175
Wait	43.52	0.065
Wait Delay	2.72	0.175

Average Current = $((0.029 \times 100) + (2.72 \times 0.175) + (43.52 \times 0.065) + (2.72 \times 0.175)) / 49 = 136\ \mu A$

Note(s):

1. Prox Accum = 16.3µs per pulse x 4 pulses = 65µs = 0.065ms
2. LED On = 7.2µs per pulse x 4 pulses = 29µs = 0.029ms

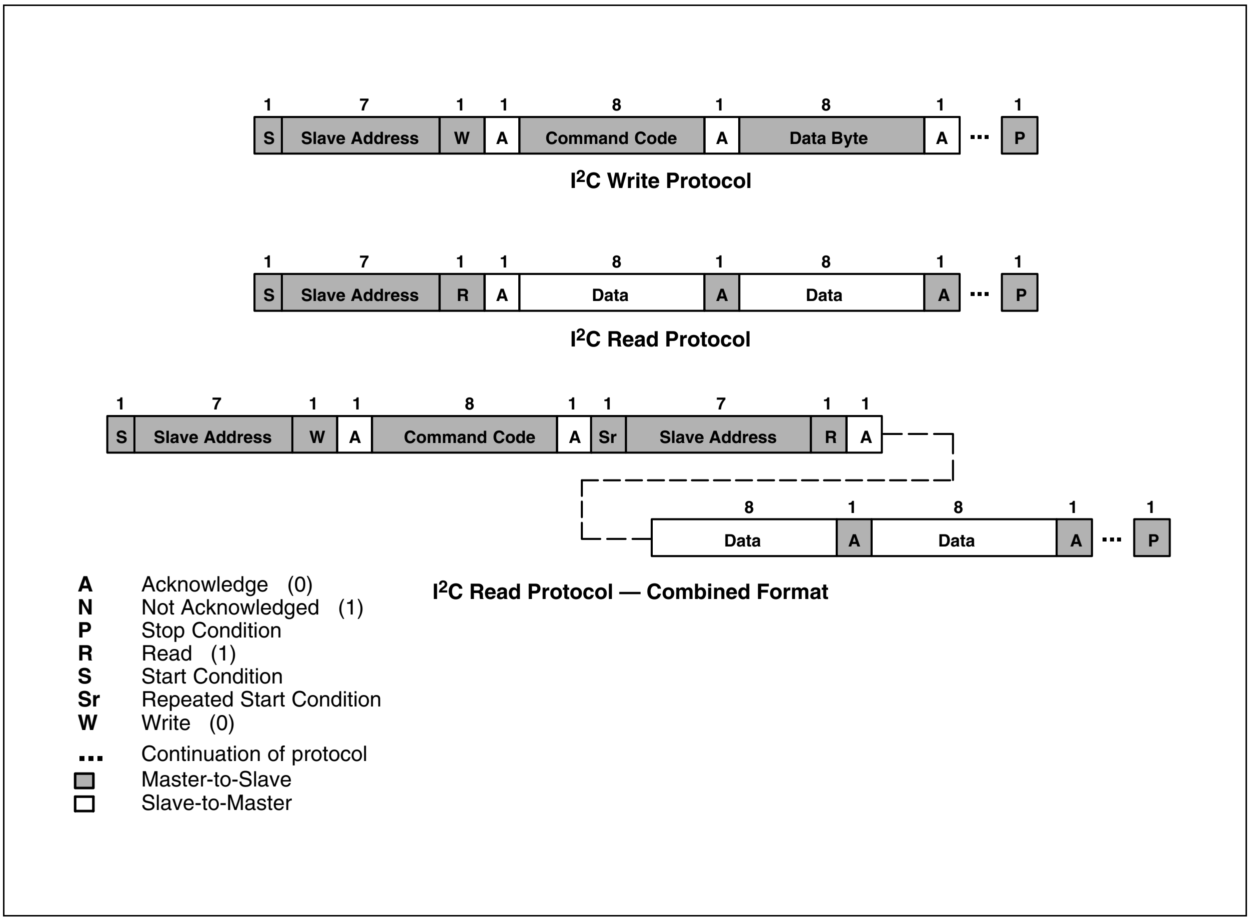
I^2C Protocol

Interface and control are accomplished through an I^2C serial compatible interface (standard or fast mode) to a set of registers that provide access to device control functions and output data. The devices support the 7-bit I^2C addressing protocol.

The I^2C standard provides for three types of bus transaction: read, write, and a combined protocol (Figure 23). During a write operation, the first byte written is a command byte followed by data. In a combined protocol, the first byte written is the command byte followed by reading a series of bytes. If a read command is issued, the register address from the previous command will be used for data access. Likewise, if the MSB of the command is not set, the device will write a series of bytes at the address stored in the last valid command with a register address. The command byte contains either control information or a 5-bit register address. The control commands can also be used to clear interrupts.

The I^2C bus protocol was developed by Philips (now NXP). For a complete description of the I^2C protocol, please review the NXP I^2C design specification at http://www.i2c-bus.org/references.

Figure 23:
I^2C Protocols



Register Set

The device is controlled and monitored by data registers and a command register accessed through the serial interface. These registers provide for a variety of control functions and can be read to determine results of the ADC conversions. The Register Set is summarized in Figure 24.

Figure 24:
Register Address

Address	Register Name	R/W	Register Function	Reset Value
----	COMMAND	W	Specifies register address	0x00
0x00	ENABLE	R/W	Enables states and interrupts	0x00
0x01	ATIME	R/W	ALS ADC time	0x00 (1)
0x02	PTIME	R/W	Proximity ADC time	0xFF
0x03	WTIME	R/W	Wait time	0xFF
0x08	PILTL	R/W	Proximity interrupt low threshold low byte	0x00
0x09	PILTH	R/W	Proximity interrupt low threshold high byte	0x00
0x0A	PIHTL	R/W	Proximity interrupt high threshold low byte	0x00
0x0B	PIHTH	R/W	Proximity interrupt high threshold high byte	0x00
0x0C	PERS	R/W	Interrupt persistence filter	0x00
0x0D	CONFIG	R/W	Configuration	0x00
0x0E	PPULSE	R/W	Proximity pulse count	0x00
0x0F	CONTROL	R/W	Control register	0x00
0x12	ID	R	Device ID	ID
0x13	STATUS	R	Device status	0x00
0x18	PDATAL	R	Proximity ADC low data register	0x00
0x19	PDATAH	R	Proximity ADC high data register	0x00

Note(s):

1. Following power on, this register should be initialized to 0xFF.

The mechanics of accessing a specific register depends on the specific protocol used. See the section on I^2C protocols on the previous pages. In general, the Command Register is written first to specify the specific control/status register for following read/write operations.

Command Register

The Command Registers specifies the address of the target register for future write and read operations.

Figure 25:
Command Register

7	6	5	4	3	2	1	0
COMMAND	**TYPE**		**ADD**				

<table>
<tr><th>Field</th><th>Bits</th><th colspan="2">Description</th></tr>
<tr><td>COMMAND</td><td>7</td><td colspan="2">Select Command Register. Must write as 1 when addressing COMMAND register.</td></tr>
<tr><td rowspan="7">TYPE</td><td rowspan="7">6:5</td><td colspan="2">Selects type of transaction to follow in subsequent data transfers:</td></tr>
<tr><td>Field Value</td><td>Description</td></tr>
<tr><td>00</td><td>Repeated byte protocol transaction</td></tr>
<tr><td>01</td><td>Auto-increment protocol transaction</td></tr>
<tr><td>10</td><td>Reserved - Do not use</td></tr>
<tr><td>11</td><td>Special function - See description below</td></tr>
<tr><td colspan="2">Transaction type 00 will repeatedly read the same register with each data access. Transaction type 01 will provide an auto-increment function to read successive register bytes.</td></tr>
<tr><td rowspan="5">ADD</td><td rowspan="5">4:0</td><td colspan="2">Address register/special function register. Depending on the transaction type, see above, this field either specifies a special function command or selects the specific control-status-register for following write and read transactions:</td></tr>
<tr><td>Field Value</td><td>Description</td></tr>
<tr><td>00000</td><td>Normal - no action</td></tr>
<tr><td>00101</td><td>Proximity interrupt clear</td></tr>
<tr><td colspan="2">Proximity Interrupt Clear clears any pending proximity interrupt. This special function is self clearing.</td></tr>
</table>

Enable Register (0x00)

The Enable Register is used to power the device on/off, enable functions, and interrupts.

Figure 26:
Enable Register

7	6	5	4	3	2	1	0
Reserved		**PIEN**	**Reserved**	**WEN**	**PEN**		**PON**

Field	Bits	Description
Reserved	7:6	Reserved. Write as 0.
PIEN	5	Proximity Interrupt Mask. When asserted, permits proximity interrupts to be generated.
Reserved	4	Reserved. Write as 0.
WEN	3	Wait Enable. This bit activates the wait feature. Writing a 1 activates the wait timer. Writing a 0 disables the wait timer.
PEN	2:1	Proximity Enable. These bits activate the proximity function. Writing a 11b enables proximity. Writing a 00b disables proximity. The Wait Time Register should be configured before asserting proximity enable.
PON [(1), (2)]	0	Power ON. This bit activates the internal oscillator to permit the timers and ADC channel to operate. Writing a 1 activates the oscillator. Writing a 0 disables the oscillator.

Note(s):

1. See Power Management section for more information.
2. A minimum interval of 2.72ms must pass after PON is asserted before proximity can be initiated. This required time is enforced by the hardware in cases where the firmware does not provide it.

ALS Timing Register (0x01)

Although this part is proximity only, the ATIME period still occurs. Note that the power-on default value is 0x00 (the longest duration). This register should be initialized by the application code to 0xFF.

Figure 27:
ALS Timing Register

Field	Bits	Description		
ATIME	7:0	**Value**	**INTEG_CYCLES**	**Time**
		0xFF	1	2.72ms
		0x00	256	696ms

Proximity Time Control Register (0x02)

The Proximity Timing Register controls the integration time of the proximity ADC in 2.72ms increments. It is recommended that this register be programmed to a value of 0xFF (1 integration cycle).

Figure 28:
Proximity Time Control Register

Field	Bits	Description			
PTIME	7:0	**Value**	**INTEG_CYCLES**	**Time**	**Max Count**
		0xFF	1	2.72ms	1023

Wait Time Register (0x03)

Wait time is set 2.72ms increments unless the WLONG bit is asserted, in which case the wait times are 12× longer. WTIME is programmed as a 2's complement number.

Figure 29:
Wait Time Register

Field	Bits	Description			
WTIME	7:0	**REGISTER VALUE**	**WAIT TIME**	**TIME (WLONG = 0)**	**TIME (WLONG = 1)**
		0xFF	1	2.72ms	0.032 s
		0xB6	74	200ms	2.4 s
		0x00	256	700ms	8.3 s

Note(s):

1. The Wait Time Register should be configured before PEN is asserted.

Proximity Interrupt Threshold Register (0x08 – 0x0B)

The Proximity Interrupt Threshold Registers provide the values to be used as the high and low trigger points for the comparison function for interrupt generation. If the value generated by proximity channel crosses below the lower threshold specified, or above the higher threshold, an interrupt is signaled to the host processor.

Figure 30:
Proximity Interrupt Threshold Register

Register	Address	Bits	Description
PILTL	0x08	7:0	Proximity low threshold lower byte
PILTH	0x09	7:0	Proximity low threshold upper byte
PIHTL	0x0A	7:0	Proximity high threshold lower byte
PIHTL	0x0B	7:0	Proximity high threshold upper byte

Persistence Register (0x0C)

The Persistence Register controls the filtering interrupt capabilities of the device. Configurable filtering is provided to allow interrupts to be generated after each ADC integration cycle or if the ADC integration has produced a result that is outside of the values specified by threshold register for some specified amount of time.

Figure 31:
Persistence Register

7	6	5	4	3	2	1	0
PPERS				**Reserved**			

Field	Bits	Description		
PPERS	7:4	Proximity Interrupt Persistence. Controls rate of proximity interrupt to the host processor.		
		Field Value	**Meaning**	**Interrupt Persistence Function**
		0000	…	Every proximity cycle generates an interrupt
		0001	1	1 proximity value out of range
		0010	2	2 consecutive proximity values out of range
		…	…	…
		1111	15	15 consecutive proximity values out of range
Reserved	3:0	Default setting is 0x00.		