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TMD2725

ALS, and Small Aperture Proximity Sensor Module

General Description

The device features advanced proximity measurement and digital ambient light sensing (ALS). The package has been designed to accommodate a single small aperture approach. The slim module incorporates an IR LED and factory calibrated LED driver. The proximity detection feature provides object detection (e.g. mobile device screen to user's ear) by photodiode detection of reflected IR energy (sourced by the integrated LED). Detect/release events are interrupt driven, and occur when proximity result crosses upper and/or lower threshold settings. The proximity engine features offset adjustment registers to compensate for unwanted IR energy reflection at the sensor. Proximity results are further improved by automatic ambient light subtraction. The ALS detection feature provides photopic light intensity data. The ALS photodiode has UV and IR blocking filters and a dedicated data converter producing 16-bit data. This architecture allows applications to accurately measure ambient light which enables devices to calculate illuminance to control display backlight.

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits & Features

The benefits and features of TMD2725, ALS, and Small Aperture Proximity Sensor Module are listed below:

Figure 1:
Added Value of Using TMD2725

Benefits	Features
• Small aperture requirements	• 1.055mm emitter to detector distance
• Single device integrated optical solution	• ALS + proximity • 2mm x 3.65mm x 1mm • Integrated IR LED • Power management features • I^2C fast mode interface compatible
• Accurate ambient light sensing	• Photopic Ambient Light Sensor (ALS) • UV / IR blocking filters • Programmable gain and integration time
• Reduced power consumption	• 1.8V power supply with 1.8V I^2C bus

Applications

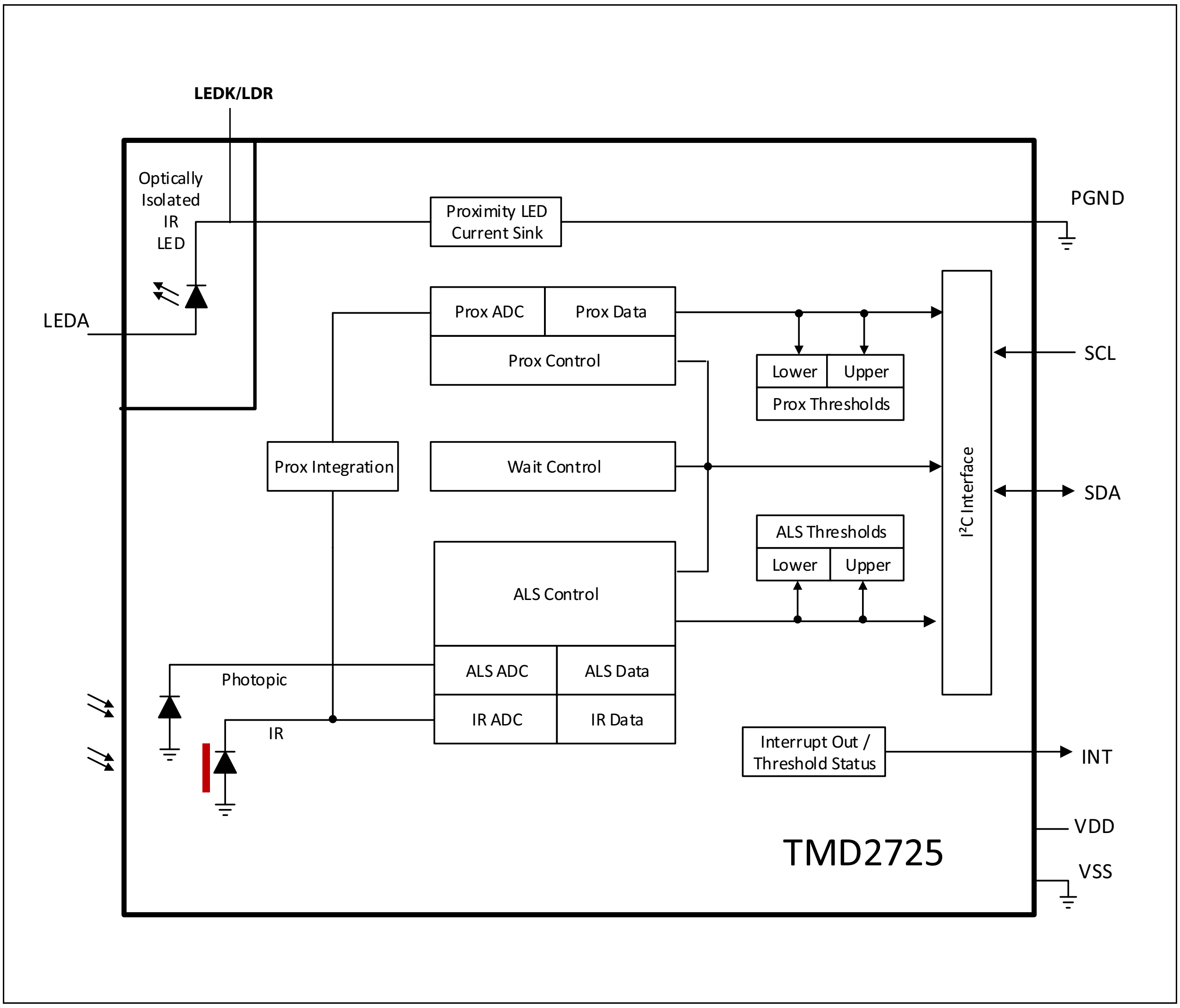
The TMD2725 applications include:

- Ambient light sensing
- Single hole proximity sensing
- Mobile phone touch screen disable

Block Diagram

The functional blocks of this device are shown below:

Figure 2:
Functional Blocks of TMD2725



Pin Assignments

Figure 3:
Pin Diagram of TMD2725

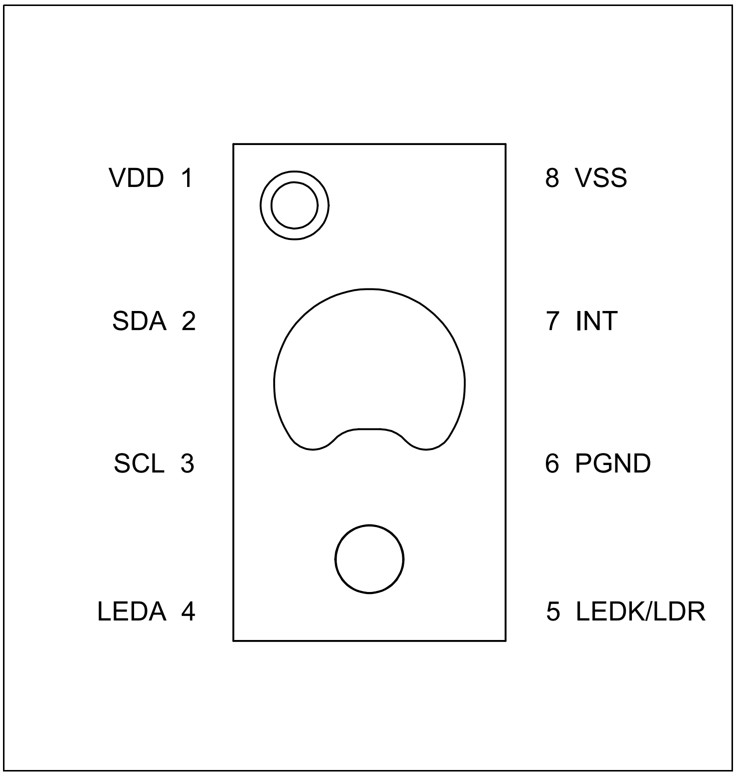


Figure 4:
Pin Description of TMD2725 (8-Pin Module)

Pin Number	Pin Name	Description
1	VDD	Supply voltage
2	SDA	I^2C serial data I/O terminal
3	SCL	I^2C serial clock input terminal
4	LEDA	LED anode
5	LEDK/LDR	This test point is the junction of the LED cathode and internal current source. Do not connect.
6	PGND	Ground for LED current sink and digital core
7	INT	Interrupt. Open drain output (active low)
8	VSS	Ground. All voltages are referenced to GND

Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Electrical Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 5:
Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Comments
Electrical Parameters					
VDD	Supply Voltage to Ground	-0.3	2.2	V	
LEDA	LED Voltage to PGND	-0.3	3.6	V	
V_{IO}	Digital I/O terminal voltage	-0.3	3.6	V	
I_{IO}	SDA, INT Output terminal current	-1	20	mA	
Electrostatic Discharge					
I_{SCR}	Input Current (latch up immunity) JEDEC JESD78D	± 100		mA	Class II
ESD_{HBM}	Electrostatic Discharge HBM JS-001-2014	± 2000		V	
ESD_{CDM}	Electrostatic Discharge CDM JEDEC JESD22-C101F	± 500		V	
Temperature Ranges and Storage Conditions					
T_{STRG}	Storage Temperature Range	-40	85	°C	
T_{BODY}	Package Body Temperature		260	°C	IPC/JEDEC J-STD-020 The reflow peak soldering temperature (body temperature) is specified according to IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices."
RH_{NC}	Relative Humidity (non-condensing)	5	85	%	
MSL	Moisture Sensitivity Level	3			Maximum floor life time 168 hours

Electrical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Figure 6:
Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
V_{DD} supply range	1.7	1.8	2.0	V
V_{LEDA}, Supply voltage range (1)	3.0	3.3	3.6	V
T_A, Operating free-air temperature(2)	-30		85	°C

Note(s):

1. The minimum required supply voltage on the LED anode (VLEDA) is the sum of the LED's VF and the voltage drop from the LDR pin to PGND pin. The minimum required VLEDA can be lowered to 2.8V if the LED's forward current doesn't exceed 102mA (PLDRIVE value of 16 or less).
2. While the device is operational across the temperature range, performance will vary with temperature. Operational characteristics are at 25°C, unless otherwise noted.

Figure 7:
Operating Characteristics, VDD = 1.8V, T_A = 25°C (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC}	Oscillator frequency			8.107		MHz
IDD	Supply Current (1)	Active ALS State (PON=AEN=1, PEN=0) (2)		80	150	µA
		Idle State (PON=1,AEN=PEN=0) (3)		30	60	
		Sleep State (4)		0.7	5	
VOL	INT, SDA output low voltage	6mA sink current			0.6	V
ILEAK	Leakage current, SDA,SCL,INT		-5		5	µA
VIH	SCL, SDA input high voltage		1.26		3.3	V
VIL	SCL, SDA input low voltage		0		0.54	V
T_{Active}	Time from power-on to ready to receive I²C commands			1.5		ms

Note(s):

1. Values are shown at the VDD pin and do not include current through the IR LED.
2. This parameter indicates the supply current during periods of ALS integration. If Wait is enabled (WEN=1), the supply current is lower during the Wait period.
3. Idle state occurs when PON=1 and all functions are not enabled.
4. Sleep state occurs when PON = 0 and I²C bus is idle. If Sleep state has been entered as the result of operational flow, SAI = 1, PON will remain high.

Typical Operating Characteristics

Figure 8:
Optical Characteristics, VDD = 1.8V, T_A = 25°C (unless otherwise noted)

Parameter	Conditions	Clear Channel			Unit
		Min	Typ	Max	
Re Irradiance responsivity Settings: AGAIN = 16x ATIME = 400ms	λ_D = 465 nm LED, 53.8 µW/cm^2		58		Count/ (µW/cm^2)
	λ_D = 530 nm LED, 43.9 µW/cm^2		490		
	λ_D = 620 nm LED, 37.5 µW/cm^2		405		
	Warm White LED, 45.6 µW/cm^2		363		
	Warm White LED, 45.6 µW/cm^2	14025	16500	18975	Counts
	λ_D = 950 nm LED, 21.1 µW/cm^2		8		Count/ (µW/cm^2)

Figure 9:
ALS Optical Characteristics, VDD = 1.8V, T_A = 25°C (unless otherwise noted)

Parameter	Conditions	Min	Typ	Max	Unit
Integration time step size		2.72	2.82	2.94	ms
Dark ADC count value	Ee = 0 µW/ cm^2 AGAIN: 64x ATIME = 100ms (0x23)	0	1	3	Counts
Gain Scaling, relative to 1x gain setting	AGAIN = 1x		1		x
	AGAIN = 4x		4		
	AGAIN = 16x		16		
	AGAIN = 64x		66		
	AGAIN = 128x		140		
ADC noise	AGAIN = 16x		0.005		% full scale

Figure 10:
Proximity Optical Characteristics, VDD = 1.8V, T_A = 25°C (unless otherwise noted)

<table>
<tr><th>Parameter</th><th>Conditions</th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td>Part to part variation [1]</td><td>Conditions:
PGAIN = 2 (4x)
PLDRIVE = 8 (54mA)
PPULSE = 15 (16 pulses)
PPULSE_LEN = 1 (8µs)
d=23mm round target
30mm target distance</td><td>75</td><td>100</td><td>125</td><td>%</td></tr>
<tr><td>Response, absolute</td><td>Basic proximity measurement [2]
Conditions:
PGAIN = 2 (4x),
PLDRIVE = 16 (102mA)
PPULSE = 15 (16 pulses)
PPULSE_LEN = 2 (16µs)
Target material:
90% reflective surface of Kodak gray card
Target Size: 100mm x 100mm
Target Distance: 100mm</td><td>128</td><td>160</td><td>192</td><td rowspan="2">Counts</td></tr>
<tr><td>Response, no target</td><td>PGAIN = 2 (4x)
ILEDDRIVE = 16 (102mA)
PPULSE = 16 (17 Pulses)
Pulse Length = 2 (16µS)</td><td>0</td><td></td><td>20</td></tr>
<tr><td>Noise/Signal [3]</td><td>PGAIN = 2 (4x)
IRLEDDRIVE = 8 (54mA)
PPULSE = 15 (16 pulses)
PPULSE_LEN = 1 (8µs)
d=23mm round target
30mm target distance</td><td></td><td></td><td>1.2</td><td>%</td></tr>
</table>

Note(s):

1. Production tested result is the average of 5 readings expressed relative to a calibrated response.
2. Representative result by characterization.
3. Production tested result is the average of 20 readings divided by the maximum proximity value 255.

Figure 11:
Spectral Responsivity

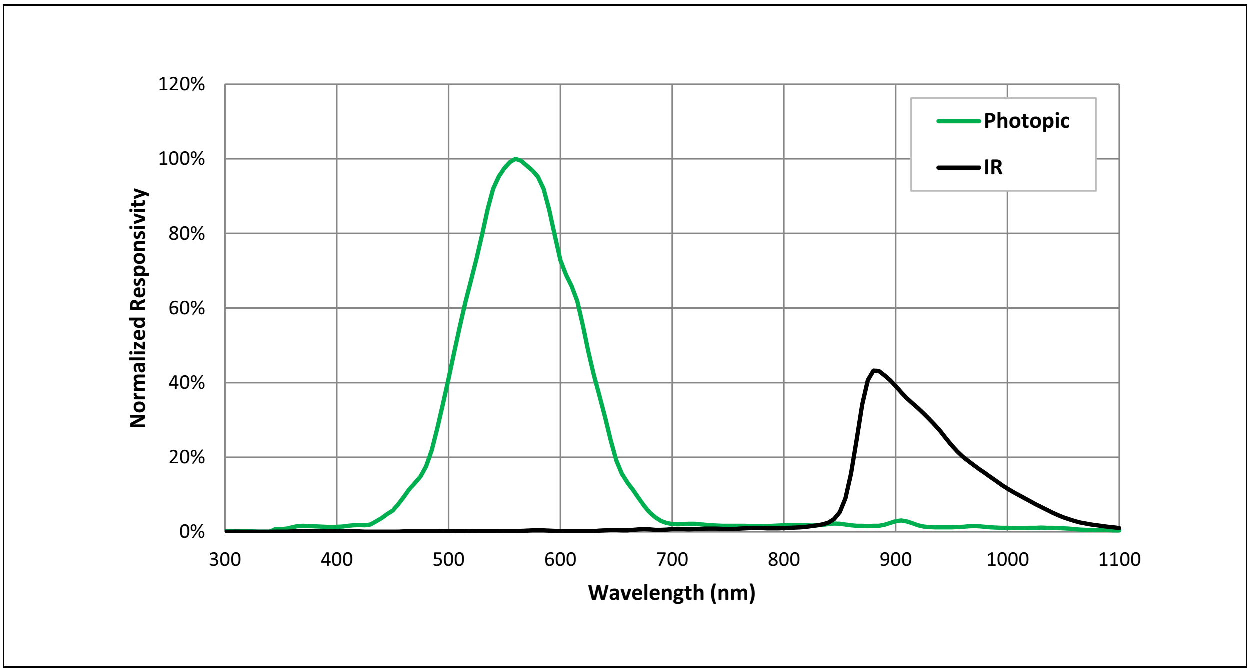


Figure 12:
ALS Responsivity vs Angular Displacement

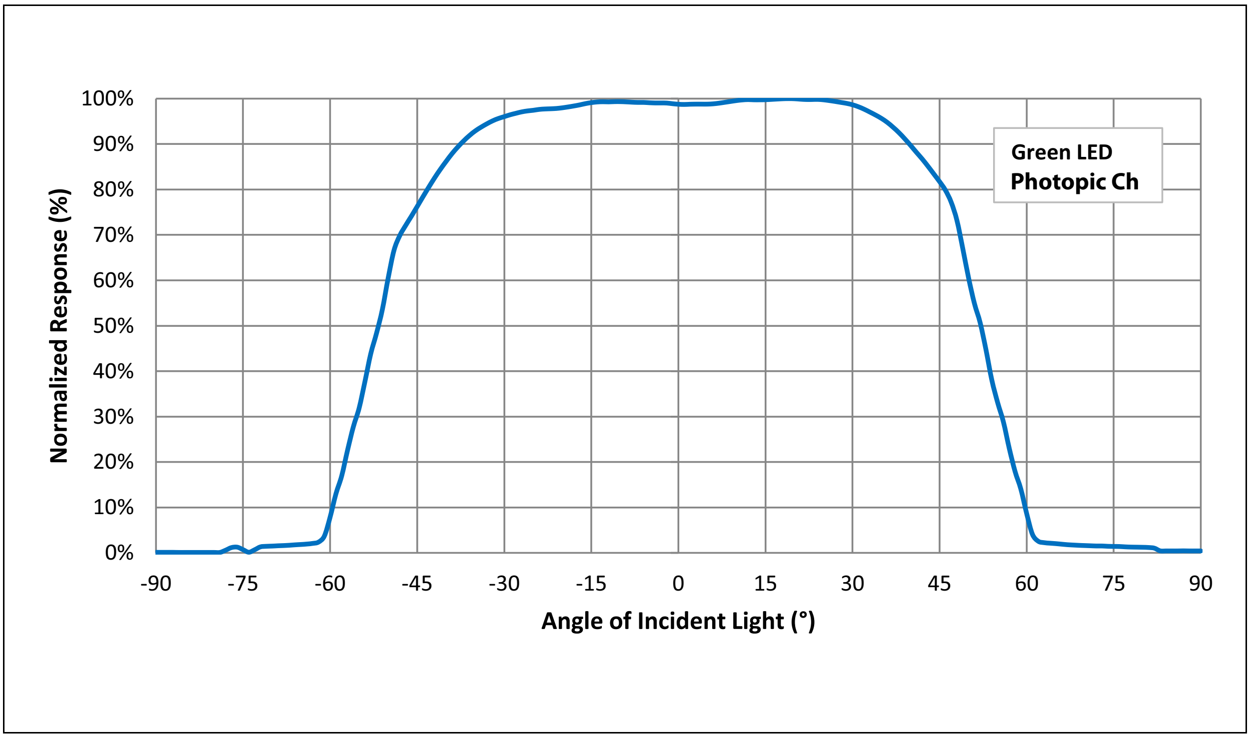


Figure 13:
ALS Linearity

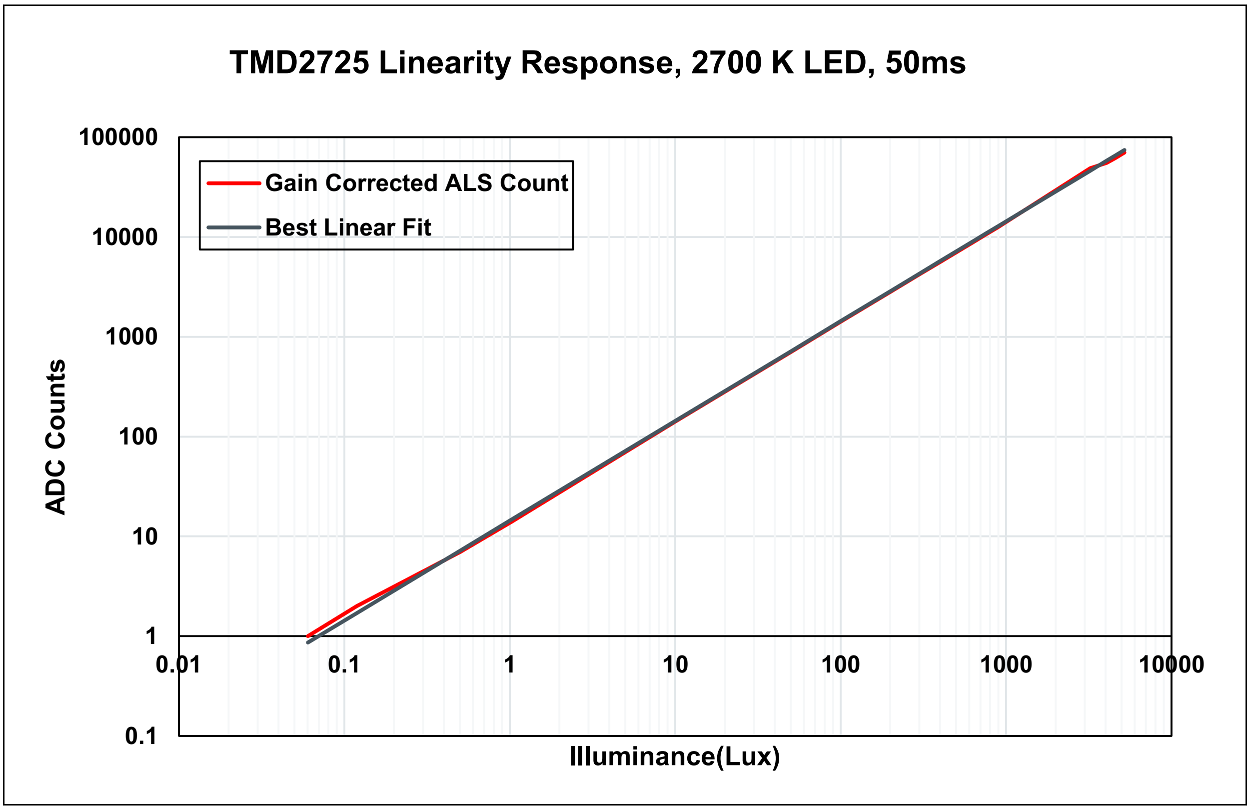
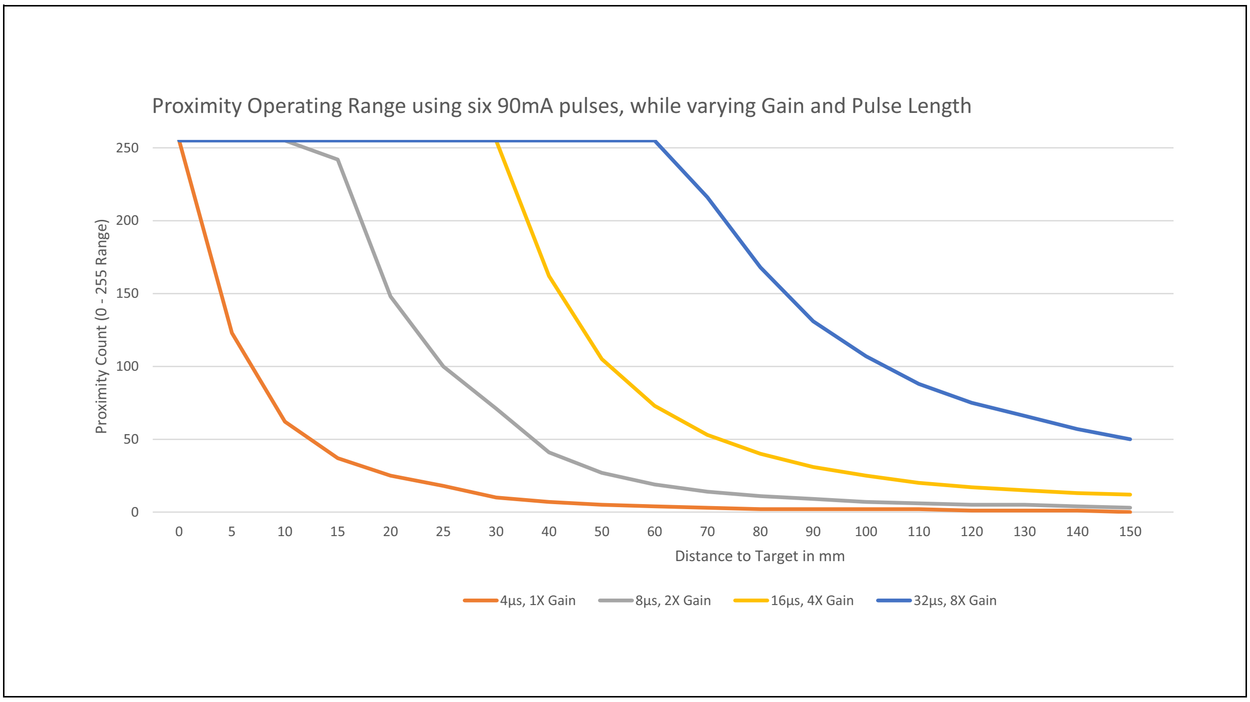


Figure 14:
Proximity Operation of TMD2725



Proximity Operation: By varying Gain, LED drive current, number of LED pulses and LED pulse duration the proximity detection range can be adjusted.

Detailed Description

Proximity

Proximity results are affected by three fundamental factors: the integrated IR LED emission, IR reception, and environmental factors, including target distance and surface reflectivity.

The IR reception signal path begins with IR detection from a photodiode and ends with the 8-bit proximity result in PDATA register. Signal from the photodiode is amplified, and offset adjusted to optimize performance. Offset correction or cross-talk compensation is accomplished by adjustment to the POFFSET register.

The analog circuitry of the device applies the offset value as a subtraction to the signal accumulation; therefore a positive offset value has the effect of decreasing the results.

Ambient Light Sensing, ALS

The ALS reception signal path begins as photodiodes receive filtered light and ends with the 16-bit results in the PHOTOPICL/H and ALS_IRL/H registers. The Photopic photodiode is filtered with a UV and IR filter. The ALS_IR photodiode is filtered to receive only IR. Signal from the photodiodes simultaneously accumulate for a period of time set by the value in ATIME before the results are available. Gain is adjustable from 1x to 64x to facilitate operation over a wide range of lighting conditions. Custom LUX equations are used to calculate the amount of ambient light, as well as, determine the light type (e.g. LED, fluorescent, incandescent, etc.) using the two ALS results.

I²C Characteristics

The device uses I²C serial communication protocol for communication. The device supports 7-bit chip addressing and both standard and fast clock frequency modes with a chip address of 0x39. Read and Write transactions comply with the standard set by Philips (now NXP).

Internal to the device, an 8-bit buffer stores the register address location of the desired byte to read or write. This buffer auto-increments upon each byte transfer and is retained between transaction events (I.e. valid even after the master issues a STOP command and the I²C bus is released). During consecutive Read transactions, the future/repeated I²C Read transaction may omit the memory address byte normally following the chip address byte; the buffer retains the last register address + 1.

I²C Write Transaction

A Write transaction consists of a START, CHIP-ADDRESS WRITE, REGISTER-ADDRESS, DATA BYTE(S), and STOP. Following each byte (9TH clock pulse) the slave places an ACKNOWLEDGE/ NOT-ACKNOWLEDGE (ACK/NACK) on the bus. If NACK is transmitted by the slave, the master may issue a STOP.

I²C Read Transaction

A Read transaction consists of a START, CHIP-ADDRESS WRITE, REGISTER-ADDRESS, START, CHIP-ADDRESS READ, DATA BYTE(S), and STOP. Following all but the final byte the master places an ACK on the bus (9TH clock pulse). Termination of the Read transaction is indicated by a NACK being placed on the bus by the master, followed by STOP.

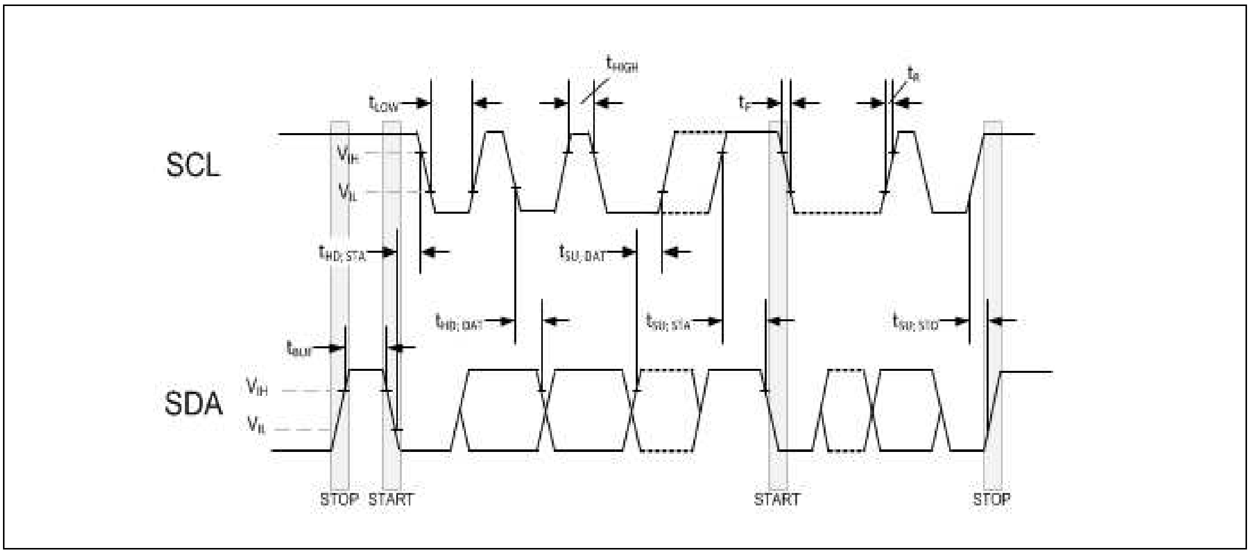
Alternately, if the previous I²C transaction was a Read, the internal register address buffer is still valid, allowing the transaction to proceed without "re"-specifying the register address. In this case the transaction consists of a START, $\text{CHIP-ADDRESS}_{\text{READ}}$, DATA BYTE(S), and STOP. Following all but the final byte the master places an ACK on the bus (9^{TH} clock pulse). Termination of the Read transaction is indicated by a NACK being placed on the bus by the master, followed by STOP.

The I²C bus protocol was developed by Philips (now NXP). For a complete description of the I²C protocol, please review the NXP I²C design specification at:

http://www.i2c-bus.org/references/

Timing Diagrams

Figure 15:
I²C Timing



Principles of Operation

System State Machine

An internal state machine provides system control of the ALS, proximity detection, and power management features of the device. At power up, an internal power-on-reset initializes the device and puts it in a lowpower Sleep state. When a write on I^2C bus to the Enable register (0x80) PON bit is set, the device transitions to the Idle state. If PON is disabled, the device will return to the Sleep state to save power. Otherwise, the device will remain in the Idle state until a Proximity or ALS function is enabled. Once enabled, the device will execute the ALS, Proximity and Wait states in sequence as indicated in Figure 16 and Figure 17. Upon completion, the device will automatically begin a new ALS-Prox-Wait cycle as long as PON and either PEN or AEN remain enabled. If the Prox or ALS function generates an interrupt and the Sleep-After-Interrupt (SAI) feature is enabled, the device will transition to the Sleep state and remain in a low-power mode until an I^2C command is received clearing the interrupts in the STATUS register. See Interrupts for additional information.

Figure 16:
Detailed State Diagram

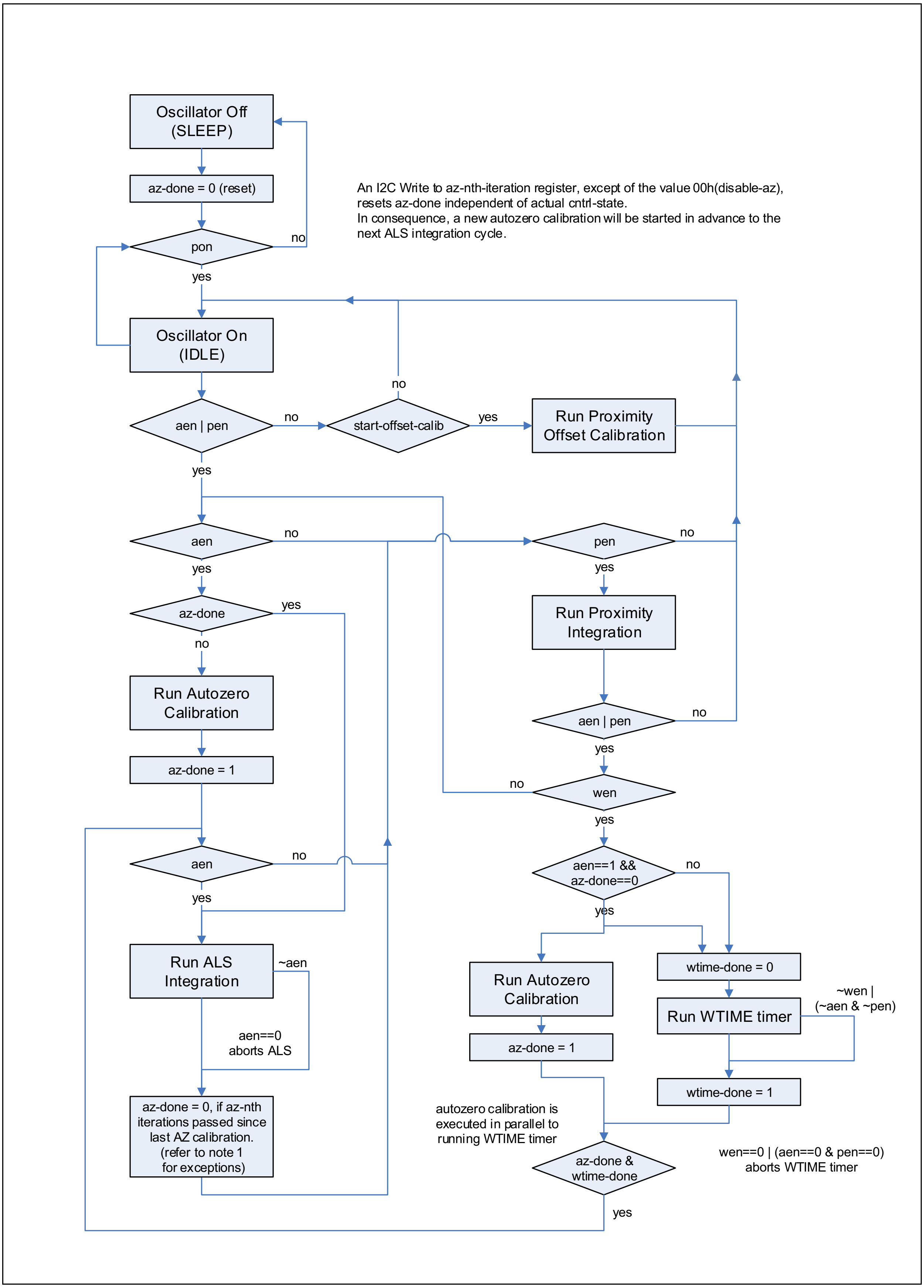
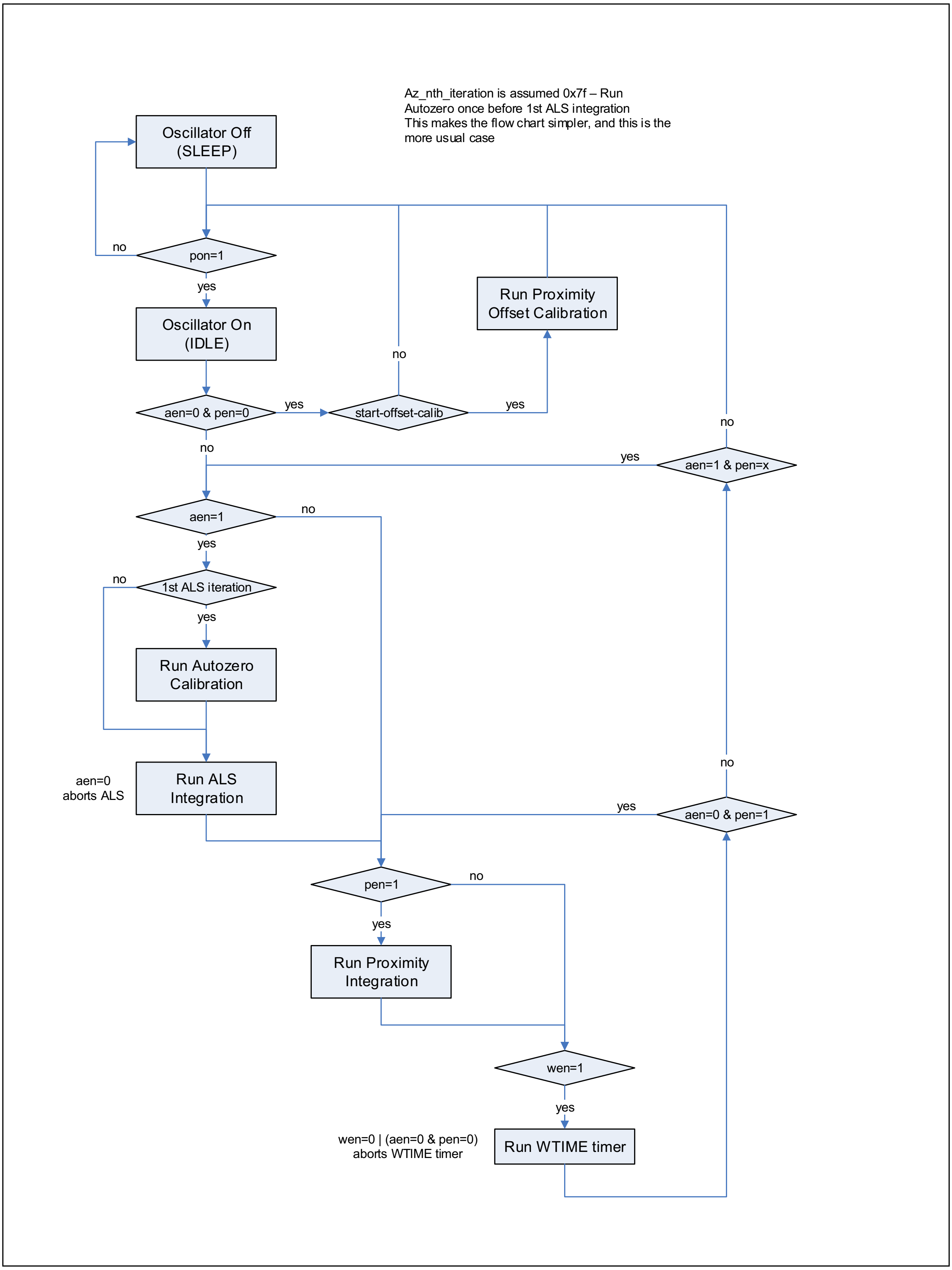


Figure 17:
Simplified State Diagram



Register Description

Register Overview

Figure 18:
Register Overview

Address	Register Name	R/W	Register Function	Reset Value
0x80	ENABLE	R/W	Enables states and functions	0x00
0x81	ATIME	R/W	ALS integration time	0x00
0x82	PRATE	R/W	Proximity sampling time	0x1F
0x83	WTIME	R/W	Wait time	0x00
0x84	AILTL	R/W	ALS interrupt low threshold low byte	0x00
0x85	AILTH	R/W	ALS interrupt low threshold high byte	0x00
0x86	AIHTL	R/W	ALS interrupt high threshold low byte	0x00
0x87	AIHTH	R/W	ALS interrupt high threshold high byte	0x00
0x88	PILT	R/W	Proximity interrupt low threshold	0x00
0x8A	PIHT	R/W	Proximity interrupt high threshold	0x00
0x8C	PERS	R/W	Interrupt persistence filters	0x00
0x8D	CFG0	R/W	Configuration register zero	0x80
0x8E	PCFG0	R/W	Proximity configuration register zero	0x4F
0x8F	PCFG1	R/W	Proximity configuration register one	0x80
0x90	CFG1	R/W	Configuration register one	0x00
0x91	REVID	R	Revision ID	0x20
0x92	ID	R	Device ID	0xE4
0x93	STATUS	R	Device status register	0x00
0x94	PHOTOPICL	R	Photopic channel data low byte	0x00
0x95	PHOTOPICH	R	Photopic channel data high byte	0x00
0x96	ALS_IRL	R	IR channel data low byte	0x00
0x97	ALS_IRH	R	IR channel data high byte	0x00
0x9C	PDATA	R	Proximity channel data	0x00
0x9E	REVID2	R	Auxiliary ID	0x00
0x9F	CFG2	R/W	Configuration register two	0x04
0xAB	CFG3	R/W	Configuration register three	0x4C

Address	Register Name	R/W	Register Function	Reset Value
0xC0	POFFSETL	R/W	Proximity offset magnitude	0x00
0xC1	POFFSETH	R/W	Proximity offset sign	0x00
0xD6	AZ_CONFIG	R/W	Autozero configuration	0x7F
0xD7	CALIB	R/W	Calibration start	0x00
0xD9	CALIBCFG	R/W	Calibration configuration	0x50
0xDC	CALIBSTAT	R/W	Calibration status	0x00
0xDD	INTENAB	R/W	Interrupt enables	0x00

Note(s):

1. Address 0x98 and 0x99 will contain the results for the IR photodiode when controlled by the Green/IR MUX.
   Register Access:
   R = Read Only
   W = Write Only
   R/W = Read or Write
   SC = Self Clearing after access

Detailed Register Description

Enable Register (Address 0x80)

Figure 19:
Enable Register

Addr: 0x80		Enable		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	RESERVED	0000	RW	Reserved.
3	WEN	0	RW	This bit activates the wait feature. Active high.
2	PEN	0	RW	This bit activates the proximity detection. Active high.
1	AEN	0	RW	This bit actives the ALS function. Active high. *Set AEN=1 and PON=1 in the same command to ensure auto-zero function is run prior to the first measurement.
0	PON	0	RW	This field activates the internal oscillator and ADC channels. Active high.

Before activating AEN or PEN, preset each applicable operating mode registers and bits.

ATIME Register (Address 0x81)

Figure 20:
ATIME Register

<table>
<tr><th colspan="2">Addr: 0x81</th><th colspan="6">ATIME</th></tr>
<tr><th>Bit</th><th>Bit Name</th><th>Default</th><th>Access</th><th colspan="4">Bit Description</th></tr>
<tr><td rowspan="8">7:0</td><td rowspan="8">ATIME</td><td rowspan="8">0x00</td><td rowspan="8">RW</td><td colspan="4">ALS value that specifies the integration time in 2.78ms intervals. 0x00 indicates 2.8ms. The maximum ALS value depends on the integration time. For every 2.78ms, the maximum value increases by 1024. This means that to be able to reach ALS full scale, the integration time has to be at least 64*2.8ms.</td></tr>
<tr><td>Value</td><td>Integration Cycles</td><td>Integration Time</td><td>Maximum ALS Value</td></tr>
<tr><td>0x00</td><td>1</td><td>2.8ms</td><td>1023</td></tr>
<tr><td>0x01</td><td>2</td><td>5.6ms</td><td>2047</td></tr>
<tr><td>…</td><td>…</td><td>…</td><td>…</td></tr>
<tr><td>0x3F</td><td>64</td><td>180ms</td><td>65535</td></tr>
<tr><td>…</td><td>…</td><td>…</td><td>…</td></tr>
<tr><td>0xFF</td><td>256</td><td>719ms</td><td>65535</td></tr>
</table>

The ATIME register controls the integration time of the ALS ADCs. The timer is implemented with a down counter with 0x00 as the terminal count. The timer is clocked at a 2.8ms nominal rate. Loading 0x00 will generate a 2.8ms integration time, loading 0x01 will generate a 5.6ms integration time, and so forth. The RC oscillator runs at 8MHz nominal rate. This gets divided by 11 to generate the integration clock of 727kHz. One count in ATIME (nominal 2.8ms) are 2.78ms. This is 2048 integration clock cycles: 125ns*11*8*256=2.8ms.

PTIME Register (Address 0x82)

Figure 21:
PTIME Register

Addr: 0x82		PTIME		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	PTIME	0x1F	RW	This register defines the duration of 1 Prox Sample, which is (PTIME + 1)*88µs.

WTIME Register (Address 0x83)

Figure 22:
WTIME Register

Addr: 0x83		WTIME				
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**		
7:0	WTIME	0x00	RW	Value that specifies the wait time between ALS cycles in 2.78ms increments.		
				Value	**Increments**	**Wait Time**
				0x00	1	2.8ms (33.8ms)
				0x01	2	5.6ms (67.6ms)
				…	…	…
				0x3F	64	180ms (2.16s)
				…	…	…
				0xFF	256	719ms (8.65s)

The wait timer is implemented using a down counter. Wait time = (value +1) x 2.8ms. If WLONG is enabled then Wait time = (value +1) x 2.8ms. x 12.

AILTL Register (Address 0x84)

Figure 23:
AILTL Register

Addr: 0x84		AILTL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	AILTL	0x00	RW	This register sets the low byte of the LOW ALS threshold.

The photopic channel is compared against low-going 16-bit threshold value set by AILTL and AILTH.

AILTH Register (Address 0x85)

Figure 24:
AILTH Register

Addr: 0x85		AILTH		
Bit	Bit Name	Default	Access	Bit Description
7:0	AILTH	0x00	RW	This register sets the high byte of the LOW ALS threshold.

The photopic channel is compared against low-going 16-bit threshold value set by AILTL and AILTH.
The contents of the AILTH and AILTL registers are combined and treated as a sixteen bit threshold value. If the value generated by the photopic channel is below the AILTL/H threshold and the APERS value is reached, the AINT bit is asserted. If AIEN is set, then the INT pin will also assert.
When setting the 16-bit ALS threshold AILTL must be written first, immediately follow by AILTH. Internally, the lower 8-bits are buffered until the upper 8-bits are written. As the upper 8-bits are written both the high and low bytes are simultaneously latched as a 16-bit value.

AIHTL Register (Address 0x86)

Figure 25:
AIHTL Register

Addr: 0x86		AIHTL		
Bit	Bit Name	Default	Access	Bit Description
7:0	AIHTL	0x00	RW	This register sets the low byte of the HIGH ALS threshold.

The photopic channel is compared against high-going 16-bit threshold value set by AIHTL and AIHTH.
The contents of the AIHTH and AIHTL registers are combined and treated as a sixteen bit threshold value. If the value generated by the photopic channel is above the AIHTL/H threshold and the APERS value is reached, the AINT bit is asserted. If AIEN is set, then the INT pin will also assert. When setting the 16-bit ALS threshold AIHTL must be written first, immediately follow by AIHTH. Internally, the lower 8-bits are buffered until the upper 8-bits are written. As the upper 8-bits are written both the high and low bytes are simultaneously latched as a 16-bit value.

AIHTH Register (Address 0x87)

Figure 26:
AIHTH Register

Addr: 0x87		AIHTH		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	AIHTH	0x00	RW	This register sets the high byte of the HIGH ALS threshold.

The photopic channel is compared against high-going 16-bit threshold value set by AIHTL and AIHTH.
The contents of the AIHTH and AIHTL registers are combined and treated as a sixteen bit threshold value. If the value generated by the photopic channel is above the AIHTL/H threshold and the APERS value is reached, the AINT bit is asserted. If AIEN is set, then the INT pin will also assert.
When setting the 16-bit ALS threshold AIHTL must be written first, immediately follow by AIHTH. Internally, the lower 8-bits are buffered until the upper 8-bits are written. As the upper 8-bits are written both the high and low bytes are simultaneously latched as a 16-bit value.

PILT Register (Address 0x88)

Figure 27:
PILT Register

Addr: 0x88		PILT		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	PILT	0x00	RW	This register sets the Proximity ADC channel low threshold.

The proximity channel is compared against low-going 8-bit threshold value set by PILT.
If the value generated by the Proximity channel is below the PILT threshold and the PPERS value is reached, the PINT bit is asserted. If PIEN is set, then the INT pin will also assert.

PIHT Register (Address 0x8A)

Figure 28:
PIHT Register

Addr: 0x8A		PIHT		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	PIHT	0x00	RW	This register sets the Proximity ADC channel high threshold.

The proximity channel is compared against high-going 8-bit threshold value set by PIHT.
If the value generated by the Proximity channel is above the PIHT threshold and the PPERS value is reached, the PINT bit is asserted. If PIEN is set, then the INT pin will also assert.

PERS Register (Address 0x8C)

Figure 29:
PERS Register

Addr: 0x8C		PERS			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
7:4	PPERS	0000	RW	This register sets the Proximity persistence filter.	
				Value	**Interrupt**
				0	Every Proximity Cycle
				1	Any value outside PILT/PIHT thresholds
				2	2 consecutive proximity values out of range
				3	3 consecutive proximity values out of range
				…	….
				15	15 consecutive proximity values out of range

Addr: 0x8C		PERS			
Bit	Bit Name	Default	Access	Bit Description	
3:0	APERS	0000	RW	This register sets the ALS persistence filter.	
				0	Every ALS Cycle
				1	Any value outside ALS thresholds
				2	2 consecutive ALS values out of range
				3	3 consecutive ALS values out of range
				4	5 consecutive ALS values out of range
				5	10 consecutive ALS values out of range
				6	15 consecutive ALS values out of range
				7	20 consecutive ALS values out of range
				…	…
				13	50 consecutive ALS values out of range
				14	55 consecutive ALS values out of range
				15	60 consecutive ALS values out of range

The frequency of consecutive proximity channel results outside of threshold limits are counted; this count value is compared against the PPERS value. If the counter is equal to the PPERS value an interrupt is asserted. Any time a proximity channel result is inside the threshold values the counter is cleared. The frequency of consecutive photopic channel results outside of threshold limits are counted; this count value is compared against the APERS value. If the counter is equal to the APERS setting an interrupt is asserted. Any time a photopic channel result is inside the threshold values the counter is cleared.

CFG0 Register (Address 0x8D)

Figure 30:
CFG0 Register

Addr: 0x8D		CFG0		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:3	Reserved	10000	RW	This field must be set to the default value.
2	WLONG	0	RW	When Wait Long is asserted the wait period as set by WTIME is increased by a factor of 12.
1:0	Reserved	00	RW	This field must be set to the default value.

The wait timer is implemented using a down counter. Wait time = (value +1) x 2.8ms. If WLONG is enabled then Wait time = (value +1) x 2.8ms x 12.

PCFG0 Register (Address 0x8E)

Figure 31:
PCFG0 Register

Addr: 0x8E		PCFG0			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
7:6	PPULSE_LEN	01	RW	Proximity Pulse Length	
				Value	**Pulse Length**
				0	4μs
				1	8μs
				2	16μs
				3	32μs
5:0	PPULSE	001111	RW	Maximum Number of Pulses in a single proximity cycle.	
				Value	**Maximum Number of Pulses**
				0	1
				1	2
				2	3
				…	…
				63	64

The PPULSE_LEN field sets the width of all IR LED pulses within the proximity cycle. Longer pulses result in increased proximity range and typically result in less electrical noise generated in the analog front end. However, a setting of 8μs is recommended because less cumulative noise is generated during a proximity cycle.

The PPULSE field sets the maximum number of IR LED pulses that may occur in a proximity cycle. The proximity engine will automatically continue to add IR LED pulses, up to the value set in PPULSE or if a near-saturation condition occurs.

The dynamic range of the sensor is automatically adjusted to detect distant targets as well as prevent saturation from close targets.

This operation also reduces power consumption because proximity integration period is automatically shortened when a target is either to close or far from the sensor.