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TOSHIBA

32 Bit RISC Microcontroller
TX03 Series

TMPM366FDXBG/FYXBG/FWXBG

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TOSHIBA CORPORATION

Semiconductor & Storage Products Company

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Introduction: Notes on the description of SFR (Special Function Register) under this specification

An SFR (Special Function Register) is a control register for peripheral circuits (IP).

The SFR addresses of IPs are described in the chapter on memory map, and the details of SFR are given in the chapter of each IP.

Definition of SFR used in this specification is in accordance with the following rules.

- a. SFR table of each IP as an example
 - SFR tables in each chapter of IP provides register names, addresses and brief descriptions.
 - All registers have a 32-bit unique address and the addresses of the registers are defined as follows, with some exceptions: "Base address + (Unique) address"

Base Address = 0x0000_0000

Register name		Address(Base+)
Control register	SAMCR	0x0004
		0x000C

Note: **SAMCR register address is 32 bits wide from the address 0x0000_0004 (Base Address(0x00000000) + unique address (0x0004)).**

Note: **The register shown above is an example for explanation purpose and not for demonstration purpose. This register does not exist in this microcontroller.**

- b. SFR(register)
 - Each register basically consists of a 32-bit register (some exceptions).
 - The description of each register provides bits, bit symbols, types, initial values after reset and functions.

1.2.2 SAMCR(Control register)

	31	30	29	28	27	26	25	24
bit symbol	-	-	-	-	-	-	-	-
After reset	0	0	0	0	0	0	0	0
	23	22	21	20	19	18	17	16
bit symbol	-	-	-	-	-	-	-	-
After reset	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8
bit symbol	-	-	-	-	-	-	MODE	
After reset	0	0	0	0	0	0	0	0
	7	6	5	4	3	2	1	0
bit symbol	MODE		TDATA					
After reset	0	0	0	1	0	0	0	0

Bit	Bit Symbol	Type	Function
31-10	-	R	"0" can be read.
9-7	MODE[2:0]	R/W	Operation mode settings 000 : Sample mode 0 001 : Sample mode 1 010 : Sample mode 2 011 : Sample mode 3 The settings other than those above: Reserved
6-0	TDATA[6:0]	W	Transmitted data

Note: The Type is divided into three as shown below.

R / W READ WRITE
 R READ
 W WRITE

c. Data description

Meanings of symbols used in the SFR description are as shown below.

- x:channel numbers/ports
- n,m:bit numbers

d. Register description

Registers are described as shown below.

- Register name <Bit Symbol>
 Example: SAMCR<MODE>="000" or SAMCR<MODE[2:0]>="000"
 <MODE[2:0]> indicates bit 2 to bit 0 in bit symbol mode (3bit width).
- Register name [Bit]
 Example: SAMCR[9:7]="000"
 It indicates bit 9 to bit 7 of the register SAMCR (32 bit width).

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Revision History

Date	Revision	Comment
2011/5/10	Tentative 1	First Release of Revised
2011/10/19	1	First Release
2011/11/17	2	Contents Revised
2013/6/11	3	Contents Revised

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24. Package Dimensions

Not Recommended
for New Design

TMPM366FDXBG/FYXBG/FWXBG

The TMPM366FDXBG/FYXBG/FWXBG is a 32-bit RISC microprocessor series with an ARM Cortex™-M3 microprocessor core.

Product Name	ROM (FLASH)	RAM	Package
TMPM366FDXBG	512 Kbyte	64 Kbyte	P-TFBGA109-0909-0.65-002
TMPM366FYXBG	256 Kbyte	48 Kbyte	
TMPM366FWXBG	128 Kbyte	32 Kbyte	

Features of the TMPM366FDXBG/FYXBG/FWXBG are as follows:

1.1 Features

1. ARM Cortex-M3 microprocessor core
 - a. Improved code efficiency has been realized through the use of Thumb® -2 instruction.
 - New 16-bit Thumb instructions for improved program flow
 - New 32-bit Thumb instructions for improved performance
 - New Thumb mixed 16-/32-bit instruction set can produce faster, more efficient code.
 - b. Both high performance and low power consumption have been achieved.
 - [High performance]
 - A 32-bit multiplication ($32 \times 32 = 32$ bit) can be executed with one clock.
 - Division takes between 2 and 12 cycles depending on dividend and divisor
 - [Low power consumption]
 - Optimized design using a low power consumption library
 - Standby function that stops the operation of the micro controller core
 - c. High-speed interrupt response suitable for real-time control
 - An interruptible long instruction.
 - Stack push automatically handled by hardware.
2. On chip program memory and data memory
 - On chip SRAM : 64 Kbyte / 48 Kbyte / 32 Kbyte
 - On chip Flash ROM : 512 Kbyte / 256 Kbyte / 128 Kbyte
3. External bus interface (EBIF)
 - Up to 16Mbytes access area (Program / Data)
 - External data bus (Separate / Multiplex): 8 /16bit bus width
 - Chip select / Wait controller: 2 channels
4. DMA controller (DMAC) : 2 units 4 channels