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Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

TOSHIBA

32 Bit RISC Microcontroller
TX03 Series

TMPM369FDFG

TOSHIBA CORPORATION
Semiconductor & Storage Products Company

Important Notices

Make sure to read read this chapter before using the product.

1 Serial bus interface

There are restrictions on the use of I2C bus mode when the multi-master function is used.

1.1 Description

When the multi-master function is used in I2C bus mode, if these masters start the communications simultaneously, the following phenomena may occur:

1. Communications may be locked up.
2. SCL pulse widths shorten; therefore these pulses may not satisfy I2C Specifications.

1.2 Condition

These phenomena occur only when the multi-master function is used in I2C bus mode. If a single master is used, these phenomena do not occur.

1.3 Workaround

There is no workaround for these phenomena. Perform recovery process by software.

1.4 How to Recover from These Phenomena

Perform recovery process by software.

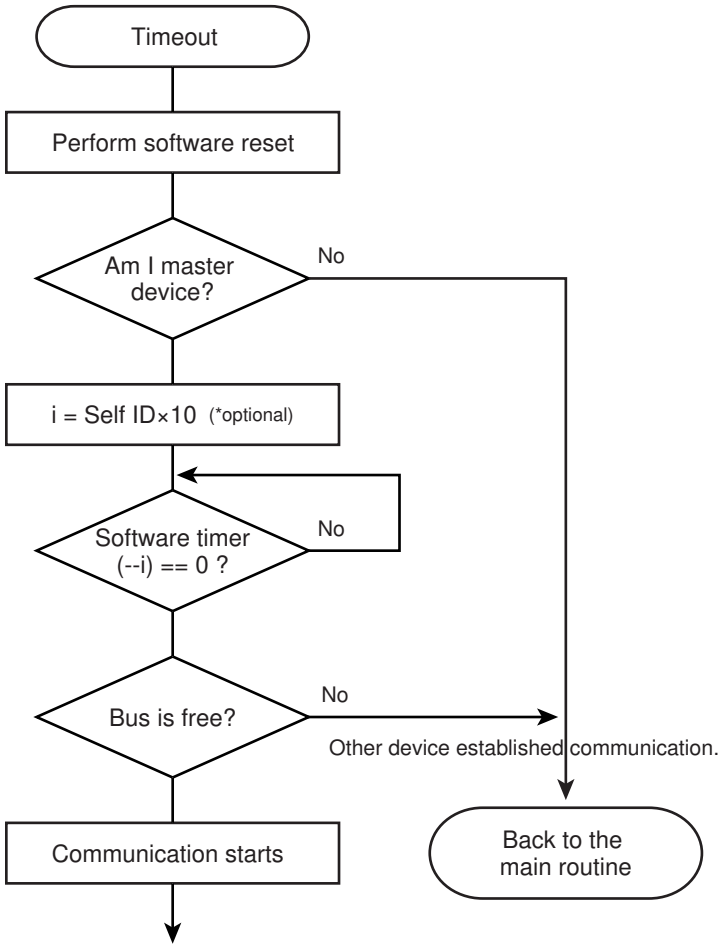
By using a timer, add timeout process to check whether communication is in a lock-up state.

An example of recovery process:

1. Start a timer count synchronously with start of the transmission.
2. If a serial interface interrupt (INTSBIx) does not occur in a certain period, the MCU determines the timeout.
3. If the MCU determines the timeout, communications may be locked up. Perform software reset on the serial bus interface circuit. This circuit is initialized to release communication from the lock up state.
4. Resend transmission data.

Mostly, Process 1 to 4 are enough to recovery; however if the multiple products are connected to the same bus line, add a delay time between each product's recovery process before Process 4 (resending data) is performed. This delay makes a time difference between each master; therefore bus collision can be avoided when the data is sent again.

Example: Recovery process after a timeout is detected.



2 Transitions to Low-power Consumption Mode and Generating a Non-maskable Interrupt

This chapter describes the precautions at which non-maskable interrupt (NMI) occurs when the MCU enters low-power consumption mode.

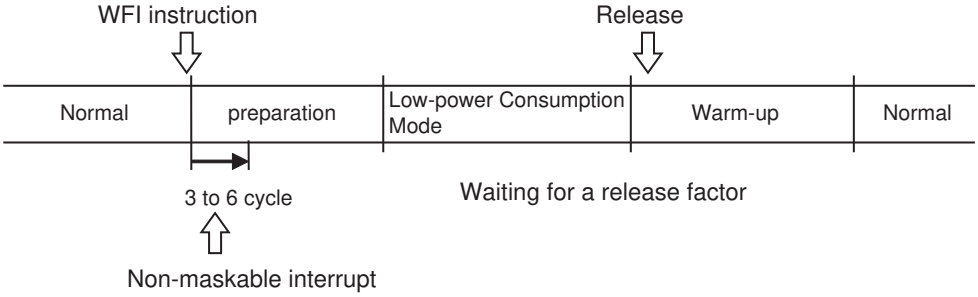
- STOP1
- STOP2

2.1 Description

When the WFI instruction is executed to enter the above-mentioned low-power consumption mode, if a non-maskable interrupt (NMI) occurs, the MCU may enter low-power consumption mode without the process for releasing low-power consumption mode.

Note 1: An NMI notice and flag setting to the CPU are normal; therefore the NMI process after low-power consumption mode is released can be performed.

Note 2: When the MCU has entered low-power consumption mode, factors other than an NMI are accepted; however an NMI may not be accepted.



2.2 Conditions

- The WFI instruction is executed to enter low-power consumption mode.
- A non-maskable interrupt occurs after WFI instruction execution and within 3 to 6 cycles.

2.3 Workaround

Do not use a non-maskable interrupt as a release factor for the above-mentioned low-power consumption modes.

To avoid generating a non-maskable interrupt, the following settings should be specified before the MCU enters the above-mentioned low-power consumption mode.

- NMI pin: This input pin must be fixed to "High".
- Watchdog timer: Stop the watchdog timer or set the reset function.
- Voltage detection circuit: Stop the voltage detection circuit or set the reset function.

3 Restrictions on the Use of the DMA function

There are restrictions on the use of the DMA function.

3.1 Description

When the synchronous serial interface (SSP) or the asynchronous serial communication circuit (UART) is used to transmit data or receive data, the following problems may occur:

- At transmission : A part of communication data may be lost (the FIFO buffer may overflow).
- At reception : Unnecessary data may be transferred (the FIFO buffer may underflow).

3.2 Conditions

The table below lists the peripheral functions that are connectable at DMA transfer. When the SSP <ch4 to 9> or UART <ch10 to 13> are used, if single-transfer is enabled (the connection channel of DMAxChnlUseburstSet is set to "0"), the problem may occur.

ch	Peripheral circuit	TMPM367FDFG TMPM367FDXBG TMPM368FDFG TMPM368FDXBG TMPM369FDFG TMPM369FDXBG	TMPM36BFYFG TMPM36BF10FG	ch	Peripheral circuit	TMPM367FDFG TMPM367FDXBG TMPM368FDFG TMPM368FDXBG TMPM369FDFG TMPM369FDXBG	TMPM36BFYFG TMPM36BF10FG
0	ADC conversion completion	–	o	16	SIO/UART1 reception	o	o
	ADC A conversion completion	o	–	17	SIO/UART1 transmission	o	o
1	ADC B conversion completion	o	–	18	SIO/UART2 reception	o	o
2	DAC0 conversion trigger	o	–	19	SIO/UART2 transmission	o	o
3	DAC1 conversion trigger	o	–	20	SIO/UART3 reception	o	o
4	SSP0 reception	o	o	21	SIO/UART3 transmission	o	o
5	SSP0 transmission	o	o	22	I2C/SIO0 transmission/ reception	o	o
6	SSP1 reception	o	o	23	I2C/SIO1 transmission/ reception	o	o
7	SSP1 transmission	o	o	24	I2C/SIO2 transmission/ reception	o	o
8	SSP2 reception	o	o	25	TMRB0 compare match	o	o
9	SSP2 transmission	o	o	26	TMRB1 compare match	o	o
10	UART4 reception	o	o	27	TMRB2 compare match	o	o
11	UART4 transmission	o	o	28	TMRB3 compare match	o	o
12	UART5 reception	o	o	29	TMRB4 compare match	o	o
13	UART5 transmission	o	o	30	DMA request pin	o	o
14	SIO/UART0 reception	o	o	31	Software trigger	o	–
15	SIO/UART0 transmission	o	o				

o: Connectable peripheral circuit –: Not supported

3.3 Explanation

- At transmission

  Under the following circumstance, one additional DMA request may occur compared with the number of unused data space of the FIFO of the SSP or UART. Therefore, DMA transfer is executed even if the FIFO is full and the FIFO overflow occurs.

  - The number of data of the FIFO becomes lower than the watermark level while the DMA is transferring data to the FIFO.

- At reception

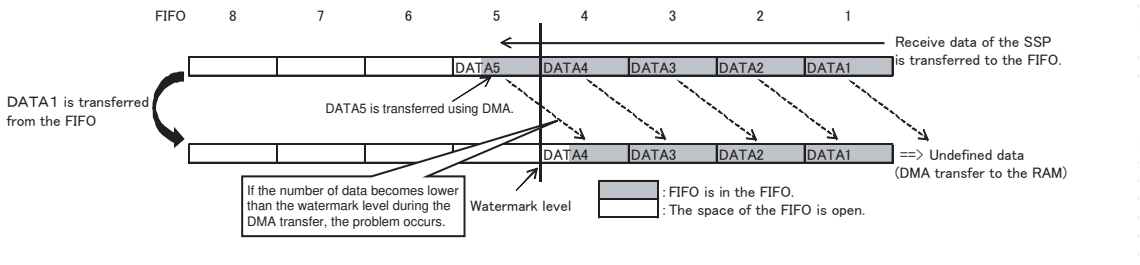
  Under the following circumstance, one additional DMA request may occur compared with the number of stored data. Therefore, invalid data is transferred from the FIFO of the SSP or UART and the FIFO underflow occurs.

  - The number of data of the FIFO becomes higher than the watermark level while the DMA is tranferring data from the FIFO of the SSP or UART.

Note: Wartermark level:

SSP	Fixed to 4
UART	Full level of UARTxIFLS<RXIFSEL[2:0]> or <TXIFSEL[2:0]>

Example of relationship between the condition of the FIFO and the watermark level (SSP transmission)



3.4 Workaround

When the DMA function is used, set "1" to the corresponding channel of DMAxChnlUseburstSet (single-transfer is prohibited).

However, there are several conditions and restrictions.

Note: These conditions and restrictions vary depending on transmission or reception.

3.4.1 Transmission

When single-transfer is prohibited, arbitration setting is subject to a constraint. According to the number of transfers, select the appropriate method below:

a. When the number of transfers is a multiple of the watermark level of the FIFO.

Set the arbitration rates to the watermark level of the FIFO. After the number of specified transfers is complete, arbitration for the priorities between the peripheral functions that are connected to the DMA controller unit is issued. Therefore, the DMA transfer can be performed at high-speed.

Set the number of arbitration rates <R_power> for the control data to the watermark level of the FIFO.

b. When the number of transfers is not a multiple of the watermark level of the FIFO.

Set the arbitration rates to "after one transfer". This setting can be used in every case. After each transfer is complete, arbitration for the priorities between the peripheral functions that are connected to the DMA controller unit is issued. Therefore, the DMA transfer is performed at slower speed than the case of (a).

Specify "0000" as the arbitration rate setting <R_power> for the control data.

3.4.2 Reception

Disable or Enable single-transfer according to the number of transfers of control data <n_minus_1>.

a. When the number of transfers is a multiple of the watermark level.

This setting can be used when the number of transfers is a multiple of the watermark level. For example, the watermark level is n, "n Å~integer number " can be set as the number of transfers.

Set "1" (disable the single-transfer) to the corresponding channel of DMAxChnlUseburstSet.

Set the number of arbitration rates <R_power> for the control data to the watermark level of the FIFO.

b. When the number of transfers is less than the watermark level.

This setting can be used when the number of transfers is less than the watermark level.

Set "0" (enable the single-transfer) to the corresponding channel of DMAxChnlUseburstSet.

Specify "0000" as the arbitration rate <R_power> for the control data.

c. When the number of transfers is other than the above.

This setting can be used when the number of transfers is set to over the watermark level and the setting is not a multiple of the watermark level.

Use "Peripheral scatter-gather" as the transfer mode and combine the two tasks at DMA transfer.

For example, in the case of the number of transfers = (n × watermark) + m

Set Task A to the same as (a).

Disable single-transfer. Set the number of arbitration rates <R_power> for the control data to the watermark level of the FIFO. Set "watermark level × n" as the number of transfers.

Set Task B to the same as (b).

Enable single-transfer. Set "0000" to <R_power>. Set "m" as the number of transfers.

Example of setting

The peripheral circuit that performs DMA transfer.		SSO(reception)	
The number of DMA transfers to be set		15 times	
Watermark level		4 (Fixed to 4 for SSP communication)	
The DMA register setting		DMAxChnlUseburstSet<ch4>=1 : Disable single-transfer	
Channel control data setting (Alternative data)	Task A Use the same setting as (a).	<n_minus_1>=0x00B	The number of transfers 4 × 3 = 12 times
		<R_power>=0011	Arbitration is issued after four transfers are complete.
		<next_useburst>=0	Enables Task B to perform single-transfer
		<cycle_ctrl>=111	Peripheral scatter-gather mode
	Task B Use the same setting as (b).	<n_minus_1>=0x002	The number of transfers 15 - 12 = 3 times
		<R_power>=0000	Arbitration is issued after one transfer is complete.
		<cycle_ctrl>=001	The transfer ends in basic mode.

Introduction: Notes on the description of SFR (Special Function Register) under this specification

An SFR (Special Function Register) is a control register for periperal circuits (IP).

The SFR addressses of IPs are described in the chapter on memory map, and the details of SFR are given in the chapter of each IP.

Definition of SFR used in this specification is in accordance with the following rules.

a. SFR table of each IP as an example
   - SFR tables in each chapter of IP provides register names, addresses and brief descriptions.
   - All registers have a 32-bit unique address and the addresses of the registers are defined as follows, with some exceptions: "Base address + (Unique) address"

Base Address = 0x0000_0000

Register name		Address(Base+)
Control register	SAMCR	0x0004
		0x000C

Note: **SAMCR register address is 32 bits wide from the address 0x0000_0004 (Base Address(0x00000000) + unique address (0x0004)).**

Note: **The register shown above is an example for explanation purpose and not for demonstration purpose. This register does not exist in this microcontroller.**

b. SFR(register)
   - Each register basically consists of a 32-bit register (some exceptions).
   - The description of each register provides bits, bit symbols, types, initial values after reset and functions.

1.2.2 SAMCR(Control register)

	31	30	29	28	27	26	25	24
bit symbol	-	-	-	-	-	-	-	-
After reset	0	0	0	0	0	0	0	0
	23	22	21	20	19	18	17	16
bit symbol	-	-	-	-	-	-	-	-
After reset	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8
bit symbol	-	-	-	-	-	-	MODE	
After reset	0	0	0	0	0	0	0	0
	7	6	5	4	3	2	1	0
bit symbol	MODE	TDATA						
After reset	0	0	0	1	0	0	0	0

Bit	Bit Symbol	Type	Function
31-10	−	R	"0" can be read.
9-7	MODE[2:0]	R/W	Operation mode settings 000 : Sample mode 0 001 : Sample mode 1 010 : Sample mode 2 011 : Sample mode 3 The settings other than those above: Reserved
6-0	TDATA[6:0]	W	Transmitted data

Note: **The Type is divided into three as shown below.**

R / W	READ WRITE
R	READ
W	WRITE

c. Data descriptopn

Meanings of symbols used in the SFR description are as shown below.

- x:channel numbers/ports
- n,m:bit numbers

d. Register descriptoption

Registers are described as shown below.

- Register name <Bit Symbol>

  Exmaple: SAMCR<MODE>="000" or SAMCR<MODE[2:0]>="000"

  <MODE[2:0]> indicates bit 2 to bit 0 in bit symbol mode (3bit width).

- Register name [Bit]

  Example: SAMCR[9:7]="000"

  It indicates bit 9 to bit 7 of the register SAMCR (32 bit width).

Revision History

Date	Revision	Comment
2012/11/7	1	First Release
2013/10/22	2	Contents Revised

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