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XMC™ 1200 AB-Step

Microcontroller Series
for Industrial Applications

XMC™ 1000 Family

ARM® Cortex®-M0
32-bit processor core

Data Sheet

V1.7 2016-08

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Page	Subjects
many	Added XMC™ trademark
10 , 11 , 12	Added new marking variants XMC1201-T028F0016, XMC1201-T028F0032 and XMC1202-T016X0064
53	Flash Memory Parameters Table: <ul style="list-style-type: none">• Erase time per page parameter is renamed to Erase time per page / sector.• Erase cycles parameter is renamed to include test condition of sum of page and sector erase cycles.• Added parameter for fixed wait states configuration.

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About this Document

This Data Sheet is addressed to embedded hardware and software developers. It provides the reader with detailed descriptions about the ordering designations, available features, electrical and physical characteristics of the XMC1200 series devices.

The document describes the characteristics of a superset of the XMC1200 series devices. For simplicity, the various device types are referred to by the collective term XMC1200 throughout this document.

XMC™1000 Family User Documentation

The set of user documentation includes:

- **Reference Manual**
 - describes the functionality of the superset of devices.
- **Data Sheets**
 - list the complete ordering designations, available features and electrical characteristics of derivative devices.
- **Errata Sheets**
 - list deviations from the specifications given in the related Reference Manual or Data Sheets. Errata Sheets are provided for the superset of devices.

Attention: Please consult all parts of the documentation set to attain consolidated knowledge about your device.

Application related guidance is provided by **Users Guides** and **Application Notes**.

Please refer to <http://www.infineon.com/xmc1000> to get access to the latest versions of those documents.

1 Summary of Features

The XMC1200 devices are members of the XMC™1000 Family of microcontrollers based on the ARM Cortex-M0 processor core. The XMC1200 series devices are optimized for LED Lighting and Human-Machine interface (HMI) applications.

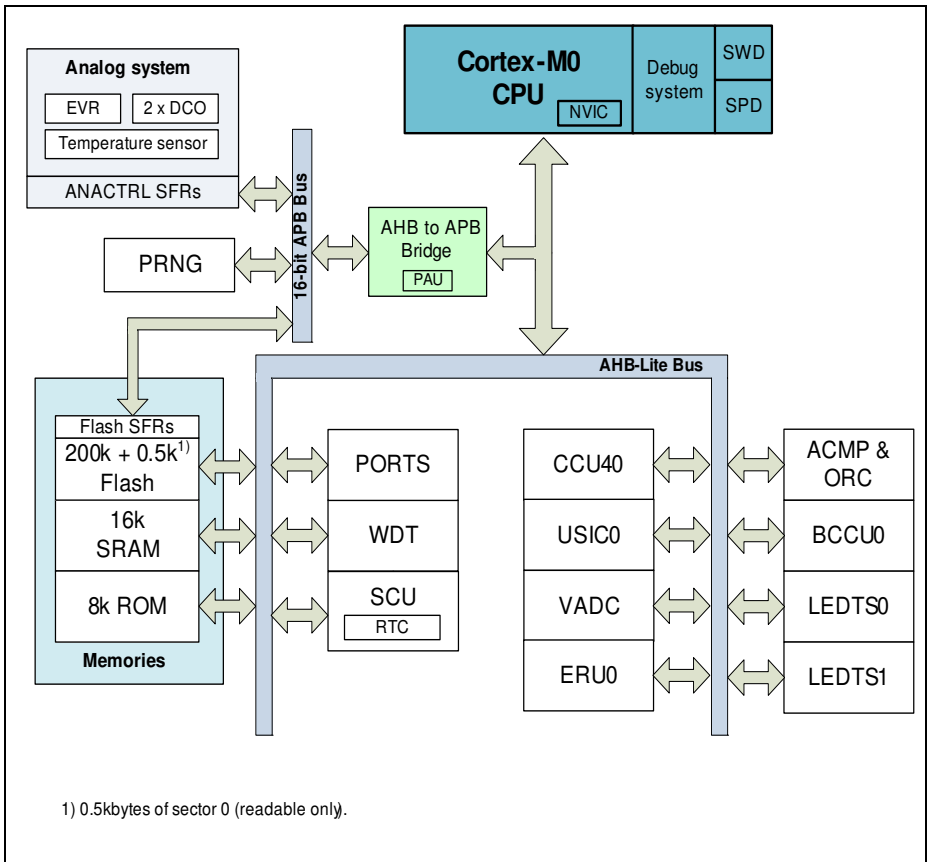


Figure 1 System Block Diagram

CPU Subsystem

- CPU Core
 - High-performance 32-bit ARM Cortex-M0 CPU
 - Most 16-bit Thumb and subset of 32-bit Thumb2 instruction set
 - Single cycle 32-bit hardware multiplier

Summary of Features

- System timer (SysTick) for Operating System support
- Ultra low power consumption
- Nested Vectored Interrupt Controller (NVIC)
- Event Request Unit (ERU) for processing of external and internal service requests

On-Chip Memories

- 8 kbytes on-chip ROM
- 16 kbytes on-chip high-speed SRAM
- up to 200 kbytes on-chip Flash program and data memory

Communication Peripherals

- Two Universal Serial Interface Channels (USIC), usable as UART, double-SPI, quad-SPI, IIC, IIS and LIN interfaces
- LED and Touch-Sense Controller (LEDTS) for Human-Machine interface

Analog Frontend Peripherals

- A/D Converters
 - up to 12 analog input pins
 - 2 sample and hold stages with 8 analog input channels each
 - fast 12-bit analog to digital converter with adjustable gain
- Up to 8 channels of out of range comparators (ORC)
- Up to 3 fast analog comparators (ACMP)
- Temperature Sensor (TSE)

Industrial Control Peripherals

- Capture/Compare Units 4 (CCU4) as general purpose timers
- Brightness and Colour Control Unit (BCCU), for LED color and dimming application

System Control

- Window Watchdog Timer (WDT) for safety sensitive applications
- Real Time Clock module with alarm support (RTC)
- System Control Unit (SCU) for system configuration and control
- Pseudo random number generator (PRNG) for fast random data generation

Input/Output Lines

- Programmable port driver control module (PORTS)
- Individual bit addressability
- Tri-stated in input mode
- Push/pull or open drain output mode
- Configurable pad hysteresis

On-Chip Debug Support

- Support for debug features: 4 breakpoints, 2 watchpoints
- Various interfaces: ARM serial wire debug (SWD), single pin debug (SPD)

1.1 Ordering Information

The ordering code for an Infineon microcontroller provides an exact reference to a specific product. The code "XMC1<DDD>-<Z><PPP><T><FFFF>" identifies:

- <DDD> the derivatives function set
- <Z> the package variant
 - T: TSSOP
 - Q: VQFN
- <PPP> package pin count
- <T> the temperature range:
 - F: -40°C to 85°C
 - X: -40°C to 105°C
- <FFFF> the Flash memory size.

For ordering codes for the XMC1200 please contact your sales representative or local distributor.

This document describes several derivatives of the XMC1200 series, some descriptions may not apply to a specific product. Please see [Table 1](#).

For simplicity the term **XMC1200** is used for all derivatives throughout this document.

1.2 Device Types

These device types are available and can be ordered through Infineon's direct and/or distribution channels.

Table 1 Synopsis of XMC1200 Device Types

Derivative	Package	Flash Kbytes	SRAM Kbytes
XMC1201-T028F0016	PG-TSSOP-28-16	16	16
XMC1201-T028F0032	PG-TSSOP-28-16	32	16
XMC1201-T038F0016	PG-TSSOP-38-9	16	16
XMC1201-T038F0032	PG-TSSOP-38-9	32	16
XMC1201-T038F0064	PG-TSSOP-38-9	64	16
XMC1201-T038F0128	PG-TSSOP-38-9	128	16
XMC1201-T038F0200	PG-TSSOP-38-9	200	16
XMC1200-T038F0200	PG-TSSOP-38-9	200	16

Summary of Features
Table 1 Synopsis of XMC1200 Device Types (cont'd)

Derivative	Package	Flash Kbytes	SRAM Kbytes
XMC1202-T028X0016	PG-TSSOP-28-16	16	16
XMC1202-T028X0032	PG-TSSOP-28-16	32	16
XMC1202-T028X0064	PG-TSSOP-28-16	64	16
XMC1202-T016X0016	PG-TSSOP-16-8	16	16
XMC1202-T016X0032	PG-TSSOP-16-8	32	16
XMC1202-T016X0064	PG-TSSOP-16-8	64	16
XMC1202-Q024X0016	PG-VQFN-24-19	16	16
XMC1202-Q024X0032	PG-VQFN-24-19	32	16
XMC1201-Q040F0016	PG-VQFN-40-13	16	16
XMC1201-Q040F0032	PG-VQFN-40-13	32	16
XMC1201-Q040F0064	PG-VQFN-40-13	64	16
XMC1201-Q040F0128	PG-VQFN-40-13	128	16
XMC1201-Q040F0200	PG-VQFN-40-13	200	16
XMC1202-Q040X0016	PG-VQFN-40-13	16	16
XMC1202-Q040X0032	PG-VQFN-40-13	32	16

1.3 Device Type Features

The following table lists the available features per device type.

Table 2 Features of XMC1200 Device Types¹⁾

Derivative	ADC channel	ACMP	BCCU	LEDTS
XMC1200-T038	16	3	1	2
XMC1201-T028	14	-	-	2
XMC1201-T038	16	-	-	2
XMC1202-T028	14	3	1	-
XMC1202-T016	11	2	1	-
XMC1202-Q024	13	3	1	-
XMC1201-Q040	16	-	-	2
XMC1202-Q040	16	3	1	-

1) Features that are not included in this table are available in all the derivatives

Table 3 ADC Channels ¹⁾

Package	VADC0 G0	VADC0 G1
PG-TSSOP-16	CH0..CH5	CH0..CH4
PG-TSSOP-28	CH0..CH7	CH0 .. CH4, CH7
PG-TSSOP-38	CH0..CH7	CH0..CH7
PG-VQFN-24	CH0..CH7	CH0..CH4
PG-VQFN-40	CH0..CH7	CH1, CH5 .. CH7

1) Some pins in a package may be connected to more than one channel. For the detailed mapping see the Port I/O Function table.

1.4 Chip Identification Number

The Chip Identification Number allows software to identify the marking. It is a 8 words value with the most significant 7 words stored in Flash configuration sector 0 (CS0) at address location : 1000 0F00_H (MSB) - 1000 0F1B_H (LSB). The least significant word and most significant word of the Chip Identification Number are the value of registers DBGROMID and IDCHIP, respectively.

Table 4 XMC1200 Chip Identification Number

Derivative	Value	Marking
XMC1201-T028F0016	00012022 01CF00FF 00001FF7 00006000 00000C00 00001000 00005000 201ED083 _H	AB
XMC1201-T028F0032	00012022 01CF00FF 00001FF7 00006000 00000C00 00001000 00009000 201ED083 _H	AB
XMC1201-T038F0016	00012012 01CF00FF 00001FF7 00006000 00000C00 00001000 00005000 201ED083 _H	AB
XMC1201-T038F0032	00012012 01CF00FF 00001FF7 00006000 00000C00 00001000 00009000 201ED083 _H	AB
XMC1201-T038F0064	00012012 01CF00FF 00001FF7 00006000 00000C00 00001000 00011000 201ED083 _H	AB
XMC1201-T038F0128	00012012 01CF00FF 00001FF7 00006000 00000C00 00001000 00021000 201ED083 _H	AB
XMC1201-T038F0200	00012012 01CF00FF 00001FF7 00006000 00000C00 00001000 00033000 201ED083 _H	AB
XMC1200-T038F0200	00012012 01CF00FF 00001FF7 0000E000 00000C00 00001000 00033000 201ED083 _H	AB

Summary of Features

Table 4 XMC1200 Chip Identification Number (cont'd)

Derivative	Value	Marking
XMC1202-T028X0016	00012023 01CF00FF 00001FF7 00008000 00000C00 00001000 00005000 201ED083 _H	AB
XMC1202-T028X0032	00012023 01CF00FF 00001FF7 00008000 00000C00 00001000 00009000 201ED083 _H	AB
XMC1202-T028X0064	00012023 01CF00FF 00001FF7 00008000 00000C00 00001000 00011000 201ED083 _H	AB
XMC1202-T016X0016	00012033 01CF00FF 00001FF7 00008000 00000C00 00001000 00005000 201ED083 _H	AB
XMC1202-T016X0032	00012033 01CF00FF 00001FF7 00008000 00000C00 00001000 00009000 201ED083 _H	AB
XMC1202-T016X0064	00012033 01CF00FF 00001FF7 00008000 00000C00 00001000 00011000 201ED083 _H	AB
XMC1202-Q024X0016	00012063 01CF00FF 00001FF7 00008000 00000C00 00001000 00005000 201ED083 _H	AB
XMC1202-Q024X0032	00012063 01CF00FF 00001FF7 00008000 00000C00 00001000 00009000 201ED083 _H	AB
XMC1201-Q040F0016	00012042 01CF00FF 00001FF7 00006000 00000C00 00001000 00005000 201ED083 _H	AB
XMC1201-Q040F0032	00012042 01CF00FF 00001FF7 00006000 00000C00 00001000 00009000 201ED083 _H	AB
XMC1201-Q040F0064	00012042 01CF00FF 00001FF7 00006000 00000C00 00001000 00011000 201ED083 _H	AB
XMC1201-Q040F0128	00012042 01CF00FF 00001FF7 00006000 00000C00 00001000 00021000 201ED083 _H	AB
XMC1201-Q040F0200	00012042 01CF00FF 00001FF7 00006000 00000C00 00001000 00033000 201ED083 _H	AB
XMC1202-Q040X0016	00012043 01CF00FF 00001FF7 00008000 00000C00 00001000 00005000 201ED083 _H	AB
XMC1202-Q040X0032	00012043 01CF00FF 00001FF7 00008000 00000C00 00001000 00009000 201ED083 _H	AB

2 General Device Information

This section summarizes the logic symbols and package pin configurations with a detailed list of the functional I/O mapping.

2.1 Logic Symbols

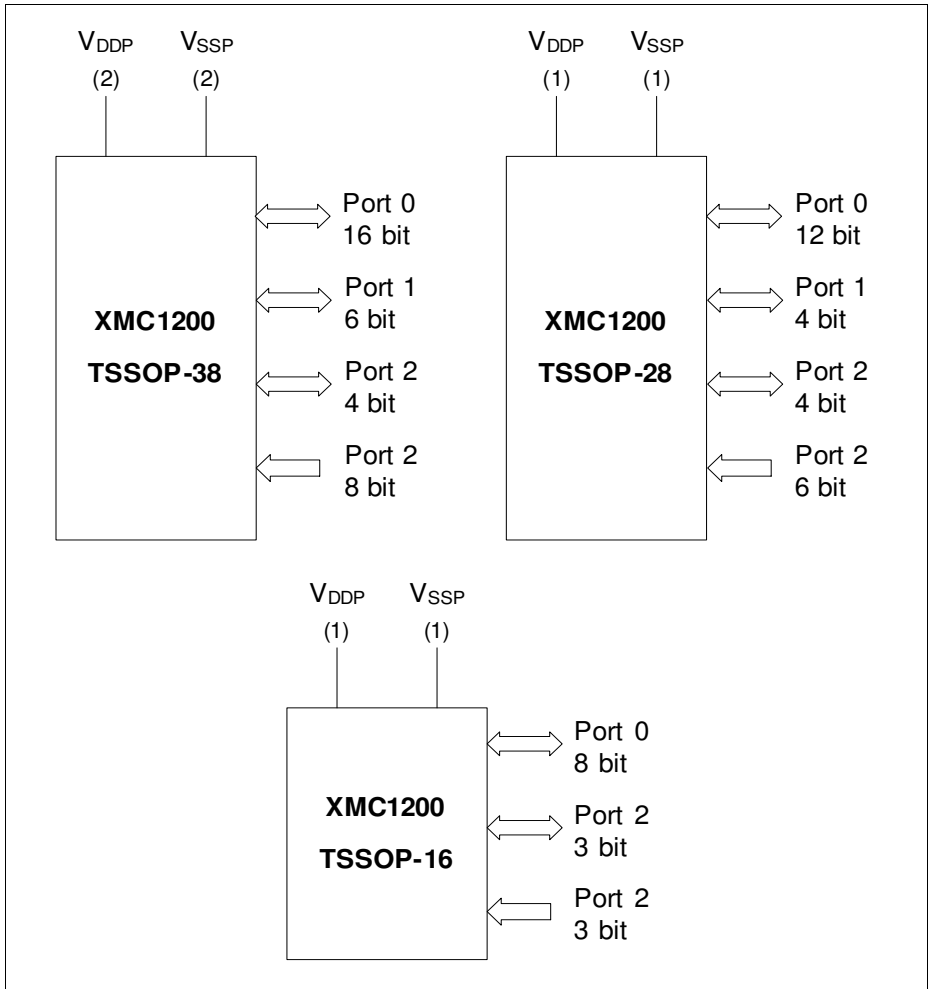


Figure 2 XMC1200 Logic Symbol for TSSOP-38, TSSOP-28 and TSSOP-16

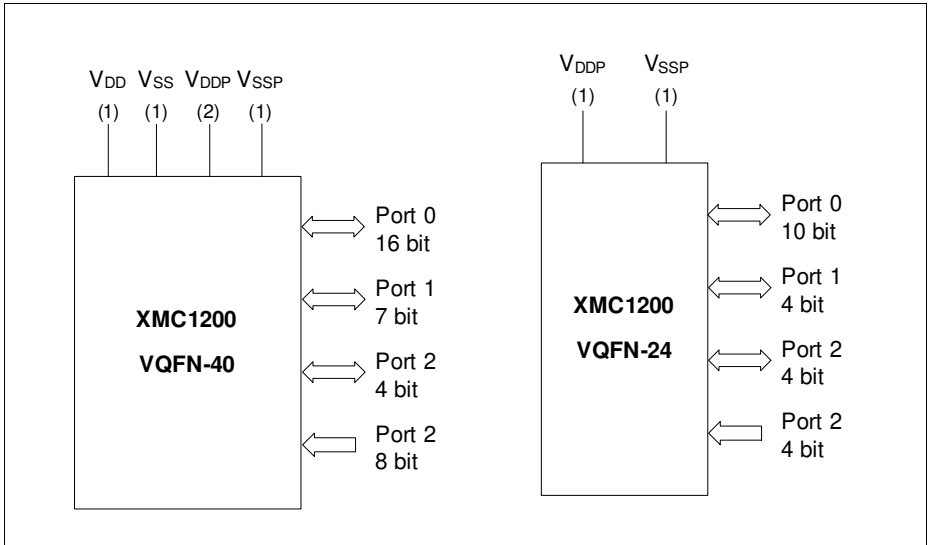


Figure 3 XMC1200 Logic Symbol for VQFN-24 and VQFN-40

2.2 Pin Configuration and Definition

The following figures summarize all pins, showing their locations on the different packages.

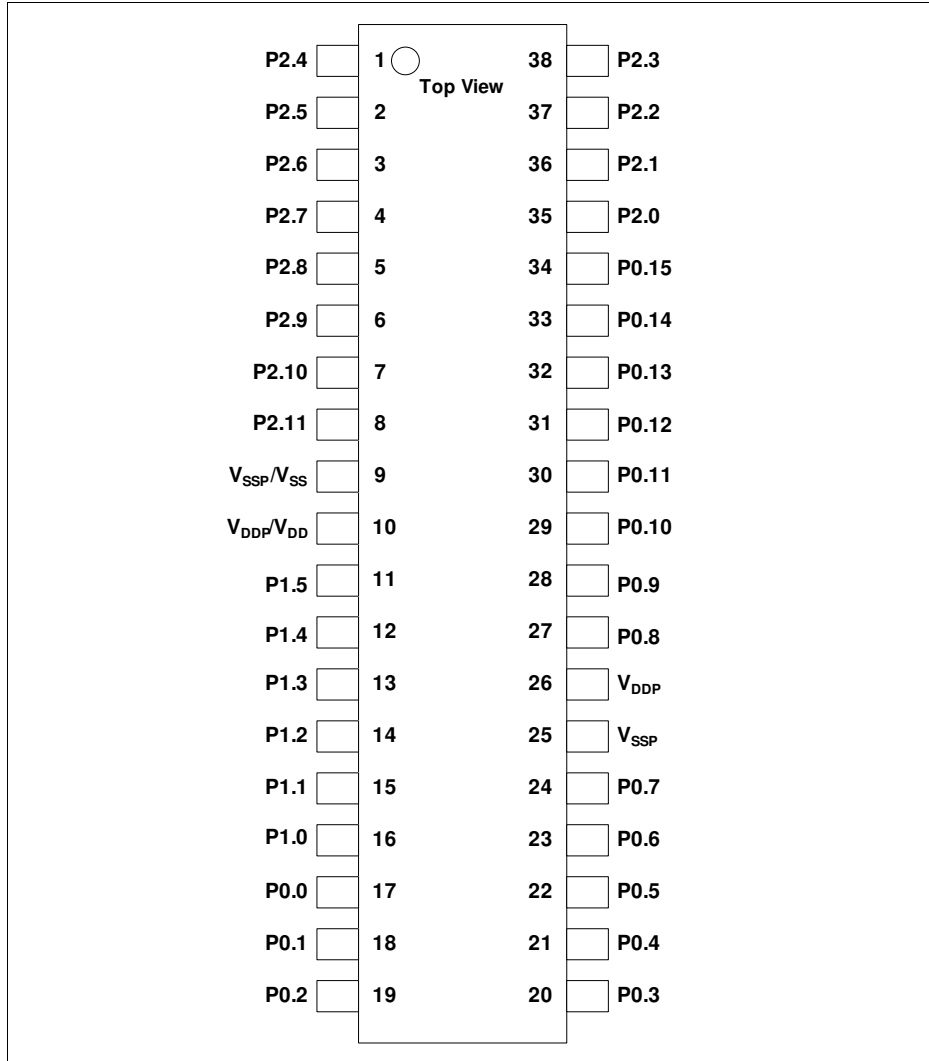


Figure 4 XMC1200 PG-TSSOP-38 Pin Configuration (top view)

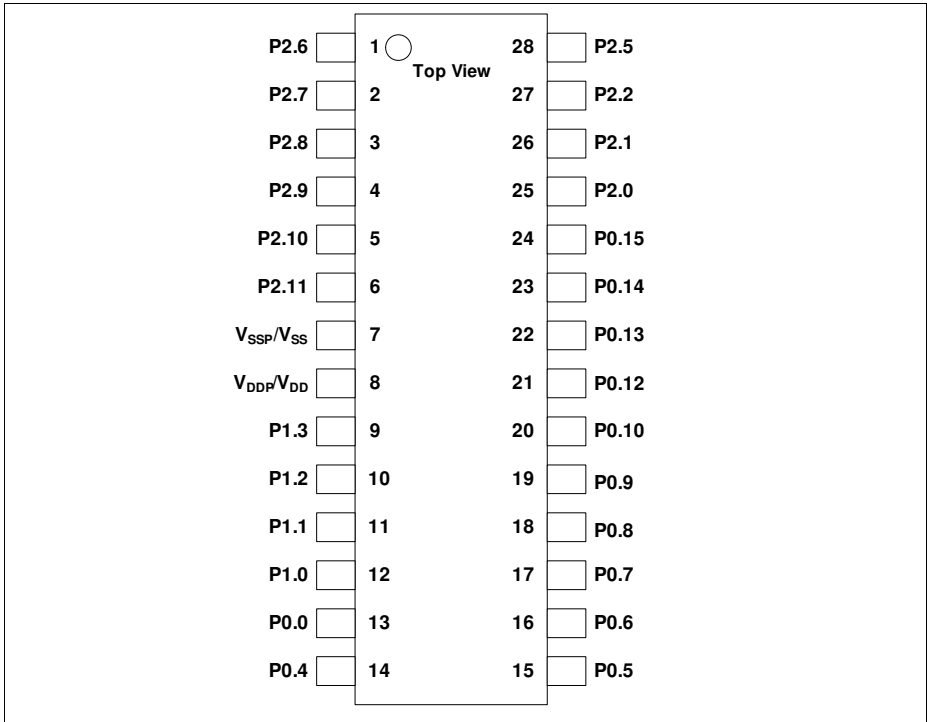


Figure 5 XMC1200 PG-TSSOP-28 Pin Configuration (top view)

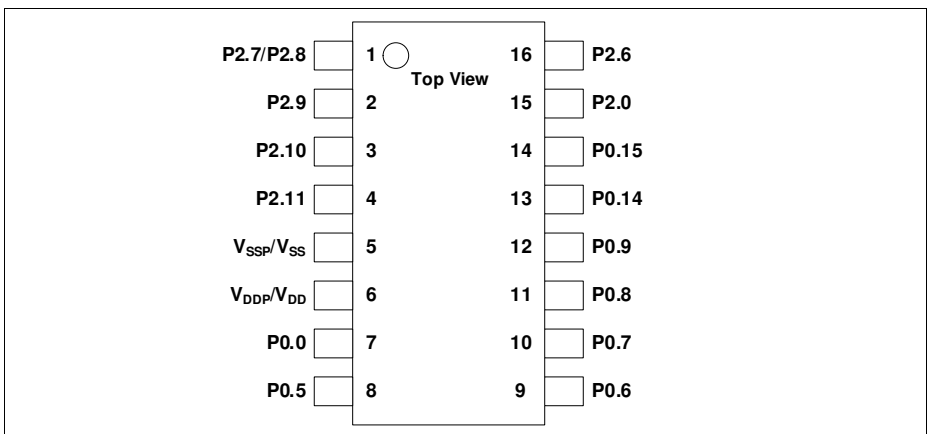


Figure 6 XMC1200 PG-TSSOP-16 Pin Configuration (top view)

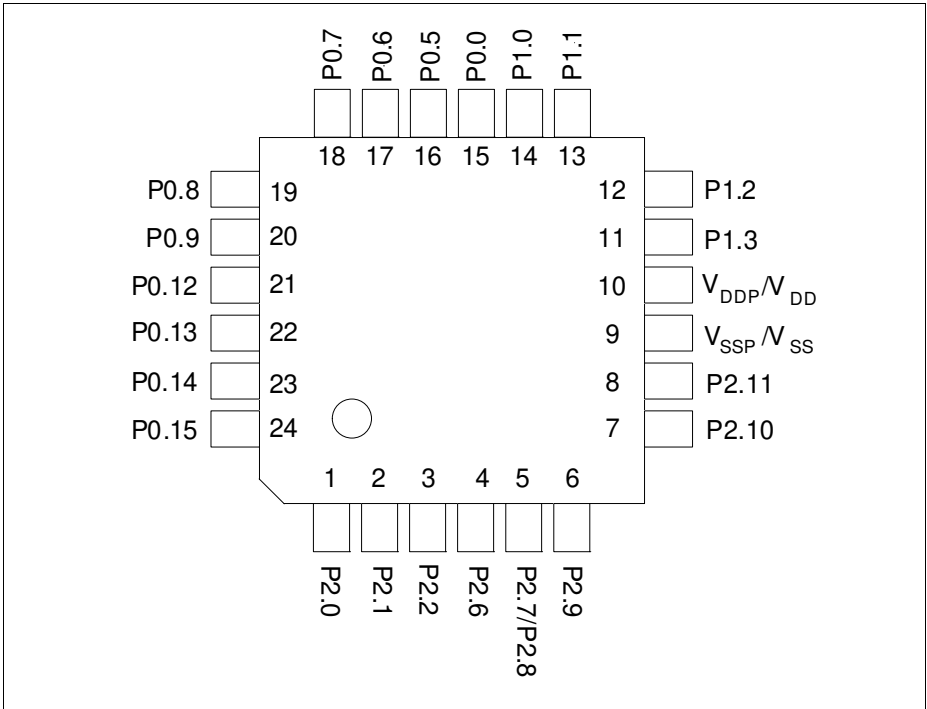


Figure 7 XMC1200 PG-VQFN-24 Pin Configuration (top view)

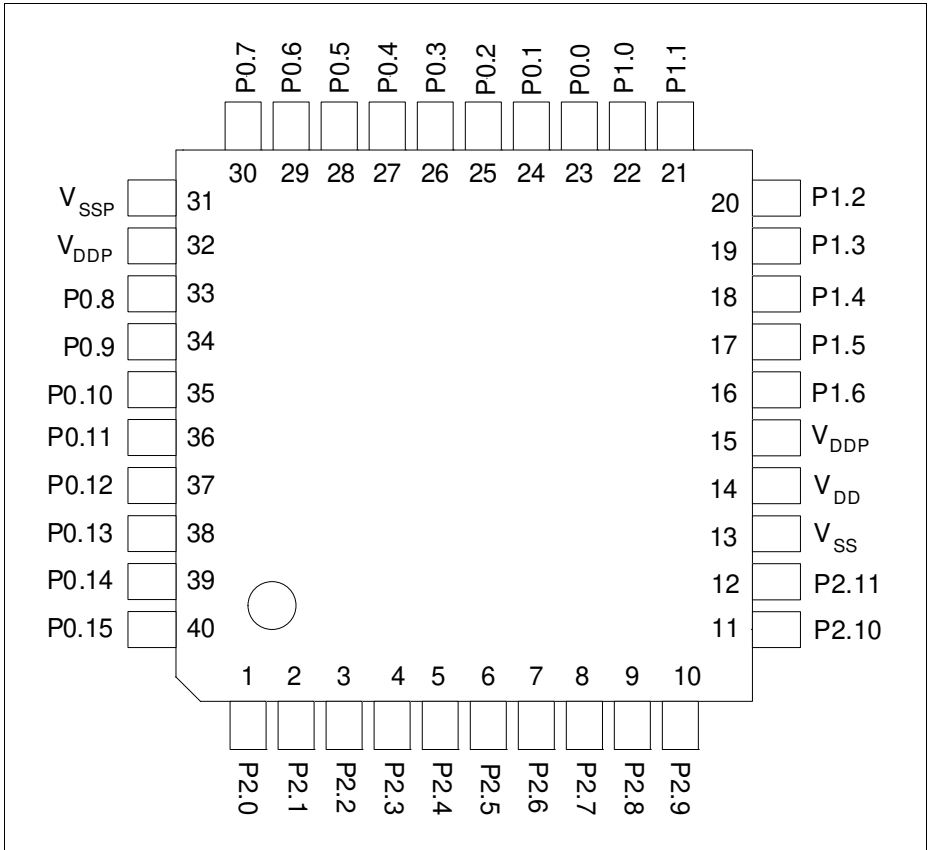


Figure 8 XMC1200 PG-VQFN-40 Pin Configuration (top view)

2.2.1 Package Pin Summary

The following general building block is used to describe each pin:

Table 5 Package Pin Mapping Description

Function	Package A	Package B	...	Pad Type
Px.y	N	N		Pad Class

The table is sorted by the “Function” column, starting with the regular Port pins (Px.y), followed by the supply pins.

The following columns, titled with the supported package variants, lists the package pin number to which the respective function is mapped in that package.

The “Pad Type” indicates the employed pad type:

- STD_INOUT (standard bi-directional pads)
- STD_INOUT/AN (standard bi-directional pads with analog input)
- High Current (high current bi-directional pads)
- STD_IN/AN (standard input pads with analog input)
- Power (power supply)

Details about the pad properties are defined in the Electrical Parameters.

Table 6 Package Pin Mapping

Function	VQFN 40	TSSOP 38	TSSOP 28	VQFN 24	TSSOP 16	Pad Type	Notes
P0.0	23	17	13	15	7	STD_INOUT	
P0.1	24	18	-	-	-	STD_INOUT	
P0.2	25	19	-	-	-	STD_INOUT	
P0.3	26	20	-	-	-	STD_INOUT	
P0.4	27	21	14	-	-	STD_INOUT	
P0.5	28	22	15	16	8	STD_INOUT	
P0.6	29	23	16	17	9	STD_INOUT	

General Device Information
Table 6 Package Pin Mapping (cont'd)

Function	VQFN 40	TSSOP 38	TSSOP 28	VQFN 24	TSSOP 16	Pad Type	Notes
P0.7	30	24	17	18	10	STD_INO UT	
P0.8	33	27	18	19	11	STD_INO UT	
P0.9	34	28	19	20	12	STD_INO UT	
P0.10	35	29	20	-	-	STD_INO UT	
P0.11	36	30	-	-	-	STD_INO UT	
P0.12	37	31	21	21	-	STD_INO UT	
P0.13	38	32	22	22	-	STD_INO UT	
P0.14	39	33	23	23	13	STD_INO UT	
P0.15	40	34	24	24	14	STD_INO UT	
P1.0	22	16	12	14	-	High Current	
P1.1	21	15	11	13	-	High Current	
P1.2	20	14	10	12	-	High Current	
P1.3	19	13	9	11	-	High Current	
P1.4	18	12	-	-	-	High Current	
P1.5	17	11	-	-	-	High Current	
P1.6	16	-	-	-	-	STD_INO UT	
P2.0	1	35	25	1	15	STD_INO UT/AN	

General Device Information
Table 6 Package Pin Mapping (cont'd)

Function	VQFN 40	TSSOP 38	TSSOP 28	VQFN 24	TSSOP 16	Pad Type	Notes
P2.1	2	36	26	2	-	STD_INO UT/AN	
P2.2	3	37	27	3	-	STD_IN/A N	
P2.3	4	38	-	-	-	STD_IN/A N	
P2.4	5	1	-	-	-	STD_IN/A N	
P2.5	6	2	28	-	-	STD_IN/A N	
P2.6	7	3	1	4	16	STD_IN/A N	
P2.7	8	4	2	5	1	STD_IN/A N	
P2.8	9	5	3	5	1	STD_IN/A N	
P2.9	10	6	4	6	2	STD_IN/A N	
P2.10	11	7	5	7	3	STD_INO UT/AN	
P2.11	12	8	6	8	4	STD_INO UT/AN	
VSS	13	9	7	9	5	Power	Supply GND, ADC reference GND
VDD	14	10	8	10	6	Power	Supply VDD, ADC reference voltage/ ORC reference voltage
VDDP	15	10	8	10	6	Power	When VDD is supplied, VDDP has to be supplied with the same voltage.

General Device Information

Table 6 Package Pin Mapping (cont'd)

Function	VQFN 40	TSSOP 38	TSSOP 28	VQFN 24	TSSOP 16	Pad Type	Notes
VSSP	31	25	-	-	-	Power	I/O port ground
VDDP	32	26	-	-	-	Power	I/O port supply
VSSP	Exp. Pad	-	-	Exp. Pad	-	Power	Exposed Die Pad The exposed die pad is connected internally to VSSP. For proper operation, it is mandatory to connect the exposed pad to the board ground. For thermal aspects, please refer to the Package and Reliability chapter.

2.2.2 Port I/O Functions

The following general building block is used to describe each PORT pin:

Table 7 Port I/O Function Description

Function	Outputs		Inputs	
	ALT1	ALTn	Input	Input
P0.0		MODA.OUT	MODC.INA	
Pn.y	MODA.OUT		MODA.INA	MODC.INB

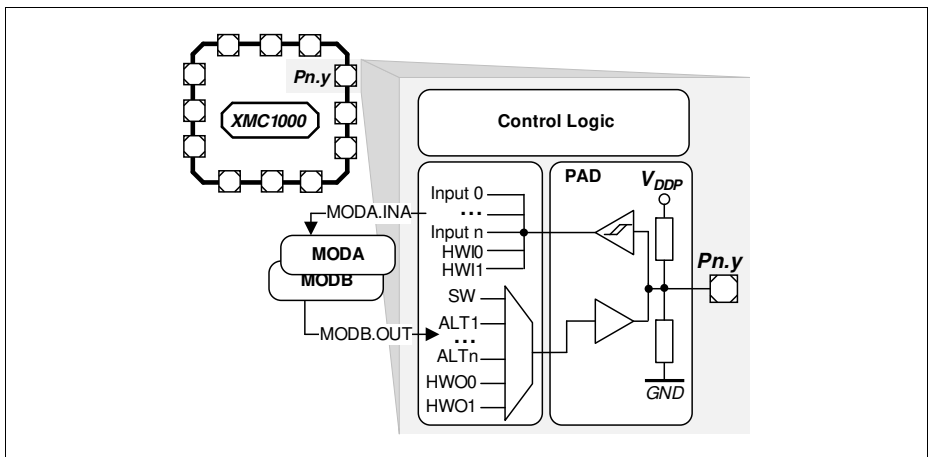


Figure 9 Simplified Port Structure

Pn.y is the port pin name, defining the control and data bits/registers associated with it. As GPIO, the port is under software control. Its input value is read via Pn_IN.y, Pn_OUT defines the output value.

Up to seven alternate output functions (ALT1/2/3/4/5/6/7) can be mapped to a single port pin, selected by Pn_IOCR.PC. The output value is directly driven by the respective module, with the pin characteristics controlled by the port registers (within the limits of the connected pad).

The port pin input can be connected to multiple peripherals. Most peripherals have an input multiplexer to select between different possible input sources.

The input path is also active while the pin is configured as output. This allows to feedback an output to on-chip resources without wasting an additional external pin.

Please refer to the [Port I/O Functions](#) table for the complete Port I/O function mapping.

2.2.3 Hardware Controlled I/O Function Description

The following general building block is used to describe the hardware I/O and pull control functions of each PORT pin:

Table 8 Hardware Controlled I/O Function Description

Function	Outputs	Inputs	Pull Control	
	HWO0	HWI0	HW0_PD	HW0_PU
P0.0	MODB.OUT	MODB.INA		
Pn.y			MODC.OUT	MODC.OUT

By Pn_HWSEL, it is possible to select between different hardware “masters” (HWO0/HWI0, HWO1/HWI1). The selected peripheral can take control of the pin(s). Hardware control overrules settings in the respective port pin registers. Additional hardware signals HW0_PD/HW1_PD and HW0_PU/HW1_PU controlled by the peripherals can be used to control the pull devices of the pin.

Please refer to the [Hardware Controlled I/O Functions](#) table for the complete hardware I/O and pull control function mapping.