Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

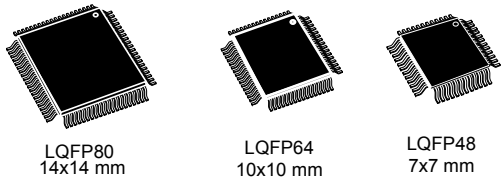
STM8AL31E8x STM8AL3LE8x

Automotive 8-bit ultra-low-power MCU, 64 KB Flash, EEPROM, RTC, AES, LCD, timers, USARTs, I2C, SPIs, ADC, DAC, COMPs

Datasheet - production data

Features

- AEC-Q100 grade 1 qualified
- Operating conditions
  - Operating power supply range 1.8 V to 3.6 V (down to 1.65 V at power down)
  - Temp. range: -40 to 85 or 125 °C
- Low-power features
  - 5 low-power modes: Wait, Low-power run (5.9 µA), Low-power wait (3 µA), Active-halt with full RTC (1.4 µA), Halt (400 nA)
  - Consumption: 200 µA/MHz+330 µA
  - Fast wake up from Halt mode (4.7 µs)
  - Ultra-low leakage per I/0: 50 nA
- Advanced STM8 core
  - Harvard architecture and 3-stage pipeline
  - Max freq: 16 MHz, 16 CISC MIPS peak
  - Up to 40 external interrupt sources
- Reset and supply management
  - Low power, ultra safe BOR reset with 5 programmable thresholds
  - Ultra-low-power POR/PDR
  - Programmable voltage detector (PVD)
- Clock management
  - 32 kHz and 1-16 MHz crystal oscillators
  - Internal 16 MHz factory-trimmed RC and 38 kHz low consumption RC
  - Clock security system
- Low-power RTC
  - BCD calendar with alarm interrupt,
  - Digital calibration with +/- 0.5ppm accuracy
  - Advanced anti-tamper detection
- DMA
  - 4 ch. for ADC, encryption hardware accelerator (AES), DACs, SPIs, I^{2}C, USARTs, Timers, 1 ch. for memory-to-memory
- LCD: 8x40 or 4x44 w/ step-up converter



- 12-bit ADC up to 1 Msps / 28 channels,
  - Temp. sensor and internal ref. voltage
- Memories
  - Up to 64 Kbytes of Flash with up to 2 Kbytes of data EEPROM with ECC and RWW
  - Flexible write/read protection modes
  - Up to 4 Kbytes of RAM
- 2x12-bit DAC (dual mode) with output buffer
- 2 ultra-low-power comparators
  - 1 with fixed threshold and 1 rail to rail
  - Wakeup capability
- Timers
  - Three 16-bit timers with 2 channels (IC, OC, PWM), quadrature encoder
  - One 16-bit advanced control timer with 3 channels, supporting motor control
  - One 8-bit timer with 7-bit prescaler
  - One window and one independent watchdog
  - Beeper timer with 1, 2 or 4 kHz frequencies
- Communication interfaces
  - Two synchronous serial interface (SPI)
  - Fast I^{2}C 400 kHz SMBus and PMBus
  - Three USARTs (IrDA, LIN 1.3, LIN2.0)
- Up to 67 I/Os, all mappable on interrupt vectors
- Fast on-chip programming and non-intrusive debugging with SWIM, Bootloader using USART
- 96-bit unique ID

This is information on a product in full production. www.st.com

Table 1. Device summary

Reference	Part number
STM8AL31E8x	STM8AL31E88, STM8AL31E89, STM8AL31E8A
STM8AL3LE8x	STM8AL3LE88, STM8AL3LE89, STM8AL3LE8A

Contents

1 Introduction 10

2 Description 11

2.1 STM8AL ultra-low-power 8-bit family benefits 11

2.2 Device overview 13

3 Functional overview 14

3.1 Low-power modes 15

3.2 Central processing unit STM8 16

3.2.1 Advanced STM8 Core 16

3.2.2 Interrupt controller 16

3.3 Reset and supply management 17

3.3.1 Power supply scheme 17

3.3.2 Power supply supervisor 17

3.3.3 Voltage regulator 18

3.4 Clock management 18

3.5 Low-power real-time clock 19

3.6 LCD (Liquid crystal display) 20

3.7 Memories 20

3.8 DMA 20

3.9 Analog-to-digital converter 21

3.10 Digital-to-analog converter 21

3.11 Ultra-low-power comparators 21

3.12 System configuration controller and routing interface 22

3.13 AES 22

3.14 Timers 22

3.14.1 16-bit advanced control timer (TIM1) 23

3.14.2 16-bit general purpose timers (TIM2, TIM3, TIM5) 23

3.14.3 8-bit basic timer (TIM4) 23

3.15 Watchdog timers 23

3.15.1 Window watchdog timer 23

3.15.2 Independent watchdog timer 23

3.16 Beeper 24
3.17 Communication interfaces 24
3.17.1 SPI 24
3.17.2 I^2C 24
3.17.3 USART 25
3.18 Infrared (IR) interface 25
3.19 Development support 25

4 Pin description 27

5 Memory and register map 39
5.1 Memory mapping 39
5.2 Register map 40

6 Interrupt vector mapping 60

7 Option byte 62

8 Unique ID 65

9 Electrical parameters 66
9.1 Parameter conditions 66
9.1.1 Minimum and maximum values 66
9.1.2 Typical values 66
9.1.3 Typical curves 66
9.1.4 Loading capacitor 66
9.1.5 Pin input voltage 67
9.2 Absolute maximum ratings 67
9.3 Operating conditions 69
9.3.1 General operating conditions 69
9.3.2 Embedded reset and power control block characteristics 70
9.3.3 Supply current characteristics 72
9.3.4 Clock and timing characteristics 85
9.3.5 Memory characteristics 90
9.3.6 I/O current injection characteristics 92
9.3.7 I/O port pin characteristics 92
9.3.8 Communication interfaces 100

9.3.9 LCD controller (STM8AL3LE8x only) 105
9.3.10 Embedded reference voltage 106
9.3.11 Temperature sensor 107
9.3.12 Comparator characteristics 107
9.3.13 12-bit DAC characteristics 109
9.3.14 12-bit ADC1 characteristics 112
9.3.15 EMC characteristics 117
9.4 Thermal characteristics 119

10 Package information 120
10.1 LQFP80 package information 120
10.2 LQFP64 package information 124
10.3 LQFP48 package information 127

11 Ordering information 131

12 Revision history 132

List of tables

Table 1. Device summary . . . 2
Table 2. High-density STM8AL3xE8x low-power device features and peripheral counts . . . 13
Table 3. Timer feature comparison . . . 22
Table 4. Legend/abbreviation . . . 30
Table 5. High-density STM8AL3xE8x pin description . . . 30
Table 6. Flash and RAM boundary addresses . . . 40
Table 7. Factory conversion registers . . . 40
Table 8. I/O port hardware register map . . . 40
Table 9. General hardware register map . . . 42
Table 10. CPU/SWIM/debug module/interrupt controller registers . . . 58
Table 11. Interrupt mapping . . . 60
Table 12. Option byte addresses . . . 62
Table 13. Option byte description . . . 63
Table 14. Unique ID registers (96 bits) . . . 65
Table 15. Voltage characteristics . . . 67
Table 16. Current characteristics . . . 68
Table 17. Thermal characteristics . . . 68
Table 18. Operating lifetime (OLF) . . . 68
Table 19. General operating conditions . . . 69
Table 20. Embedded reset and power control block characteristics . . . 70
Table 21. Total current consumption in Run mode . . . 72
Table 22. Total current consumption in Wait mode . . . 75
Table 23. Total current consumption and timing in low-power run mode at VDD = 1.65 V to 3.6 V . . . 77
Table 24. Total current consumption in low-power wait mode at VDD = 1.65 V to 3.6 V . . . 78
Table 25. Total current consumption and timing in Active-halt mode at VDD = 1.65 V to 3.6 V . . . 79
Table 26. Typical current consumption in Active-halt mode, RTC clocked by LSE external crystal . . . 80
Table 27. Total current consumption and timing in Halt mode at VDD = 1.65 to 3.6 V . . . 82
Table 28. Peripheral current consumption . . . 83
Table 29. Current consumption under external reset . . . 85
Table 30. HSE external clock characteristics . . . 85
Table 31. LSE external clock characteristics . . . 86
Table 32. HSE oscillator characteristics . . . 86
Table 33. LSE oscillator characteristics . . . 88
Table 34. HSI oscillator characteristics . . . 89
Table 35. LSI oscillator characteristics . . . 90
Table 36. RAM and hardware registers . . . 90
Table 37. Flash program memory/data EEPROM memory . . . 91
Table 38. Flash program memory . . . 91
Table 39. Data memory . . . 91
Table 40. I/O current injection susceptibility . . . 92
Table 41. I/O static characteristics . . . 93
Table 42. Output driving current (high sink ports) . . . 96
Table 43. Output driving current (true open drain ports) . . . 96
Table 44. Output driving current (PA0 with high sink LED driver capability) . . . 96
Table 45. NRST pin characteristics . . . 98
Table 46. SPI1 characteristics . . . 100

Table 47. I2C characteristics . . . 103
Table 48. LCD characteristics . . . 105
Table 49. Reference voltage characteristics . . . 106
Table 50. TS characteristics . . . 107
Table 51. Comparator 1 characteristics . . . 107
Table 52. Comparator 2 characteristics . . . 108
Table 53. DAC characteristics . . . 109
Table 54. DAC accuracy . . . 110
Table 55. DAC output on PB4-PB5-PB6 . . . 111
Table 56. ADC1 characteristics . . . 112
Table 57. ADC1 accuracy with VDDA = 3.3 V to 2.5 V . . . 114
Table 58. ADC1 accuracy with VDDA = 2.4 V to 3.6 V . . . 114
Table 59. ADC1 accuracy with VDDA = VREF+ = 1.8 V to 2.4 V . . . 114
Table 60. EMS data . . . 117
Table 61. EMI data . . . 118
Table 62. ESD absolute maximum ratings . . . 118
Table 63. Electrical sensitivities . . . 119
Table 64. Thermal characteristics . . . 119
Table 65. LQFP80 - 80-pin, 14 x 14 mm low-profile quad flat package mechanical data . . . 121
Table 66. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data . . . 124
Table 67. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data . . . 128
Table 68. STM8AL31E8x STM8AL3LE8x ordering information scheme . . . 131
Table 69. Document revision history . . . 132

List of figures

Figure 1. High-density STM8AL3xE8x device block diagram . . . 14
Figure 2. Clock tree diagram . . . 19
Figure 3. STM8AL31E8A 80-pin package pinout (without LCD) . . . 27
Figure 4. STM8AL3LE8A 80-pin package pinout (with LCD) . . . 27
Figure 5. STM8AL31E89 64-pin pinout (without LCD) . . . 28
Figure 6. STM8AL3LE89 64-pin pinout (with LCD) . . . 28
Figure 7. STM8AL31E88 48-pin pinout (without LCD) . . . 29
Figure 8. STM8AL3LE88 48-pin pinout (with LCD) . . . 29
Figure 9. Memory map . . . 39
Figure 10. Pin loading conditions . . . 66
Figure 11. Pin input voltage . . . 67
Figure 12. Power supply thresholds . . . 71
Figure 13. Typical $I_{DD(RUN)}$ from RAM vs. V_{DD} (HSI clock source), f_{CPU} =16 MHz(1) . . . 73
Figure 14. Typical $I_{DD(RUN)}$ from Flash vs. V_{DD} (HSI clock source), f_{CPU} = 16 MHz(1) . . . 74
Figure 15. Typical $I_{DD(Wait)}$ from RAM vs. V_{DD} (HSI clock source), f_{CPU} = 16 MHz(1) . . . 76
Figure 16. Typical $I_{DD(Wait)}$ from Flash (HSI clock source), f_{CPU} = 16 MHz(1) . . . 76
Figure 17. Typical $I_{DD(LPR)}$ vs. V_{DD} (LSI clock source), all peripherals OFF . . . 77
Figure 18. Typical $I_{DD(LPW)}$ vs. V_{DD} (LSI clock source), all peripherals OFF(1) . . . 78
Figure 19. Typical IDD(AH) vs. V_{DD} (LSI clock source) . . . 81
Figure 20. Typical IDD(Halt) vs. V_{DD} (internal reference voltage OFF) . . . 82
Figure 21. HSE oscillator circuit diagram . . . 87
Figure 22. LSE oscillator circuit diagram . . . 88
Figure 23. Typical HSI frequency vs. V_{DD} . . . 89
Figure 24. Typical LSI clock source frequency vs. VDD . . . 90
Figure 25. Typical VIL and VIH vs. VDD (standard I/Os) . . . 94
Figure 26. Typical VIL and VIH vs. VDD (true open drain I/Os) . . . 94
Figure 27. Typical pull-up resistance R_{PU} vs. V_{DD} with VIN=VSS . . . 95
Figure 28. Typical pull-up current I_{pu} vs. V_{DD} with VIN=VSS . . . 95
Figure 29. Typical VOL @ VDD = 3.0 V (high sink ports) . . . 97
Figure 30. Typical VOL @ VDD = 1.8 V (high sink ports) . . . 97
Figure 31. Typical VOL @ VDD = 3.0 V (true open drain ports) . . . 97
Figure 32. Typical VOL @ VDD = 1.8 V (true open drain ports) . . . 97
Figure 33. Typical VDD - VOH @ VDD = 3.0 V (high sink ports) . . . 97
Figure 34. Typical VDD - VOH @ VDD = 1.8 V (high sink ports) . . . 97
Figure 35. Typical NRST pull-up resistance R_{PU} vs. V_{DD} . . . 98
Figure 36. Typical NRST pull-up current I_{pu} vs. V_{DD} . . . 99
Figure 37. Recommended NRST pin configuration . . . 99
Figure 38. SPI1 timing diagram - slave mode and CPHA=0 . . . 101
Figure 39. SPI1 timing diagram - slave mode and CPHA=1(1) . . . 101
Figure 40. SPI1 timing diagram - master mode(1) . . . 102
Figure 41. Typical application with I2C bus and timing diagram(1)) . . . 104
Figure 42. ADC1 accuracy characteristics . . . 115
Figure 43. Typical connection diagram using the ADC . . . 115
Figure 44. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA}) . . . 116
Figure 45. Power supply and reference decoupling (VREF+ connected to VDDA) . . . 116
Figure 46. LQFP80 - 80-pin, 14 x 14 mm low-profile quad flat package outline . . . 120
Figure 47. LQFP80 - 80-pin, 14 x 14 mm low-profile quad flat package recommended footprint . . . 122

Figure 48. LQFP80 marking example (package top view) . . . 123
Figure 49. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package outline . . . 124
Figure 50. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package recommended footprint . . . 125
Figure 51. LQFP64 marking example (package top view) . . . 126
Figure 52. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline . . . 127
Figure 53. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package recommended footprint . . . 129
Figure 54. LQFP48 marking example (package top view) . . . 130

1 Introduction

This document describes the features, pinout, mechanical data and ordering information of the high-density STM8AL31E8x and STM8AL3LE8x devices (microcontrollers with 64 Kbyte Flash memory density). These devices are referred to as high-density devices in STM8L051/L052 Value Line, STM8L151/L152, STM8L162, STM8AL31, STM8AL3L MCU lines reference manual (RM0031) and in the STM8L and STM8AL Flash programming manual (PM0054).

For more details on the whole STMicroelectronics ultra-low-power family please refer to *Section 3: Functional overview on page 14*.

For information on the debug module and SWIM (single wire interface module), refer to the *STM8 SWIM communication protocol and debug module user manual* (UM0470).

For information on the STM8 core, please refer to the *STM8 CPU programming manual* (PM0044).

2 Description

The high-density STM8AL3xE8x ultra-low-power devices feature an enhanced STM8 CPU core providing increased processing power (up to 16 MIPS at 16 MHz) while maintaining the advantages of a CISC architecture with improved code density, a 24-bit linear addressing space and an optimized architecture for low-power operations.

The family includes an integrated debug module with a hardware interface (SWIM) which allows non-intrusive in-application debugging and ultrafast Flash programming.

All high-density STM8AL3xE8x microcontrollers feature embedded data EEPROM and low-power low-voltage single-supply program Flash memory.

The devices incorporate an extensive range of enhanced I/Os and peripherals, a 12-bit ADC, two DACs, two comparators, a real-time clock, AES, 8x40 or 4x44-segment LCD, four 16-bit timers, one 8-bit timer, as well as standard communication interfaces such as two SPIs, an I^2C interface, and three USARTs. One 8x40 or 4x44-segment LCD is available on the STM8AL3LE8x devices. The modular design of the peripheral set allows the same peripherals to be found in different ST microcontroller families including 32-bit families. This makes any transition to a different family very easy, and simplified even more by the use of a common set of development tools.

2.1 STM8AL ultra-low-power 8-bit family benefits

High-density STM8AL3xE8x devices are part of the STM8AL automotive ultra-low-power 8-bit family providing the following benefits:

- Integrated system
  - 64 Kbytes of high-density embedded Flash program memory
  - 2 Kbytes of data EEPROM
  - 4 Kbytes of RAM
  - Internal high-speed and low-power low speed RC.
  - Embedded reset
- Ultra-low-power consumption
  - 1 µA in Active-halt mode
  - Clock gated system and optimized power management
  - Capability to execute from RAM for Low-power wait mode and Low-power run mode
- Advanced features
  - Up to 16 MIPS at 16 MHz CPU clock frequency
  - Direct memory access (DMA) for memory-to-memory or peripheral-to-memory access.
- Short development cycles
  - Application scalability across a common family product architecture with compatible pinout, memory map and modular peripherals.
  - Wide choice of development tools

STM8AL ultra-low-power microcontrollers operates either from 1.8 to 3.6 V (down to 1.65 V at power-down) or from 1.65 to 3.6 V. They are available in the -40 to +85 °C and -40 to +125 °C temperature ranges.

These features make the STM8AL ultra-low-power microcontroller families suitable for a wide range of applications.

The devices are offered in one 48-pin package. Different sets of peripherals are included depending on the device. Refer to *Section 3* for an overview of the complete range of peripherals proposed in this family.

All STM8AL ultra-low-power products are based on the same architecture with the same memory mapping and a coherent pinout.

Figure 1 shows the block diagram of the high-density STM8AL3xE8x families.

2.2 Device overview

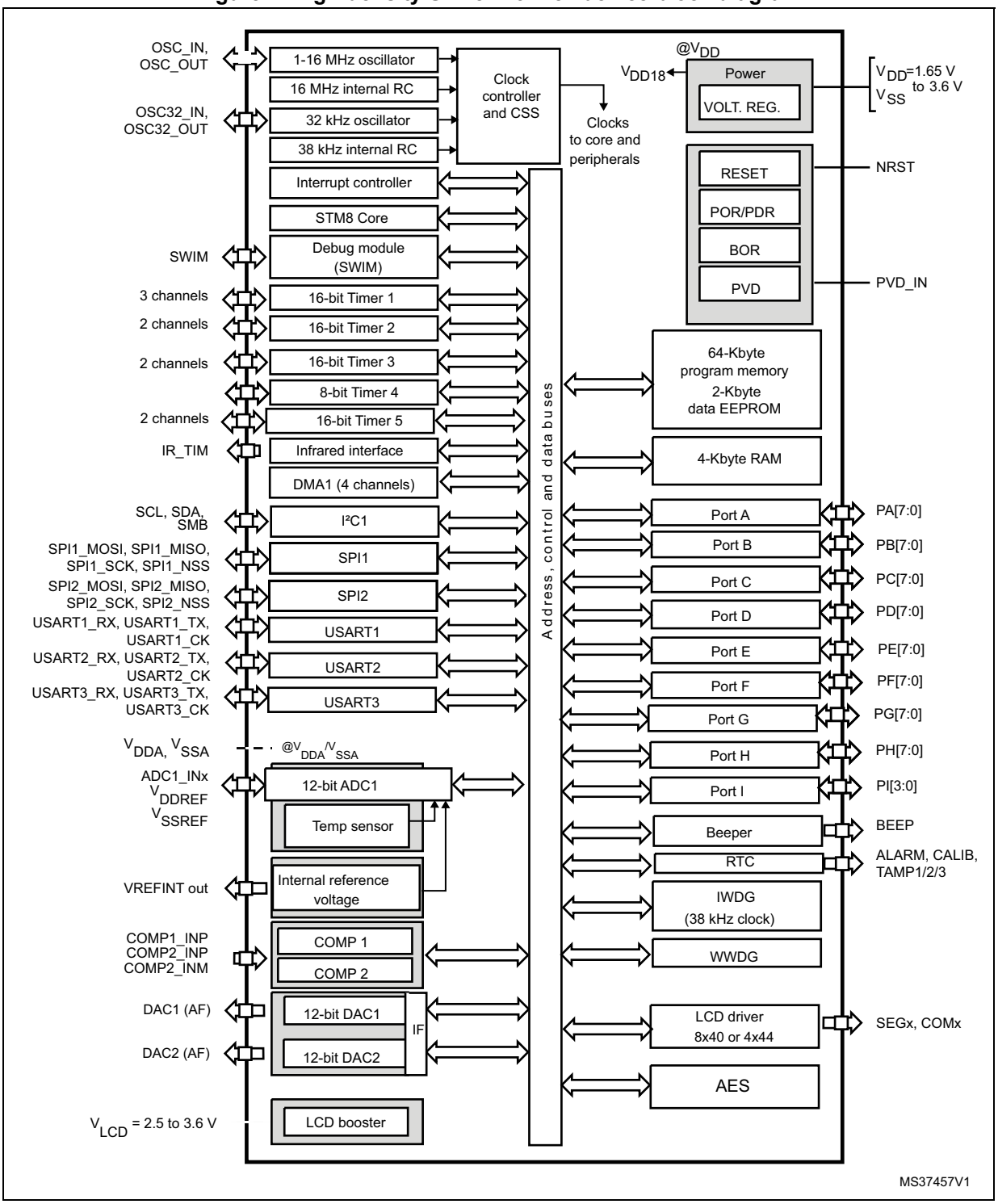
Table 2. High-density STM8AL3xE8x low-power device features and peripheral counts

Features		STM8AL3xx8	STM8AL3xx9	STM8AL3xxA
Flash (Kbyte)		64		
Data EEPROM (Kbyte)		2		
AES		1		
LCD		8x28 or 4x32(1)	8x36 or 4x40(1)	8x40 or 4x44(1)
Timers	Basic	1 (8-bit)	1 (8-bit)	1 (8-bit)
	General purpose	3 (16-bit)	3 (16-bit)	3 (16-bit)
	Advanced control	1 (16-bit)	1 (16-bit)	1 (16-bit)
Communication interfaces	SPI	2	2	2
	I2C	1	1	1
	USART	3	3	3
GPIOs		41(2)	54(2)	68(2)
12-bit synchronized ADC (number of channels)		1 (25)	1 (28)	1 (28)
12-Bit DAC Number of channels		2 2	2 2	2 2
Comparators (COMP1/COMP2)		2	2	2
Others		RTC, window watchdog, independent watchdog, 16-MHz and 38-kHz internal RC, 1- to 16-MHz and 32-kHz external oscillator		
CPU frequency		16 MHz		
Operating voltage		1.8 to 3.6 V (down to 1.65 V at power-down) with BOR		
Operating temperature		-40 to +85 °C / -40 to +125 °C		
Packages		LQFP48	LQFP64	LQFP80

1. STM8AL3LE8x versions only.
2. The number of GPIOs given in this table includes the NRST/PA1 pin but the application can use the NRST/PA1 pin as general purpose output only (PA1).

3 Functional overview

Figure 1. High-density STM8AL3xE8x device block diagram



1. **Legend**: AF: alternate function
   ADC: Analog-to-digital converter
   AES: Advanced encryption standard hardware accelerator

BOR: Brownout reset
DMA: Direct memory access
DAC: Digital-to-analog converter
I²C: Inter-integrated circuit multimaster interface
IWDG: Independent watchdog
LCD: Liquid crystal display
POR/PDR: Power on reset / power-down reset
RTC: Real-time clock
SPI: Serial peripheral interface
SWIM: Single wire interface module
USART: Universal synchronous asynchronous receiver transmitter
WWDG: Window watchdog

3.1 Low-power modes

The high-density STM8AL3xE8x devices support five low-power modes to achieve the best compromise between low-power consumption, short startup time and available wakeup sources:

- **Wait mode**: CPU clock is stopped, but selected peripherals keep running. An internal or external interrupt or a Reset is used to exit the microcontroller from Wait mode (WFE or WFI mode).
- **Low-power run mode**: The CPU and the selected peripherals are running. Execution is done from RAM with a low speed oscillator (LSI or LSE). Flash memory and data EEPROM are stopped and the voltage regulator is configured in ultra-low-power mode. The microcontroller enters Low-power run mode by software and exits from this mode by software or by a reset.
  All interrupts must be masked and are not used to exit the microcontroller from this mode.
- **Low-power wait mode:** This mode is entered when executing a Wait for event in Low-power run mode. It is similar to Low-power run mode except that the CPU clock is stopped. The wakeup from this mode is triggered by a Reset or by an internal or external event (peripheral event generated by the timers, serial interfaces, DMA controller (DMA1), comparators and I/O ports). When the wakeup is triggered by an event, the system goes back to Low-power run mode.
  All interrupts must be masked and arenot used to exit the microcontroller from this mode.
- **Active-halt mode**: CPU and peripheral clocks are stopped, except RTC. The wakeup is triggered by RTC interrupts, external interrupts or reset.
- **Halt mode**: CPU and peripheral clocks are stopped, the device remains powered on. The RAM content is preserved. The wakeup is triggered by an external interrupt or reset. A few peripherals have also a wakeup from Halt capability. Switching off the internal reference voltage reduces power consumption. Through software configuration it is also possible to wake up the device without waiting for the internal reference voltage wakeup time to have a fast wakeup time of 5 µs.

3.2 Central processing unit STM8

3.2.1 Advanced STM8 Core

The 8-bit STM8 core is designed for code efficiency and performance with an Harvard architecture and a 3-stage pipeline.

It contains 6 internal registers which are directly addressable in each execution context, 20 addressing modes including indexed indirect and relative addressing, and 80 instructions.

Architecture and registers

- Harvard architecture
- 3-stage pipeline
- 32-bit wide program memory bus - single cycle fetching most instructions
- X and Y 16-bit index registers - enabling indexed addressing modes with or without offset and read-modify-write type data manipulations
- 8-bit accumulator
- 24-bit program counter - 16 Mbyte linear memory space
- 16-bit stack pointer - access to a 64 Kbyte level stack
- 8-bit condition code register - 7 condition flags for the result of the last instruction

Addressing

- 20 addressing modes
- Indexed indirect addressing mode for lookup tables located anywhere in the address space
- Stack pointer relative addressing mode for local variables and parameter passing

Instruction set

- 80 instructions with 2-byte average instruction size
- Standard data movement and logic/arithmetic functions
- 8-bit by 8-bit multiplication
- 16-bit by 8-bit and 16-bit by 16-bit division
- Bit manipulation
- Data transfer between stack and accumulator (push/pop) with direct stack access
- Data transfer using the X and Y registers or direct memory-to-memory transfers

3.2.2 Interrupt controller

The high-density STM8AL3xE8x devices feature a nested vectored interrupt controller:

- Nested interrupts with 3 software priority levels
- 32 interrupt vectors with hardware priority
- Up to 40 external interrupt sources on 11 vectors
- Trap and reset interrupts

3.3 Reset and supply management

3.3.1 Power supply scheme

The device requires a 1.65 V to 3.6 V operating supply voltage (V_{DD}). The external power supply pins must be connected as follows:

- V_{SS1}, V_{DD1}, V_{SS2}, V_{DD2}, V_{SS3}, V_{DD3}, V_{SS4}, V_{DD4}= 1.65 to 3.6 V: external power supply for I/Os and for the internal regulator. Provided externally through V_{DD} pins, the corresponding ground pin is V_{SS}. V_{SS1}/V_{SS2}/V_{SS3}/V_{SS4} and V_{DD1}/V_{DD2}/V_{DD3}/V_{DD4} must not be left unconnected.
- V_{SSA}, V_{DDA} = 1.65 to 3.6 V: external power supplies for analog peripherals (minimum voltage to be applied to V_{DDA} is 1.8 V when the ADC1 is used). V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.
- V_{REF+}, V_{REF-} (for ADC1): external reference voltage for ADC1. Must be provided externally through V_{REF+} and V_{REF-} pin.
- V_{REF+} (for DAC1/2): external voltage reference for DAC1 and DAC2 must be provided externally through V_{REF+}.

3.3.2 Power supply supervisor

The device has an integrated ZEROPOWER power-on reset (POR)/power-down reset (PDR), coupled with a brownout reset (BOR) circuitry. At power-on, BOR is always active, and ensures proper operation starting from 1.8 V. As soon as the 1.8 V BOR threshold is reached, the option byte loading process starts, either to confirm or modify the default thresholds, or to disable BOR permanently. In this latter case, the V_{DD} min value at power down is 1.65 V.

Five BOR thresholds are available through option byte, starting from 1.8 V to 3 V. To reduce the power consumption in Halt mode, it is possible to automatically switch off the internal reference voltage (and consequently the BOR) in Halt mode. The device remains in reset state when V_{DD} is below a specified threshold, $V_{POR/PDR}$ or V_{BOR}, without the need for any external reset circuit.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. This PVD offers 7 different levels between 1.85 V and 3.05 V, chosen by software, with a step around 200 mV. An interrupt is generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine generates then a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.3.3 Voltage regulator

The high-density STM8AL3xE8x devices embed an internal voltage regulator for generating the 1.8 V power supply for the core and peripherals.

This regulator has two different modes:

- Main voltage regulator mode (MVR) for Run, Wait for interrupt (WFI) and Wait for event (WFE) modes.
- Low-power voltage regulator mode (LPVR) for Halt, Active-halt, Low-power run and Low-power wait modes.

When entering Halt or Active-halt modes, the system automatically switches from the MVR to the LPVR in order to reduce current consumption.

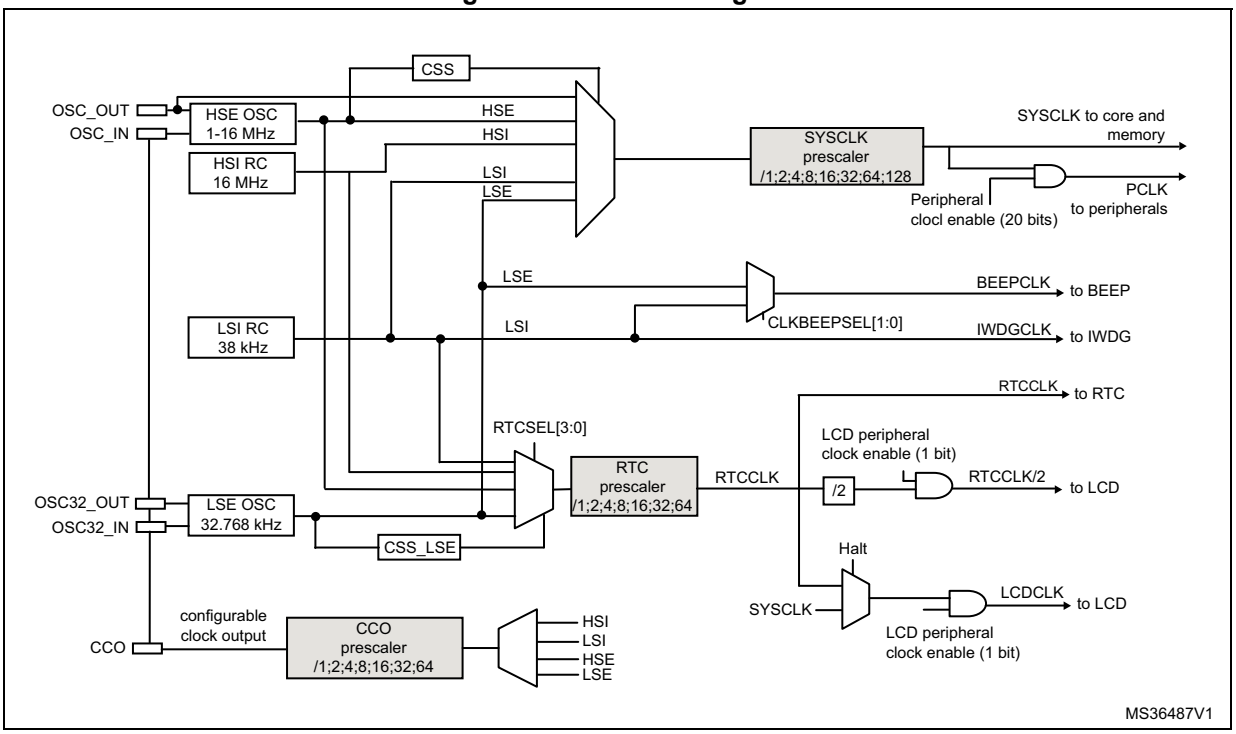
3.4 Clock management

The clock controller distributes the system clock (SYSCLK) coming from different oscillators to the core and the peripherals. It also manages clock gating for low-power modes and ensures clock robustness.

Features

- **Clock prescaler:** to get the best compromise between speed and current consumption, the clock frequency to the CPU and peripherals has to be adjusted by a programmable prescaler
- **Safe clock switching:** Clock sources are adaptable safely on the fly in run mode through a configuration register.
- **Clock management:** To reduce power consumption, the clock controller stops the clock to the core, individual peripherals or memory.
- **System clock sources:** 4 different clock sources are available to drive the system clock:
  - 1-16 MHz High speed external crystal (HSE)
  - 16 MHz High speed internal RC oscillator (HSI)
  - 32.768 Low speed external crystal (LSE)
  - 38 kHz Low speed internal RC (LSI)
- **RTC and LCD clock sources:** the above four sources are available to clock the RTC and the LCD, whatever the system clock.
- **Startup clock:** After reset, the microcontroller restarts by default with an internal 2 MHz clock (HSI/8). The prescaler ratio and clock source is adjustable by the application program as soon as the code execution starts.
- **Clock security system (CSS):** This feature is enabled by software. If a HSE clock failure occurs, the system clock is automatically switched to HSI.
- **Configurable main clock output (CCO):** This outputs an external clock for use by the application.

Figure 2. Clock tree diagram



1. The HSE clock source is either an external crystal/ceramic resonator or an external source (HSE bypass). Refer to Section HSE clock in STM8L051/L052 Value Line, STM8L151/L152, STM8L162, STM8AL31, STM8AL3L MCU lines reference manual (RM0031).
2. The LSE clock source is either an external crystal/ceramic resonator or a external source (LSE bypass). Refer to Section LSE clock in STM8L051/L052 Value Line, STM8L151/L152, STM8L162, STM8AL31, STM8AL3L MCU lines reference manual (RM0031).

3.5 Low-power real-time clock

The real-time clock (RTC) is an independent binary coded decimal (BCD) timer/counter.

Six byte locations contain the second, minute, hour (12/24 hour), week day, date, month, year, in BCD (binary coded decimal) format. Correction for 28, 29 (leap year), 30, and 31 day months are made automatically. The subsecond field is also readable in binary format.

The calendar is adjustable from 1 to 32767 RTC clock pulses. This allows to make a synchronization to a master clock.

The RTC offers a digital calibration which allows an accuracy of +/-0.5ppm.

It provides a programmable alarm and programmable periodic interrupts with wakeup from Halt capability.

- Periodic wakeup time using the 32.768 kHz LSE with the lowest resolution (of 61 µs) is from min. 122 µs to max. 3.9 s. With a different resolution, the wakeup time reaches 36 hours
- Periodic alarms based on the calendar are generated from LSE period to every year

A clock security system detects a failure on LSE, and provides an interrupt with wakeup capability. The RTC clock automatically switches to LSI in case of LSE failure.

The RTC also provides 3 anti-tamper detection pins. This detection embeds a programmable filter and wakes-up the MCU.

3.6 LCD (Liquid crystal display)

The LCD is only available on STM8AL3LE8x devices.

The liquid crystal display drives up to 8 common terminals and up to 40 segment terminals to drive up to 320 pixels. This LCD is configurable to drive up to 4 common and 44 segments (up to 176 pixels).

- Internal step-up converter to guarantee contrast control whatever V_{DD}.
- Static 1/2, 1/3, 1/4, 1/8 duty supported.
- Static 1/2, 1/3, 1/4 bias supported.
- Phase inversion to reduce power consumption and EMI.
- Up to 8 pixels programmable to blink.
- The LCD controller operating in Halt mode.

Note: Unnecessary segments and common pins can be used as general I/O pins.

3.7 Memories

The high-density STM8AL3xE8x devices have the following main features:

- 4 Kbytes of RAM
- The non-volatile memory is divided into three arrays:
  - 64 Kbytes of medium-density embedded Flash program memory
  - 2 Kbytes of Data EEPROM
  - Option byte.

The memory supports the read-while-write (RWW): it is possible to execute the code from the program matrix while programming/erasing the data matrix.

The option byte protects part of the Flash program memory from write and readout piracy.

3.8 DMA

A 4-channel direct memory access controller (DMA1) offers a memory-to-memory and peripherals-from/to-memory transfer capability. The 4 channels are shared between the following IPs with DMA capability: ADC1, DAC1,DAC2, AES, I2C1, SPI1, SPI2, USART1, USART2, USART3, and the 5 Timers.

3.9 Analog-to-digital converter

- 12-bit analog-to-digital converter (ADC1) with 28 channels (including 4 fast channel), temperature sensor and internal reference voltage
- Conversion time down to 1 µs with f_{SYSCLK}= 16 MHz
- Programmable resolution
- Programmable sampling time
- Single and continuous mode of conversion
- Scan capability: automatic conversion performed on a selected group of analog inputs
- Analog watchdog: interrupt generation when the converted voltage is outside the programmed threshold
- Triggered by timer

Note: ADC1 can be served by DMA1.

3.10 Digital-to-analog converter

- 12-bit DAC with 2 buffered outputs (two digital signals are converted into two analog voltage signal outputs)
- Synchronized update capability using timers
- DMA capability for each channel
- External triggers for conversion
- Noise-wave generation
- Triangular-wave generation
- Dual DAC channels with independent or simultaneous conversions
- Input reference voltage V_{REF+} for better resolution

Note: DAC can be served by DMA1.

3.11 Ultra-low-power comparators

The high-density STM8AL3xE8x devices embed two comparators (COMP1 and COMP2) sharing the same current bias and voltage reference. The voltage reference is an internal or external (coming from an I/O).

- One comparator with fixed threshold (COMP1).
- One comparator rail to rail with fast or slow mode (COMP2). The threshold is one of the following:
  - DAC output
  - External I/O
  - Internal reference voltage or internal reference voltage submultiple (1/4, 1/2, 3/4)

The two comparators are usable together to offer a window function. They wake up from Halt mode.

3.12 System configuration controller and routing interface

The system configuration controller provides the capability to remap some alternate functions on different I/O ports. TIM4 and ADC1 DMA channels can also be remapped.

The highly flexible routing interface allows application software to control the routing of different I/Os to the TIM1 timer input captures. It also controls the routing of internal analog signals to ADC1, COMP1, COMP2, DAC1 and the internal reference voltage V_{REFINT}. It also provides a set of registers for efficiently managing the charge transfer acquisition sequence.

3.13 AES

The AES Hardware Accelerator can be used to encipher and decipher data using the AES algorithm (compatible with FIPS PUB 197, 2001 Nov 26).

- Key scheduler
- Key derivation for decryption
- 128-bit data block processed
- 128-bit key length
- 892 clock cycles to encrypt/decrypt one 128-bit block

AES data flow can be served by the DMA1 controller

3.14 Timers

The high-density STM8AL3xE8x devices contain one advanced control timer (TIM1), three 16-bit general purpose timers (TIM2,TIM3 and TIM5) and one 8-bit basic timer (TIM4).

All the timers are served by DMA1.

Table 3 compares the features of the advanced control, general-purpose and basic timers.

Table 3. Timer feature comparison

Timer	Counter resolution	Counter type	Prescaler factor	DMA1 request generation	Capture/compare channels	Complementary outputs
TIM1	16-bit	up/down	Any integer from 1 to 65536	Yes	3 + 1	3
TIM2			Any power of 2 from 1 to 128		2	None
TIM3						
TIM5						
TIM4	8-bit	up	Any power of 2 from 1 to 32768		0	

3.14.1 16-bit advanced control timer (TIM1)

This is a high-end timer designed for a wide range of control applications. With its complementary outputs, dead-time control and center-aligned PWM capability, the field of applications is extended to motor control, lighting and half-bridge driver.

- 16-bit up, down and up/down autoreload counter with 16-bit prescaler
- 3 independent capture/compare channels (CAPCOM) configurable as input capture, output compare, PWM generation (edge and center aligned mode) and single pulse mode output
- 1 additional capture/compare channel which is not connected to an external I/O
- Synchronization module to control the timer with external signals
- Break input to force timer outputs into a defined state
- 3 complementary outputs with adjustable dead time
- Encoder mode
- Interrupt capability on various events (capture, compare, overflow, break, trigger)

3.14.2 16-bit general purpose timers (TIM2, TIM3, TIM5)

- 16-bit autoreload (AR) up/down-counter
- 7-bit prescaler adjustable to fixed power of 2 ratios (1…128)
- 2 individually configurable capture/compare channels
- PWM mode
- Interrupt capability on various events (capture, compare, overflow, break, trigger)
- Synchronization with other timers or external signals (external clock, reset, trigger and enable)

3.14.3 8-bit basic timer (TIM4)

The 8-bit timer consists of an 8-bit up auto-reload counter driven by a programmable prescaler. This timer is used for timebase generation with interrupt generation on timer overflow or for DAC trigger generation.

3.15 Watchdog timers

The watchdog system is based on two independent timers providing maximum security to the applications.

3.15.1 Window watchdog timer

The window watchdog (WWDG) is used to detect the occurrence of a software fault, usually generated by external interferences or by unexpected logical conditions, which cause the application program to abandon its normal sequence.

3.15.2 Independent watchdog timer

The independent watchdog peripheral (IWDG) is used to resolve processor malfunctions due to hardware or software failures.

It is clocked by the internal LSI RC clock source, and thus stays active even in case of a CPU clock failure.

3.16 Beeper

The beeper function outputs a signal on the BEEP pin for sound generation. The signal is in the range of 1, 2 or 4 kHz.

3.17 Communication interfaces

3.17.1 SPI

The serial peripheral interfaces (SPI1 and SPI2) provide half/ full duplex synchronous serial communication with external devices.

- Maximum speed: 8 Mbit/s ($f_{SYSCLK}/2$) both for master and slave
- Full duplex synchronous transfers
- Simplex synchronous transfers on 2 lines with a possible bidirectional data line
- Master or slave operation - selectable by hardware or software
- Hardware CRC calculation
- Slave/master selection input pin

Note: SPI1 and SPI2 can be served by the DMA1 Controller.

3.17.2 I^2C

The I^2C bus interface (I2C1) provides multi-master capability, and controls all I²C bus-specific sequencing, protocol, arbitration and timing.

- Master, slave and multi-master capability
- Standard mode up to 100 kHz and fast speed modes up to 400 kHz.
- 7-bit and 10-bit addressing modes.
- SMBus 2.0 and PMBus support
- Hardware CRC calculation

Note: I^2C1 can be served by the DMA1 Controller.

3.17.3 USART

The USART interfaces (USART1, USART2 and USART3) allow full duplex, asynchronous communications with external devices requiring an industry standard NRZ asynchronous serial data format. It offers a very wide range of baud rates.

- 1 Mbit/s full duplex SCI
- SPI1 emulation
- High precision baud rate generator
- Smartcard emulation
- IrDA SIR encoder decoder
- Single wire half duplex mode

Note: USART1, USART2 and USART3 can be served by the DMA1 Controller.

USART interfaces are used to implement LIN slave communication, with LIN Break detection on the framing error flag (FE in USART_SR register) with a value of 0 in the USART data register (USART_DR).

3.18 Infrared (IR) interface

The high-density STM8AL3xE8x devices contain an infrared interface which is used with an IR LED for remote control functions. Two timer output compare channels are used to generate the infrared remote control signals.

3.19 Development support

Development tools

Development tools for the STM8 microcontrollers include:

- The STice emulation system offering tracing and code profiling
- The STVD high-level language debugger including C compiler, assembler and integrated development environment
- The STVP Flash programming software

The STM8 also comes with starter kits, evaluation boards and low-cost in-circuit debugging/programming tools.

Single wire data interface (SWIM) and debug module

The debug module with its single wire data interface (SWIM) permits non-intrusive real-time in-circuit debugging and fast memory programming.

The Single wire interface is used for direct access to the debugging module and memory programming. The interface is activated in all device operation modes.

The non-intrusive debugging module features a performance close to a full-featured emulator. Beside memory and peripherals, CPU operation is also monitored in real-time by means of shadow registers.