



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of "Quality Parts,Customers Priority,Honest Operation,and Considerate Service",our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China





# N-Channel Enhancement-Mode Vertical DMOS FET

## Features

- ▶ Low threshold - 2.0V max.
- ▶ High input impedance
- ▶ Low input capacitance - 50pF typical
- ▶ Fast switching speeds
- ▶ Low on-resistance
- ▶ Free from secondary breakdown
- ▶ Low input and output leakage

## Applications

- ▶ Logic level interfaces – ideal for TTL and CMOS
- ▶ Solid state relays
- ▶ Battery operated systems
- ▶ Photo voltaic drives
- ▶ Analog switches
- ▶ General purpose line drivers
- ▶ Telecom switches

## General Description

This low threshold, enhancement-mode (normally-off) transistor utilizes a vertical DMOS structure and Supertex's well-proven, silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

## Ordering Information

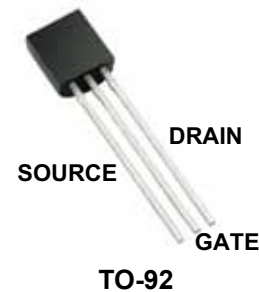
Part Number	Package Option	Packing
TN0106N3-G	TO-92	1000/Bag
TN0106N3-G P002	TO-92	2000/Reel
TN0106N3-G P003		
TN0106N3-G P005		
TN0106N3-G P013		
TN0106N3-G P014		

-G denotes a lead (Pb)-free / RoHS compliant package.  
 Contact factory for Wafer / Die availability.  
 Devices in Wafer / Die form are lead (Pb)-free / RoHS compliant.

## Product Summary

$BV_{DSS}/BV_{DGS}$	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	$V_{GS(th)}$ (max)
60V	3.0Ω	2.0A	2.0V

## Pin Configuration



## Absolute Maximum Ratings

Parameter	Value
Drain-to-source voltage	$BV_{DSS}$
Drain-to-gate voltage	$BV_{DGS}$
Gate-to-source voltage	±20V
Operating and storage temperature	-55°C to +150°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

## Product Marking



YY = Year Sealed  
 WW = Week Sealed  
 \_\_\_\_\_ = "Green" Packaging

Package may or may not include the following marks: Si or   
 TO-92

## Typical Thermal Resistance

Package	$\theta_{ja}$
TO-92	132°C/W



## Thermal Characteristics

Package	$I_D$ (continuous) <sup>†</sup>	$I_D$ (pulsed)	Power Dissipation @ $T_c = 25^\circ\text{C}$	$I_{DR}$ <sup>†</sup>	$I_{DRM}$
TO-92	350mA	2.0A	1.0W	350mA	2.0A

**Notes:**

<sup>†</sup>  $I_D$  (continuous) is limited by max rated  $T_J$ .

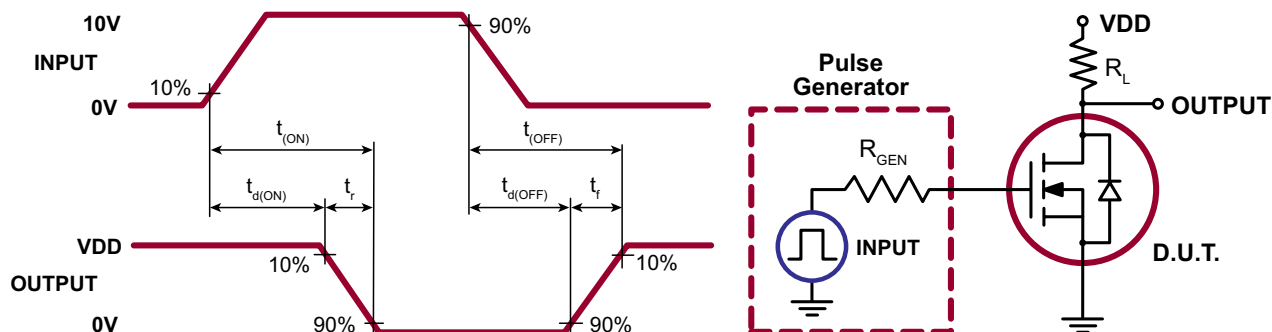
## Electrical Characteristics ( $T_A = 25^\circ\text{C}$ unless otherwise specified)

Sym	Parameter	Min	Typ	Max	Units	Conditions
$BV_{DSS}$	Drain-to-source breakdown voltage	60	-	-	V	$V_{GS} = 0V, I_D = 1.0mA$
$V_{GS(th)}$	Gate threshold voltage	0.6	-	2.0	V	$V_{GS} = V_{DS}, I_D = 0.5mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with temperature	-	-3.2	-5.0	mV/°C	$V_{GS} = V_{DS}, I_D = 1.0mA$
$I_{GSS}$	Gate body leakage	-	-	100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$
$I_{DSS}$	Zero Gate voltage drain current	-	-	10	$\mu\text{A}$	$V_{GS} = 0V, V_{DS} = \text{Max Rating}$ $V_{DS} = 0.8 \text{ Max Rating},$ $V_{GS} = 0V, T_A = 125^\circ\text{C}$
		-	-	500		
$I_{D(ON)}$	On-state drain current	0.75	1.4	-	A	$V_{GS} = 5.0V, V_{DS} = 25V$ $V_{GS} = 10V, V_{DS} = 25V$
		2.0	3.4	-		
$R_{DS(ON)}$	Static drain-to-source on-state resistance	-	2.0	4.5	$\Omega$	$V_{GS} = 4.5V, I_D = 250mA$ $V_{GS} = 10V, I_D = 500mA$
		-	1.6	3.0		
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with temperature	-	0.6	1.1	%/°C	$V_{GS} = 10V, I_D = 500mA$
$G_{FS}$	Forward transductance	225	400	-	mmho	$V_{DS} = 25V, I_D = 500mA$
$C_{ISS}$	Input capacitance	-	50	60	pF	$V_{GS} = 0V,$ $V_{DS} = 25V,$ $f = 1.0MHz$
$C_{OSS}$	Common source output capacitance	-	25	35		
$C_{RSS}$	Reverse transfer capacitance	-	4.0	8.0		
$t_{d(ON)}$	Turn-on delay time	-	2.0	5.0	ns	$V_{DD} = 25V,$ $I_D = 1.0A,$ $R_{GEN} = 25\Omega$
$t_r$	Rise time	-	3.0	5.0		
$t_{d(OFF)}$	Turn-off delay time	-	6.0	7.0		
$t_f$	Fall time	-	3.0	6.0		
$V_{SD}$	Diode forward voltage drop	-	1.0	1.5	V	$V_{GS} = 0V, I_{SD} = 500mA$
$t_{rr}$	Reverse recovery time	-	400	-	ns	$V_{GS} = 0V, I_{SD} = 500mA$

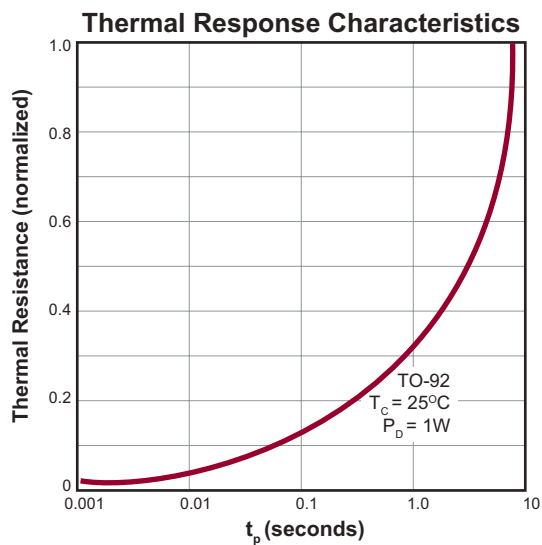
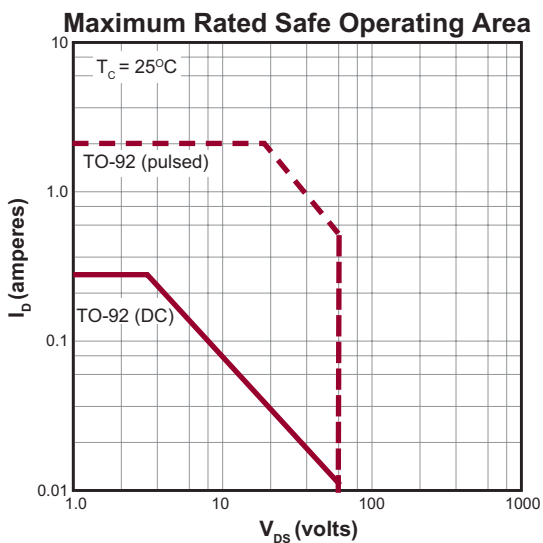
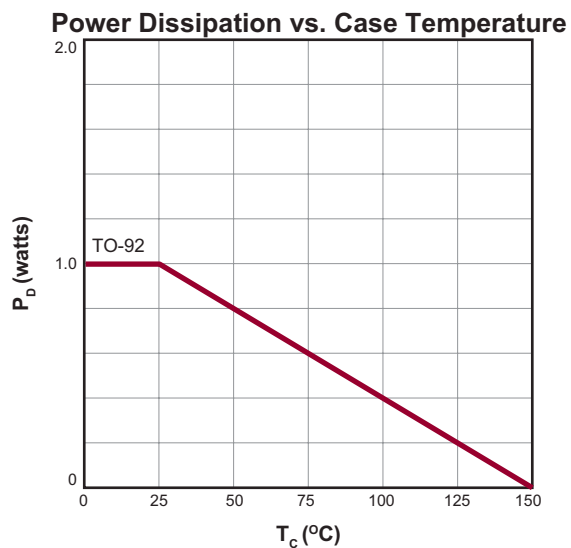
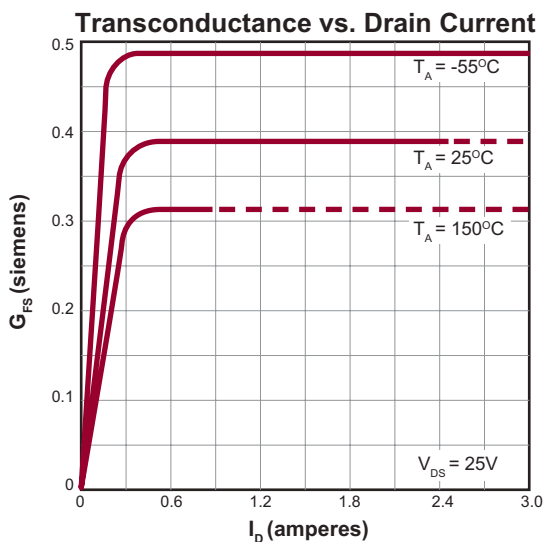
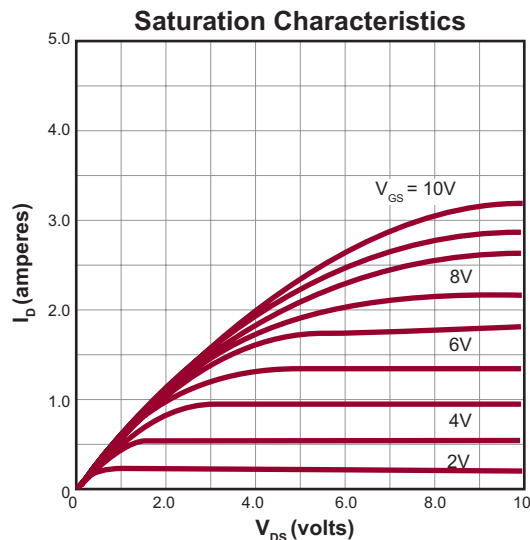
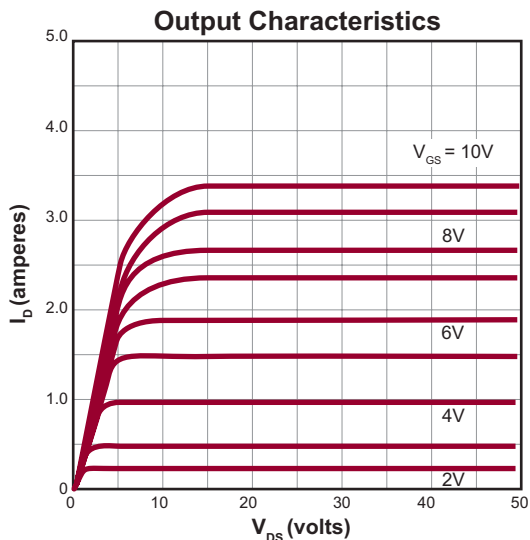
**Notes:**

- All D.C. parameters 100% tested at  $25^\circ\text{C}$  unless otherwise stated. (Pulse test:  $300\mu\text{s}$  pulse, 2% duty cycle.)
- All A.C. parameters sample tested.

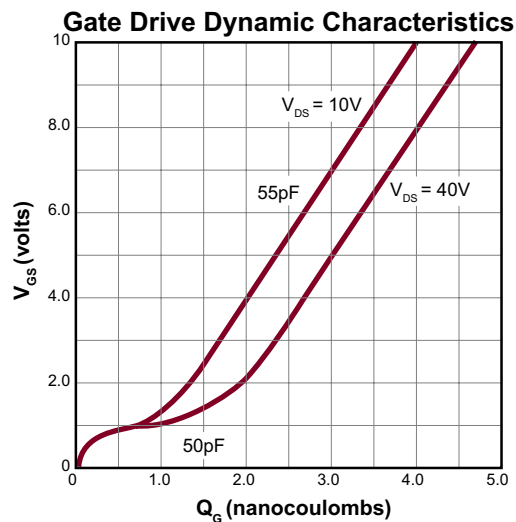
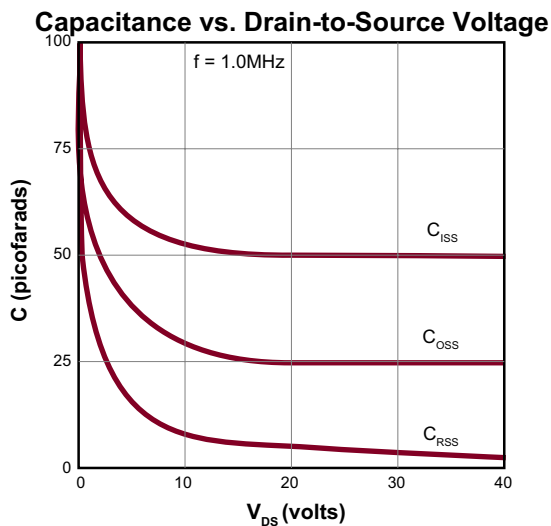
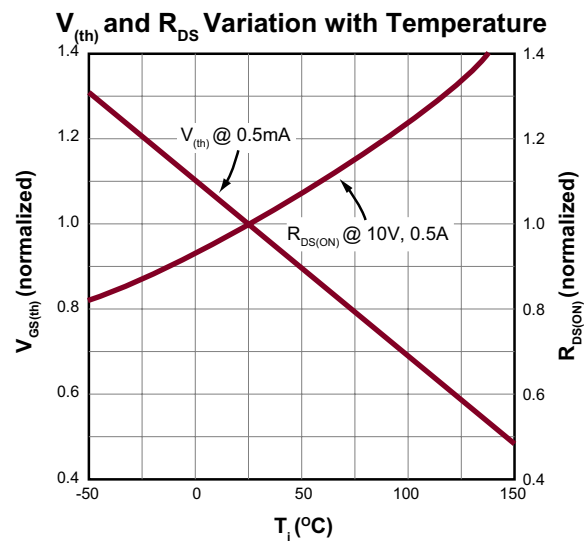
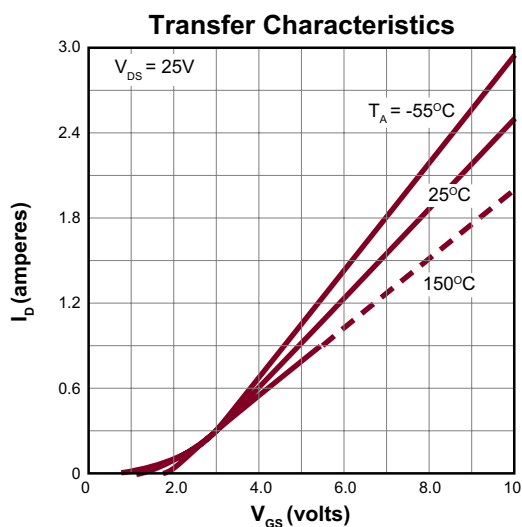
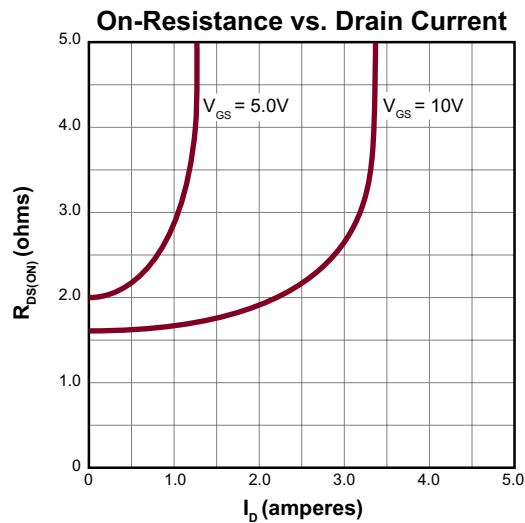
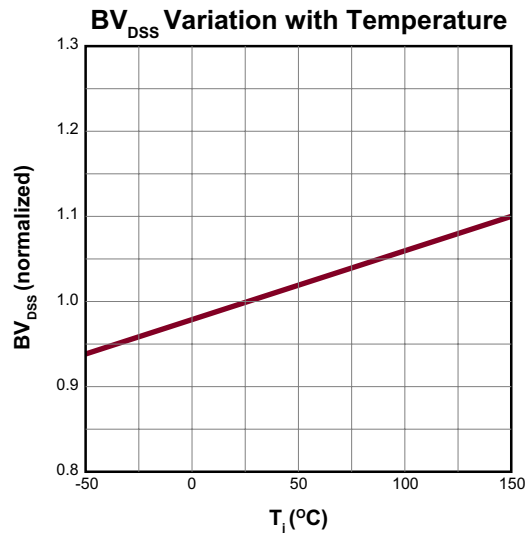
## Switching Waveforms and Test Circuit



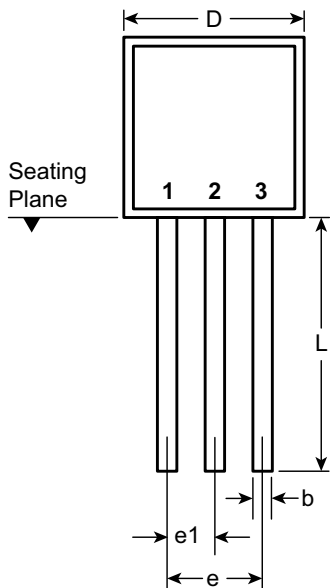
# Typical Performance Curves



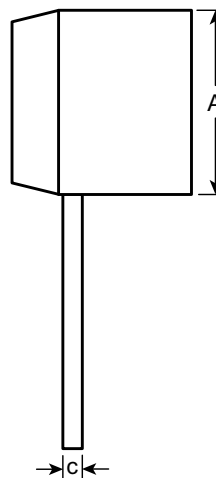
Typical Performance Curves (cont.)



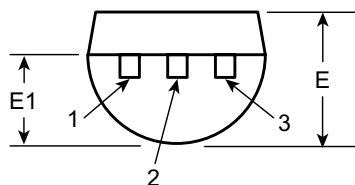
### 3-Lead TO-92 Package Outline (N3)



**Front View**



**Side View**



**Bottom View**

Symbol	A	b	c	D	E	E1	e	e1	L
Dimensions (inches)	MIN	.170	.014 <sup>†</sup>	.175	.125	.080	.095	.045	.500
	NOM	-	-	-	-	-	-	-	-
	MAX	.210	.022 <sup>†</sup>	.022 <sup>†</sup>	.205	.165	.105	.105	.610*

JEDEC Registration TO-92.

\* This dimension is not specified in the JEDEC drawing.

† This dimension differs from the JEDEC drawing.

**Drawings not to scale.**

**Supertex Doc.#:** DSPD-3TO92N3, Version E041009.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

**Supertex inc.** does not recommend the use of its products in life support applications, and will not knowingly sell them for use in such applications unless it receives an adequate "product liability indemnification insurance agreement." **Supertex inc.** does not assume responsibility for use of devices described, and limits its liability to the replacement of the devices determined defective due to workmanship. No responsibility is assumed for possible omissions and inaccuracies. Circuitry and specifications are subject to change without notice. For the latest product specifications refer to the **Supertex inc.** (website: <http://www.supertex.com>)