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N-Channel Enhancement-Mode Vertical DMOS FET

Features

- Low Threshold (2V Maximum)
- High Input Impedance and High Gain
- Free from Secondary Breakdown
- Low CISS and Fast Switching Speeds

Applications

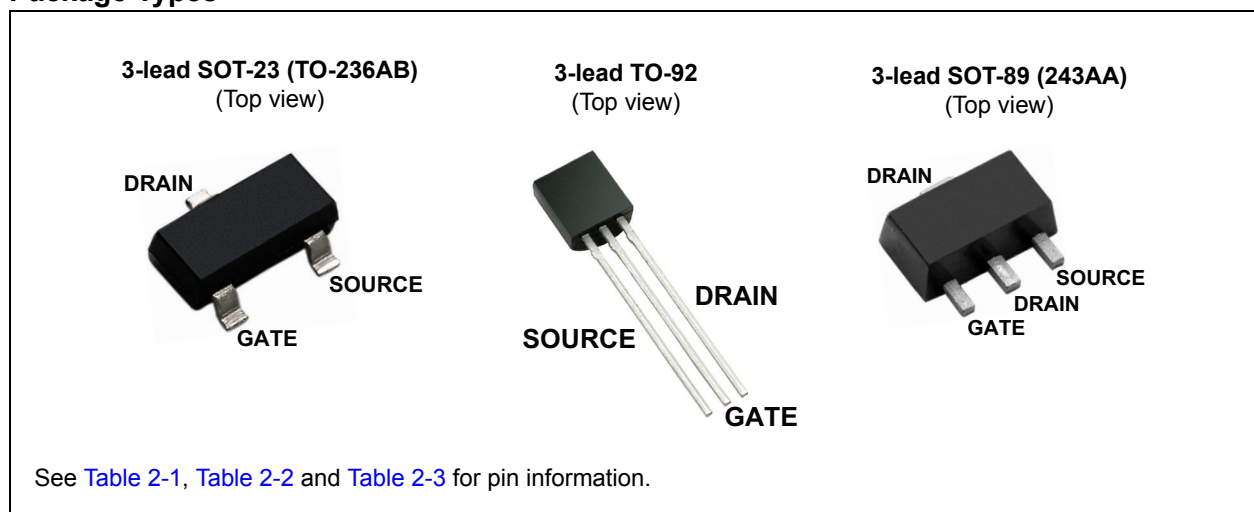
- Logic-level Interfaces (Ideal for TTL and CMOS)
- Solid State Relays
- Battery-operated Systems
- Photo-voltaic Drives
- Analog Switches
- General Purpose Line Drivers
- Telecommunication Switches

General Description

The TN5325 is a low-threshold, Enhancement-mode (normally-off) transistor that utilizes a vertical DMOS structure and a well-proven silicon gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally induced secondary breakdown.

Microchip's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance and fast switching speeds are desired.

Package Types



TN5325

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Drain-to-source Voltage	BV_{DSX}
Drain-to-gate Voltage	BV_{DGX}
Gate-to-source Voltage	$\pm 20V$
Operating Ambient Temperature, T_A	$-55^{\circ}C$ to $+150^{\circ}C$
Storage Temperature, T_S	$-55^{\circ}C$ to $+150^{\circ}C$

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS ¹

Electrical Specifications: Unless otherwise specified, for all specifications $T_A = T_J = +25^{\circ}C$.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Drain-to-source Breakdown Voltage	BV_{DSS}	250	—	—	V	$V_{GS} = 0V, I_D = 100 \mu A$
Gate Threshold Voltage	$V_{GS(th)}$	0.6	—	2	V	$V_{GS} = V_{DS}, I_D = 1 mA$
Change in $V_{GS(th)}$ with Temperature	$\Delta V_{GS(th)}$	—	—	-4.5	mV/ $^{\circ}C$	$V_{GS} = V_{DS}, I_D = 1 mA$ (Note 2)
Gate Body Leakage	I_{GSS}	—	—	100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$
Zero-gate Voltage Drain Current	I_{DSS}	—	—	1	μA	$V_{GS} = 0V, V_{DS} = 100V$
		—	—	10		$V_{GS} = 0V, V_{DS} = \text{Maximum Rating}$
		—	—	1	mA	$V_{DS} = 0.8 \text{ Maximum Rating}, V_{GS} = 0V, T_A = 125^{\circ}C$ (Note 2)
On-state Drain Current	$I_{D(ON)}$	0.6	—	—	A	$V_{GS} = 4.5V, V_{DS} = 25V$
		1.2	—	—		$V_{GS} = 10V, V_{DS} = 25V$
Static Drain-to-source On-state Resistance	$R_{DS(ON)}$	—	—	8	Ω	$V_{GS} = 4.5V, I_D = 150 mA$
		—	—	7		$V_{GS} = 10V, I_D = 1A$
Change in $R_{DS(ON)}$ with Temperature	$\Delta R_{DS(ON)}$	—	—	1	%/ $^{\circ}C$	$V_{GS} = 4.5V, I_D = 150 mA$ (Note 2)

Note 1: All DC parameters are 100% tested at $25^{\circ}C$ unless otherwise stated. Pulse test: 300 μs pulse, 2% duty cycle.

2: Specification is obtained by characterization and is not 100% tested.

AC ELECTRICAL CHARACTERISTICS ²

Electrical Specifications: Unless otherwise specified, for all specifications $T_A = T_J = +25^\circ\text{C}$.						
Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Forward Transconductance	G_{FS}	150	—	—	mmho	$V_{DS} = 25\text{V}, I_D = 200\text{ mA}$
Input Capacitance	C_{ISS}	—	—	110	pF	$V_{GS} = 0\text{V},$ $V_{DS} = 25\text{V},$ $f = 1\text{ MHz}$
Common Source Output Capacitance	C_{OSS}	—	—	60		
Reverse Transfer Capacitance	C_{RSS}	—	—	23		
Turn-on Delay Time	$t_{d(ON)}$	—	—	20	ns	$V_{DD} = 25\text{V},$ $I_D = 150\text{ mA},$ $R_{GEN} = 25\Omega$
Rise Time	t_r	—	—	15		
Turn-off Delay Time	$t_{d(OFF)}$	—	—	25		
Fall Time	t_f	—	—	25		
DIODE PARAMETER						
Diode Forward Voltage Drop	V_{SD}	—	—	1.8	V	$V_{GS} = 0\text{V}, I_{SD} = 200\text{ mA}$ (Note 1)
Reverse Recovery Time	t_{rr}	—	300	—	ns	$V_{GS} = 0\text{V}, I_{SD} = 200\text{ mA}$ (Note 2)

Note 1: All DC parameters are 100% tested at 25°C unless otherwise stated. Pulse test: 300 μs pulse, 2% duty cycle.

Note 2: Specification is obtained by characterization and is not 100% tested.

TEMPERATURE SPECIFICATIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
TEMPERATURE RANGE						
Operating Ambient Temperature	T_A	-55	—	+150	$^\circ\text{C}$	
Storage Temperature	T_S	-55	—	+150	$^\circ\text{C}$	
PACKAGE THERMAL RESISTANCE						
3-lead SOT-23	θ_{JA}	—	350	—	$^\circ\text{C/W}$	
	θ_{JC}	—	200	—	$^\circ\text{C/W}$	
3-lead TO-92	θ_{JA}	—	170	—	$^\circ\text{C/W}$	
	θ_{JC}	—	125	—	$^\circ\text{C/W}$	
3-lead SOT-89	θ_{JA}	—	78	—	$^\circ\text{C/W}$	Note 1
	θ_{JC}	—	15	—	$^\circ\text{C/W}$	

Note 1: Mounted on FR5 25 mm x 25 mm x 1.57 mm

THERMAL CHARACTERISTICS

Package	$I_D^{(1)}$ (Continuous) (mA)	I_D (Pulsed) (A)	Power Dissipation at $T_A = 25^\circ\text{C}$ (W)	$I_{DR}^{(1)}$ (mA)	I_{DRM} (A)
3-lead SOT-23	150	0.4	0.36	150	0.4
3-lead TO-92	215	0.8	0.74	215	0.8
3-lead SOT-89	316	1.5	1.6 ⁽²⁾	316	1.5

Note 1: I_D (continuous) is limited by maximum T_J .

Note 2: Mounted on FR5 board, 25 mm x 25 mm x 1.57 mm

TN5325

2.0 PIN DESCRIPTION

Table 2-1, Table 2-2 and Table 2-3 show the description of pins in TN5325 3-lead SOT-23, 3-lead TO-92 and 3-lead SOT-89, respectively. Refer to [Package Types](#) for the location of pins.

TABLE 2-1: SOT-23 PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	Gate	Gate
2	Source	Source
3	Drain	Drain

TABLE 2-2: TO-92 PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	Source	Source
2	Gate	Gate
3	Drain	Drain

TABLE 2-3: SOT-89 PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	Gate	Gate
2	Drain	Drain
3	Source	Source
4	Drain	Drain

3.0 FUNCTIONAL DESCRIPTION

Figure 3-1 illustrates the switching waveforms and test circuit for TN5325.

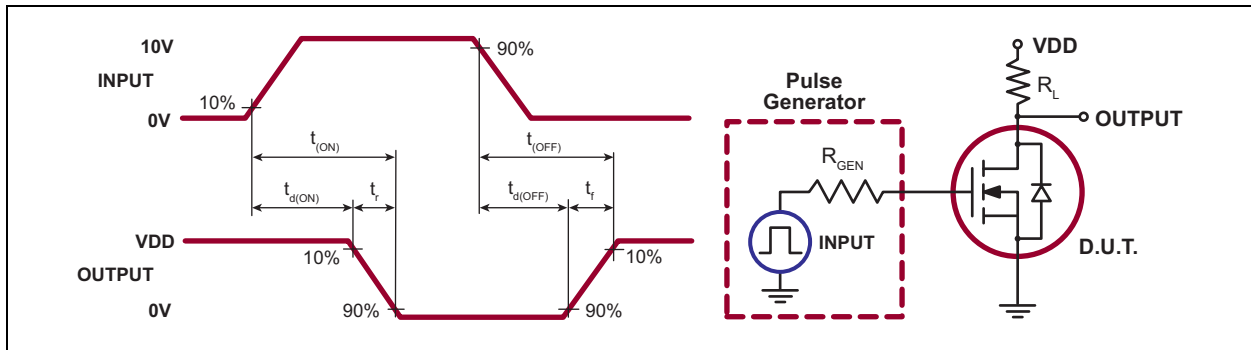


FIGURE 3-1: Switching Waveforms and Test Circuit.

PRODUCT SUMMARY

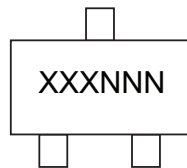
BV_{DSS}/BV_{DGS} (V)	$R_{DS(ON)}$ (Maximum) (Ω)	$I_{D(ON)}$ (Minimum) (A)	$V_{GS(th)}$ (Maximum) (V)
250V	7	1.2	2

TN5325

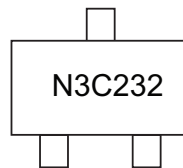
4.0 PACKAGING INFORMATION

4.1 Package Marking Information

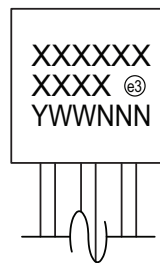
3-lead SOT-23



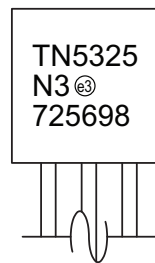
Example



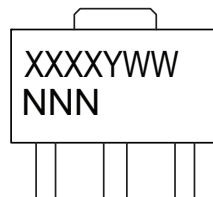
3-lead TO-92



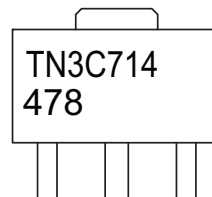
Example



3-lead SOT-89

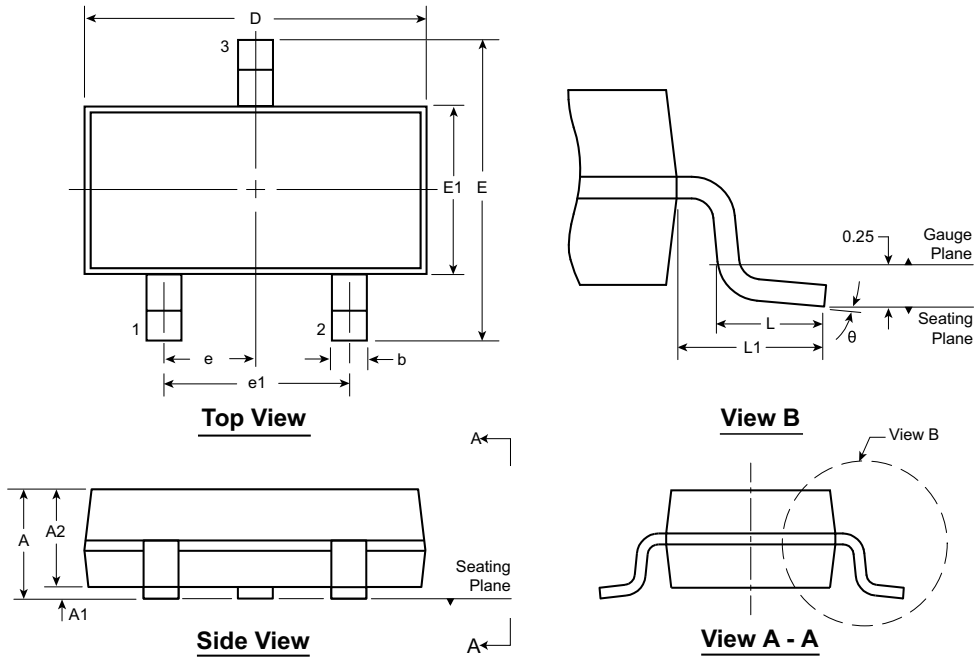


Example



Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.	

3-Lead TO-236AB (SOT-23) Package Outline (K1/T) 2.90x1.30mm body, 1.12mm height (max), 1.90mm pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

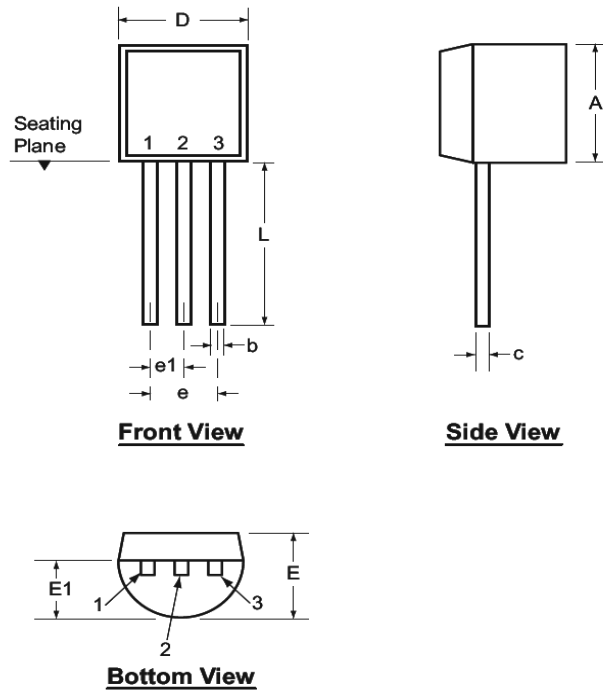
Symbol		A	A1	A2	b	D	E	E1	e	e1	L	L1	θ
Dimension (mm)	MIN	0.89	0.01	0.88	0.30	2.80	2.10	1.20	0.95 BSC	1.90 BSC	0.20 [†]	0.54 REF	0°
	NOM	-	-	0.95	-	2.90	-	1.30			0.50		-
	MAX	1.12	0.10	1.02	0.50	3.04	2.64	1.40			0.60		8°

JEDEC Registration TO-236, Variation AB, Issue H, Jan. 1999.

[†] This dimension differs from the JEDEC drawing.

Drawings not to scale.

3-Lead TO-92 Package Outline (L/LL/N3)



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Symbol	A	b	c	D	E	E1	e	e1	L	
Dimensions (inches)	MIN	.170	.014 [†]	.014 [†]	.175	.125	.080	.095	.045	.500
	NOM	-	-	-	-	-	-	-	-	-
	MAX	.210	.022 [†]	.022 [†]	.205	.165	.105	.105	.055	.610*

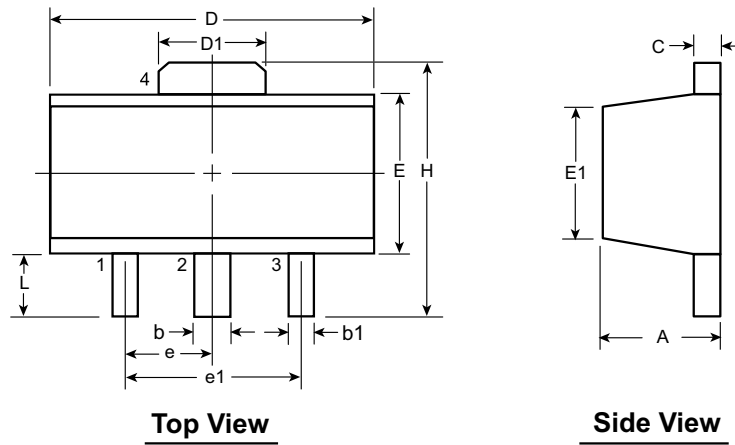
JEDEC Registration TO-92.

* This dimension is not specified in the JEDEC drawing.

† This dimension differs from the JEDEC drawing.

Drawings not to scale.

3-Lead TO-243AA (SOT-89) Package Outline (N8)



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Symbol	A	b	b1	C	D	D1	E	E1	e	e1	H	L		
Dimensions (mm)	MIN	1.40	0.44	0.36	0.35	4.40	1.62	2.29	2.00 [†]	1.50 BSC	3.00 BSC	3.94	0.73 [†]	
	NOM	-	-	-	-	-	-	-	-			-	-	-
	MAX	1.60	0.56	0.48	0.44	4.60	1.83	2.60	2.29			4.25	1.20	

JEDEC Registration TO-243, Variation AA, Issue C, July 1986.

[†] This dimension differs from the JEDEC drawing

Drawings not to scale.

TN5325

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (April 2017)

- Converted Supertex Doc# DSFP-TN5325 to Microchip DS20005709A
- Changed the part marking format
- Removed the N3 P003, N3 P005, N3 P013 and N3 P014 media types
- Made minor text changes throughout the document

TN5325

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

<u>PART NO.</u>		<u>XX</u>	-	<u>X</u>	-	<u>X</u>
Device		Package Options		Environmental		Media Type
Device:	TN5325	=		N-Channel Enhancement-Mode Vertical DMOS FET		
Packages:	K1	=		3-lead SOT-23		
	N3	=		3-lead TO-92		
	N8	=		3-lead SOT-89		
Environmental:	G	=		Lead (Pb)-free/RoHS-compliant Package		
Media Types:	(blank)	=		3000/Reel for a K1 Package		
		=		1000/Bag for an N3 Package		
		=		2000/Reel for an N8 Package		
	P002	=		2000/Reel for an N3 Package		

Examples:	
a) TN5325K1-G:	N-Channel Enhancement-Mode Vertical DMOS FET, 3-lead SOT-23, 3000/Reel
b) TN5325N3-G:	N-Channel Enhancement-Mode Vertical DMOS FET, 3-lead TO-92, 1000/Bag
c) TN5325N3-G-P002:	N-Channel Enhancement-Mode Vertical DMOS FET, 3-lead TO-92, 2000/Reel
d) TN5325N8-G:	N-Channel Enhancement-Mode Vertical DMOS FET, 3-lead SOT-89, 2000/Reel

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