Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

TNY375-380
TinySwitch®-PK Family

Energy-Efficient, Off-Line Switcher With Enhanced Peak Power Performance

Product Highlights

Lowest System Cost with Enhanced Flexibility

- Simple ON/OFF control, no loop compensation needed
- Unique Peak Mode feature extends power range without increasing transformer size
  - Maximum frequency and current limit boosted at peak loads
- Selectable current limit through BP/M capacitor value
  - Higher current limit extends maximum power in open frame
  - Lower current limit improves efficiency in enclosed adapters
  - Allows optimum TinySwitch-PK choice by swapping devices with no other circuit redesign
- Tight I^2f parameter tolerance reduces system cost
  - Maximizes MOSFET and magnetics power delivery
- ON time extension – typically extends low line regulation range/ hold-up time to reduce input bulk capacitance
- Self-biased: no bias winding required for TNY375-376; winding required for TNY377-380
- Frequency jittering reduces EMI filter costs
- Optimized pin out eases pcb/external heat sinking
- Quiet source-connected heat sink pins for low EMI

Enhanced Safety and Reliability Features

- Accurate hysteretic thermal shutdown with automatic recovery provides complete system level overload protection and eliminates need for manual reset
- Auto-restart delivers <3% maximum power in short circuit and open loop fault conditions
- Output overvoltage shutdown with optional Zener
- Line undervoltage detect threshold set using a single resistor
- Very low component count enhances reliability and enables single sided printed circuit board layout
- High bandwidth provides fast turn on with no overshoot and excellent transient load response
- Extended creepage between DRAIN and all other pins improves field reliability

EcoSmart®– Extremely Energy Efficient

- Easily meets all global energy efficiency regulations
- No-load <170 mW at 265 VAC without bias winding, <60 mW with bias winding
- ON/OFF control provides constant efficiency down to very light loads – ideal for mandatory CEC efficiency regulations and 1 W PC standby requirements

Applications

- Applications with high peak-to-continuous power demands – DVDs, PVRs, active speakers (e.g. PC audio), audio amplifiers, modems, photo printers
- Applications with high power demands at startup (large output capacitance or motor loads) – PC standby, low voltage motor drives

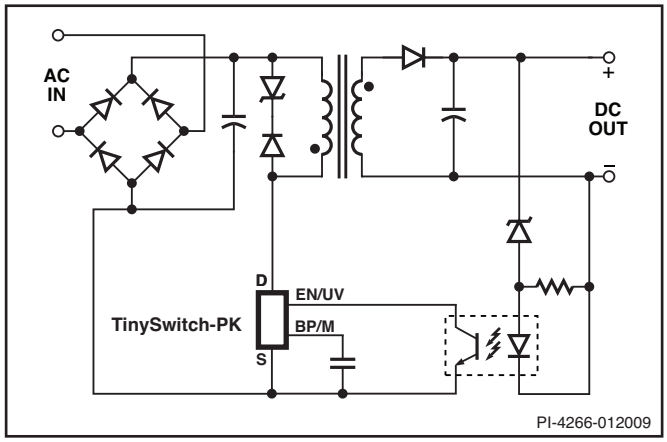


Figure 1. Typical Peak Power Application.

Output Power Table

Product[3]	230 VAC ± 15%			85-265 VAC		
	Adapter[1]	Open Frame[2]	Peak	Adapter[1]	Open Frame[2]	Peak
TNY375P/G/D[4]	8.5 W	15 W	16.5 W	6 W	11.5 W	12.5 W
TNY376P/G/D[4]	10 W	19 W	22 W	7 W	15 W	17 W
TNY377P/G	13 W	23.5 W	28 W	8 W	18 W	23 W
TNY378P/G	16 W	28 W	34 W	10 W	21.5 W	27 W
TNY379P/G	18 W	32 W	39 W	12 W	25 W	31 W
TNY380P/G	20 W	36.5 W	45 W	14 W	28.5 W	35 W

Table 1. Output Power Table.

Notes:
1. Minimum continuous power in a typical non-ventilated enclosed adapter measured at +50 °C ambient. Use of an external heat sink will increase power capability.
2. Minimum continuous power in an open frame design (see Key Applications Considerations).
3. Packages: P: DIP-8C, G: SMD-8C, D: SO-8C. Lead free only. See Part Ordering Information.
4. See Key Application Considerations.

Description

TinySwitch-PK incorporates a 700 V MOSFET, oscillator, high-voltage switched current source, current limit (user selectable), and thermal shutdown circuitry. A unique peak mode feature boosts current limit and frequency for peak load conditions. The boosted current limit provides the peak output power while the increased peak mode frequency ensures the transformer can be sized for continuous load conditions rather than peak power demands.

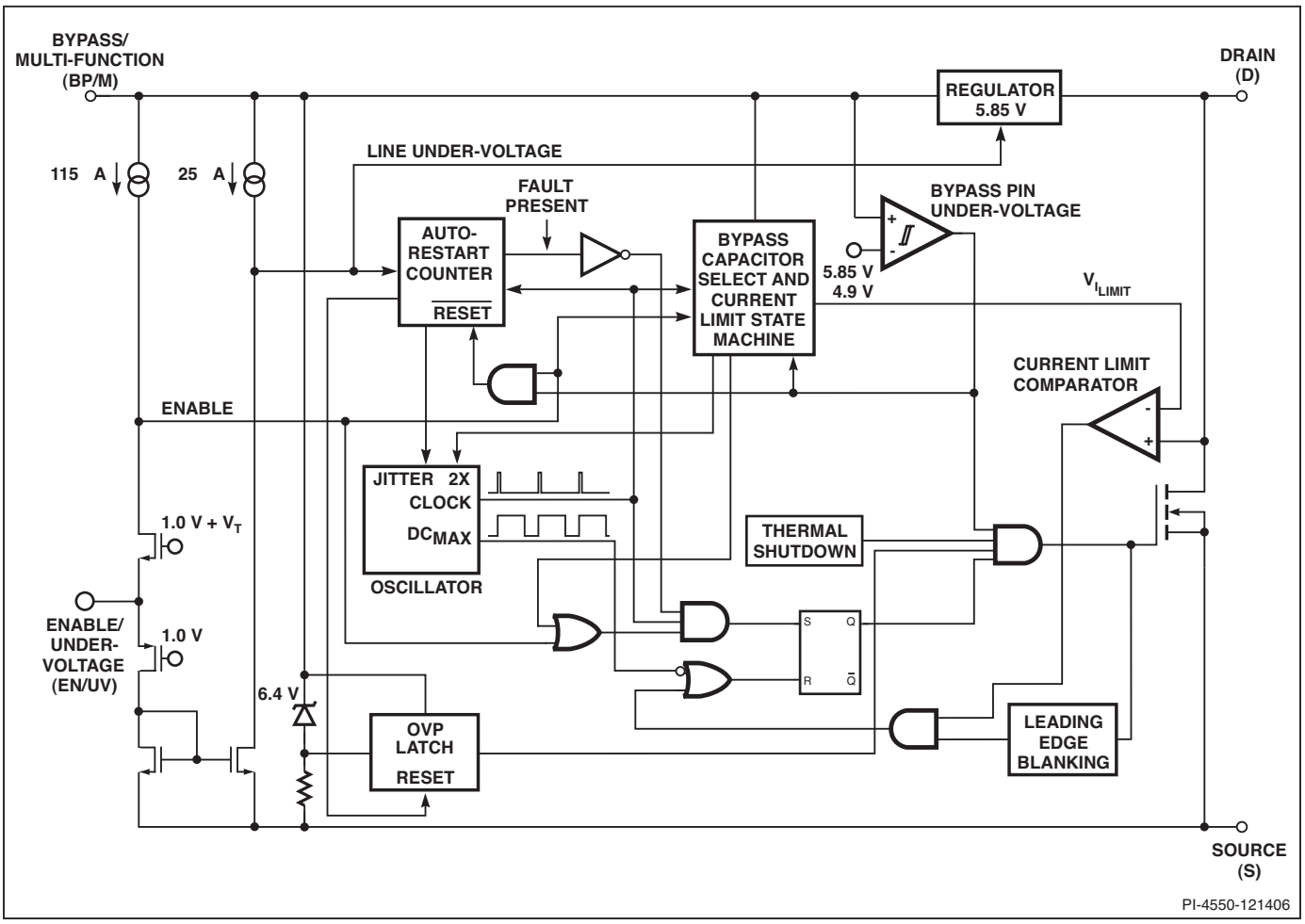


Figure 2 Functional Block Diagram.

Pin Functional Description

DRAIN (D) Pin:
This pin is the power MOSFET drain connection. It provides internal operating current for both start-up and steady-state operation.

BYPASS/MULTI-FUNCTION (BP/M) Pin:
This pin has multiple functions:

1. It is the connection point for an external bypass capacitor for the internally generated 5.85 V supply.
2. It is a mode selector for the current limit value, depending on the value of the capacitance added. Use of a 0.1 μF capacitor results in the standard current limit value. Use of a 1 μF capacitor results in the current limit being reduced to that of the next smaller device size. Use of a 10 μF capacitor results in the current limit being increased to that of the next larger device.
3. It provides a shutdown function. When the current into the bypass pin exceeds 7 mA, the device latches off until the BP/M voltage drops below 4.9 V, during a power down or when a line undervoltage is detected. This can be used to provide an output overvoltage function with a Zener diode connected from the BP/M pin to a bias winding supply.

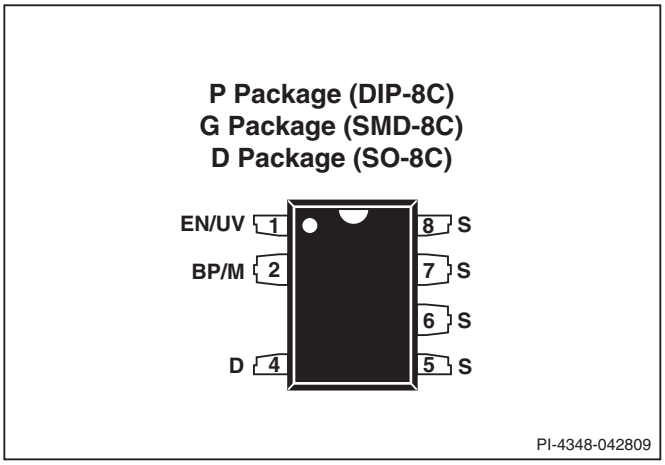


Figure 3. Pin Configuration.

ENABLE/UNDERVOLTAGE (EN/UV) Pin:
This pin has dual functions: enable input and line undervoltage sense. During normal operation, switching of the power MOSFET is controlled by this pin. MOSFET switching is terminated when a current greater than a threshold current is drawn from this pin. Switching resumes when the current being

pulled from the pin drops to less than a threshold current. A modulation of the threshold current reduces group pulsing. The threshold current is between 75 μA and 115 μA.

The EN/UV pin also senses line undervoltage conditions through an external resistor connected to the DC line voltage. If there is no external resistor connected to this pin, TinySwitch-PK detects its absence and disables the line under-voltage function.

SOURCE (S) Pin:
This pin is internally connected to the output MOSFET source for high voltage power return and control circuit common.

TinySwitch-PK Functional Description

TinySwitch-PK combines a high voltage power MOSFET switch with a power supply controller in one device. Unlike conventional PWM (pulse width modulator) controllers, it uses a simple ON/OFF control to regulate the output voltage.

The controller consists of an oscillator, enable circuit (sense and logic), current limit state machine, 5.85 V regulator, BYPASS/MULTI-FUNCTION pin undervoltage, overvoltage circuit, and current limit selection circuitry, over-temperature protection, current limit circuit, leading edge blanking, and a 700 V power MOSFET. TinySwitch-PK incorporates additional circuitry for line undervoltage sense, auto-restart, adaptive switching cycle on-time extension, and frequency jitter. Figure 2 shows the functional block diagram with the most important features.

Oscillator
The typical oscillator frequency is internally set to an average of 264 kHz (at the highest current limit level). Two signals are generated from the oscillator: the maximum duty cycle signal (DC_{MAX}) and the clock signal that indicates the beginning of each cycle.

The oscillator incorporates circuitry that introduces a small amount of frequency jitter, typically ±3% of the oscillator frequency, to minimize EMI emission. The modulation rate of the frequency jitter is set to 1 kHz to optimize EMI reduction for both average and quasi-peak emissions. The frequency jitter should be measured with the oscilloscope triggered at the falling edge of the DRAIN waveform. The waveform in Figure 4 illustrates the frequency jitter with an oscillator frequency of 264 kHz.

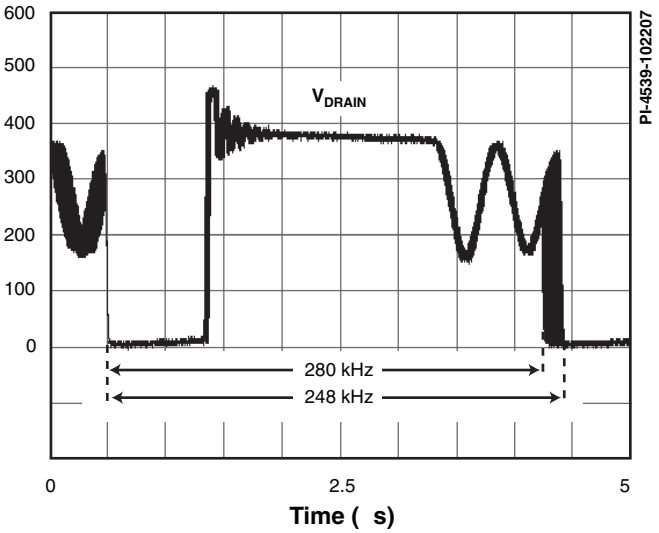


Figure 4. Frequency Jitter.

Enable Input and Current Limit State Machine
The enable input circuit at the EN/UV pin consists of a low impedance source follower output set at 1.2 V. The current through the source follower is limited to 115 μA. When the current out of this pin exceeds the threshold current, a low logic level (disable) is generated at the output of the enable circuit until the current out of this pin is reduced to less than the threshold current. This enable circuit output is sampled at the beginning of each cycle on the rising edge of the clock signal. If high, the power MOSFET is turned on for that cycle (enabled). If low, the power MOSFET remains off (disabled). Since the sampling is done only at the beginning of each cycle, subsequent changes in the EN/UV pin voltage or current during the remainder of the cycle are ignored. When a cycle is disabled, the EN/UV pin is sampled at 264 kHz. This faster sampling enables the power supply to respond faster without being required to wait for completion of the full period.

The current limit state machine reduces the current limit by discrete amounts at light loads when TinySwitch-PK is likely to switch in the audible frequency range. The lower current limit raises the effective switching frequency above the audio range and reduces the transformer flux density, including the associated audible noise. The state machine monitors the sequence of enable events to determine the load condition and adjusts the current limit level accordingly in discrete amounts.

Under most operating conditions (except when close to no-load), the low impedance of the source follower keeps the voltage on the EN/UV pin from going much below 1.2 V in the disabled state. This improves the response time of the optocoupler that is usually connected to this pin.

5.85 V Regulator and 6.4 V Shunt Voltage Clamp
The 5.85 V regulator charges the bypass capacitor connected to the BYPASS pin to 5.85 V by drawing a current from the voltage on the DRAIN pin whenever the MOSFET is off. The BYPASS/MULTI-FUNCTION pin is the internal supply voltage node. When the MOSFET is on, the device operates from the energy stored in the bypass capacitor. Extremely low power consumption of the internal circuitry allows the TNY375 and TNY376 to operate continuously from current taken from the DRAIN pin. A bypass capacitor value of 0.1 μF is sufficient for both high frequency decoupling and energy storage.

In addition, there is a 6.4 V shunt regulator clamping the BYPASS/MULTI-FUNCTION pin at 6.4 V when current is provided to the BYPASS/MULTI-FUNCTION pin through an external resistor. This facilitates powering of TinySwitch-PK externally through a bias winding as required for TNY377-380. Powering the TinySwitch-PK externally in this way also decreases the no-load consumption to below 60 mW.

BYPASS/MULTI-FUNCTION Pin Undervoltage

The BYPASS/MULTI-FUNCTION pin undervoltage circuitry disables the power MOSFET when the BYPASS/MULTI-FUNCTION pin voltage drops below 4.9 V in steady state operation. Once the BYPASS/MULTI-FUNCTION pin voltage drops below 4.9 V in steady state operation, it must rise back to 5.85 V to enable (turn-on) the power MOSFET.

Over Temperature Protection

The thermal shutdown circuitry senses the die temperature. The threshold is typically set at 142 °C with 75 °C hysteresis. When the die temperature rises above this threshold, the power MOSFET is disabled and remains disabled, until the die temperature falls by 75 °C, at which point it is re-enabled. A large hysteresis of 75 °C (typical) is provided to prevent overheating of the PC board due to a continuous fault condition.

Current Limit

The current limit circuit senses the current in the power MOSFET. When this current exceeds the internal threshold (I_{LIMIT}), the power MOSFET is turned off for the remainder of that cycle. The current limit state machine reduces the current limit threshold by discrete amounts under medium and light loads.

The leading edge blanking circuit inhibits the current limit comparator for a short time (t_{LEB}) after the power MOSFET is turned on. This leading edge blanking time has been set so that current spikes caused by typical capacitance and secondary-side rectifier reverse recovery time will not cause premature termination of the switching pulse.

Auto-Restart

In the event of a fault condition such as output overload, output short circuit, or an open loop condition, TinySwitch-PK enters into auto-restart operation. An internal counter clocked by the oscillator is reset every time the EN/UV pin is pulled low. If the EN/UV pin is not pulled low for 8192 switching cycles (or 32 ms), the power MOSFET switching is normally disabled for 1 second (except in the case of line undervoltage condition, in which case it is disabled until the condition is removed). The auto-restart alternately enables and disables the switching of the power MOSFET until the fault condition is removed. Figure 5 illustrates auto-restart circuit operation in the presence of an output short circuit.

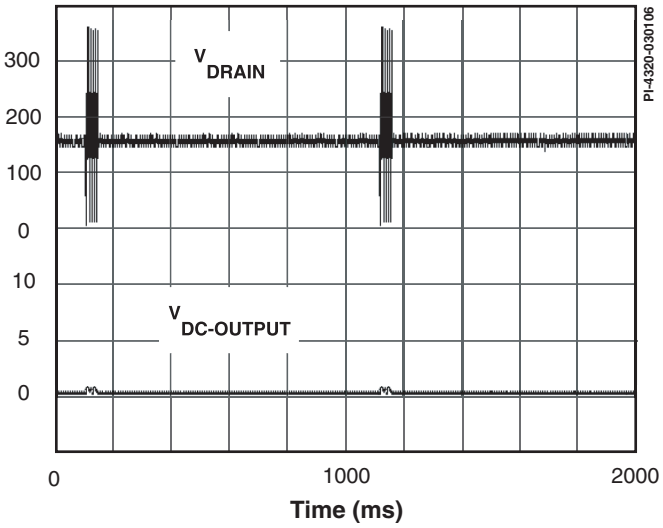


Figure 5. Auto-Restart Operation.

In the event of a line undervoltage condition, the switching of the power MOSFET is disabled beyond its normal 1 second until the line undervoltage condition ends.

Adaptive Switching Cycle On-Time Extension

Adaptive switching cycle on-time extension keeps the cycle on until current limit is reached, instead of prematurely terminating after the DC_{MAX} signal goes low. This feature reduces the minimum input voltage required to maintain regulation, typically extending hold-up time and minimizing the size of bulk capacitor required. The on-time extension is disabled during the startup of the power supply, and after auto-restart, until the power supply output reaches regulation.

Line Undervoltage Sense Circuit

The DC line voltage can be monitored by connecting an external resistor from the DC line to the EN/UV pin. During power-up or when the switching of the power MOSFET is disabled in auto-restart, the current into the EN/UV pin must exceed 25 μA to initiate switching of the power MOSFET. During power-up, this is accomplished by holding the BYPASS/MULTI-FUNCTION pin to 4.9 V while the line undervoltage condition exists. After the line undervoltage condition goes away and the BYPASS/MULTI-FUNCTION pin has stabilized at 5.85 V, switching is initiated. Once MOSFET switching is enabled, the DC line voltage is ignored unless the power supply enters auto-restart mode in the event of a fault condition. When the switching of the power MOSFET is disabled in auto-restart mode and a line undervoltage condition exists, the auto-restart counter is stopped. This stretches the disable time beyond its normal 1 second until the line undervoltage condition ends.

The line undervoltage circuit also detects when there is no external resistor connected to the EN/UV pin (less than ~1 μA into the pin). In this case the line undervoltage function is disabled.

TinySwitch-PK Operation

TinySwitch-PK devices operate in the current limit mode. When enabled, the oscillator turns the power MOSFET on at the beginning of each cycle. The MOSFET is turned off when the current ramps up to the current limit or when the DC_{MAX} limit is reached (applicable when On-Time Extension is disabled). Since the highest current limit level and frequency of a TinySwitch-PK design are constant, the power delivered to the load is proportional to the primary inductance of the transformer and peak primary current squared. Hence, designing the supply involves calculating the primary inductance of the transformer for the maximum output power required. If the TinySwitch-PK is appropriately chosen for the power level, the current in the calculated inductance will ramp up to current limit before the DC_{MAX} limit is reached.

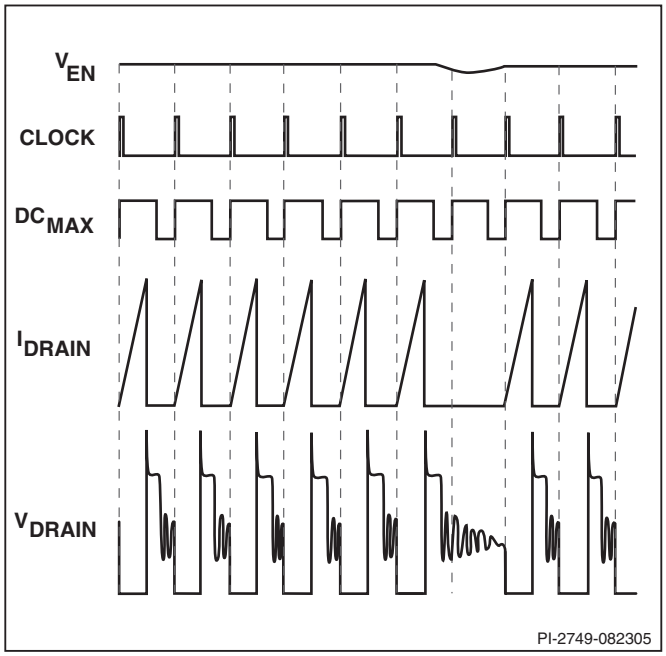


Figure 6. Operation at Near Maximum Loading (f_{OSC} 264 kHz).

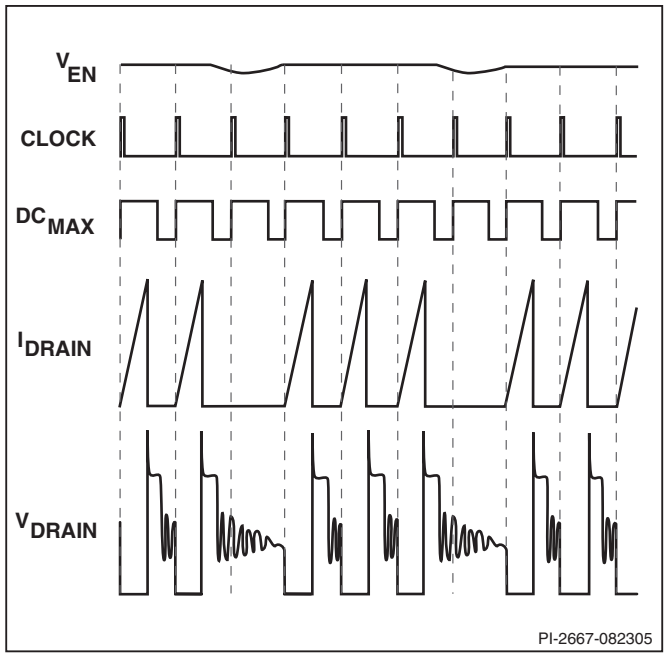


Figure 7. Operation at Moderately Heavy Loading (f_{OSC} 264 kHz).

Enable Function

TinySwitch-PK senses the EN/UV pin to determine whether or not to proceed with the next switching cycle. The sequence of cycles is used to determine the current limit. Once a cycle is started, it always completes the cycle (even when the EN/UV pin changes state halfway through the cycle). This operation results in a power supply in which the output voltage ripple is determined by the output capacitor, amount of energy per switch cycle, and the delay of the feedback.

The EN/UV pin signal is generated on the secondary by comparing the power supply output voltage with a reference voltage. The EN/UV pin signal is high when the power supply output voltage is less than the reference voltage. In a typical implementation, the EN/UV pin is driven by an optocoupler. The collector of the optocoupler transistor is connected to the EN/UV pin, and the emitter is connected to the SOURCE pin. The optocoupler LED is connected in series with a Zener diode across the DC output voltage to be regulated. When the output voltage exceeds the target regulation voltage level (optocoupler LED voltage drop plus Zener voltage), the optocoupler LED will start to conduct, pulling the EN/UV pin low. The Zener diode can be replaced by a TL431 reference circuit for improved accuracy.

ON/OFF Operation with Current Limit State Machine

The internal clock of the TinySwitch-PK runs at all times. At the beginning of each clock cycle, it samples the EN/UV pin to decide whether or not to implement a switch cycle, and based on the sequence of samples over multiple cycles, it determines the appropriate current limit. At high loads, the state machine sets the current limit to its highest value. With TinySwitch-PK, when the state machine sets the current limit to its highest value, the oscillator frequency is also doubled, providing the unique peak mode operation. At lighter loads, the state machine sets the current limit to reduced values. At these lower current limit levels, the oscillator frequency returns to the standard value.

At near maximum load, TinySwitch-PK will conduct during nearly all of its clock cycles (Figure 6). At slightly lower load, it will “skip” additional cycles in order to maintain voltage regulation at the power supply output (Figure 7). At medium loads, more cycles will be skipped, the current limit will be

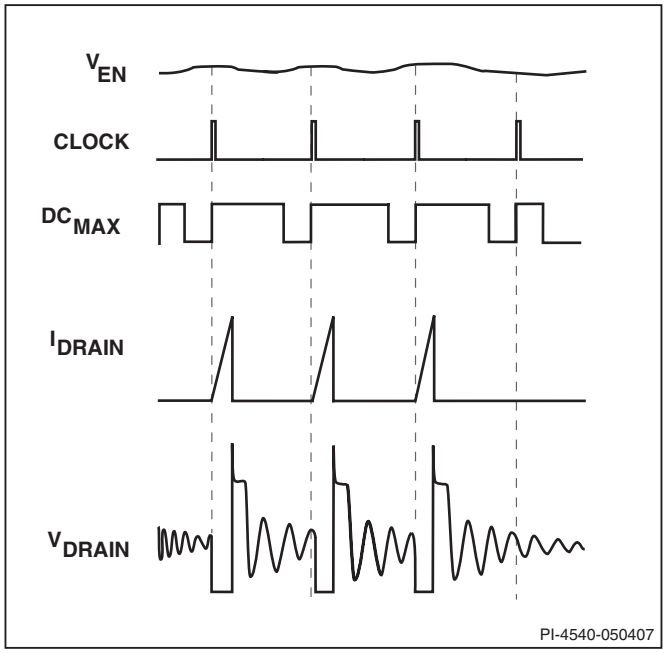


Figure 8. Operation at Medium Loading (f_{OSC} 132 kHz).

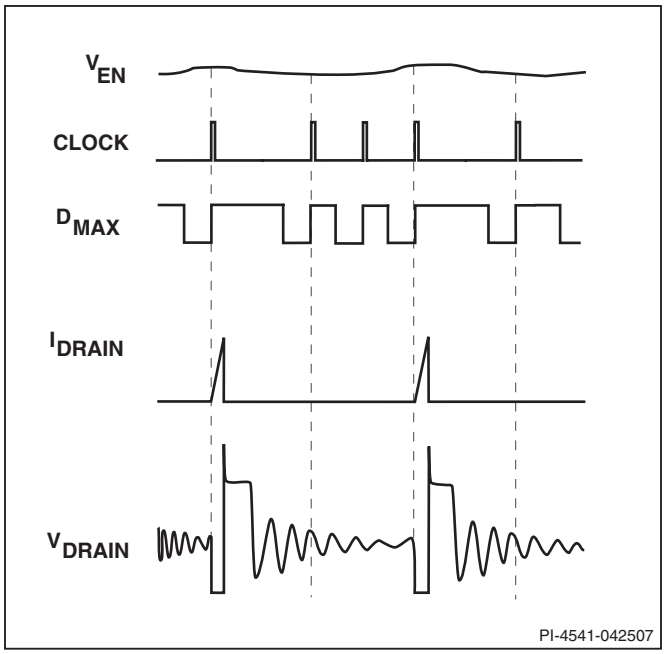


Figure 9. Operation at Very Light Load (f_{OSC} 132 kHz).

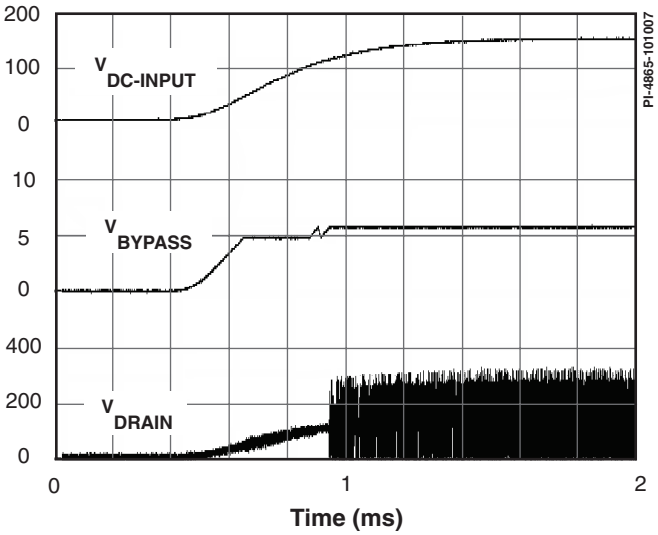


Figure 10. Power-up With Optional External UV Resistor (4 MΩ) Connected to EN/UV Pin.

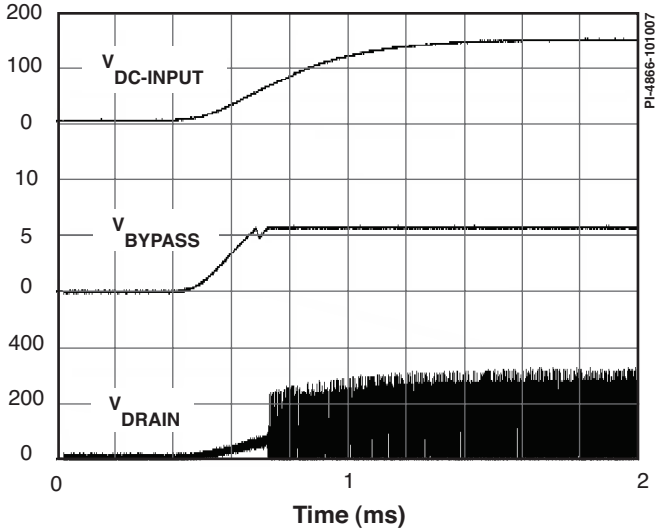


Figure 11. Power-up Without Optional External UV Resistor Connected to EN/UV Pin.

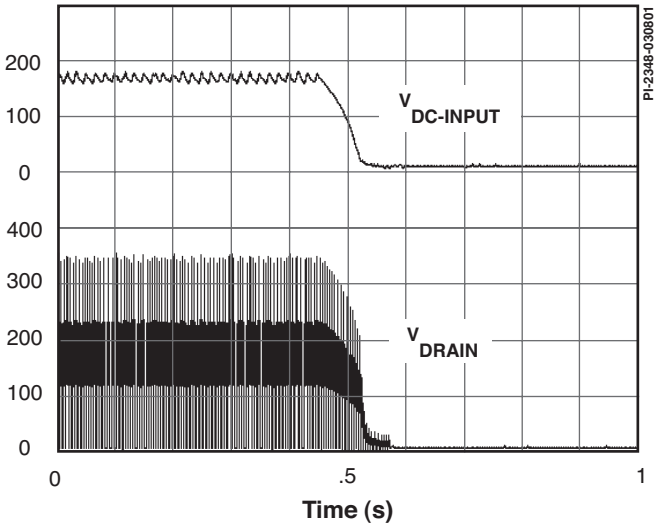


Figure 12. Normal Power-down Timing (Without UV Resistor).

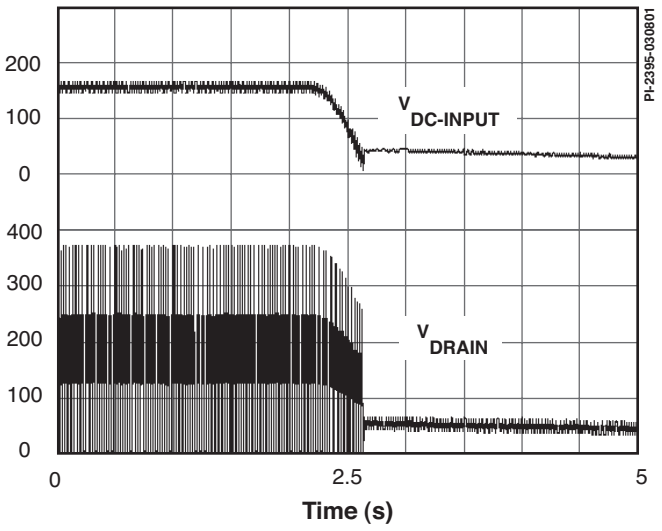


Figure 13. Slow Power-down Timing With Optional External (4 MΩ) UV Resistor Connected to EN/UV Pin.

reduced, and the clock frequency is reduced to half that at the highest current limit level (Figure 8). At very light loads, the current limit will be reduced even further (Figure 9). Only a small percentage of cycles will occur to satisfy the power consumption of the power supply. The response time of the ON/OFF control scheme is very fast compared to PWM control. This provides tight regulation and excellent transient response.

Power Up/Down

The TinySwitch-PK requires only a 0.1 μF capacitor on the BYPASS/MULTI-FUNCTION pin to operate with standard current limit. Because of its small size, the time to charge this capacitor is kept to an absolute minimum, typically 0.6 ms. The time to charge will vary in proportion to the BYPASS/MULTI-FUNCTION pin capacitor value when selecting different current limits. Due to the high bandwidth of the ON/OFF feedback, there is no overshoot at the power supply output. When an external resistor (4 MΩ) is connected from the power supply positive DC input to the EN/UV pin, the power MOSFET switching will be delayed during power-up until the DC line voltage exceeds the threshold (100 V). Figures 10 and 11 show the power-up timing waveform in applications with and without an external resistor (4 MΩ) connected to the EN/UV pin.

During power-down, when an external resistor is used, the power MOSFET will switch for 32 ms after the output loses regulation. The power MOSFET will then remain off without any glitches since the undervoltage function prohibits restart when the line voltage is low.

Figure 12 illustrates a typical power-down timing waveform. Figure 13 illustrates a very slow power-down timing waveform, as in standby applications. The external resistor (4 MΩ) is connected to the EN/UV pin in this case to prevent unwanted restarts.

With the TNY375 and TNY376, no bias winding is needed to provide power to the chip because it draws the power directly from the DRAIN pin (see Functional Description above). This eliminates the cost of a bias winding and associated components. For the TNY377-380 or for applications that require very low no-load power consumption (50 mW), a resistor from a bias winding to the BYPASS/MULTI-FUNCTION pin can provide the power to the chip. The minimum recommended current supplied is $I_{S2} + I_{DIS}$. The BYPASS/MULTI-FUNCTION pin in this case will be clamped at 6.4 V. This method will eliminate the power draw from the DRAIN pin, thereby reducing the no-load power consumption and improving full-load efficiency.

Current Limit Operation

Each switching cycle is terminated when the DRAIN current reaches the current limit of the device. Current limit operation provides good line ripple rejection and relatively constant power delivery independent of input voltage.

BYPASS/MULTI-FUNCTION Pin Capacitor

The BYPASS/MULTI-FUNCTION pin can use a ceramic capacitor as small as 0.1 μF for decoupling the internal power supply of the device. A larger capacitor size can be used to adjust the current limit. A 1 μF BP/M pin capacitor will select a lower current limit equal to the standard current limit of the next smaller device, and a 10 μF BP/M pin capacitor will select a higher current limit equal to the standard current limit of the next larger device. The TNY375 and TNY376 MOSFETs do not have the capability to match the current limit of the next larger devices in the family. The current limit is therefore increased to the maximum capability of their respective MOSFETs. The higher current limit level of the TNY380 is set to 1105 mA typical. The smaller current limit of the TNY375 is set to 325 mA.

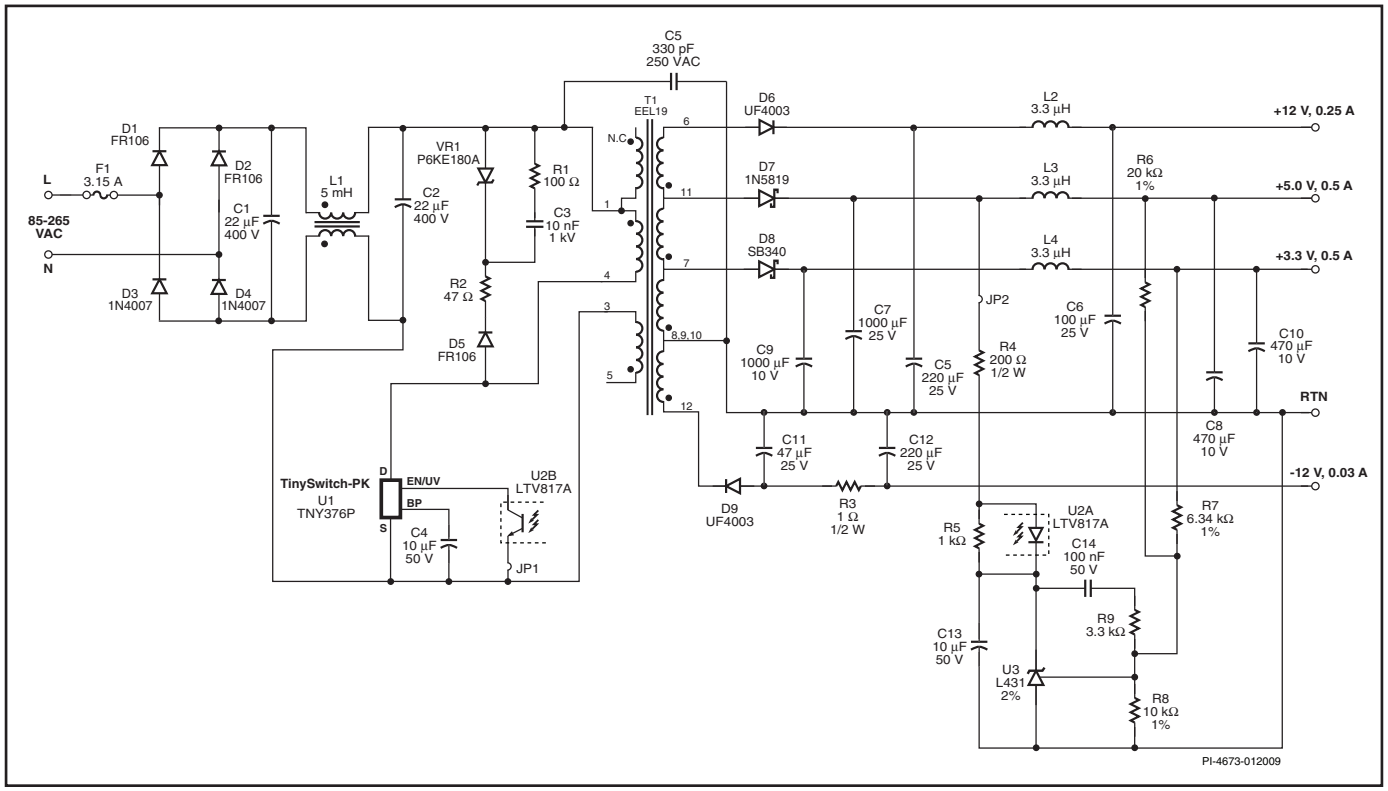


Figure 14. TNY376PN, Four Output, 7.5 W, 13 W Peak Universal Input Power Supply.

Applications Examples

The circuit shown in Figure 14 is a low cost universal AC input, four-output flyback power supply utilizing a TNY376. The continuous output power is 7.5 W with a peak of 13 W. The output voltages are 3.3 V, 5 V, 12 V, and –12 V.

The rectified and filtered input voltage is applied to the primary winding of T1. The other side of the transformer's primary is driven by the integrated MOSFET in U1. Diode D5, C3, R1, R2, and VR1 compose the clamp circuit, limiting the leakage inductance turn-off voltage spike on the DRAIN pin to a safe value. The use of a combination Zener clamp and parallel RC optimizes both EMI and energy efficiency.

Both the 3.3 V and 5 V outputs are sensed through resistors R6 and R7. The voltage across R8 is regulated to 2.5 V by reference IC U3. If the voltage across R8 begins to exceed 2.5 V, then current will flow in the LED inside the optocoupler U2, driven by the cathode of U3. This will cause the transistor of the optocoupler to sink current from the EN/UV pin of U1. When the current exceeds the ENABLE pin threshold current, the next switching cycle is inhibited. Conversely, when the voltage across resistor R8 falls below 2.5 V, and the current out of the ENABLE pin is below the threshold, a conduction cycle is allowed to occur. By adjusting the number of enabled cycles, regulation is maintained. As the load reduces, the number of enabled cycles decreases, lowering the effective switching frequency and scaling switching losses with load. This provides almost constant efficiency down to very light loads, ideal for meeting energy efficiency requirements.

The input filter circuit (C1, L1 and C2) reduces conducted EMI. To improve common mode EMI, this design makes use of E-Shield™ shielding techniques in the transformer, reducing common mode displacement currents, and reducing EMI. These techniques, combined with the frequency jitter of TNY376, give excellent EMI performance, with this design achieving >10 dBµV of margin to EN55022 Class B conducted EMI limits.

For design flexibility, the value of C4 can be selected to pick one of the three current limit options in U4. Doing so allows the designer to select the current limit appropriate for the application.

- Standard current limit is selected with a 0.1 µF BP/M pin capacitor and is the normal choice for typical applications.
- When a 1 µF BP/M pin capacitor is used, the current limit is reduced, offering reduced RMS device currents and therefore improved efficiency, but at the expense of maximum power capability. This is ideal for thermally challenging designs where dissipation must be minimized.
- When a 10 µF BP/M pin capacitor is used, the current limit is increased, extending the power capability for applications requiring higher peak power or continuous power where the thermal conditions allow.

Further flexibility comes from the current limits between adjacent TinySwitch-PK family members being compatible. The reduced current limit of a given device is equal to the standard current limit of the next smaller device, and the increased current limit is equal to the standard current limit of the next larger device.

Key Application considerations

TinySwitch-PK Design Considerations

Output Power Table

Data sheet maximum output power table (Table 1) represents the maximum practical continuous output power level that can be obtained under the following assumed conditions:

1. The minimum DC input voltage is 100 V or higher for 85 VAC input, or 220 V or higher for 230 VAC input or 115 VAC with a voltage doubler. The value of the input capacitance should be sized to meet these criteria for AC input designs.
2. Efficiency of 75%.
3. Minimum data sheet value of I^2f.
4. Transformer primary inductance tolerance of ±10%.
5. Reflected output voltage (V_{OR}) of 135 V.
6. Voltage only output of 12 V with an ultrafast PN rectifier diode.
7. Continuous conduction mode operation with transient K_P* value of 0.25.
8. Increased current limit is selected for peak and open frame power columns and standard current limit for adapter columns.
9. The part is board mounted with SOURCE pins soldered to sufficient area of copper and/or a heat sink is used to keep the SOURCE pin temperature at or below 110 °C for P and G package and 100 °C for D packaged devices.
10. Ambient temperature of 50 °C for open frame designs and 40 °C for sealed adapters.

*K_P. Below a value of 1, K_P is the ratio of ripple to peak primary current. A transient K_P limit of ≥0.25 is recommended to avoid premature termination of switching cycles due to initial current limit (I_{INIT}) being exceeded, which reduces maximum output power capability.

Peak Output Power Table

Product	230 VAC ± 15%			85-265 VAC		
	$I_{LIMIT-PEAKred}$	$I_{LIMITPEAK}$	$I_{LIMIT-PEAKinc}$	$I_{LIMIT-PEAKred}$	$I_{LIMITPEAK}$	$I_{LIMIT-PEAKinc}$
TNY375P/G/D	8.5 W	14.5 W	16.5 W	5.5 W	11.5 W	12.5 W
TNY376P/G/D	10 W	19 W	22 W	6 W	15 W	17 W
TNY377P/G	13 W	23 W	28 W	8 W	18 W	23 W
TNY378P/G	16 W	27.5 W	34 W	10 W	21.5 W	27 W
TNY379P/G	18 W	31.5 W	39 W	12 W	25 W	31 W
TNY380P/G	20 W	36 W	45 W	14 W	28 W	35 W

Table 2. Peak Output Power Capability vs Current Limit Mode Selection.

The values shown in Table 1 for peak power assume operation in $I_{LIMITPEAKinc}$. For reference, Table 2 provides peak output powers for each family member at all three selectable current limit modes.

For both Table 1 and Table 2, the peak output power values are limited electronically, based on minimum device I^2f. Stated differently, with sufficient heat sinking, these values could be delivered indefinitely, but in most cases this would be impractical. Adapter and open frame power values are thermally limited and represent the practical continuous (or average) output power in two common thermal environments.

Over Voltage Protection

The output overvoltage protection provided by TinySwitch-PK uses an internal latch that is triggered by a threshold current of approximately 7 mA into the BYPASS pin. In addition to an internal filter, the BYPASS pin capacitor forms an external filter, providing noise immunity from inadvertent triggering. For the bypass capacitor to be effective as a high frequency filter, it

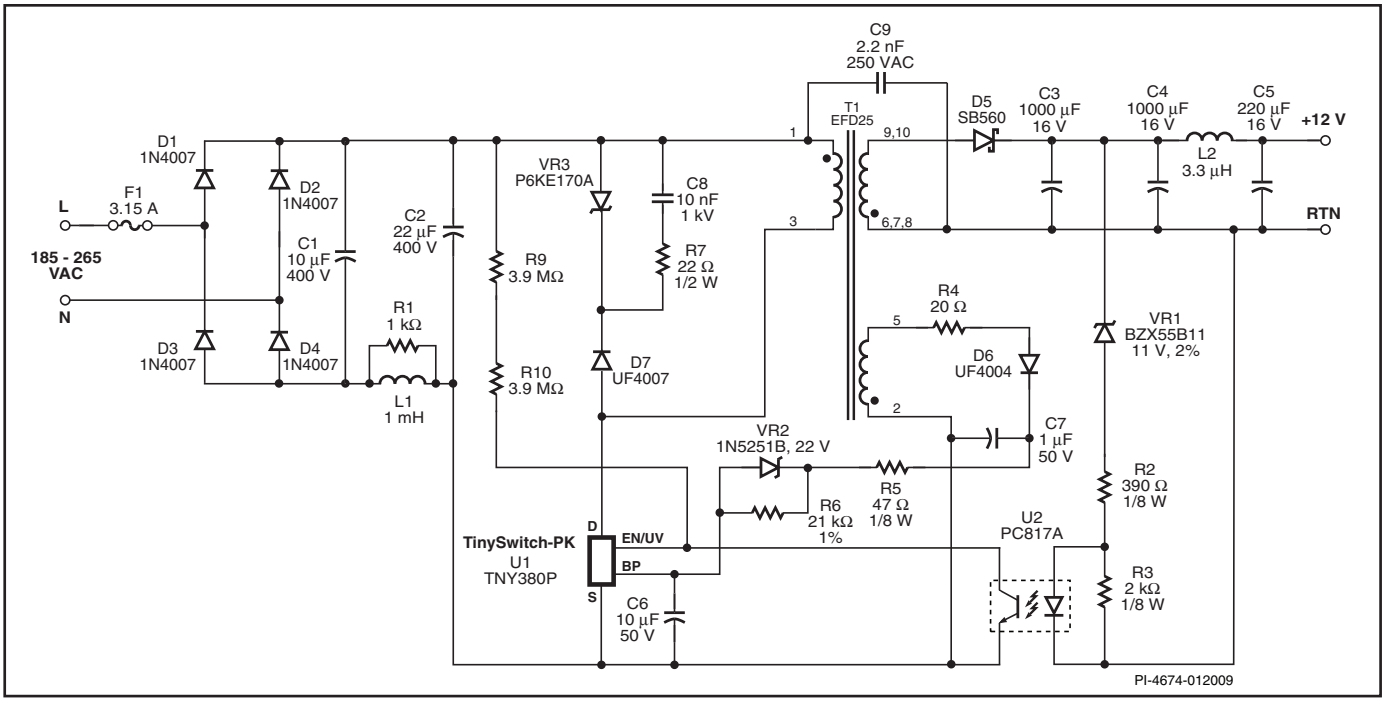


Figure 15. Single 230 VAC Input 20 W Continuous and 45 W Peak Power Supply Using TNY380PN.

should be located as close as possible to the SOURCE and BYPASS pins of the device.

For best performance of the OVP function, it is recommended that a relatively high bias winding voltage is used, in the range of 15 V-30 V. This minimizes the error voltage on the bias winding due to leakage inductance and also ensures adequate voltage during no-load operation from which to supply the IC device consumption.

Selecting the Zener diode voltage to be approximately 6 V above the bias winding voltage (28 V for 22 V bias winding) gives good OVP performance for most designs but can be adjusted to compensate for variations in leakage inductance. Adding additional filtering can be achieved by inserting a low value (10 Ω to 47 Ω) resistor in series with the bias winding diode and/or the OVP Zener, as shown by R4 and R5 in Figure 15. The resistor in series with the OVP Zener also limits the maximum current into the BYPASS pin.

Reducing No-load Consumption
With the exception of the TNY375 and TNY376, a bias winding must be used to provide supply current for the IC. This has the additional benefit of reducing the typical no-load consumption to <60 mW. Select the value of the resistor (R6 in Figure 15) to provide the data sheet supply current equal to $I_{S2} + |I_{DIS}|$. Although in practice the bias voltage falls at low load, the reduction in supply current through R6 is balanced against the reduced IC consumption as the effective switching frequency reduces with load.

Audible Noise
The cycle skipping mode of operation used in the TinySwitch-PK devices can generate audio frequency components in the transformer. To limit this audible noise generation, the transformer should be designed such that the peak core flux density is below 3000 Gauss (300 mT). Following this guideline, and using the standard transformer production technique of dip varnishing practically eliminates audible noise. Vacuum impregnation of the transformer should not be used due to the high primary capacitance and increased losses that results.

Ceramic capacitors that use dielectrics such as Z5U, when used in clamp circuits, may also generate audio noise. If this is the case, try replacing them with a capacitor having a different dielectric or construction such as the film foil or metallized foil type.

TinySwitch-PK Layout Considerations

Single Point Grounding
Use a single point ground connection from the input filter capacitor to the area of copper connected to the SOURCE pins.

When used as an auxiliary supply in a larger converter, a local DC bus decoupling capacitor is recommended. A value of 100 nF is typical.

The bias winding should be returned directly to the input or decoupling capacitor. This routes surge currents away from the device during common mode line surge events.

Bypass Capacitor (C_{BP})
The BYPASS pin capacitor should be located as near as possible to the BYPASS and SOURCE pins using a Kelvin connection. No power current should flow through traces connected to the BYPASS pin capacitor or optocoupler. If using SMD components, a capacitor can be placed underneath the package directly between BP and SOURCE pins.

When using a capacitor value of 1 μF or 10 μF to select the reduced or increased current limit mode, it is recommended that an additional 0.1 μF ceramic capacitor is placed directly between BP and SOURCE pins.

Enable/Undervoltage Pin Node Connections
The EN/UV pin is a low-current, low-voltage pin, and noise coupling can cause poor regulation and/or inaccurate line UV levels. Traces connected to the EN/UV pin must be routed away from any high current or high-voltage switching nodes, including the drain pin and clamp components. This also applies to the placement of the line undervoltage sense resistor (R_{UV}). Drain connected traces must not be routed underneath this component.

TinySwitch-PK determines the presence of the UV resistor via a ~1 μA current into the EN/UV pin at startup. When the under-voltage feature is not used ensure that leakage current into the EN/UV pin is <<1 μA. This prevents false detection of the presence of a UV resistor which may prevent correct start-up.

As the use of no-clean flux may increase leakage currents (by reducing surface resistivity) care should be taken to follow the flux suppliers guidance, specifically avoiding flux contamination.

Placing a 100 kΩ, 5% resistor between BP and EN/UV pins eliminates this requirement by feeding current $>I_{LUV(MAX)}$ into the EN/UV pin.

Primary Loop Area
The area of the primary loop that connects the input filter capacitor, transformer primary, and TinySwitch-PK device should be kept as small as possible.

Primary Clamp Circuit
A clamp is used to limit peak voltage on the DRAIN pin at turn off. This can be achieved by using an RCD clamp or a Zener and diode clamp across the primary winding. In all cases, to minimize EMI, care should be taken to minimize the loop length from the clamp components to the transformer and the TinySwitch-PK device.

Thermal Considerations
The four SOURCE pins are internally connected to the IC lead frame and provide the main path to remove heat from the device. Therefore all the SOURCE pins should be connected to a copper area underneath the TinySwitch-PK integrated circuit to act not only as a single point ground, but also as a heat sink. As this area is connected to the quiet source node, it should be maximized for good heat sinking. Similarly, for axial output diodes, maximize the PCB area connected to the cathode.

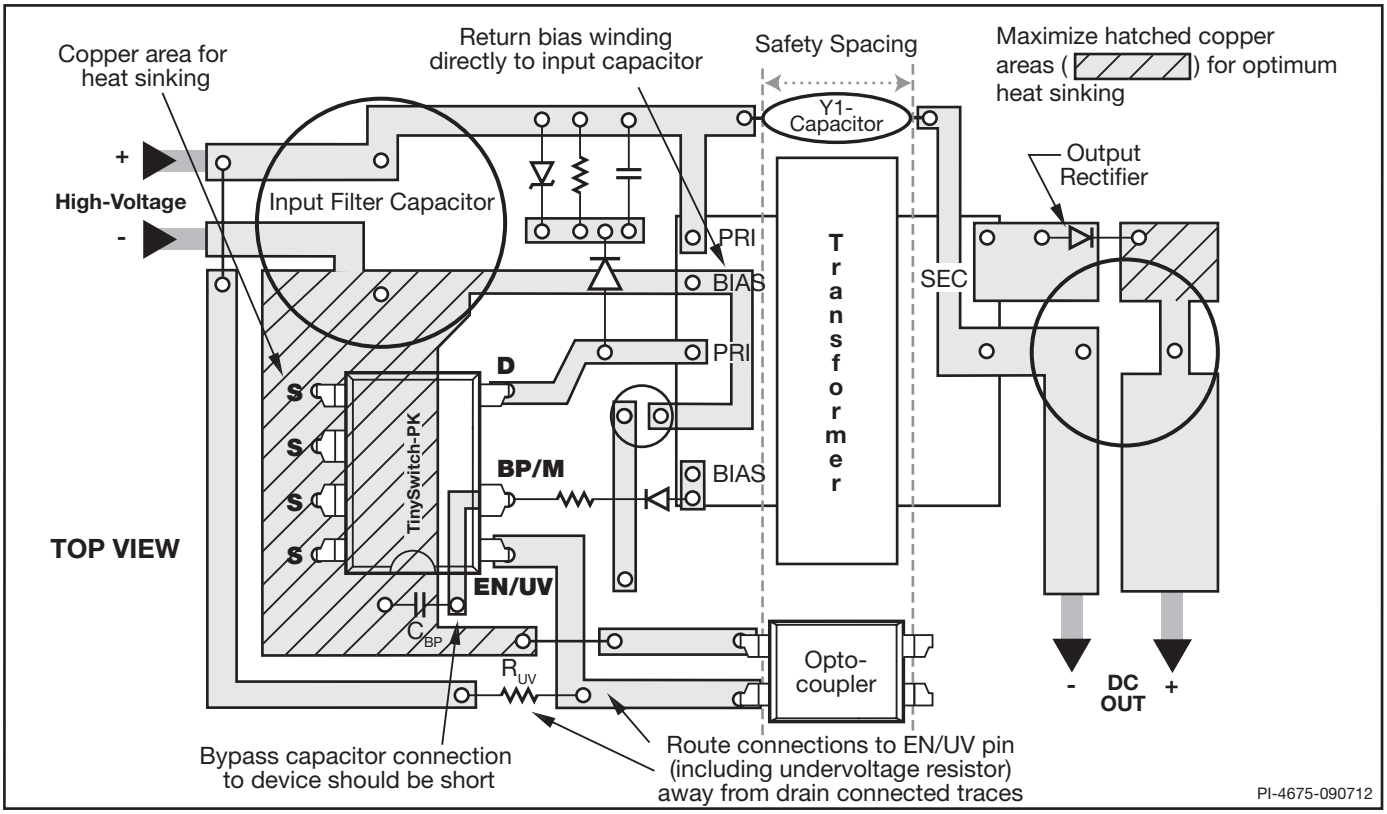


Figure 16. Layout Considerations for TinySwitch-PK Using P Package.

Y-Capacitor

The placement of the Y-capacitor should be directly from the primary input filter capacitor positive terminal to the common/return terminal of the transformer secondary. Such a placement will route high magnitude common mode surge currents away from the TinySwitch-PK device. Note – if an input π (C, L, C) EMI filter is used, then the inductor in the filter should be placed between the negative terminals on the input filter capacitors.

Optocoupler

Place the optocoupler physically close to the TinySwitch-PK device to minimize the primary side trace lengths. Keep the high current, high voltage drain and clamp traces away from the optocoupler to prevent noise pick up.

Output Diode

For best performance, the area of the loop connecting the secondary winding, the Output Diode, and the Output Filter Capacitor should be minimized. In addition, for axial diodes, sufficient copper area should be provided at the anode and cathode terminal of diode for heat sinking. A larger area is preferred at the quiet cathode terminal. A large anode area can increase high frequency radiated EMI.

Quick Design Checklist

As with any power supply design, all TinySwitch-PK designs should be verified on the bench to make sure that component specifications are not exceeded under worst case conditions. The following minimum set of tests is strongly recommended:

1. Maximum drain voltage – Verify the V_{DS} does not exceed 650 V at highest input voltage and peak (overload) output power. The 50 V margin to the 700 V BV_{DSS} specification gives margin for design variation.
2. Maximum drain current – At maximum ambient temperature, maximum input voltage, and peak output (overload) power, verify drain current waveforms for any signs of transformer saturation and excessive leading edge current spikes at startup. Repeat under steady state conditions and verify that the leading edge current spike event is below I_{INIT} at the end of the $t_{LEB(Min)}$. Under all conditions the maximum drain current should be below the specified absolute maximum ratings.
3. Thermal Check – At specified maximum output power, minimum input voltage, and maximum ambient temperature, verify that the temperature specifications are not exceeded for TinySwitch-PK device, transformer, output diode, and output capacitors. Enough thermal margin should be allowed for part-to-part variation of the $R_{DS(ON)}$ of TinySwitch-PK device as specified in the data sheet. Under low-line maximum power, a maximum TinySwitch-PK device SOURCE pin temperature of 110 °C is recommended to allow for these variations.

Design Tools

Up-to-date information on design tools can be found at the Power Integrations web site: www.powerint.com.

Absolute Maximum Ratings[1,4]

DRAIN Voltage .....-0.3 V to 700 V
DRAIN Peak Current: TNY375 ..... 0.6 A[5]
TNY376 ..... 0.8 A[5]
TNY377 ..... 1.4 A[5]
TNY378 .....2.2 A[5]
TNY379 ..... 2.9 A[5]
TNY380 ..... 4.3 A[5]
EN/UV Voltage ..... -0.3 V to 9 V
EN/UV Current ..... 100 mA
BP/M Voltage ....-0.3 V to 9 V
Storage Temperature ..... -65 °C to 150 °C
Operating Junction Temperature[2]..... -40 °C to 150 °C
Lead Temperature[3] .....260 °C

Notes:
1. All voltages referenced to SOURCE, T_A = 25 °C.
2. Normally limited by internal circuitry.
3. 1/16 in. from case for 5 seconds.
4. Maximum ratings specified may be applied one at a time without causing permanent damage to the product. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect product reliability.
5. The peak DRAIN current is allowed while the DRAIN voltage is simultaneously less than 400 V.

Thermal Impedance

Thermal Impedance: P or G Package:
(θ_{JA}) .....70 °C/W[2]; 60 °C/W[3]
(θ_{JC})[1] ....11 °C/W
D Package:
(θ_{JA}) .....100 °C/W[2]; 80 °C/W[3]
(θ_{JC})[2] ....30 °C/W

Notes:
1. Measured on the SOURCE pin close to plastic interface.
2. Soldered to 0.36 sq. in. (232 mm^2), 2 oz. (610 g/m^2) copper clad.
3. Soldered to 1 sq. in. (645 mm^2), 2 oz. (610 g/m^2) copper clad.

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 to 125 °C See Figure 17 (Unless Otherwise Specified)		Min	Typ	Max	Units
Control Functions							
Output Frequency See Note A	f_{OSC}	State Machine at Highest Current Limit Level T_J = 25 °C	Average	248	264	280	kHz
			pk-pk Jitter		16		
	f_{OSC}-Low	All Lower Current Limit Levels T_J = 25 °C	Average		132		
			pk-pk Jitter		8		
Maximum Duty Cycle	DC_{MAX}	S1 Open		62	65		%
EN/UV Pin Upper Turnoff Threshold Current	I_{DIS}			-150	-115	-90	µA
EN/UV Pin Voltage	V_{EN}	$I_{EN/UV}$ = 25 µA		1.8	2.2	2.6	V
		$I_{EN/UV}$ = -25 µA		0.8	1.2	1.6	
DRAIN Supply Current	I_{S1}	EN/UV Current > I_{DIS} (MOSFET Not Switching) See Note B			290		µA
	I_{S2}	EN/UV Open (MOSFET Switching at f_{OSC}) See Note C	TNY375		385	520	µA
			TNY376		460	600	
			TNY377		570	710	
			TNY378		740	900	
			TNY379		870	1060	
			TNY380		1100	1350	

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 to 125 °C See Figure 17 (Unless Otherwise Specified)		Min	Typ	Max	Units
Control Functions (cont.)							
BP/M Pin Charge Current	I_{CH1}	$V_{BP/M}$ = 0 V, T_J = 25 °C See Note D, E	TNY375-378	-8.3	-5.4	-2.5	µA
			TNY379-380	-9.7	-7.1	-3.9	
	I_{CH2}	$V_{BP/M}$ = 4 V, T_J = 25 °C See Note D, E	TNY375-378	-5	-3.5	-1.5	
			TNY379-380	-6.6	-4.8	-2.1	
BP/M Pin Voltage	$V_{BP/M}$	See Note D		5.6	5.85	6.15	V
BP/M Pin Voltage Hysteresis	$V_{BP/MH}$			0.80	0.95	1.20	V
BP/M Pin Shunt Voltage	V_{SHUNT}	I_{BP} = 2 mA		6.0	6.4	6.7	V
EN/UV Pin Line Under-voltage Threshold	I_{LUV}	T_J = 25 °C		22.5	25	27.5	µA
Circuit Protection							
Peak Current Limit (BP/M Capacitor = 0.1 µF) See Note E	$I_{LIMITPEAK}$	di/dt = 72 mA/µs T_J = 25 °C See Note F	TNY375P	330	355	380	mA
			TNY375G/D	330	355	387	
		di/dt = 91 mA/µs T_J = 25 °C See Note F	TNY376P	423	455	487	
			TNY376G/D	423	455	496	
		di/dt = 117 mA/µs T_J = 25 °C See Note F	TNY377P	544	585	626	
			TNY377G	544	585	638	
		di/dt = 143 mA/µs T_J = 25 °C See Note F	TNY378P	665	715	765	
			TNY378G	665	715	779	
		di/dt = 169 mA/µs T_J = 25 °C See Note F	TNY379P	786	845	904	
			TNY379G	786	845	921	
		di/dt = 195 mA/µs T_J = 25 °C See Note F	TNY380P	907	975	1043	
			TNY380G	907	975	1063	
Peak Current Limit (BP/M Capacitor = 1 µF) See Note E	$I_{LIMITPEAKred}$	di/dt = 72 mA/µs T_J = 25 °C See Note F	TNY375P	302	325	361	mA
			TNY375G/D	302	325	367	
		di/dt = 91 mA/µs T_J = 25 °C See Note F	TNY376P	330	355	391	
			TNY376G/D	330	355	401	
		di/dt = 117 mA/µs T_J = 25 °C See Note F	TNY377P	423	455	501	
			TNY377G	423	455	514	
		di/dt = 143 mA/µs T_J = 25 °C See Note F	TNY378P	544	585	644	
			TNY378G	544	585	661	
		di/dt = 169 mA/µs T_J = 25 °C See Note F	TNY379P	665	715	787	
			TNY379G TNY380GN	665	715	808	
		di/dt = 195 mA/µs T_J = 25 °C See Note F	TNY380P	786	845	930	
			TNY380G	786	845	955	

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 to 125 °C See Figure 17 (Unless Otherwise Specified)		Min	Typ	Max	Units
Circuit Protection (cont.)							
Peak Current Limit (BP/M Capacitor = 10 µF) See Note E	$I_{LIMITPEAKinc}$	di/dt = 72 mA/µs T_J = 25 °C See Note F	TNY375P	349	375	413	mA
			TNY375G/D	349	375	424	
		di/dt = 91 mA/µs T_J = 25 °C See Note F	TNY376P	465	500	550	
			TNY376G/D	465	500	565	
		di/dt = 117 mA/µs T_J = 25 °C See Note F	TNY377P	665	715	787	
			TNY377G	665	715	808	
		di/dt = 143 mA/µs T_J = 25 °C See Note F	TNY378P	786	845	930	
			TNY378G	786	845	955	
		di/dt = 169 mA/µs T_J = 25 °C See Note F	TNY379P	907	975	1073	
			TNY379G	907	975	1102	
		di/dt = 195 mA/µs T_J = 25 °C See Note F	TNY380P	1028	1105	1216	
			TNY380G	1028	1105	1249	
Power Coefficient	I^2f	$I^2f = I_{LIMITPEAK(TYP)}^2 \times f_{OSC(TYP)}$ T_J = 25 °C BP/M Capacitor = 0.1 µF	TNY375-380P	0.9 × I^2f	I^2f	1.12 × I^2f	A^2Hz
			TNY375-376D	0.9 × I^2f	I^2f	1.16 × I^2f	
			TNY375-380G	0.9 × I^2f	I^2f	1.16 × I^2f	
		$I^2f = I_{LIMITPEAKred(TYP)}^2 \times f_{OSC(TYP)}$ T_J = 25 °C BP/M Capacitor = 1 µF	TNY375-380P	0.9 × I^2f	I^2f	1.16 × I^2f	
			TNY375-376D	0.9 × I^2f	I^2f	1.20 × I^2f	
			TNY375-380G	0.9 × I^2f	I^2f	1.20 × I^2f	
		$I^2f = I_{LIMITPEAKinc(TYP)}^2 \times f_{OSC(TYP)}$ T_J = 25 °C BP/M Capacitor = 10 µF	TNY375-380P	0.9 × I^2f	I^2f	1.16 × I^2f	
			TNY375-376D	0.9 × I^2f	I^2f	1.20 × I^2f	
			TNY375-380G	0.9 × I^2f	I^2f	1.20 × I^2f	
Initial Current Limit	I_{INIT}	See Figure 20 T_J = 25 °C, See Note G		0.75 × $I_{LIMIT(MIN)}$			mA
Leading Edge Blanking Time	t_{LEB}	T_J = 25 °C See Note G	TNY375-377	190	235		ns
			TNY378-380	145	190		
Current Limit Delay	t_{ILD}	T_J = 25 °C See Note G, H			200		ns
Thermal Shutdown Temperature	T_{SD}			135	142	150	°C
Thermal Shutdown Hysteresis	T_{SDH}				75		°C
BP/M Pin Shutdown Threshold Current	I_{SD}			4	7	9	mA
BP/M Pin Power-Up Reset Threshold Voltage	$V_{BP/M(RESET)}$			1.6	2.6	3.6	V

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 to 125 °C See Figure 17 (Unless Otherwise Specified)		Min	Typ	Max	Units
Output							
ON-State Resistance	$R_{DS(ON)}$	TNY375 I_D = 28 mA	T_J = 25 °C		19	22	Ω
			T_J = 100 °C		29	33	
		TNY376 I_D = 35 mA	T_J = 25 °C		14	16	
			T_J = 100 °C		21	24	
		TNY377 I_D = 45 mA	T_J = 25 °C		7.8	9.0	
			T_J = 100 °C		11.7	13.5	
		TNY378 I_D = 55 mA	T_J = 25 °C		5.2	6.0	
			T_J = 100 °C		7.8	9.0	
		TNY379 I_D = 65 mA	T_J = 25 °C		3.9	4.5	
			T_J = 100 °C		5.8	6.7	
		TNY380 I_D = 75 mA	T_J = 25 °C		2.6	3.0	
			T_J = 100 °C		3.9	4.5	
OFF-State Drain Leakage Current	I_{DSS1}	$V_{BP/M}$ = 6.2 V $V_{EN/UV}$ = 0 V V_{DS} = 560 V T_J = 125 °C See Note I	TNY375-376			50	µA
			TNY377-378			100	
			TNY379-380			200	
	I_{DSS2}	$V_{BP/M}$ = 6.2 V $V_{EN/UV}$ = 0 V	V_{DS} = 375 V, T_J = 50 °C See Note G, I		15		
Breakdown Voltage	BV_{DSS}	V_{BP} = 6.2 V, $V_{EN/UV}$ = 0 V, See Note J, T_J = 25 °C		700			V
DRAIN Supply Voltage				50			V
Auto-Restart ON-Time At f_{osc}	t_{AR}	T_J = 25 °C See Note K			32		ms
Auto-Restart Duty Cycle	DC_{AR}	T_J = 25 °C			3		%

NOTES:

A. For all BP/M pin capacitor values.

B. I_{S1} is an accurate estimate of device controller current consumption at no-load, since operating frequency is so low under these conditions. Total device consumption at no-load is the sum of I_{S1} and I_{DSS2}.

C. Since the output MOSFET is switching, it is difficult to isolate the switching current from the supply current at the DRAIN. An alternative is to measure the BP/M pin current at 6.1 V.

D. BP/M pin is not intended for sourcing supply current to external circuitry.

E. To ensure correct current limit, it is recommended that nominal 0.1 μF / 1 μF / 10 μF capacitors are used. In addition, the BP/M capacitor value tolerance should be equal to or better than indicated below across the ambient temperature range of the target application. The minimum and maximum capacitor values are guaranteed by characterization.

Nominal BP/M Pin Cap Value	**Tolerance Relative to Nominal Capacitor Value**	
	Min	Max
0.1 μF	-60%	+100%
1 μF	-50%	+100%
10 μF	-50%	NA

F. For current limit at other di/dt values, refer to Figure 24. Measurements made with device self-biased.

G. This parameter is derived from characterization.

H. This parameter is derived from the change in current limit measured at 1X and 4X of the di/dt shown in the I_{LIMIT} specification.

I. I_{DSS1} is the worst-case OFF state leakage specification at 80% of BV_{DSS} and maximum operating junction temperature. I_{DSS2} is a typical specification under worst-case application conditions (rectified 265 VAC) for no-load consumption calculations.

J. Breakdown voltage may be checked against minimum BV_{DSS} specification by ramping the DRAIN pin voltage up to but not exceeding minimum BV_{DSS}.

K. Auto-restart on time has the same temperature characteristics as the oscillator (inversely proportional to frequency).

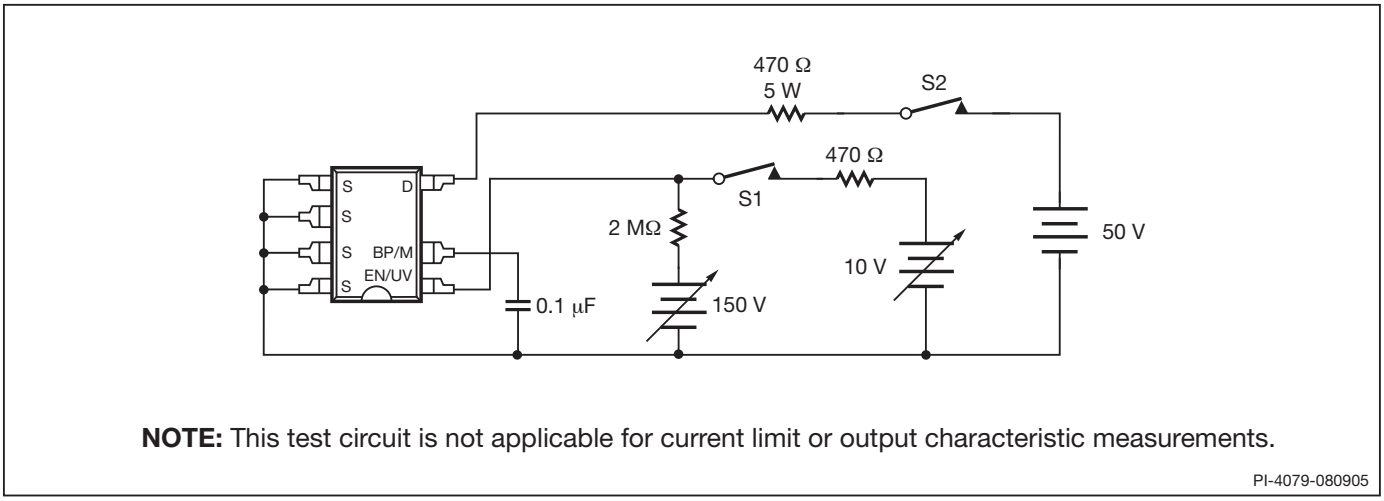


Figure 17. General Test Circuit.

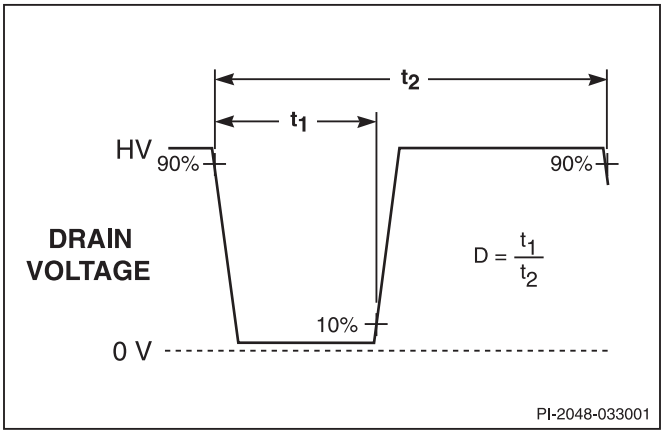


Figure 18. Duty Cycle Measurement.

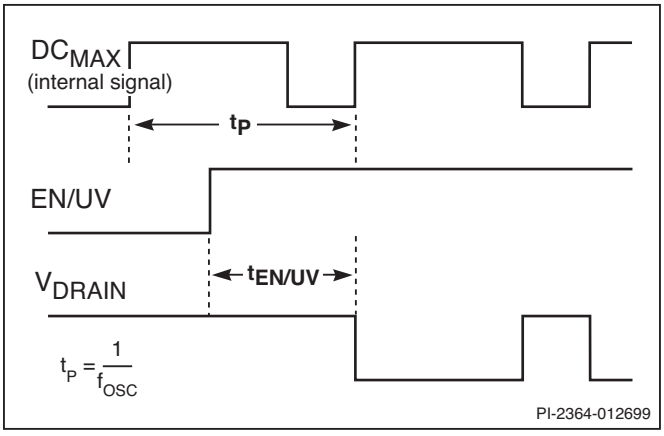


Figure 19. Output Enable Timing.

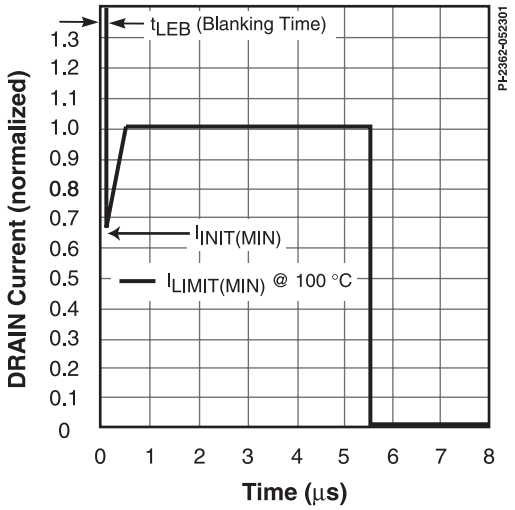


Figure 20. Current Limit Envelope at f_{OSC} = 132 kHz.

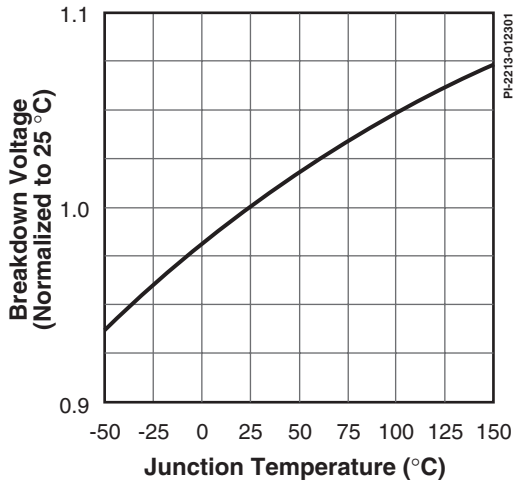


Figure 21. Breakdown vs. Temperature.

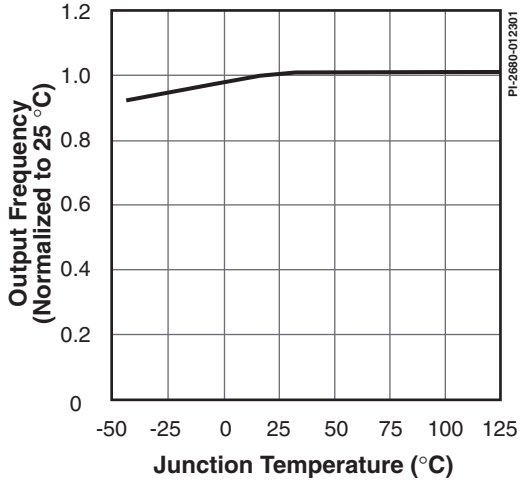


Figure 22. Frequency vs. Temperature.

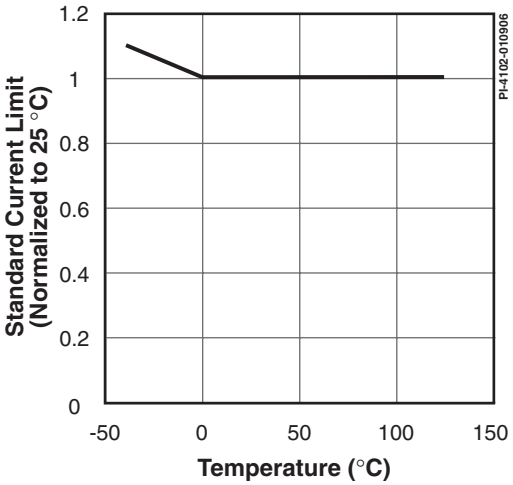


Figure 23. Standard Current Limit vs. Temperature.

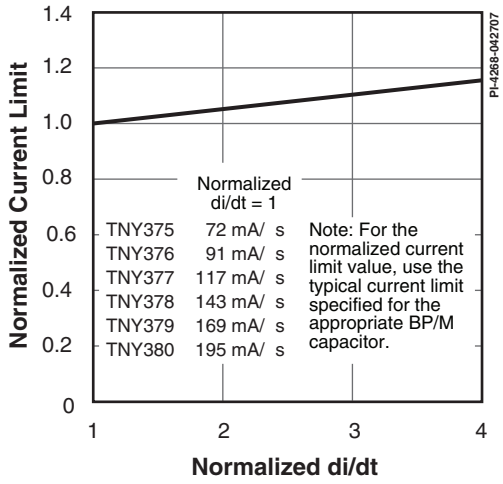


Figure 24. Current Limit vs. di/dt.

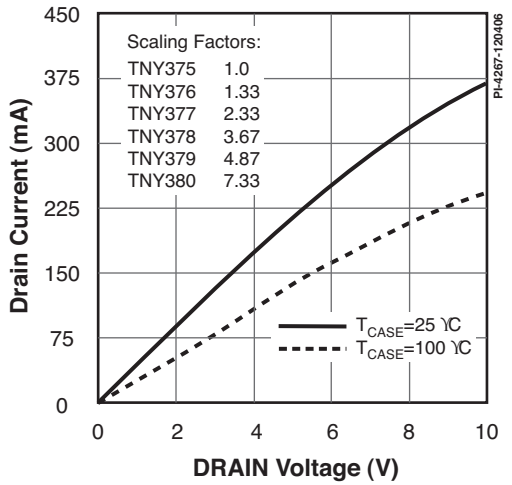


Figure 25. Output Characteristics.

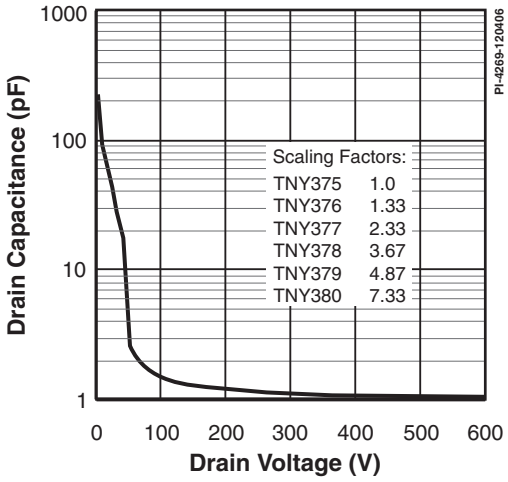


Figure 26. C_{OSS} vs. Drain Voltage.

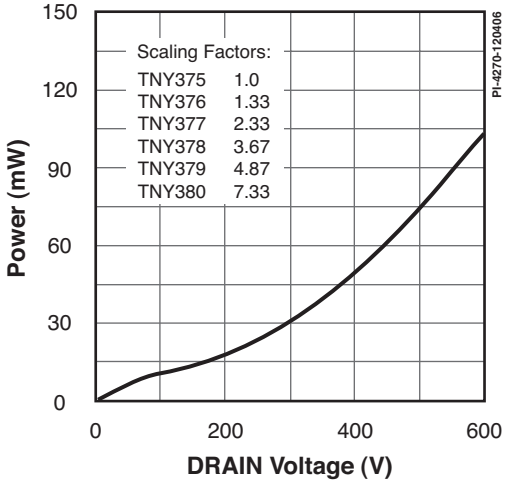


Figure 27. Drain Capacitance Power.

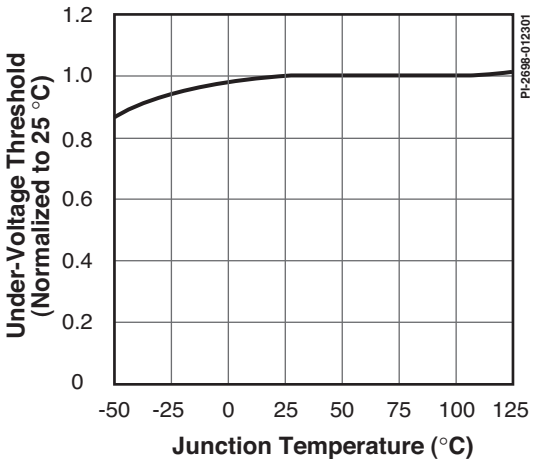
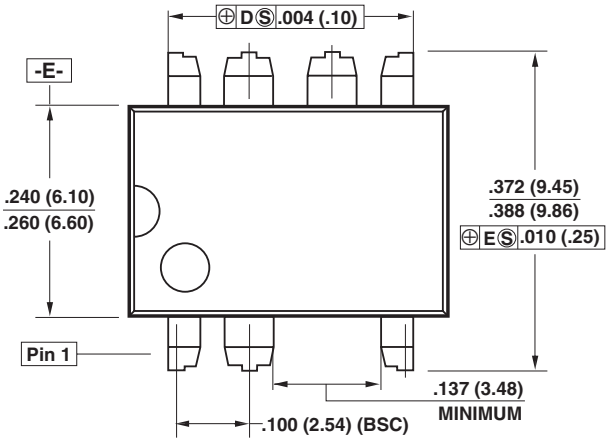
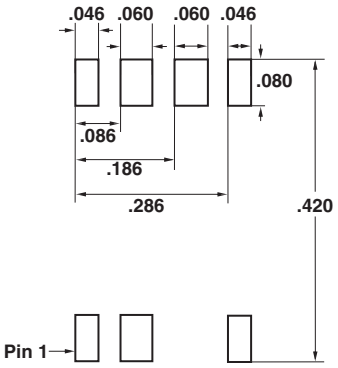


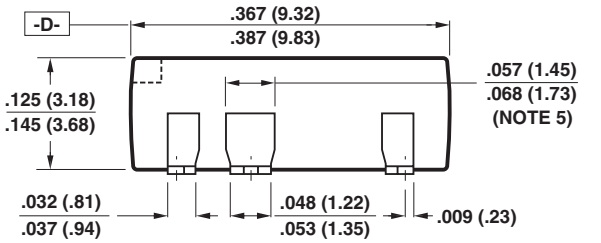
Figure 28. Undervoltage Threshold vs. Temperature.

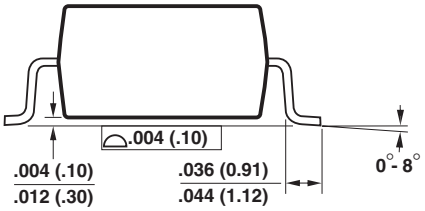
SMD-8C (G Package)





Solder Pad Dimensions





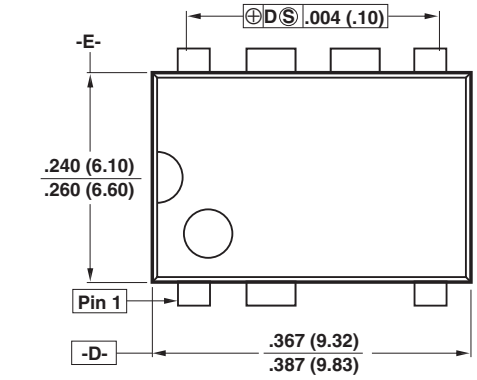
Notes:

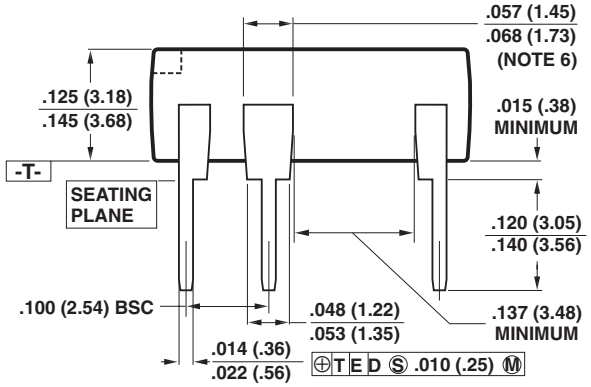
1. **Controlling dimensions are inches. Millimeter sizes are shown in parentheses.**
2. **Dimensions shown do not include mold flash or other protrusions. Mold flash or protrusions shall not exceed .006 (.15) on any side.**
3. **Pin locations start with Pin 1, and continue counter-clockwise to Pin 8 when viewed from the top. Pin 3 is omitted.**
4. **Minimum metal to metal spacing at the package body for the omitted lead location is .137 inch (3.48 mm).**
5. **Lead width measured at package body.**
6. **D and E are referenced datums on the package body.**

G08C

PI-4015-101507

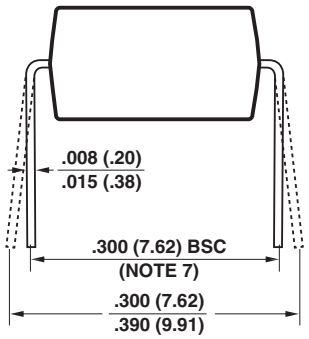
PDIP-8C (P Package)





Notes:

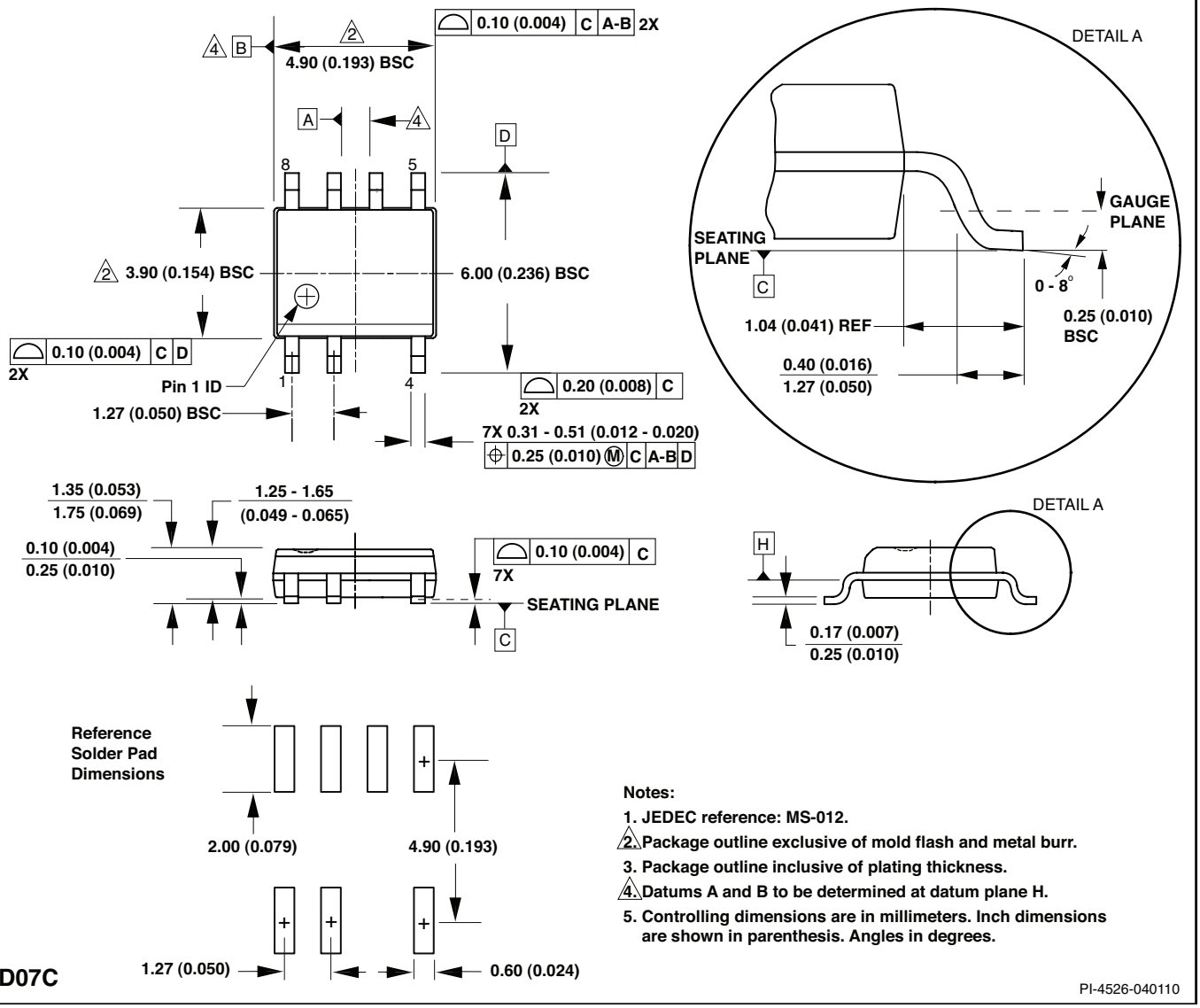
1. **Package dimensions conform to JEDEC specification MS-001-AB (Issue B 7/85) for standard dual-in-line (DIP) package with .300 inch row spacing.**
2. **Controlling dimensions are inches. Millimeter sizes are shown in parentheses.**
3. **Dimensions shown do not include mold flash or other protrusions. Mold flash or protrusions shall not exceed .006 (.15) on any side.**
4. **Pin locations start with Pin 1, and continue counter-clockwise to Pin 8 when viewed from the top. The notch and/or dimple are aids in locating Pin 1. Pin 3 is omitted.**
5. **Minimum metal to metal spacing at the package body for the omitted lead location is .137 inch (3.48 mm).**
6. **Lead width measured at package body.**
7. **Lead spacing measured with the leads constrained to be perpendicular to plane T.**



P08C

PI-3933-040110

SO-8C (D Package)



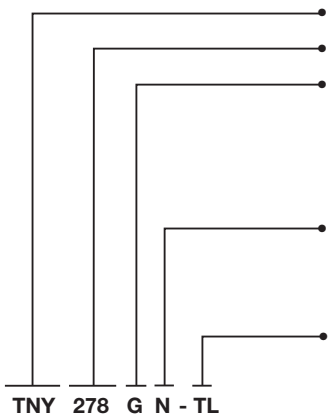
Notes:

1. JEDEC reference: MS-012.
2. Package outline exclusive of mold flash and metal burr.
3. Package outline inclusive of plating thickness.
4. Datums A and B to be determined at datum plane H.
5. Controlling dimensions are in millimeters. Inch dimensions are shown in parenthesis. Angles in degrees.

D07C

PI-4526-040110

Part Ordering Information



- **TinySwitch Product Family**
- **Series Number**
- **Package Identifier**

G	Plastic Surface Mount SMD-8C
P	Plastic DIP-8C
D	Plastic Surface Mount SO-8C

- **Lead Finish**

N	Pure Matte Tin (Pb-Free) (Not available in D Package)
G	RoHS Compliant and Halogen Free (D Package only)

- **Tape & Reel and Other Options**

Blank	Standard Configuration
TL	Tape & Reel, 1000 pcs min./mult., G Package, 2500 pcs min./mult., D Package

Revision	Notes	Date
A	Release final data sheet.	05/07
B	Added G package and updated Limits.	11/07
C	Updated Part Ordering Information section with Halogen Free and added D package parts.	07/09
C	Updated Figure 16 layout schematic.	09/12

For the latest updates, visit our website: www.powerint.com

Power Integrations reserves the right to make changes to its products at any time to improve reliability or manufacturability. Power Integrations does not assume any liability arising from the use of any device or circuit described herein. POWER INTEGRATIONS MAKES NO WARRANTY HEREIN AND SPECIFICALLY DISCLAIMS ALL WARRANTIES INCLUDING, WITHOUT LIMITATION, THE IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF THIRD PARTY RIGHTS.

Patent Information

The products and applications illustrated herein (including transformer construction and circuits external to the products) may be covered by one or more U.S. and foreign patents, or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations patents may be found at www.powerint.com. Power Integrations grants its customers a license under certain patent rights as set forth at http://www.powerint.com/ip.htm.

Life Support Policy

POWER INTEGRATIONS PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF POWER INTEGRATIONS. As used herein:

1. A Life support device or system is one which, (i) is intended for surgical implant into the body, or (ii) supports or sustains life, and (iii) whose failure to perform, when properly used in accordance with instructions for use, can be reasonably expected to result in significant injury or death to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

Power Integrations Worldwide Sales Support Locations

World Headquarters
5245 Hellyer Avenue
San Jose, CA 95138, USA.
Main: +1-408-414-9200
Customer Service:
Phone: +1-408-414-9665
Fax: +1-408-414-9765
e-mail: usasales@powerint.com

China (Shanghai)
Rm 1601/1610, Tower 1,
Kerry Everbright City
No. 218 Tianmu Road West,
Shanghai, P.R.C. 200070
Phone: +86-21-6354-6323
Fax: +86-21-6354-6325
e-mail: chinasales@powerint.com

China (ShenZhen)
3rd Floor, Block A,
Zhongtou International Business
Center, No. 1061, Xiang Mei Rd,
FuTian District, ShenZhen,
China, 518040
Phone: +86-755-8379-3243
Fax: +86-755-8379-5828
e-mail: chinasales@powerint.com

Germany
Lindwurmstrasse 114
80337 Munich
Germany
Phone: +49-895-527-39110
Fax: +49-895-527-39200
e-mail: eurosales@powerint.com

India
#1, 14th Main Road
Vasanthanagar
Bangalore-560052 India
Phone: +91-80-4113-8020
Fax: +91-80-4113-8023
e-mail: indiasales@powerint.com

Italy
Via Milanese 20, 3rd. Fl.
20099 Sesto San Giovanni (MI)
Italy
Phone: +39-024-550-8701
Fax: +39-028-928-6009
e-mail: eurosales@powerint.com

Japan
Kosei Dai-3 Bldg.
2-12-11, Shin-Yokomana,
Kohoku-ku
Yokohama-shi Kanagwan
222-0033 Japan
Phone: +81-45-471-1021
Fax: +81-45-471-3717
e-mail: japansales@powerint.com

Korea
RM 602, 6FL
Korea City Air Terminal B/D, 159-6
Samsung-Dong, Kangnam-Gu,
Seoul, 135-728, Korea
Phone: +82-2-2016-6610
Fax: +82-2-2016-6630
e-mail: koreasales@powerint.com

Singapore
51 Newton Road
#15-08/10 Goldhill Plaza
Singapore, 308900
Phone: +65-6358-2160
Fax: +65-6358-2015
e-mail: singaporesales@powerint.com

Taiwan
5F, No. 318, Nei Hu Rd., Sec. 1
Nei Hu Dist.
Taipei, Taiwan 114, R.O.C.
Phone: +886-2-2659-4570
Fax: +886-2-2659-4550
e-mail: taiwansales@powerint.com

Europe HQ
1st Floor, St. James's House
East Street, Farnham
Surrey GU9 7TJ
United Kingdom
Phone: +44 (0) 1252-730-141
Fax: +44 (0) 1252-727-689
e-mail: eurosales@powerint.com

Applications Hotline
World Wide +1-408-414-9660

Applications Fax
World Wide +1-408-414-9760