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C8051F336/7/8/9

Mixed-Signal Byte-Programmable EPROM MCU

Analog Peripherals
- **10-Bit ADC (‘F336/8 only)**
  - Up to 200 ksps
  - Up to 20 external single-ended or differential inputs
  - VREF from on-chip VREF, external pin or V_{DD}
  - Internal or external start of conversion source
  - Built-in temperature sensor
- **10-Bit Current Output DAC (‘F336/8 only)**
- **Comparator**
  - Programmable hysteresis and response time
  - Configurable as interrupt or reset source

On-Chip Debug
- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, inspect/modify memory and registers
- Superior performance to emulation systems using ICE-chips, target pods, and sockets
- Low cost, **complete** development kit

Supply Voltage 2.7 to 3.6 V
- Built-in voltage supply monitor

High-Speed 8051 µC Core
- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz clock
- Expanded interrupt handler

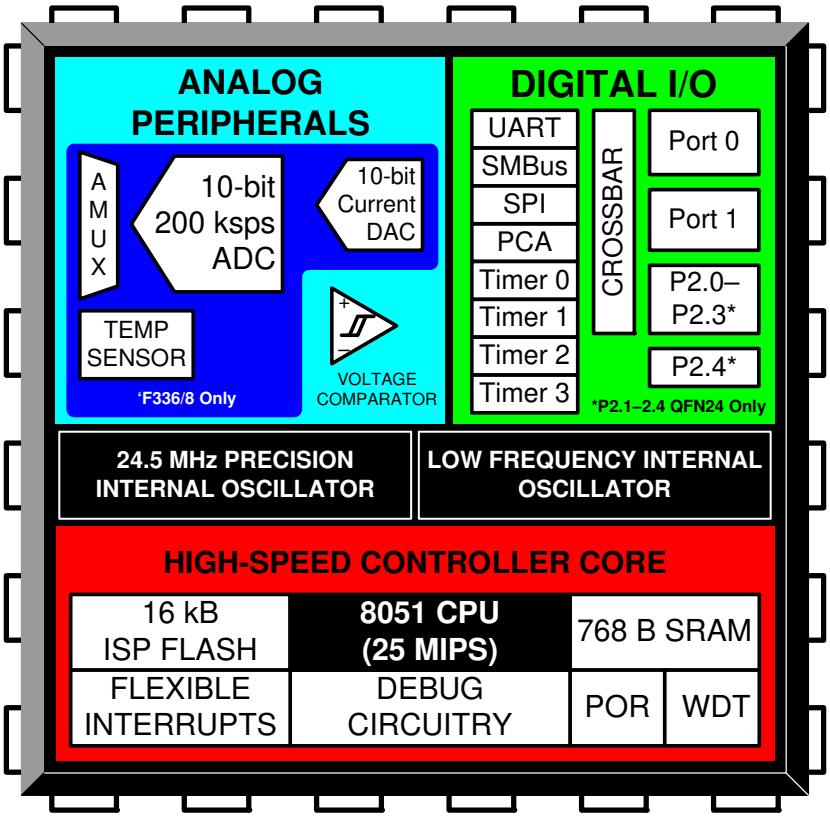
Temperature Range: –40 to +85 °C

Memory
- 768 bytes internal data RAM (256 + 512)
- 16 kB Flash; In-system programmable in 512-byte Sectors (512 bytes are reserved)

Digital Peripherals
- 21 or 17 Port I/O; All 5 V tolerant with high sink current
- **Pin-compatible with C8051F330 family of MCUs**
- Hardware enhanced UART, SMBus™ (I^2C compatible), and enhanced SPI™ serial ports
- Four general purpose 16-bit counter/timers
- 16-Bit programmable counter array (PCA) with three capture/compare modules and enhanced PWM functionality
- Real time clock mode using timer and crystal

Clock Sources
- 24.5 MHz ±2% Oscillator
  - Supports crystal-less UART operation
  - Low-power suspend mode with fast wake time
- 80/20/40/10 kHz low-frequency, low-power oscillator
- External oscillator: Crystal, RC, C, or clock (1 or 2 pin modes)
- Can switch between clock sources on-the-fly; useful in power saving modes

20 or 24-Pin QFN (4 x 4 mm)



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1. System Overview

C8051F336/7/8/9 devices are fully integrated mixed-signal System-on-a-Chip MCUs. Highlighted features are listed below. Refer to **Section "2. Ordering Information" on page 18** for specific product feature selection and part ordering numbers.

- High-speed pipelined 8051-compatible microcontroller core (up to 25 MIPS)
- In-system, full-speed, non-intrusive debug interface (on-chip)
- True 10-bit 200 ksps 20-channel single-ended/differential ADC with analog multiplexer
- 10-bit Current Output DAC
- Precision programmable 24.5 MHz internal oscillator
- Low-power, low-frequency oscillator
- 16 kB of on-chip Flash memory—512 bytes are reserved
- 768 bytes of on-chip RAM
- SMBus/I2C, Enhanced UART, and Enhanced SPI serial interfaces implemented in hardware
- Four general-purpose 16-bit timers
- Programmable Counter/Timer Array (PCA) with three capture/compare modules and Watchdog Timer function
- On-chip Power-On Reset, V_{DD} Monitor, and Temperature Sensor
- On-chip Voltage Comparator
- 21 or 17 Port I/O (5 V tolerant)
- Low-power suspend mode with fast wake-up time

With on-chip Power-On Reset, V_{DD} monitor, Watchdog Timer, and clock oscillator, the C8051F336/7/8/9 devices are truly stand-alone System-on-a-Chip solutions. The Flash memory can be reprogrammed even in-circuit, providing non-volatile data storage, and also allowing field upgrades of the 8051 firmware. User software has complete control of all peripherals, and may individually shut down any or all peripherals for power savings.

The on-chip Silicon Labs 2-Wire (C2) Development Interface allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection and modification of memory and registers, setting breakpoints, single stepping, run and halt commands. All analog and digital peripherals are fully functional while debugging using C2. The two C2 interface pins can be shared with user functions, allowing in-system debugging without occupying package pins.

Each device is specified for 2.7 to 3.6 V operation over the industrial temperature range (–40 to +85 °C). The Port I/O and $\overline{\text{RST}}$ pins are tolerant of input signals up to 5 V. The C8051F336/7 are available in a 20-pin QFN package and the C8051F338/9 are available in a 24-pin QFN package. Both package options are lead-free and RoHS compliant. See **Section "2. Ordering Information" on page 18** for ordering information. Block diagrams are included in Figure 1.1 and Figure 1.2.

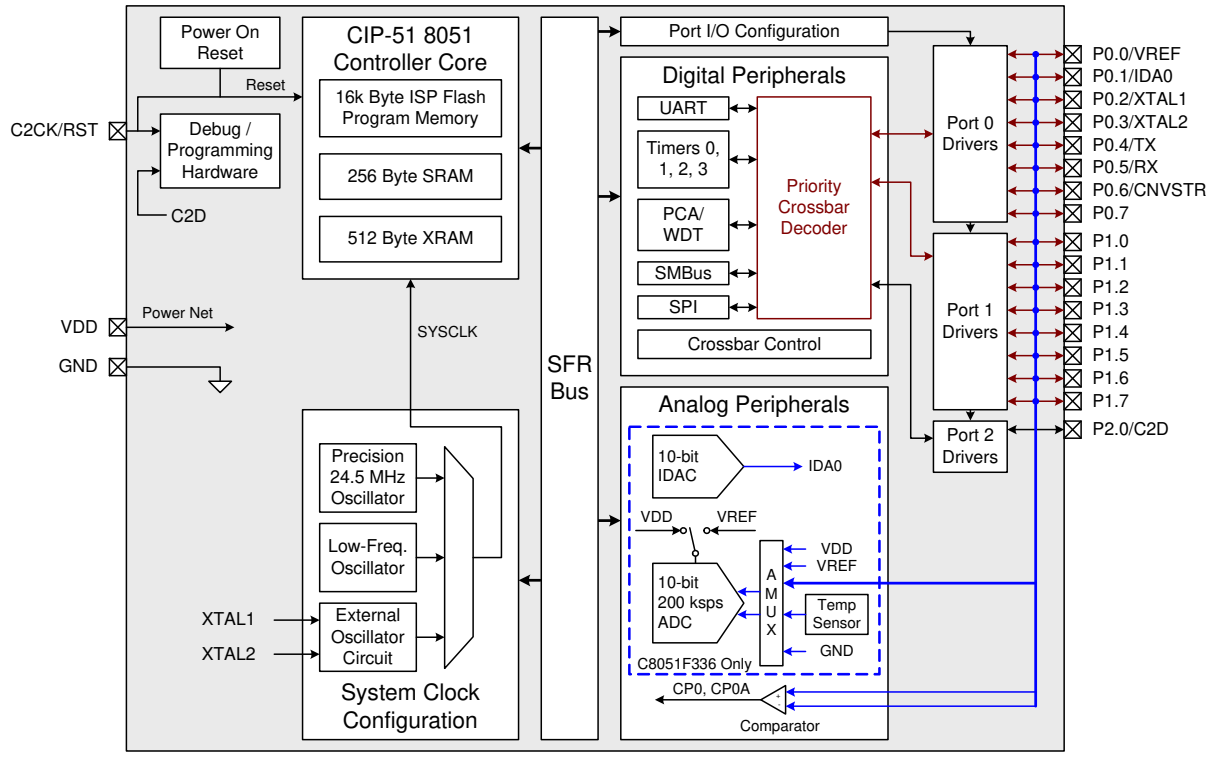

Figure 1.1. C8051F336/7 Block Diagram

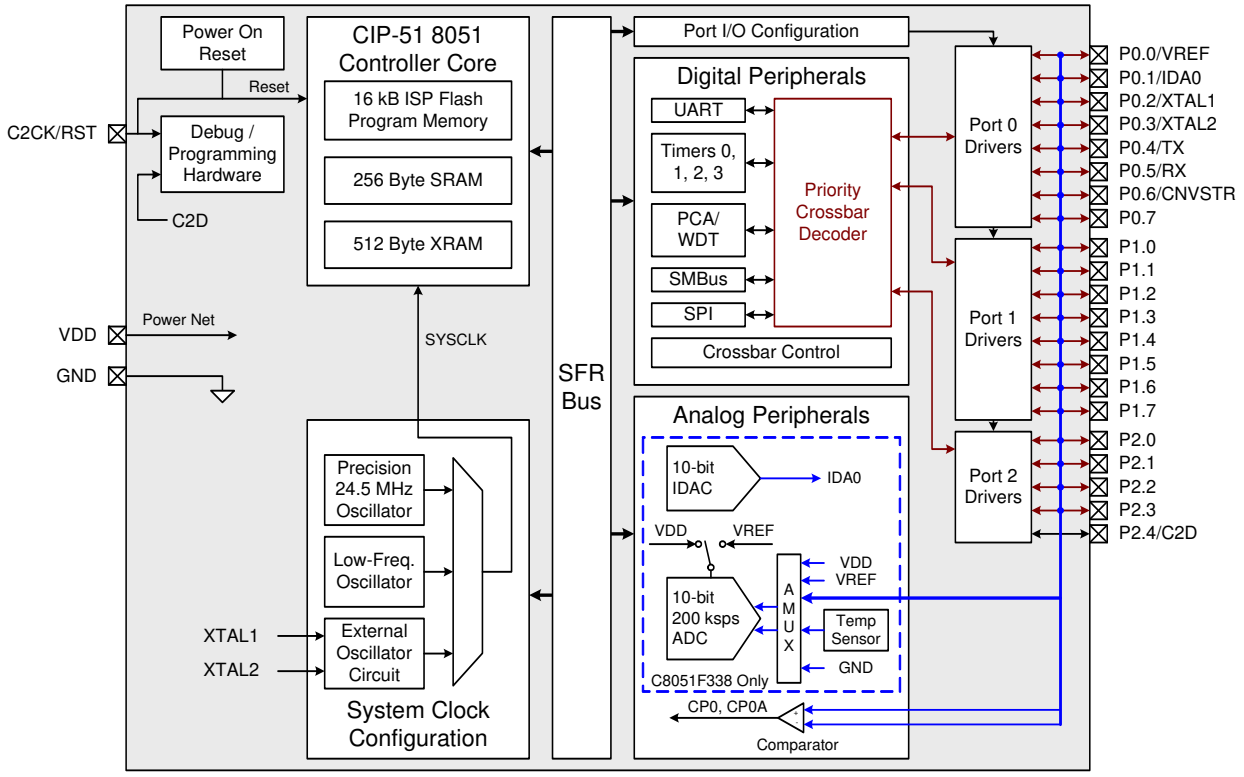

Figure 1.2. C8051F338/9 Block Diagram

2. Ordering Information

Table 2.1. Product Selection Guide

Ordering Part Number	MIPS (Peak)	Flash Memory (kB)	RAM (bytes)	Calibrated Internal 24.5 MHz Oscillator	Internal 80 kHz Oscillator	SMBus/I2C	Enhanced SPI	UART	Timers (16-bit)	RTC OPeration	Programmable Counter Array	Digital Port I/Os	10-bit 200ksps ADC	10-bit Current Output DAC	Internal Voltage Reference	Temperature Sensor	Analog Comparator	Lead-Free / RoHS Compliant	Package
C8051F336-GM	25	16	768	Y	Y	Y	Y	Y	4	Y	Y	17	Y	Y	Y	Y	Y	Y	QFN-20
C8051F337-GM	25	16	768	Y	Y	Y	Y	Y	4	Y	Y	17	—	—	—	—	Y	Y	QFN-20
C8051F338-GM	25	16	768	Y	Y	Y	Y	Y	4	Y	Y	21	Y	Y	Y	Y	Y	Y	QFN-24
C8051F339-GM	25	16	768	Y	Y	Y	Y	Y	4	Y	Y	21	—	—	—	—	Y	Y	QFN-24

3. Pin Definitions

Table 3.1. Pin Definitions for the C8051F336/7/8/9

Name	Pin 'F336/7	Pin 'F338/9	Type	Description
V_{DD}	3	4		Power Supply Voltage.
GND	2	3		Ground. This ground connection is required. The center pad may optionally be connected to ground also.
$\overline{RST}$/	4	5	D I/O	Device Reset. Open-drain output of internal POR or V_{DD} monitor. An external source can initiate a system reset by driving this pin low for at least 10 µs.
C2CK			D I/O	Clock signal for the C2 Debug Interface.
C2D	5	6	D I/O	Bi-directional data signal for the C2 Debug Interface. Shared with P2.0 on 20-pin packaging and P2.4 on 24-pin packaging.
P0.0/	1	2	D I/O or A In	Port 0.0.
VREF			A In	External VREF input.
P0.1	20	1	D I/O or A In	Port 0.1.
IDA0			A Out	IDA0 Output.
P0.2/	19	24	D I/O or A In	Port 0.2.
XTAL1			A In	External Clock Input. This pin is the external oscillator return for a crystal or resonator.
P0.3/	18	23	D I/O or A In	Port 0.3.
XTAL2			A I/O or D In	External Clock Output. For an external crystal or resonator, this pin is the excitation driver. This pin is the external clock input for CMOS, capacitor, or RC oscillator configurations.
P0.4	17	22	D I/O or A In	Port 0.4.
P0.5	16	21	D I/O or A In	Port 0.5.
P0.6/	15	20	D I/O or A In	Port 0.6.
CNVSTR			D In	ADC0 External Convert Start or IDA0 Update Source Input.

Table 3.1. Pin Definitions for the C8051F336/7/8/9 (Continued)

Name	Pin 'F336/7	Pin 'F338/9	Type	Description
P0.7	14	19	D I/O or A In	Port 0.7.
P1.0	13	18	D I/O or A In	Port 1.0.
P1.1	12	17	D I/O or A In	Port 1.1.
P1.2	11	16	D I/O or A In	Port 1.2.
P1.3	10	15	D I/O or A In	Port 1.3.
P1.4	9	14	D I/O or A In	Port 1.4.
P1.5	8	13	D I/O or A In	Port 1.5.
P1.6	7	12	D I/O or A In	Port 1.6.
P1.7	6	11	D I/O or A In	Port 1.7.
P2.0	5	10	D I/O or A In	Port 2.0. (Also C2D on 20-pin Packaging)
P2.1	—	9	D I/O or A In	Port 2.1.
P2.2	—	8	D I/O or A In	Port 2.2.
P2.3	—	7	D I/O or A In	Port 2.3.
P2.4	—	6	D I/O	Port 2.4. (Also C2D on 24-pin Packaging)

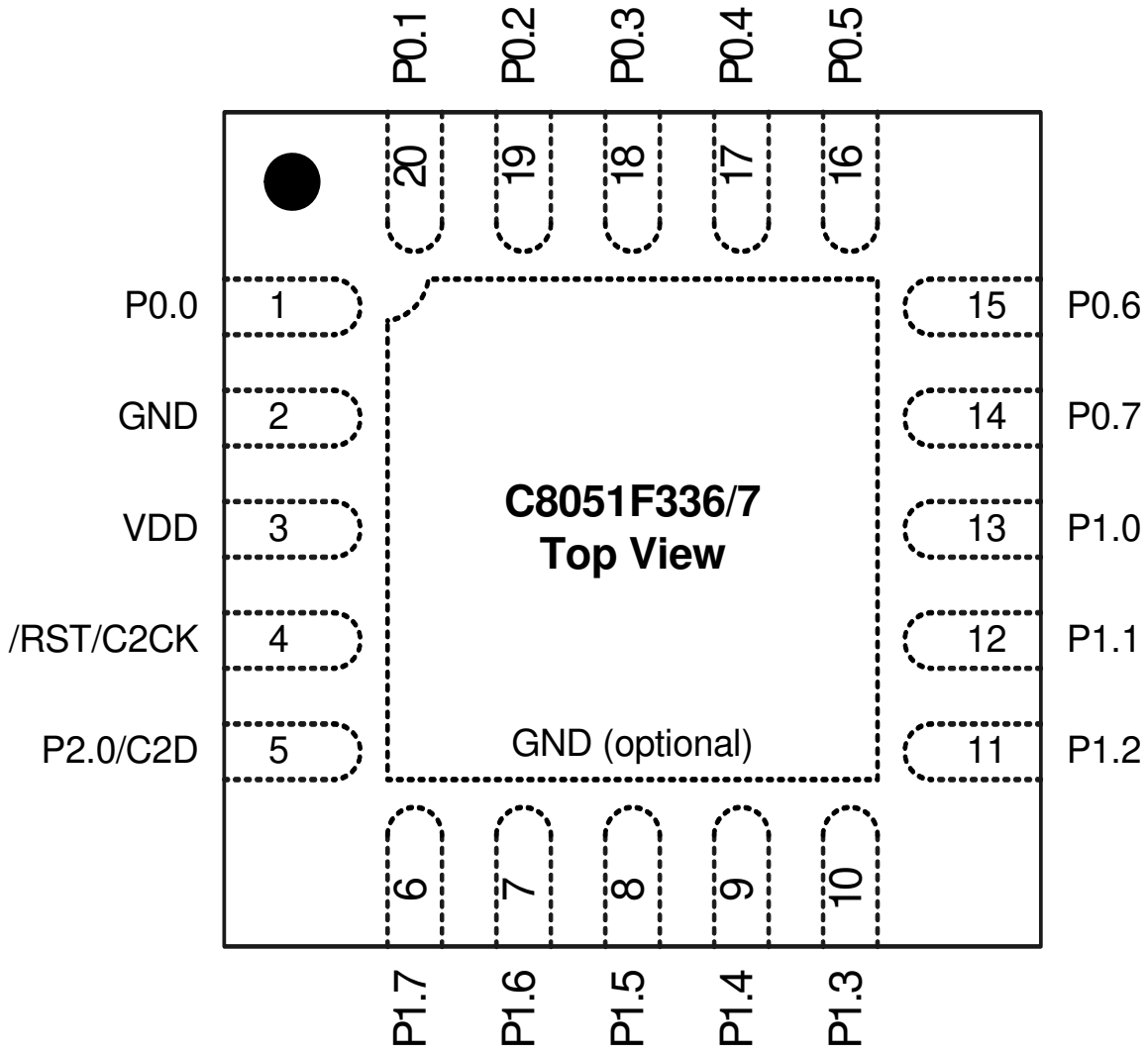

Figure 3.1. QFN-20 Pinout Diagram (Top View)

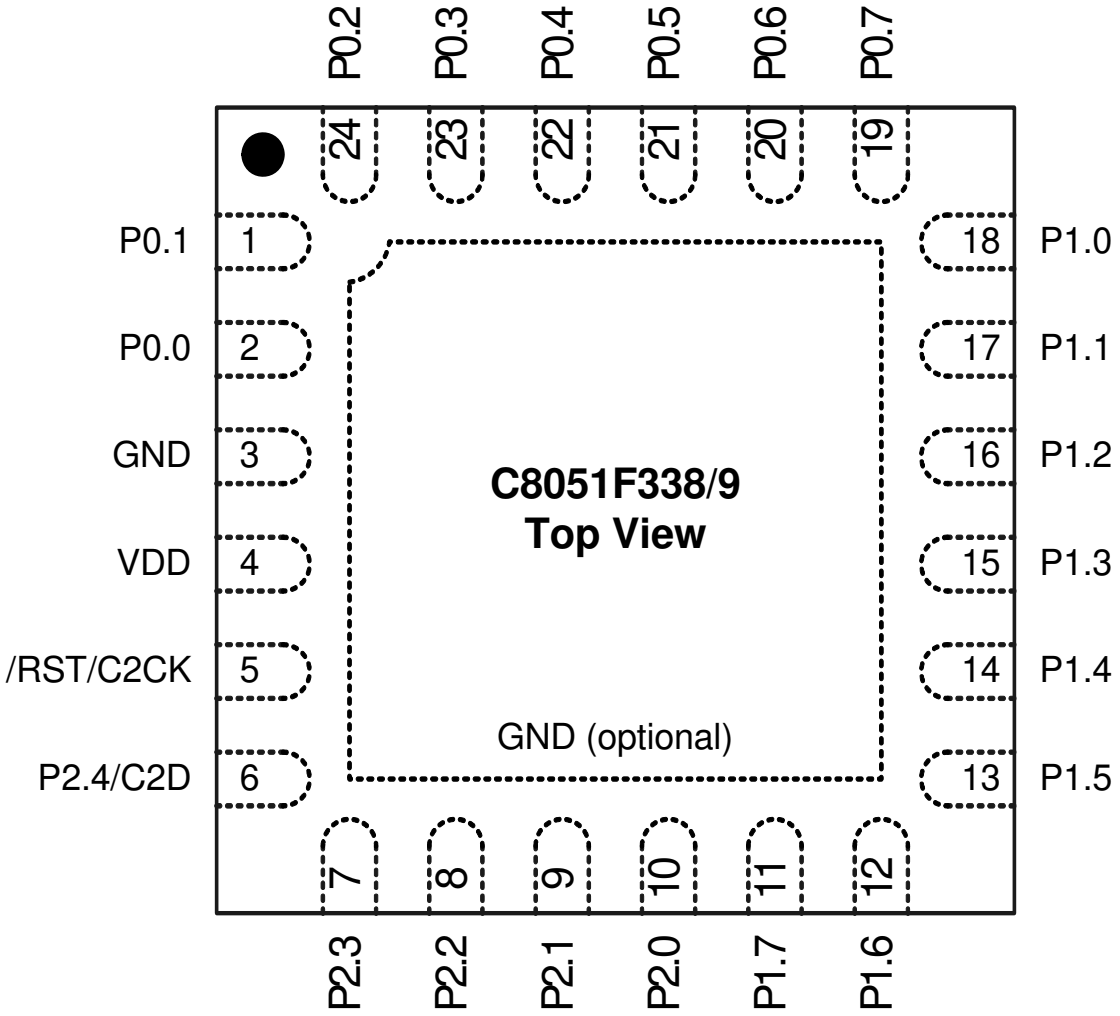

Figure 3.2. QFN-24 Pinout Diagram (Top View)

4. QFN-20 Package Specifications

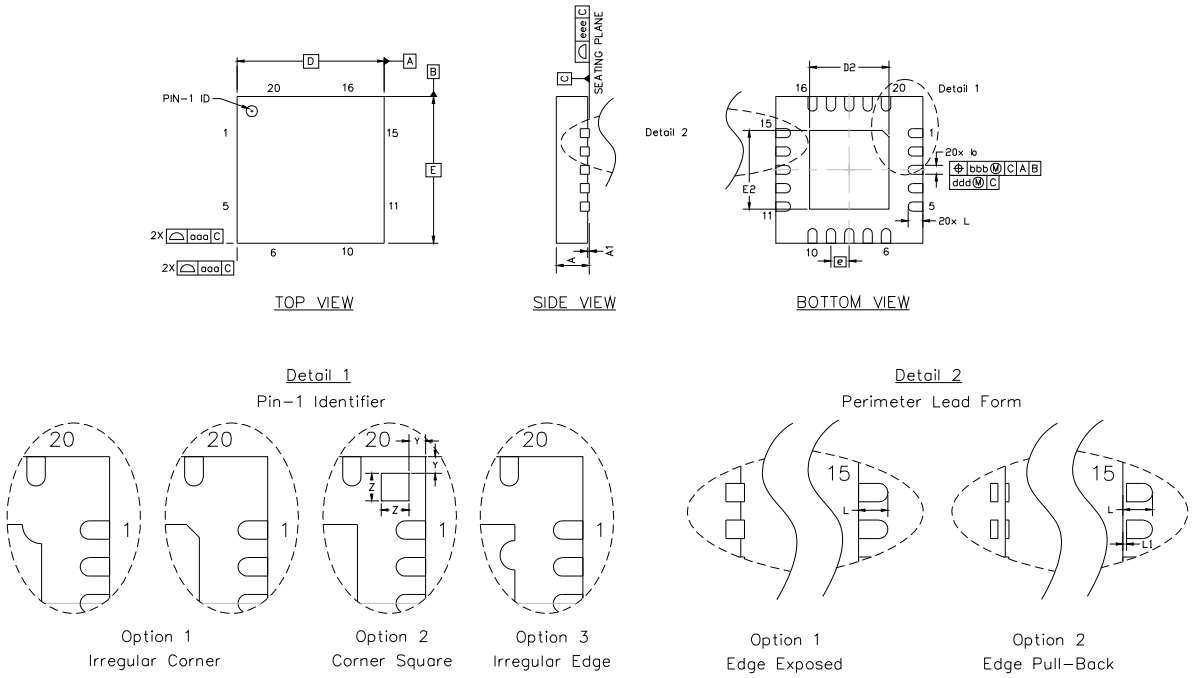

Figure 4.1. QFN-20 Package Drawing

Table 4.1. QFN-20 Package Dimensions

Dimension	Min	Typ	Max		Dimension	Min	Typ	Max
A	0.80	0.90	1.00		L	0.45	0.55	0.65
A1	0.00	0.02	0.05		L1	0.00	—	0.15
b	0.18	0.25	0.30		aaa	—	—	0.15
D	4.00 BSC.				bbb	—	—	0.10
D2	2.00	2.15	2.25		ddd	—	—	0.05
e	0.50 BSC.				eee	—	—	0.08
E	4.00 BSC.				Z	—	0.43	—
E2	2.00	2.15	2.25		Y	—	0.18	—

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220, variation VGGD except for custom features D2, E2, Z, Y, and L which are toleranced per supplier designation.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

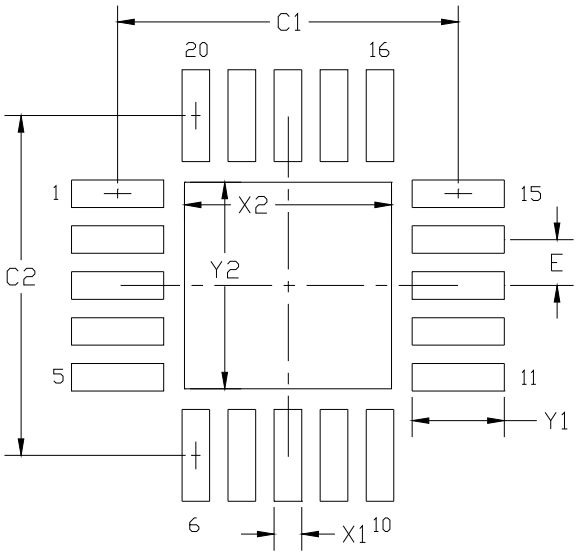

Figure 4.2. QFN-20 Recommended PCB Land Pattern

Table 4.2. QFN-20 PCB Land Pattern Dimesions

Dimension	Min	Max
C1	3.70	
C2	3.70	
E	0.50	
X1	0.20	0.30

Dimension	Min	Max
X2	2.15	2.25
Y1	0.90	1.00
Y2	2.15	2.25

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.

Solder Mask Design

4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60µm minimum, all the way around the pad.

Stencil Design

5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
6. The stencil thickness should be 0.125mm (5 mils).
7. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pins.
8. A 2x2 array of 0.95mm openings on a 1.1mm pitch should be used for the center pad to assure the proper paste volume (71% Paste Coverage).

Card Assembly

9. A No-Clean, Type-3 solder paste is recommended.
10. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

5. QFN-24 Package Specifications

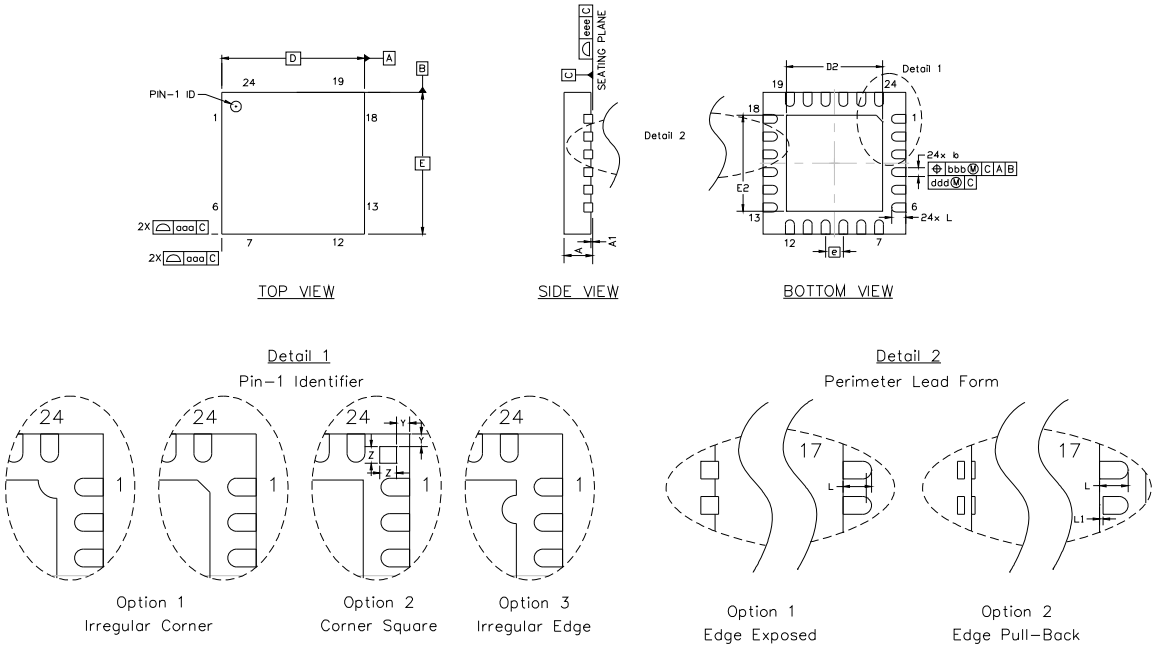

Figure 5.1. QFN-24 Package Drawing

Table 5.1. QFN-24 Package Dimensions

Dimension	Min	Typ	Max		Dimension	Min	Typ	Max
A	0.70	0.75	0.80		L	0.30	0.40	0.50
A1	0.00	0.02	0.05		L1	0.00	—	0.15
b	0.18	0.25	0.30		aaa	—	—	0.15
D		4.00 BSC.			bbb	—	—	0.10
D2	2.55	2.70	2.80		ddd	—	—	0.05
e		0.50 BSC.			eee	—	—	0.08
E		4.00 BSC.			Z	—	0.24	—
E2	2.55	2.70	2.80		Y	—	0.18	—

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC Solid State Outline MO-220, variation WGGD except for custom features D2, E2, Z, Y, and L which are toleranced per supplier designation.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.