



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



### Analog Peripherals

- **12-Bit ADC**
  - Programmable throughput up to 200 ksps
  - Up to 6/16 external inputs
  - Data dependent windowed interrupt generator
  - Built-in temperature sensor
- **Comparator**
  - Programmable hysteresis and response time
  - Configurable as wake-up or reset source
  - Low current
- **POR/Brownout Detector**
- **Voltage Reference—1.5 and 2.2 V (programmable)**

### On-Chip Debug

- On-chip debug circuitry facilitates full-speed, non-intrusive in-system debug (No emulator required)
- Provides breakpoints, single stepping
- Inspect/modify memory and registers
- Complete development kit

### Supply Voltage 2.0 to 5.25 V

- Built-in LDO regulator

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to **25 MIPS** throughput with 25 MHz system clock
- Expanded interrupt handler

### Memory

- 8/4/2 kB Flash; In-system byte programmable in 512 byte sectors
- 256 bytes internal data RAM

### Digital Peripherals

- 16/6 port I/O; push-pull or open-drain, 5 V tolerant
- Hardware SPI™, and UART serial port
- LIN 2.1 Controller (Master and Slave capable); no crystal required
- Three general purpose 16-bit counter/timers
- Programmable 16-bit counter/timer array with three capture/compare modules, WDT

### Clock Sources

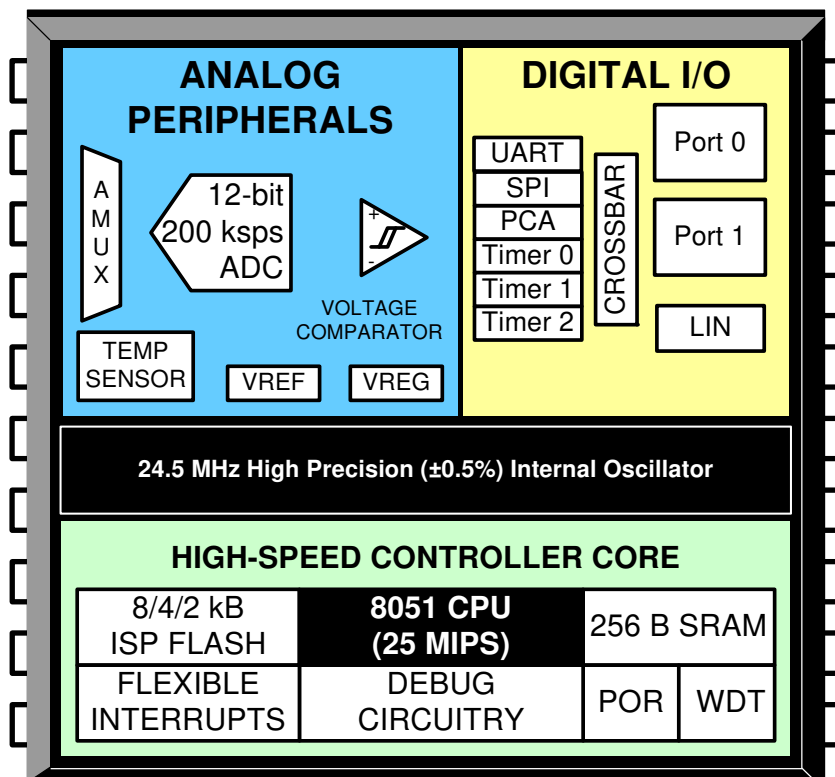
- Internal oscillators: 24.5 MHz  $\pm 0.5\%$  accuracy supports UART and LIN-Master operation
- External oscillator: Crystal, RC, C, or Clock (1 or 2 pin modes)
- Can switch between clock sources on-the-fly

### Packages

- 10-Pin DFN (3 x 3 mm)
- 20-pin QFN (4 x 4 mm)
- 20-pin TSSOP

### Automotive Qualified

- Temperature Range:  $-40$  to  $+125$  °C
- Compliant to AEC-Q100



# C8051F52x/F52xA/F53x/F53xA

---



## Table of Contents

|  |           |
|--|-----------|
| <b>1. System Overview .....</b>                    | <b>13</b> |
| 1.1. Ordering Information.....                     | 14        |
| 1.2. CIP-51™ Microcontroller .....                 | 18        |
| 1.2.1. Fully 8051 Compatible Instruction Set ..... | 18        |
| 1.2.2. Improved Throughput.....                    | 18        |
| 1.2.3. Additional Features .....                   | 18        |
| 1.2.4. On-Chip Debug Circuitry .....               | 18        |
| 1.3. On-Chip Memory .....                          | 20        |
| 1.4. Operating Modes .....                         | 21        |
| 1.5. 12-Bit Analog to Digital Converter .....      | 22        |
| 1.6. Programmable Comparator .....                 | 23        |
| 1.7. Voltage Regulator.....                        | 23        |
| 1.8. Serial Port.....                              | 23        |
| 1.9. Port Input/Output .....                       | 24        |
| <b>2. Electrical Characteristics .....</b>         | <b>25</b> |
| 2.1. Absolute Maximum Ratings.....                 | 25        |
| 2.2. Electrical Characteristics .....              | 26        |
| <b>3. Pinout and Package Definitions .....</b>     | <b>35</b> |
| <b>4. 12-Bit ADC (ADC0).....</b>                   | <b>52</b> |
| 4.1. Analog Multiplexer .....                      | 52        |
| 4.2. Temperature Sensor.....                       | 53        |
| 4.3. ADC0 Operation .....                          | 54        |
| 4.3.1. Starting a Conversion.....                  | 54        |
| 4.3.2. Tracking Modes.....                         | 54        |
| 4.3.3. Timing .....                                | 55        |
| 4.3.4. Burst Mode.....                             | 57        |
| 4.3.5. Output Conversion Code.....                 | 59        |
| 4.3.6. Settling Time Requirements.....             | 60        |
| 4.4. Selectable Gain .....                         | 60        |
| 4.4.1. Calculating the Gain Value.....             | 61        |
| 4.4.2. Setting the Gain Value .....                | 62        |
| 4.5. Programmable Window Detector.....             | 69        |
| 4.5.1. Window Detector In Single-Ended Mode .....  | 71        |
| <b>5. Voltage Reference.....</b>                   | <b>72</b> |
| <b>6. Voltage Regulator (REG0).....</b>            | <b>74</b> |
| <b>7. Comparator .....</b>                         | <b>76</b> |
| <b>8. CIP-51 Microcontroller.....</b>              | <b>81</b> |
| 8.1. Instruction Set.....                          | 82        |
| 8.1.1. Instruction and CPU Timing .....            | 82        |
| 8.1.2. MOVX Instruction and Program Memory .....   | 83        |
| 8.2. Register Descriptions .....                   | 86        |
| 8.3. Power Management Modes.....                   | 89        |
| 8.3.1. Idle Mode .....                             | 90        |

# C8051F52x/F52xA/F53x/F53xA

---

|  |            |
|--|------------|
| 8.3.2. Stop Mode.....  | 90         |
| 8.3.3. Suspend Mode.....   | 90         |
| <b>9. Memory Organization and SFRs.....</b>                              | <b>92</b>  |
| 9.1. Program Memory.....   | 92         |
| 9.2. Data Memory.....  | 93         |
| 9.3. General Purpose Registers.....                                      | 93         |
| 9.4. Bit Addressable Locations.....                                      | 93         |
| 9.5. Stack.....  | 93         |
| 9.6. Special Function Registers.....                                     | 93         |
| <b>10. Interrupt Handler.....</b>  | <b>98</b>  |
| 10.1. MCU Interrupt Sources and Vectors.....                             | 98         |
| 10.2. Interrupt Priorities.....  | 98         |
| 10.3. Interrupt Latency.....   | 98         |
| 10.4. Interrupt Register Descriptions.....                               | 100        |
| 10.5. External Interrupts.....   | 104        |
| <b>11. Reset Sources.....</b>  | <b>106</b> |
| 11.1. Power-On Reset.....  | 107        |
| 11.2. Power-Fail Reset / VDD Monitors (VDDMON0 and VDDMON1).....         | 108        |
| 11.2.1. VDD Monitor Thresholds and Minimum VDD.....                      | 108        |
| 11.3. External Reset.....  | 110        |
| 11.4. Missing Clock Detector Reset.....                                  | 110        |
| 11.5. Comparator Reset.....  | 110        |
| 11.6. PCA Watchdog Timer Reset.....                                      | 110        |
| 11.7. Flash Error Reset.....   | 110        |
| 11.8. Software Reset.....  | 111        |
| <b>12. Flash Memory.....</b>   | <b>113</b> |
| 12.1. Programming The Flash Memory.....                                  | 113        |
| 12.1.1. Flash Lock and Key Functions.....                                | 113        |
| 12.1.2. Flash Erase Procedure.....                                       | 114        |
| 12.1.3. Flash Write Procedure.....                                       | 114        |
| 12.2. Flash Write and Erase Guidelines.....                              | 115        |
| 12.2.1. V <sub>DD</sub> Maintenance and the V <sub>DD</sub> monitor..... | 115        |
| 12.2.2. PSWE Maintenance.....  | 115        |
| 12.2.3. System Clock.....  | 116        |
| 12.3. Non-volatile Data Storage.....                                     | 117        |
| 12.4. Security Options.....  | 117        |
| <b>13. Port Input/Output.....</b>  | <b>120</b> |
| 13.1. Priority Crossbar Decoder.....                                     | 122        |
| 13.2. Port I/O Initialization.....                                       | 126        |
| 13.3. General Purpose Port I/O.....                                      | 128        |
| <b>14. Oscillators.....</b>  | <b>135</b> |
| 14.1. Programmable Internal Oscillator.....                              | 135        |
| 14.1.1. Internal Oscillator Suspend Mode.....                            | 136        |
| 14.2. External Oscillator Drive Circuit.....                             | 139        |
| 14.2.1. Clocking Timers Directly Through the External Oscillator.....    | 139        |

---

# C8051F52x/F52xA/F53x/F53xA

---

|   |            |
|---|------------|
| 14.2.2. External Crystal Example.....                                   | 139        |
| 14.2.3. External RC Example.....  | 141        |
| 14.2.4. External Capacitor Example.....                                 | 141        |
| 14.3. System Clock Selection.....                                       | 143        |
| <b>15. UART0.....</b>   | <b>144</b> |
| 15.1. Enhanced Baud Rate Generation.....                                | 145        |
| 15.2. Operational Modes.....  | 146        |
| 15.2.1. 8-Bit UART.....   | 146        |
| 15.2.2. 9-Bit UART.....   | 147        |
| 15.3. Multiprocessor Communications.....                                | 148        |
| <b>16. Enhanced Serial Peripheral Interface (SPI0).....</b>             | <b>151</b> |
| 16.1. Signal Descriptions.....  | 152        |
| 16.1.1. Master Out, Slave In (MOSI).....                                | 152        |
| 16.1.2. Master In, Slave Out (MISO).....                                | 152        |
| 16.1.3. Serial Clock (SCK).....   | 152        |
| 16.1.4. Slave Select (NSS).....   | 152        |
| 16.2. SPI0 Master Mode Operation.....                                   | 153        |
| 16.3. SPI0 Slave Mode Operation.....                                    | 154        |
| 16.4. SPI0 Interrupt Sources.....                                       | 155        |
| 16.5. Serial Clock Timing.....  | 156        |
| 16.6. SPI Special Function Registers.....                               | 156        |
| <b>17. LIN (C8051F520/0A/3/3A/6/6A and C8051F530/0A/3/3A/6/6A).....</b> | <b>164</b> |
| 17.1. Software Interface with the LIN Peripheral.....                   | 165        |
| 17.2. LIN Interface Setup and Operation.....                            | 165        |
| 17.2.1. Mode Definition.....  | 165        |
| 17.2.2. Baud Rate Options: Manual or Autobaud.....                      | 165        |
| 17.2.3. Baud Rate Calculations—Manual Mode.....                         | 165        |
| 17.2.4. Baud Rate Calculations—Automatic Mode.....                      | 168        |
| 17.3. LIN Master Mode Operation.....                                    | 169        |
| 17.4. LIN Slave Mode Operation.....                                     | 170        |
| 17.5. Sleep Mode and Wake-Up.....                                       | 171        |
| 17.6. Error Detection and Handling.....                                 | 171        |
| 17.7. LIN Registers.....  | 172        |
| 17.7.1. LIN Direct Access SFR Registers Definition.....                 | 172        |
| 17.7.2. LIN Indirect Access SFR Registers Definition.....               | 174        |
| <b>18. Timers.....</b>  | <b>182</b> |
| 18.1. Timer 0 and Timer 1.....  | 182        |
| 18.1.1. Mode 0: 13-bit Counter/Timer.....                               | 182        |
| 18.1.2. Mode 1: 16-bit Counter/Timer.....                               | 184        |
| 18.1.3. Mode 2: 8-bit Counter/Timer with Auto-Reload.....               | 184        |
| 18.1.4. Mode 3: Two 8-bit Counter/Timers (Timer 0 Only).....            | 185        |
| 18.2. Timer 2.....  | 190        |
| 18.2.1. 16-bit Timer with Auto-Reload.....                              | 190        |
| 18.2.2. 8-bit Timers with Auto-Reload.....                              | 191        |
| 18.2.3. External Capture Mode.....                                      | 192        |

---

# C8051F52x/F52xA/F53x/F53xA

---

|  |            |
|--|------------|
| <b>19. Programmable Counter Array (PCA0)</b> .....       | <b>195</b> |
| 19.1. PCA Counter/Timer .....                            | 196        |
| 19.2. Capture/Compare Modules .....                      | 197        |
| 19.2.1. Edge-triggered Capture Mode.....                 | 198        |
| 19.2.2. Software Timer (Compare) Mode.....               | 199        |
| 19.2.3. High Speed Output Mode.....                      | 200        |
| 19.2.4. Frequency Output Mode .....                      | 201        |
| 19.2.5. 8-Bit Pulse Width Modulator Mode.....            | 202        |
| 19.2.6. 16-Bit Pulse Width Modulator Mode.....           | 203        |
| 19.3. Watchdog Timer Mode .....                          | 203        |
| 19.3.1. Watchdog Timer Operation .....                   | 204        |
| 19.3.2. Watchdog Timer Usage .....                       | 205        |
| 19.4. Register Descriptions for PCA.....                 | 206        |
| <b>20. Device Specific Behavior .....</b>                | <b>210</b> |
| 20.1. Device Identification .....                        | 210        |
| 20.2. Reset Pin Behavior.....                            | 211        |
| 20.3. Reset Time Delay .....                             | 211        |
| 20.4. VDD Monitors and VDD Ramp Time .....               | 211        |
| 20.5. VDD Monitor (VDDMON0) High Threshold Setting ..... | 212        |
| 20.6. Reset Low Time.....                                | 212        |
| 20.7. Internal Oscillator Suspend Mode .....             | 212        |
| 20.8. UART Pins.....                                     | 213        |
| 20.9. LIN .....  | 213        |
| 20.9.1. Stop Bit Check .....                             | 213        |
| 20.9.2. Synch Break and Synch Field Length Check.....    | 213        |
| <b>21. C2 Interface .....</b>                            | <b>214</b> |
| 21.1. C2 Interface Registers.....                        | 214        |
| 21.2. C2 Pin Sharing .....                               | 216        |
| <b>Document Change List.....</b>                         | <b>217</b> |
| <b>Contact Information.....</b>                          | <b>220</b> |

# C8051F52x/F52xA/F53x/F53xA

## List of Figures

|   |     |
|---|-----|
| Figure 1.1. C8051F53xA/F53x-C Block Diagram .....   | 16  |
| Figure 1.2. C8051F52xA/F52x-C Block Diagram .....   | 16  |
| Figure 1.3. C8051F53x Block Diagram (Silicon Revision A) .....                                  | 17  |
| Figure 1.4. C8051F52x Block Diagram (Silicon Revision A) .....                                  | 17  |
| Figure 1.5. Development/In-System Debug Diagram .....   | 19  |
| Figure 1.6. Memory Map .....  | 20  |
| Figure 1.7. 12-Bit ADC Block Diagram .....  | 22  |
| Figure 1.8. Comparator Block Diagram .....  | 23  |
| Figure 1.9. Port I/O Functional Block Diagram .....   | 24  |
| Figure 3.1. DFN-10 Pinout Diagram (Top View) .....  | 35  |
| Figure 3.2. DFN-10 Package Diagram .....  | 38  |
| Figure 3.3. DFN-10 Landing Diagram .....  | 39  |
| Figure 3.4. TSSOP-20 Pinout Diagram (Top View) .....  | 40  |
| Figure 3.5. TSSOP-20 Package Diagram .....  | 43  |
| Figure 3.6. TSSOP-20 Landing Diagram .....  | 44  |
| Figure 3.7. QFN-20 Pinout Diagram (Top View) .....  | 45  |
| Figure 3.8. QFN-20 Package Diagram* .....   | 48  |
| Figure 3.9. QFN-20 Landing Diagram* .....   | 50  |
| Figure 4.1. ADC0 Functional Block Diagram .....   | 52  |
| Figure 4.2. Typical Temperature Sensor Transfer Function .....                                  | 53  |
| Figure 4.3. ADC0 Tracking Modes .....   | 55  |
| Figure 4.4. 12-Bit ADC Tracking Mode Example .....  | 56  |
| Figure 4.5. 12-Bit ADC Burst Mode Example with Repeat Count Set to 4 .....                      | 58  |
| Figure 4.6. ADC0 Equivalent Input Circuits .....  | 60  |
| Figure 4.7. ADC Window Compare Example:<br>Right-Justified Single-Ended Data .....              | 71  |
| Figure 4.8. ADC Window Compare Example:<br>Left-Justified Single-Ended Data .....               | 71  |
| Figure 5.1. Voltage Reference Functional Block Diagram .....                                    | 72  |
| Figure 6.1. External Capacitors for Voltage Regulator Input/Output .....                        | 74  |
| Figure 7.1. Comparator Functional Block Diagram .....   | 76  |
| Figure 7.2. Comparator Hysteresis Plot .....  | 77  |
| Figure 8.1. CIP-51 Block Diagram .....  | 81  |
| Figure 9.1. Memory Map .....  | 92  |
| Figure 11.1. Reset Sources .....  | 106 |
| Figure 11.2. Power-On and $V_{DD}$ Monitor Reset Timing .....                                   | 107 |
| Figure 12.1. Flash Program Memory Map .....   | 117 |
| Figure 13.1. Port I/O Functional Block Diagram .....  | 120 |
| Figure 13.2. Port I/O Cell Block Diagram .....  | 121 |
| Figure 13.3. Crossbar Priority Decoder with No Pins Skipped<br>(TSSOP 20 and QFN 20) .....      | 122 |
| Figure 13.4. Crossbar Priority Decoder with Crystal Pins Skipped<br>(TSSOP 20 and QFN 20) ..... | 123 |



# C8051F52x/F52xA/F53x/F53xA

---

|  |     |
|--|-----|
| Figure 13.5. Crossbar Priority Decoder with No Pins Skipped (DFN 10) .....   | 124 |
| Figure 13.6. Crossbar Priority Decoder with Some Pins Skipped (DFN 10) ..... | 125 |
| Figure 14.1. Oscillator Diagram .....  | 135 |
| Figure 14.2. 32 kHz External Crystal Example .....                           | 140 |
| Figure 15.1. UART0 Block Diagram .....                                       | 144 |
| Figure 15.2. UART0 Baud Rate Logic .....                                     | 145 |
| Figure 15.3. UART Interconnect Diagram .....                                 | 146 |
| Figure 15.4. 8-Bit UART Timing Diagram .....                                 | 146 |
| Figure 15.5. 9-Bit UART Timing Diagram .....                                 | 147 |
| Figure 15.6. UART Multi-Processor Mode Interconnect Diagram .....            | 148 |
| Figure 16.1. SPI Block Diagram .....   | 151 |
| Figure 16.2. Multiple-Master Mode Connection Diagram .....                   | 154 |
| Figure 16.3. 3-Wire Single Master and Slave Mode Connection Diagram .....    | 154 |
| Figure 16.4. 4-Wire Single Master and Slave Mode Connection Diagram .....    | 154 |
| Figure 16.5. Data/Clock Timing Relationship .....                            | 156 |
| Figure 16.6. SPI Master Timing (CKPHA = 0) .....                             | 161 |
| Figure 16.7. SPI Master Timing (CKPHA = 1) .....                             | 161 |
| Figure 16.8. SPI Slave Timing (CKPHA = 0) .....                              | 162 |
| Figure 16.9. SPI Slave Timing (CKPHA = 1) .....                              | 162 |
| Figure 17.1. LIN Block Diagram .....   | 164 |
| Figure 18.1. T0 Mode 0 Block Diagram .....                                   | 183 |
| Figure 18.2. T0 Mode 2 Block Diagram .....                                   | 184 |
| Figure 18.3. T0 Mode 3 Block Diagram .....                                   | 185 |
| Figure 18.4. Timer 2 16-Bit Mode Block Diagram .....                         | 190 |
| Figure 18.5. Timer 2 8-Bit Mode Block Diagram .....                          | 191 |
| Figure 18.6. Timer 2 Capture Mode Block Diagram .....                        | 192 |
| Figure 19.1. PCA Block Diagram .....   | 195 |
| Figure 19.2. PCA Counter/Timer Block Diagram .....                           | 196 |
| Figure 19.3. PCA Interrupt Block Diagram .....                               | 197 |
| Figure 19.4. PCA Capture Mode Diagram .....                                  | 198 |
| Figure 19.5. PCA Software Timer Mode Diagram .....                           | 199 |
| Figure 19.6. PCA High-Speed Output Mode Diagram .....                        | 200 |
| Figure 19.7. PCA Frequency Output Mode .....                                 | 201 |
| Figure 19.8. PCA 8-Bit PWM Mode Diagram .....                                | 202 |
| Figure 19.9. PCA 16-Bit PWM Mode .....                                       | 203 |
| Figure 19.10. PCA Module 2 with Watchdog Timer Enabled .....                 | 204 |
| Figure 20.1. Device Package—TSSOP 20 .....                                   | 210 |
| Figure 20.2. Device Package—QFN 20 .....                                     | 210 |
| Figure 20.3. Device Package—DFN 10 .....                                     | 211 |
| Figure 21.1. Typical C2 Pin Sharing .....                                    | 216 |

## List of Tables

|   |     |
|---|-----|
| Table 1.1. Product Selection Guide (Recommended for New Designs) .....                    | 14  |
| Table 1.2. Product Selection Guide (Not Recommended for New Designs) .....                | 15  |
| Table 1.3. Operating Modes Summary .....  | 21  |
| Table 2.1. Absolute Maximum Ratings .....   | 25  |
| Table 2.2. Global DC Electrical Characteristics .....                                     | 26  |
| Table 2.3. ADC0 Electrical Characteristics .....  | 28  |
| Table 2.4. Temperature Sensor Electrical Characteristics .....                            | 29  |
| Table 2.5. Voltage Reference Electrical Characteristics .....                             | 29  |
| Table 2.6. Voltage Regulator Electrical Specifications .....                              | 30  |
| Table 2.7. Comparator Electrical Characteristics .....                                    | 31  |
| Table 2.8. Reset Electrical Characteristics .....   | 32  |
| Table 2.9. Flash Electrical Characteristics .....   | 33  |
| Table 2.10. Port I/O DC Electrical Characteristics .....                                  | 33  |
| Table 2.11. Internal Oscillator Electrical Characteristics .....                          | 34  |
| Table 3.1. Pin Definitions for the C8051F52x and C8051F52xA (DFN 10) .....                | 36  |
| Table 3.2. DFN-10 Package Diagram Dimensions .....  | 38  |
| Table 3.3. DFN-10 Landing Diagram Dimensions .....  | 39  |
| Table 3.4. Pin Definitions for the C8051F53x and C805153xA (TSSOP 20) .....               | 40  |
| Table 3.5. TSSOP-20 Package Diagram Dimensions .....                                      | 43  |
| Table 3.6. TSSOP-20 Landing Diagram Dimensions .....                                      | 44  |
| Table 3.7. Pin Definitions for the C8051F53x and C805153xA (QFN 20) .....                 | 46  |
| Table 3.8. QFN-20 Package Diagram Dimensions .....  | 49  |
| Table 3.9. QFN-20 Landing Diagram Dimensions .....  | 51  |
| Table 8.1. CIP-51 Instruction Set Summary .....   | 83  |
| Table 9.1. Special Function Register (SFR) Memory Map .....                               | 94  |
| Table 9.2. Special Function Registers .....   | 95  |
| Table 10.1. Interrupt Summary .....   | 99  |
| Table 12.1. Flash Security Summary .....  | 118 |
| Table 15.1. Timer Settings for Standard Baud Rates<br>Using the Internal Oscillator ..... | 150 |
| Table 16.1. SPI Slave Timing Parameters .....   | 163 |
| Table 17.1. Baud-Rate Calculation Variable Ranges .....                                   | 166 |
| Table 17.2. Manual Baud Rate Parameters Examples .....                                    | 167 |
| Table 17.3. Autobaud Parameters Examples .....  | 168 |
| Table 17.4. LIN Registers* (Indirectly Addressable) .....                                 | 174 |
| Table 19.1. PCA Timebase Input Options .....  | 196 |
| Table 19.2. PCA0CPM Register Settings for PCA Capture/Compare Modules ....                | 197 |
| Table 19.3. Watchdog Timer Timeout Intervals1 .....                                       | 205 |

## List of Registers

|  |     |
|--|-----|
| SFR Definition 4.4. ADC0MX: ADC0 Channel Select .....                | 64  |
| SFR Definition 4.5. ADC0CF: ADC0 Configuration .....                 | 65  |
| SFR Definition 4.6. ADC0H: ADC0 Data Word MSB .....                  | 66  |
| SFR Definition 4.7. ADC0L: ADC0 Data Word LSB .....                  | 66  |
| SFR Definition 4.8. ADC0CN: ADC0 Control .....                       | 67  |
| SFR Definition 4.9. ADC0TK: ADC0 Tracking Mode Select .....          | 68  |
| SFR Definition 4.10. ADC0GTH: ADC0 Greater-Than Data High Byte ..... | 69  |
| SFR Definition 4.11. ADC0GTL: ADC0 Greater-Than Data Low Byte .....  | 69  |
| SFR Definition 4.12. ADC0LTH: ADC0 Less-Than Data High Byte .....    | 70  |
| SFR Definition 4.13. ADC0LTL: ADC0 Less-Than Data Low Byte .....     | 70  |
| SFR Definition 5.1. REF0CN: Reference Control .....                  | 73  |
| SFR Definition 6.1. REG0CN: Regulator Control .....                  | 75  |
| SFR Definition 7.1. CPT0CN: Comparator0 Control .....                | 78  |
| SFR Definition 7.2. CPT0MX: Comparator0 MUX Selection .....          | 79  |
| SFR Definition 7.3. CPT0MD: Comparator0 Mode Selection .....         | 80  |
| SFR Definition 8.1. SP: Stack Pointer .....                          | 87  |
| SFR Definition 8.2. DPL: Data Pointer Low Byte .....                 | 87  |
| SFR Definition 8.3. DPH: Data Pointer High Byte .....                | 87  |
| SFR Definition 8.4. PSW: Program Status Word .....                   | 88  |
| SFR Definition 8.5. ACC: Accumulator .....                           | 89  |
| SFR Definition 8.6. B: B Register .....                              | 89  |
| SFR Definition 8.7. PCON: Power Control .....                        | 91  |
| SFR Definition 10.1. IE: Interrupt Enable .....                      | 100 |
| SFR Definition 10.2. IP: Interrupt Priority .....                    | 101 |
| SFR Definition 10.3. EIE1: Extended Interrupt Enable 1 .....         | 102 |
| SFR Definition 10.4. EIP1: Extended Interrupt Priority 1 .....       | 103 |
| SFR Definition 10.5. IT01CF: INT0/INT1 Configuration .....           | 105 |
| SFR Definition 11.1. VDDMON: VDD Monitor Control .....               | 109 |
| SFR Definition 11.2. RSTSRC: Reset Source .....                      | 112 |
| SFR Definition 12.1. PSCTL: Program Store R/W Control .....          | 119 |
| SFR Definition 12.2. FLKEY: Flash Lock and Key .....                 | 119 |
| SFR Definition 13.1. XBR0: Port I/O Crossbar Register 0 .....        | 127 |
| SFR Definition 13.2. XBR1: Port I/O Crossbar Register 1 .....        | 128 |
| SFR Definition 13.3. P0: Port0 .....                                 | 129 |
| SFR Definition 13.4. P0MDIN: Port0 Input Mode .....                  | 129 |
| SFR Definition 13.5. P0MDOUT: Port0 Output Mode .....                | 130 |
| SFR Definition 13.6. P0SKIP: Port0 Skip .....                        | 130 |
| SFR Definition 13.7. P0MAT: Port0 Match .....                        | 131 |
| SFR Definition 13.8. P0MASK: Port0 Mask .....                        | 131 |
| SFR Definition 13.9. P1: Port1 .....                                 | 132 |
| SFR Definition 13.10. P1MDIN: Port1 Input Mode .....                 | 132 |
| SFR Definition 13.11. P1MDOUT: Port1 Output Mode .....               | 133 |
| SFR Definition 13.12. P1SKIP: Port1 Skip .....                       | 133 |

# C8051F52x/F52xA/F53x/F53xA

---

|  |     |
|--|-----|
| SFR Definition 13.13. P0SKIP: Port0 Skip .....                           | 134 |
| SFR Definition 13.14. P1MAT: Port1 Match .....                           | 134 |
| SFR Definition 13.15. P1MASK: Port1 Mask .....                           | 134 |
| SFR Definition 14.1. OSCICN: Internal Oscillator Control .....           | 137 |
| SFR Definition 14.2. OSCICL: Internal Oscillator Calibration .....       | 138 |
| SFR Definition 14.3. OSCIFIN: Internal Fine Oscillator Calibration ..... | 138 |
| SFR Definition 14.4. OSCXCN: External Oscillator Control .....           | 142 |
| SFR Definition 14.5. CLKSEL: Clock Select .....                          | 143 |
| SFR Definition 15.1. SCON0: Serial Port 0 Control .....                  | 149 |
| SFR Definition 15.2. SBUF0: Serial (UART0) Port Data Buffer .....        | 150 |
| SFR Definition 16.1. SPI0CFG: SPI0 Configuration .....                   | 157 |
| SFR Definition 16.2. SPI0CN: SPI0 Control .....                          | 158 |
| SFR Definition 16.3. SPI0CKR: SPI0 Clock Rate .....                      | 159 |
| SFR Definition 16.4. SPI0DAT: SPI0 Data .....                            | 160 |
| SFR Definition 17.1. LINADDR: Indirect Address Register .....            | 172 |
| SFR Definition 17.2. LINDATA: LIN Data Register .....                    | 172 |
| SFR Definition 17.3. LINCFL: LIN Control Mode Register .....             | 173 |
| SFR Definition 17.4. LIN0DT1: LIN0 Data Byte 1 .....                     | 174 |
| SFR Definition 17.5. LIN0DT2: LIN0 Data Byte 2 .....                     | 175 |
| SFR Definition 17.6. LIN0DT3: LIN0 Data Byte 3 .....                     | 175 |
| SFR Definition 17.7. LIN0DT4: LIN0 Data Byte 4 .....                     | 175 |
| SFR Definition 17.8. LIN0DT5: LIN0 Data Byte 5 .....                     | 176 |
| SFR Definition 17.9. LIN0DT6: LIN0 Data Byte 6 .....                     | 176 |
| SFR Definition 17.10. LIN0DT7: LIN0 Data Byte 7 .....                    | 176 |
| SFR Definition 17.11. LIN0DT8: LIN0 Data Byte 8 .....                    | 176 |
| SFR Definition 17.12. LIN0CTRL: LIN0 Control Register .....              | 177 |
| SFR Definition 17.13. LIN0ST: LIN0 STATUS Register .....                 | 178 |
| SFR Definition 17.14. LIN0ERR: LIN0 ERROR Register .....                 | 179 |
| SFR Definition 17.15. LIN0SIZE: LIN0 Message Size Register .....         | 180 |
| SFR Definition 17.16. LIN0DIV: LIN0 Divider Register .....               | 180 |
| SFR Definition 17.17. LIN0MUL: LIN0 Multiplier Register .....            | 181 |
| SFR Definition 17.18. LIN0ID: LIN0 ID Register .....                     | 181 |
| SFR Definition 18.1. TCON: Timer Control .....                           | 186 |
| SFR Definition 18.2. TMOD: Timer Mode .....                              | 187 |
| SFR Definition 18.3. CKCON: Clock Control .....                          | 188 |
| SFR Definition 18.4. TL0: Timer 0 Low Byte .....                         | 189 |
| SFR Definition 18.5. TL1: Timer 1 Low Byte .....                         | 189 |
| SFR Definition 18.6. TH0: Timer 0 High Byte .....                        | 189 |
| SFR Definition 18.7. TH1: Timer 1 High Byte .....                        | 189 |
| SFR Definition 18.8. TMR2CN: Timer 2 Control .....                       | 193 |
| SFR Definition 18.9. TMR2RLL: Timer 2 Reload Register Low Byte .....     | 194 |
| SFR Definition 18.10. TMR2RLH: Timer 2 Reload Register High Byte .....   | 194 |
| SFR Definition 18.11. TMR2L: Timer 2 Low Byte .....                      | 194 |
| SFR Definition 18.12. TMR2H: Timer 2 High Byte .....                     | 194 |
| SFR Definition 19.1. PCA0CN: PCA Control .....                           | 206 |

---

# C8051F52x/F52xA/F53x/F53xA

---

|  |     |
|--|-----|
| SFR Definition 19.2. PCA0MD: PCA Mode .....                            | 207 |
| SFR Definition 19.3. PCA0CPMn: PCA Capture/Compare Mode .....          | 208 |
| SFR Definition 19.4. PCA0L: PCA Counter/Timer Low Byte .....           | 209 |
| SFR Definition 19.5. PCA0H: PCA Counter/Timer High Byte .....          | 209 |
| SFR Definition 19.6. PCA0CPLn: PCA Capture Module Low Byte .....       | 209 |
| SFR Definition 19.7. PCA0CPHn: PCA Capture Module High Byte .....      | 209 |
| C2 Register Definition 21.1. C2ADD: C2 Address .....                   | 214 |
| C2 Register Definition 21.2. DEVICEID: C2 Device ID .....              | 214 |
| C2 Register Definition 21.3. REVID: C2 Revision ID .....               | 215 |
| C2 Register Definition 21.4. FPCTL: C2 Flash Programming Control ..... | 215 |
| C2 Register Definition 21.5. FPDAT: C2 Flash Programming Data .....    | 215 |

## 1. System Overview

The C8051F52x/F52xA/F53x/F53xA family of devices are fully integrated, low power, mixed-signal system-on-a-chip MCUs. Highlighted features are listed below. Refer to Table 1.1 for specific product feature selection.

- High-speed pipelined 8051-compatible microcontroller core (up to 25 MIPS)
- In-system, full-speed, non-intrusive debug interface (on-chip)
- True 12-bit 200 ksp/s ADC with analog multiplexer and up to 16 analog inputs
- Precision programmable 24.5 MHz internal oscillator that is within  $\pm 0.5\%$  across the temperature range and for VDD voltages greater than or equal to the on-chip voltage regulator minimum output at the low setting. The oscillator is within  $\pm 1.0\%$  for VDD voltages below this minimum output setting.
- Up to 7680 bytes of on-chip Flash memory
- 256 bytes of on-chip RAM
- Enhanced UART, and SPI serial interfaces implemented in hardware
- LIN 2.1 peripheral (fully backwards compatible, master and slave modes)
- Three general-purpose 16-bit timers
- Programmable Counter/Timer Array (PCA) with three capture/compare modules and Watchdog Timer function
- On-chip Power-On Reset, V<sub>DD</sub> Monitor, and Temperature Sensor
- On-chip Voltage Comparator
- Up to 16 Port I/O

With on-chip Power-On Reset, V<sub>DD</sub> monitor, Watchdog Timer, and clock oscillator, the C8051F52x/F52xA/F53x/F53xA devices are truly standalone system-on-a-chip solutions. The Flash memory is byte writable and can be reprogrammed in-circuit, providing non-volatile data storage, and also allowing field upgrades of the 8051 firmware. User software has complete control of all peripherals, and may individually shut down any or all peripherals for power savings.

The on-chip Silicon Laboratories 2-Wire (C2) Development Interface allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection and modification of memory and registers, setting breakpoints, single stepping, run and halt commands. All analog and digital peripherals are fully functional while debugging using C2. The two C2 interface pins can be shared with user functions, allowing in-system programming and debugging without occupying package pins.

Each device is specified for 2.0 to 5.25 V operation (supply voltage can be up to 5.25 V using on-chip regulator) over the automotive temperature range ( $-40$  to  $+125$  °C). The F52x/F52xA is available in the DFN10 (3 x 3 mm) package. The F53x/F53xA is available in the QFN20 (4 x 4 mm) or the TSSOP20 package.

# C8051F52x/F52xA/F53x/F53xA

## 1.1. Ordering Information

The following features are common to all devices in this family:

- 25 MHz system clock and 25 MIPS throughput (peak)
- 256 bytes of internal RAM
- Enhanced SPI peripheral
- Enhanced UART peripheral
- Three Timers
- Three Programmable Counter Array channels
- Internal 24.5 MHz oscillator
- Internal Voltage Regulator
- 12-bit, 200 ksps ADC
- Internal Voltage Reference and Temperature Sensor
- One Analog Comparator

Table 1.1 shows the features that differentiate the devices in this family.

**Table 1.1. Product Selection Guide (Recommended for New Designs)**

| Ordering Part Number | Flash Memory (kB) | Port I/Os | LIN | Package | Ordering Part Number | Flash Memory (kB) | Port I/Os | LIN | Package  |
|----------------------|-------------------|-----------|-----|---------|----------------------|-------------------|-----------|-----|----------|
| C8051F520-C-IM       | 8                 | 6         | ✓   | DFN-10  | C8051F534-C-IM       | 4                 | 16        | —   | QFN-20   |
| C8051F521-C-IM       | 8                 | 6         | —   | DFN-10  | C8051F536-C-IM       | 2                 | 16        | ✓   | QFN-20   |
| C8051F523-C-IM       | 4                 | 6         | ✓   | DFN-10  | C8051F537-C-IM       | 2                 | 16        | —   | QFN-20   |
| C8051F524-C-IM       | 4                 | 6         | —   | DFN-10  | C8051F530-C-IT       | 8                 | 16        | ✓   | TSSOP-20 |
| C8051F526-C-IM       | 2                 | 6         | ✓   | DFN-10  | C8051F531-C-IT       | 8                 | 16        | —   | TSSOP-20 |
| C8051F527-C-IM       | 2                 | 6         | —   | DFN-10  | C8051F533-C-IT       | 4                 | 16        | ✓   | TSSOP-20 |
| C8051F530-C-IM       | 8                 | 16        | ✓   | QFN-20  | C8051F534-C-IT       | 4                 | 16        | —   | TSSOP-20 |
| C8051F531-C-IM       | 8                 | 16        | —   | QFN-20  | C8051F536-C-IT       | 2                 | 16        | ✓   | TSSOP-20 |
| C8051F533-C-IM       | 4                 | 16        | ✓   | QFN-20  | C8051F537-C-IT       | 2                 | 16        | —   | TSSOP-20 |

All devices in Table 1.1 are also available in an automotive version. For the automotive version, the -I in the ordering part number is replaced with -A. For example, the automotive version of the C8051F520-C-IM is the C8051F520-C-AM.

The -AM and -AT devices receive full automotive quality production status, including AEC-Q100 qualification (fault coverage report available upon request), registration with International Material Data System (IMDS) and Part Production Approval Process (PPAP) documentation. PPAP documentation is available at [www.silabs.com](http://www.silabs.com) with a registered NDA and approved user account. The -AM and -AT devices enable high volume automotive OEM applications with their enhanced testing and processing. Please contact Silicon Labs sales for more information regarding -AM and -AT devices for your automotive project.

# C8051F52x/F52xA/F53x/F53xA

**Table 1.2. Product Selection Guide (Not Recommended for New Designs)**

| Ordering Part Number          | Flash Memory (kB) | Port I/Os | LIN | Package | Ordering Part Number          | Flash Memory (kB) | Port I/Os | LIN | Package  |
|-------------------------------|-------------------|-----------|-----|---------|-------------------------------|-------------------|-----------|-----|----------|
| C8051F520-IM<br>C8051F520A-IM | 8                 | 6         | ✓   | DFN-10  | C8051F534-IM<br>C8051F534A-IM | 4                 | 16        | —   | QFN-20   |
| C8051F521-IM<br>C8051F521A-IM | 8                 | 6         | —   | DFN-10  | C8051F536-IM<br>C8051F536A-IM | 2                 | 16        | ✓   | QFN-20   |
| C8051F523-IM<br>C8051F523A-IM | 4                 | 6         | ✓   | DFN-10  | C8051F537-IM<br>C8051F537A-IM | 2                 | 16        | —   | QFN-20   |
| C8051F524-IM<br>C8051F524A-IM | 4                 | 6         | —   | DFN-10  | C8051F530-IT<br>C8051F530A-IT | 8                 | 16        | ✓   | TSSOP-20 |
| C8051F526-IM<br>C8051F526A-IM | 2                 | 6         | ✓   | DFN-10  | C8051F531-IT<br>C8051F531A-IT | 8                 | 16        | —   | TSSOP-20 |
| C8051F527-IM<br>C8051F527A-IM | 2                 | 6         | —   | DFN-10  | C8051F533-IT<br>C8051F533A-IT | 4                 | 16        | ✓   | TSSOP-20 |
| C8051F530-IM<br>C8051F530A-IM | 8                 | 16        | ✓   | QFN-20  | C8051F534-IT<br>C8051F534A-IT | 4                 | 16        | —   | TSSOP-20 |
| C8051F531-IM<br>C8051F531A-IM | 8                 | 16        | —   | QFN-20  | C8051F536-IT<br>C8051F536A-IT | 2                 | 16        | ✓   | TSSOP-20 |
| C8051F533-IM<br>C8051F533A-IM | 4                 | 16        | ✓   | QFN-20  | C8051F537-IT<br>C8051F537A-IT | 2                 | 16        | —   | TSSOP-20 |

The part numbers in Table 1.2 are not recommended for new designs. Instead, select the corresponding part number from Table 1.1 (silicon revision C) for your design. In Table 1.2, the part numbers in the format similar to C8051F520-IM are silicon revision A devices. The part numbers in the format similar to C8051F520A-IM are silicon revision B devices.



# C8051F52x/F52xA/F53x/F53xA

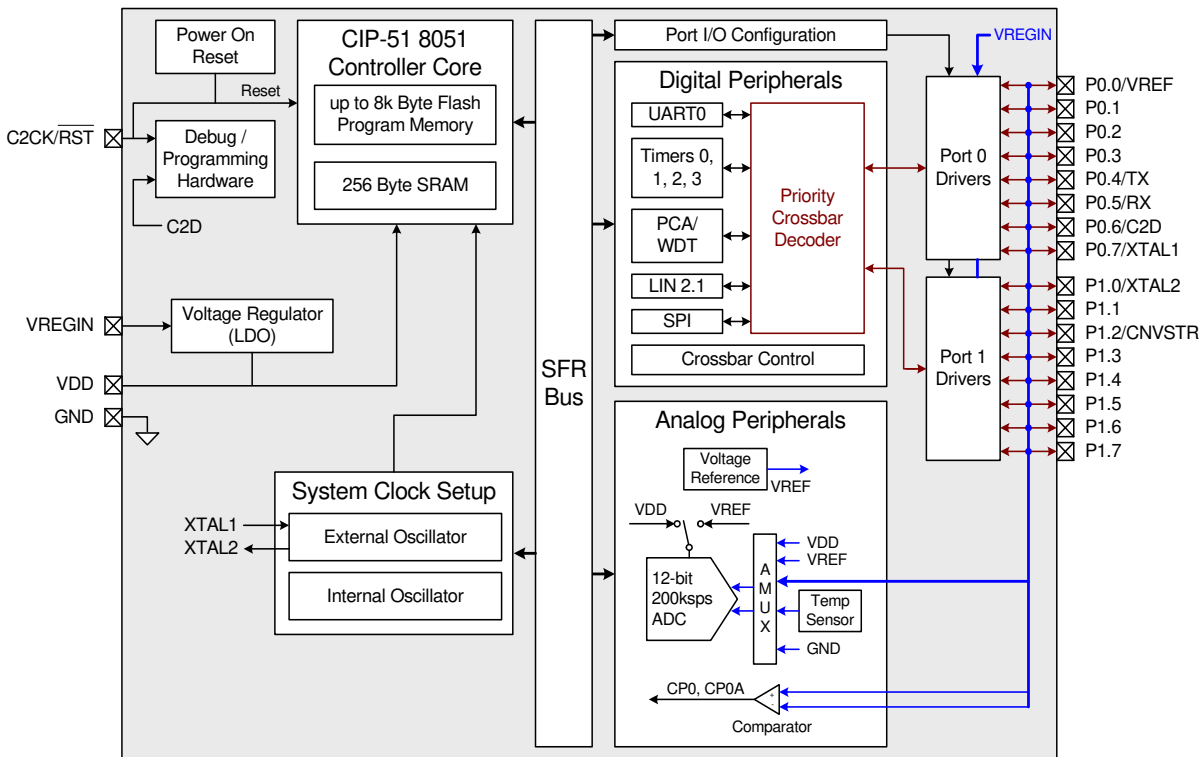


Figure 1.1. C8051F53xA/F53x-C Block Diagram

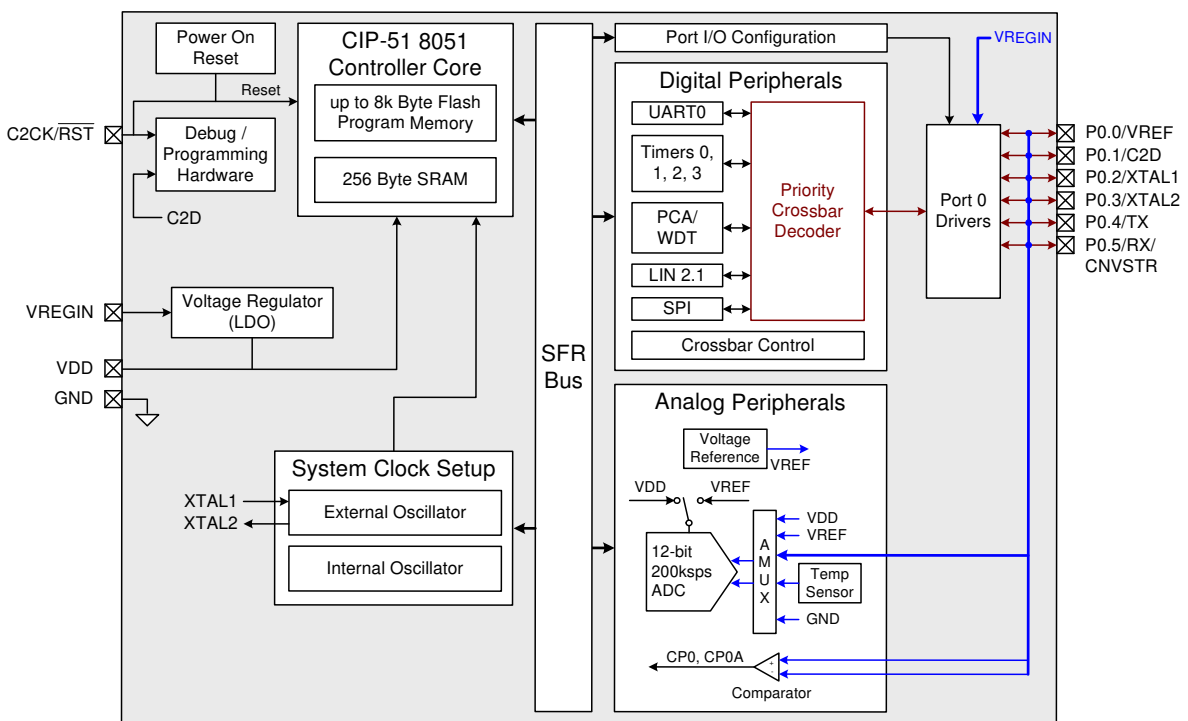


Figure 1.2. C8051F52xA/F52x-C Block Diagram

# C8051F52x/F52xA/F53x/F53xA

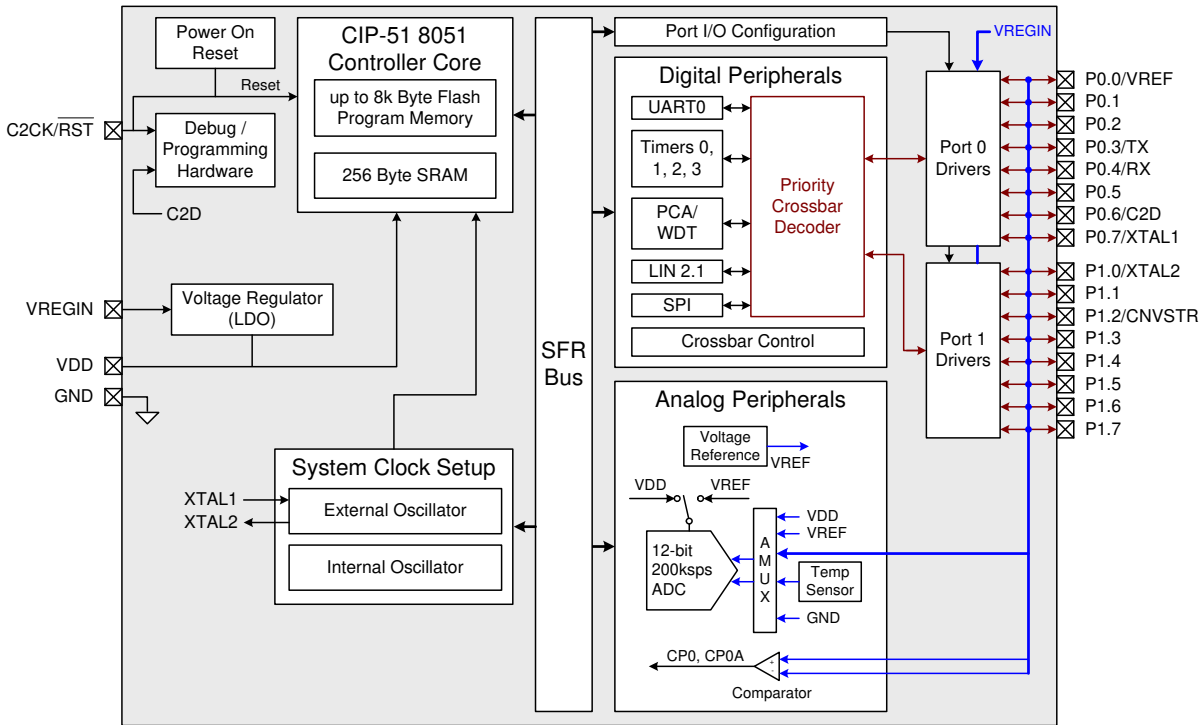


Figure 1.3. C8051F53x Block Diagram (Silicon Revision A)

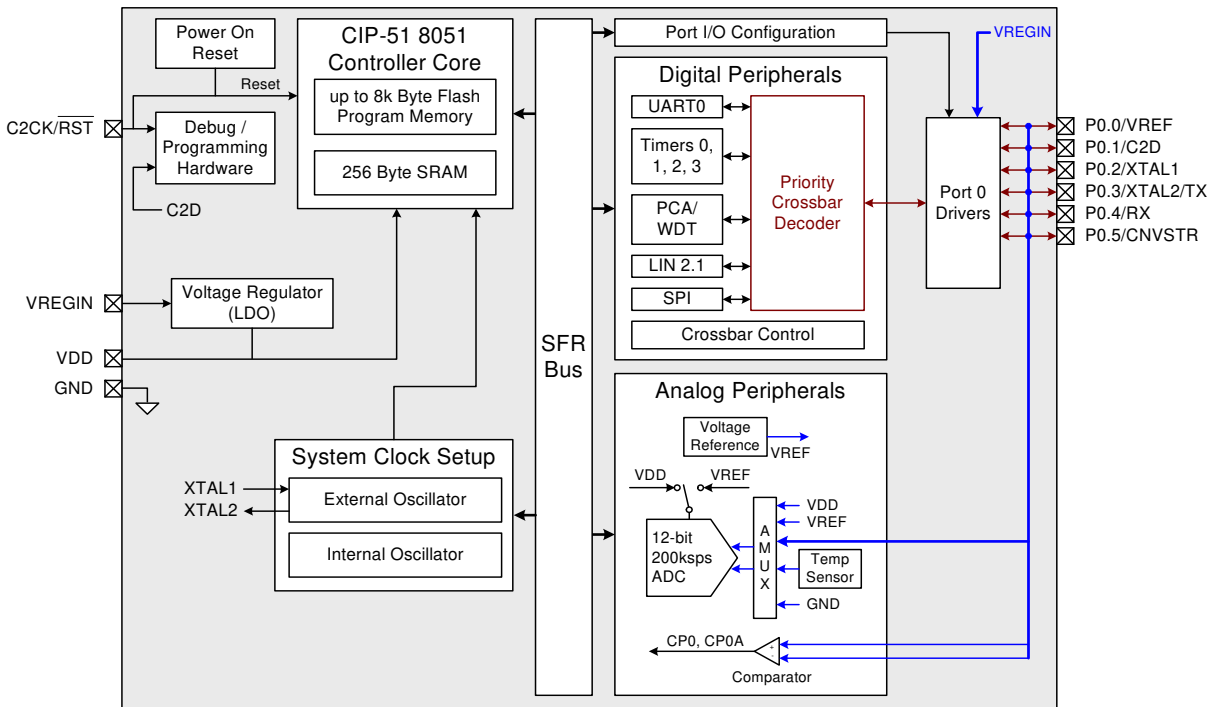


Figure 1.4. C8051F52x Block Diagram (Silicon Revision A)

# C8051F52x/F52xA/F53x/F53xA

## 1.2. CIP-51™ Microcontroller

### 1.2.1. Fully 8051 Compatible Instruction Set

The C8051F52x/F52xA/F53x/F53xA devices use Silicon Laboratories' proprietary CIP-51 microcontroller core. The CIP-51 is fully compatible with the MCS-51™ instruction set. Standard 803x/805x assemblers and compilers can be used to develop software. The C8051F52x/F52xA/F53x/F53xA family has a superset of all the peripherals included with a standard 8052.

### 1.2.2. Improved Throughput

The CIP-51 employs a pipelined architecture that greatly increases its instruction throughput over the standard 8051 architecture. In a standard 8051, all instructions except for MUL and DIV take 12 or 24 system clock cycles to execute, and usually have a maximum system clock of 12-to-24 MHz. By contrast, the CIP-51 core executes 70% of its instructions in one or two system clock cycles, with no instructions taking more than eight system clock cycles.

With the CIP-51's system clock running at 25 MHz, it has a peak throughput of 25 MIPS. The CIP-51 has a total of 109 instructions. The table below shows the total number of instructions that require each execution time.

|                        |    |    |     |    |     |   |     |   |   |
|------------------------|----|----|-----|----|-----|---|-----|---|---|
| Clocks to Execute      | 1  | 2  | 2/3 | 3  | 3/4 | 4 | 4/5 | 5 | 8 |
| Number of Instructions | 26 | 50 | 5   | 14 | 7   | 3 | 1   | 2 | 1 |

### 1.2.3. Additional Features

The C8051F52x/F52xA/F53x/F53xA family includes several key enhancements to the CIP-51 core and peripherals to improve performance and ease of use in end applications.

An extended interrupt handler allows the numerous analog and digital peripherals to operate independently of the controller core and interrupt the controller only when necessary. By requiring less intervention from the microcontroller core, an interrupt-driven system is more efficient and allows for easier implementation of multi-tasking, real-time systems.

Eight reset sources are available: power-on reset circuitry (POR), an on-chip  $V_{DD}$  monitor, a Watchdog Timer, a Missing Clock Detector, a voltage level detection from Comparator, a forced software reset, an external reset pin, and an illegal Flash access protection circuit. Each reset source except for the POR, Reset Input Pin, or Flash error may be disabled by the user in software. The WDT may be permanently enabled in software after a power-on reset during MCU initialization.

The internal oscillator is factory calibrated to 24.5 MHz  $\pm 0.5\%$  across the entire operating temperature and voltage range. An external oscillator drive circuit is also included, allowing an external crystal, ceramic resonator, capacitor, RC, or CMOS clock source to generate the system clock.

### 1.2.4. On-Chip Debug Circuitry

The C8051F52x/F52xA/F53x/F53xA devices include on-chip Silicon Laboratories 2-Wire (C2) debug circuitry that provides non-intrusive, full speed, in-circuit debugging of the production part *installed in the end application*.

Silicon Laboratories' debugging system supports inspection and modification of memory and registers, breakpoints, and single stepping. No additional target RAM, program memory, timers, or communications channels are required. All the digital and analog peripherals are functional and work correctly while debugging. All the peripherals (except for the ADC) are stalled when the MCU is halted, during single stepping, or at a breakpoint in order to keep them synchronized.

The C8051F530DK development kit provides all the hardware and software necessary to develop application code and perform in-circuit debugging with the C8051F52x/F52xA/F53x/F53xA MCUs. The kit

# C8051F52x/F52xA/F53x/F53xA

includes software with a developer's studio and debugger, a USB debug adapter, a target application board with the associated MCU installed, and the required cables and wall-mount power supply. The development kit requires a computer with Windows installed. As shown in Figure 1.5, the PC is connected to the USB debug adapter. A six-inch ribbon cable connects the USB debug adapter to the user's application board, picking up the two C2 pins and GND.

The Silicon Laboratories IDE interface is a vastly superior developing and debugging configuration, compared to standard MCU emulators that use on-board "ICE Chips" and require the MCU in the application board to be socketed. Silicon Laboratories' debug paradigm increases ease of use and preserves the performance of the precision analog peripherals.

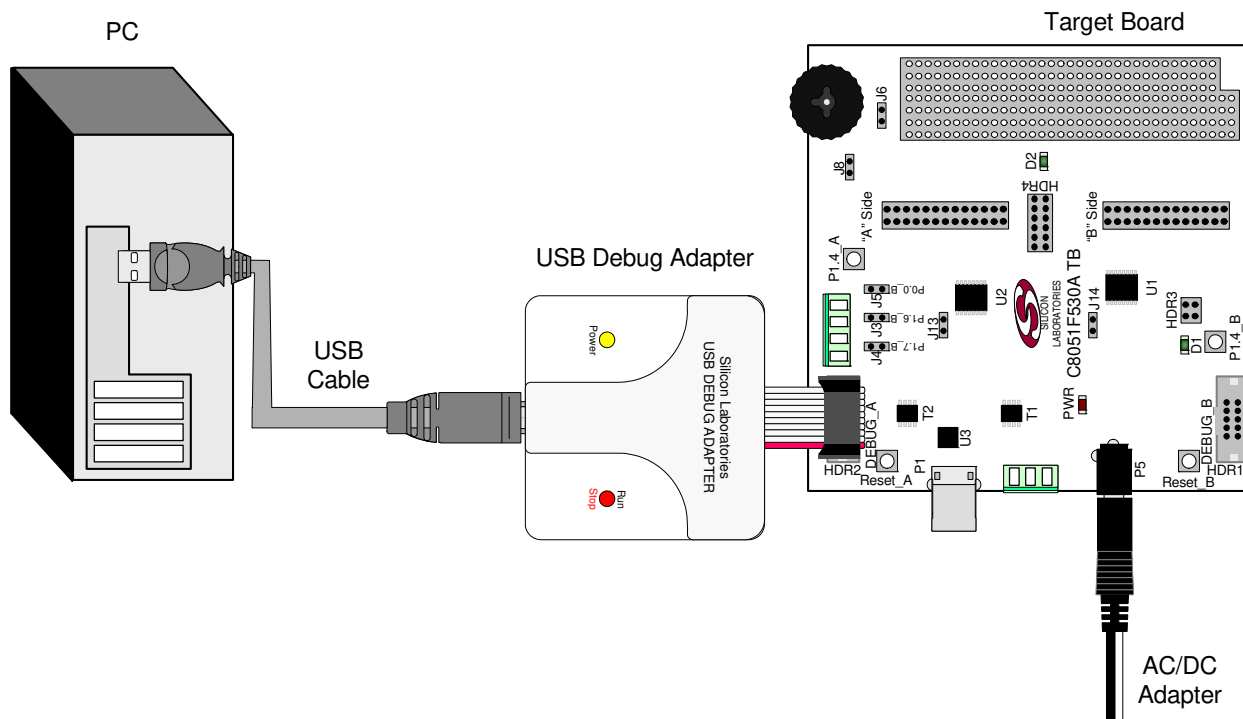


Figure 1.5. Development/In-System Debug Diagram

# C8051F52x/F52xA/F53x/F53xA

## 1.3. On-Chip Memory

The CIP-51 has a standard 8051 program and data address configuration. It includes 256 bytes of data RAM, with the upper 128 bytes dual-mapped. Indirect addressing accesses the upper 128 bytes of general purpose RAM, and direct addressing accesses the 128 byte SFR address space. The lower 128 bytes of RAM are accessible via direct and indirect addressing. The first 32 bytes are addressable as four banks of general purpose registers, and the next 16 bytes can be byte addressable or bit addressable.

Program memory consists of 7680 bytes ('F520/0A/1/1A and 'F530/0A/1/1A), 4 kB ('F523/3A/4/4A and C8051F53x/53xA), or 2 kB ('F526/6A/7/7A and 'F536/6A/7/7A) of Flash. This memory is byte writable and erased in 512-byte sectors, and requires no special off-chip programming voltage.

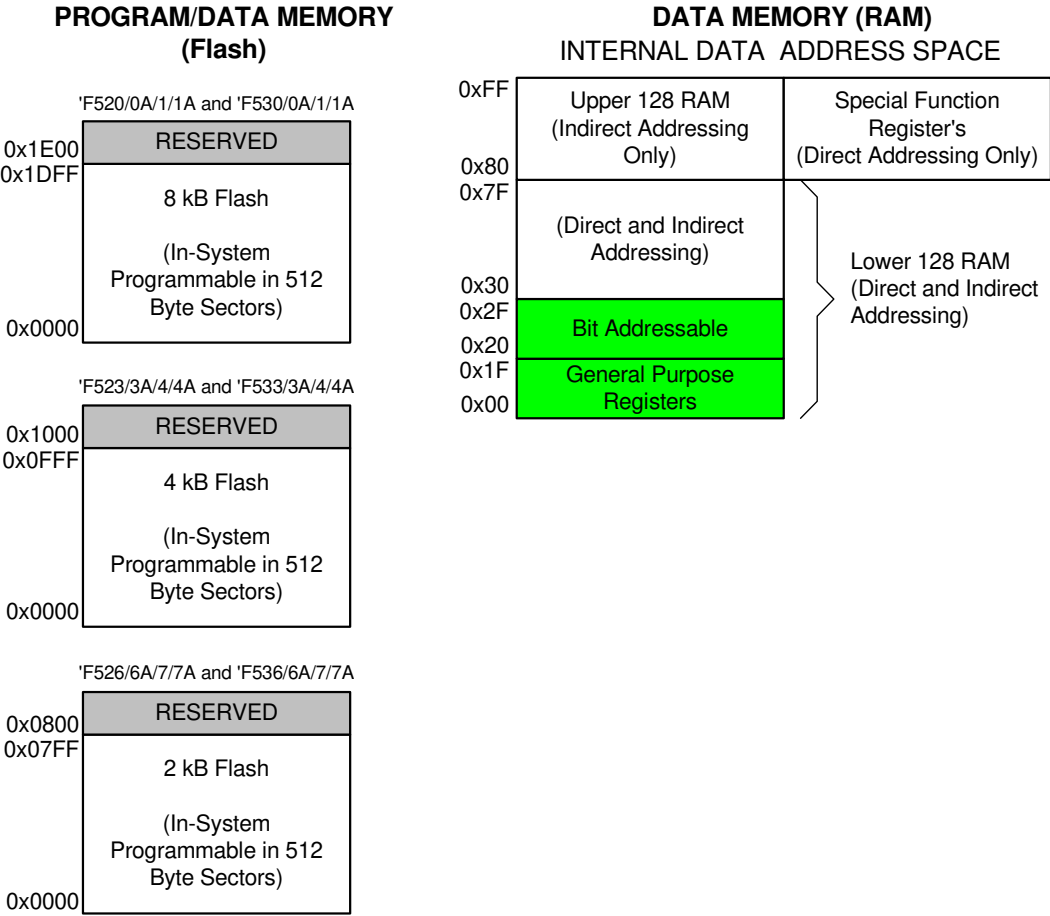


Figure 1.6. Memory Map

# C8051F52x/F52xA/F53x/F53xA

## 1.4. Operating Modes

The C8051F52x/F52xA/F53x/F53xA devices have four operating modes: Active (Normal), Idle, Suspend, and Stop. Active mode occurs during normal operation when the oscillator and peripherals are active. Idle mode halts the CPU while leaving the peripherals and internal clocks active. In Suspend and Stop mode, the CPU is halted, all interrupts and timers are inactive, and the internal oscillator is stopped. The various operating modes are described in Table 1.3 below:

**Table 1.3. Operating Modes Summary**

|         | <b>Properties</b>   | <b>Power Consumption</b> | <b>How Entered?</b> | <b>How Exited?</b>   |
|---------|---|--------------------------|---------------------|--|
| Active  | <ul style="list-style-type: none"><li>■ SYSCLK active</li><li>■ CPU active (accessing Flash)</li><li>■ Peripherals active or inactive depending on user settings</li></ul>  | Full                     | —                   | —  |
| Idle    | <ul style="list-style-type: none"><li>■ SYSCLK active</li><li>■ CPU inactive (not accessing Flash)</li><li>■ Peripherals active or inactive depending on user settings</li></ul>  | Less than Full           | IDLE (PCON.0)       | Any enabled interrupt or device reset  |
| Suspend | <ul style="list-style-type: none"><li>■ Internal oscillator inactive</li><li>■ If SYSCLK is derived from the internal oscillator, the peripherals and the CIP-51 will be stopped</li></ul>                              | Low                      | SUSPEND (OSCICN.5)  | Port 0 event match<br>Port 1 event match<br>Comparator 0 enabled and output is logic 0 |
| Stop    | <ul style="list-style-type: none"><li>■ SYSCLK inactive</li><li>■ CPU inactive (not accessing Flash)</li><li>■ Digital peripherals inactive; analog peripherals active or inactive depending on user settings</li></ul> | Very low                 | STOP (PCON.1)       | Device Reset   |

See Section “8.3. Power Management Modes” on page 89 for Idle and Stop mode details. See Section “14.1.1. Internal Oscillator Suspend Mode” on page 136 for more information on Suspend mode.

# C8051F52x/F52xA/F53x/F53xA

## 1.5. 12-Bit Analog to Digital Converter

The C8051F52x/F52xA/F53x/F53xA devices include an on-chip 12-bit SAR ADC with a maximum throughput of 200 ksp/s. The ADC system includes a configurable analog multiplexer that selects the positive ADC input, which is measured with respect to GND. Ports 0 and 1 are available as ADC inputs; additionally, the ADC includes an innovative programmable gain stage which allows the ADC to sample inputs sources greater than the VREF voltage. The on-chip Temperature Sensor output and the core supply voltage ( $V_{DD}$ ) are also available as ADC inputs. User firmware may shut down the ADC or use it in Burst Mode to save power.

Conversions can be initiated in four ways: a software command, an overflow of Timer 1, an overflow of Timer 2, or an external convert start signal. This flexibility allows the start of conversion to be triggered by software events, a periodic signal (timer overflows), or external HW signals. Conversion completions are indicated by a status bit and an interrupt (if enabled) and occur after 1, 4, 8, or 16 samples have been accumulated by a hardware accumulator. The resulting 12-bit to 16-bit data word is latched into the ADC data SFRs upon completion of a conversion. When the system clock is slow, Burst Mode allows ADC0 to automatically wake from a low power shutdown state, acquire and accumulate samples, then re-enter the low power shutdown state without CPU intervention.

Window compare registers for the ADC data can be configured to interrupt the controller when ADC data is either within or outside of a specified range. The ADC can monitor a key voltage continuously in background mode, but not interrupt the controller unless the converted data is within/outside the specified range.

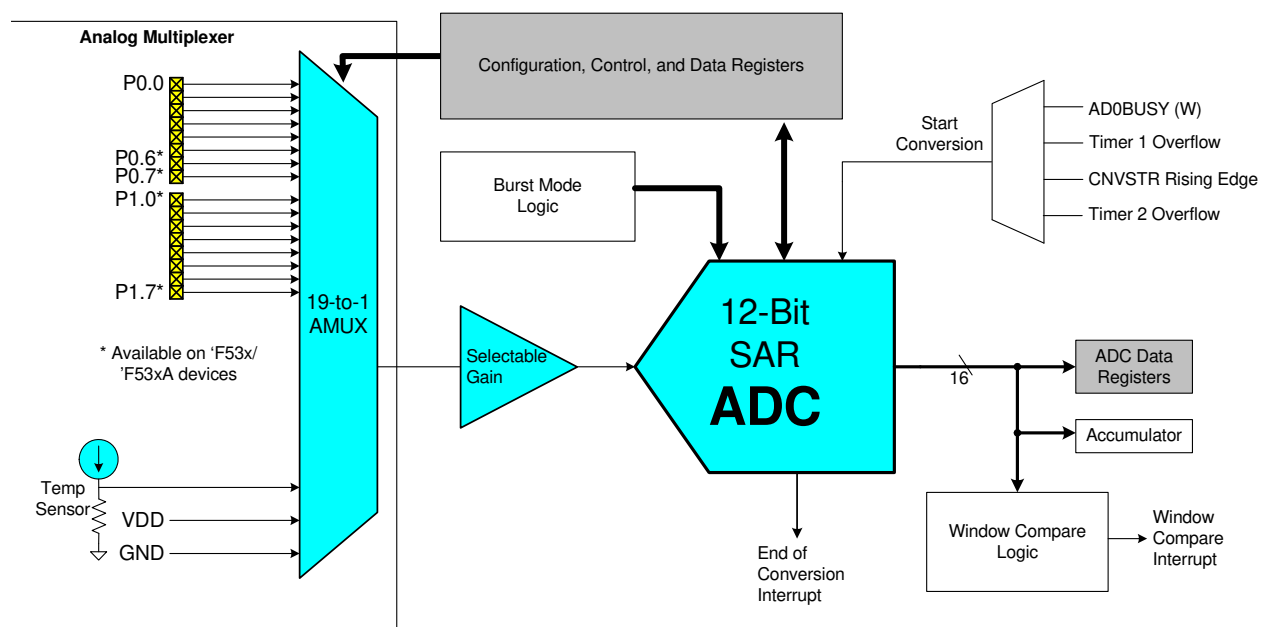


Figure 1.7. 12-Bit ADC Block Diagram

## 1.6. Programmable Comparator

C8051F52x/F52xA/F53x/F53xA devices include a software-configurable voltage comparator with an input multiplexer. The comparator offers programmable response time and hysteresis and an output that is optionally available at the Port pins: a synchronous “latched” output (CP0). The comparator interrupt may be generated on rising, falling, or both edges. When in IDLE or SUSPEND mode, these interrupts may be used as a “wake-up” source for the processor. The Comparator may also be configured as a reset source. A block diagram of the comparator is shown in Figure 1.8.

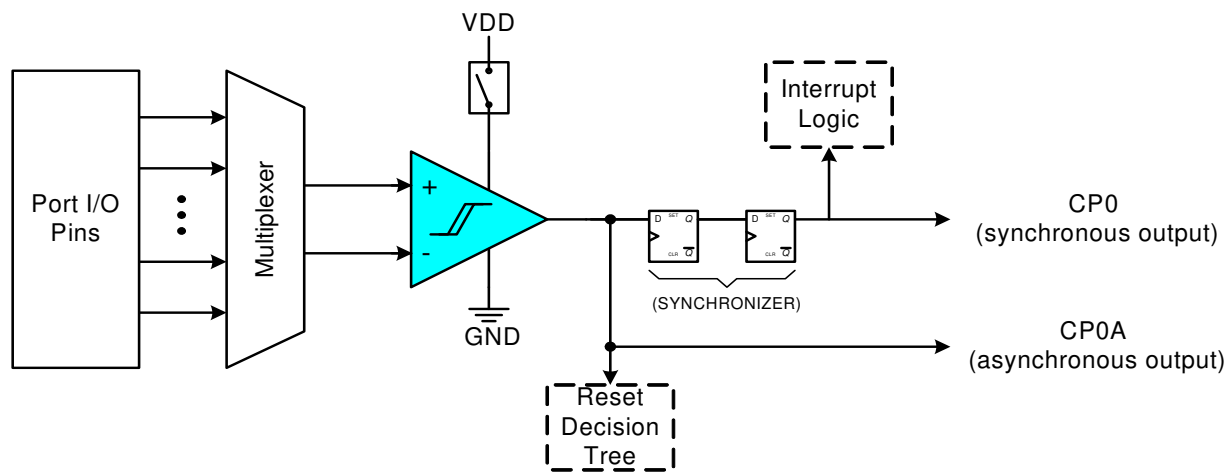


Figure 1.8. Comparator Block Diagram

## 1.7. Voltage Regulator

C8051F52x/F52xA/F53x/F53xA devices include an on-chip low dropout voltage regulator (REG0). The input to REG0 at the  $V_{\text{REGIN}}$  pin can be as high as 5.25 V. The output can be selected by software to 2.1 or 2.6 V. When enabled, the output of REG0 powers the device and drives the  $V_{\text{DD}}$  pin. The voltage regulator can be used to power external devices connected to  $V_{\text{DD}}$ .

## 1.8. Serial Port

The C8051F52x/F52xA/F53x/F53xA family includes a full-duplex UART with enhanced baud rate configuration, and an Enhanced SPI interface. Each of the serial buses is fully implemented in hardware and makes extensive use of the CIP-51's interrupts, thus requiring very little CPU intervention.



# C8051F52x/F52xA/F53x/F53xA

## 1.9. Port Input/Output

C8051F52x/F52xA/F53x/F53xA devices include up to 16 I/O pins. Port pins are organized as two byte-wide ports. The port pins behave like typical 8051 ports with a few enhancements. Each port pin can be configured as a digital or analog I/O pin. Pins selected as digital I/O can be configured for push-pull or open-drain operation. The “weak pullups” that are fixed on typical 8051 devices may be globally disabled to save power.

The Digital Crossbar allows mapping of internal digital system resources to port I/O pins. On-chip counter/timers, serial buses, hardware interrupts, and other digital signals can be configured to appear on the port pins using the Crossbar control registers. This allows the user to select the exact mix of general-purpose port I/O, digital, and analog resources needed for the application.

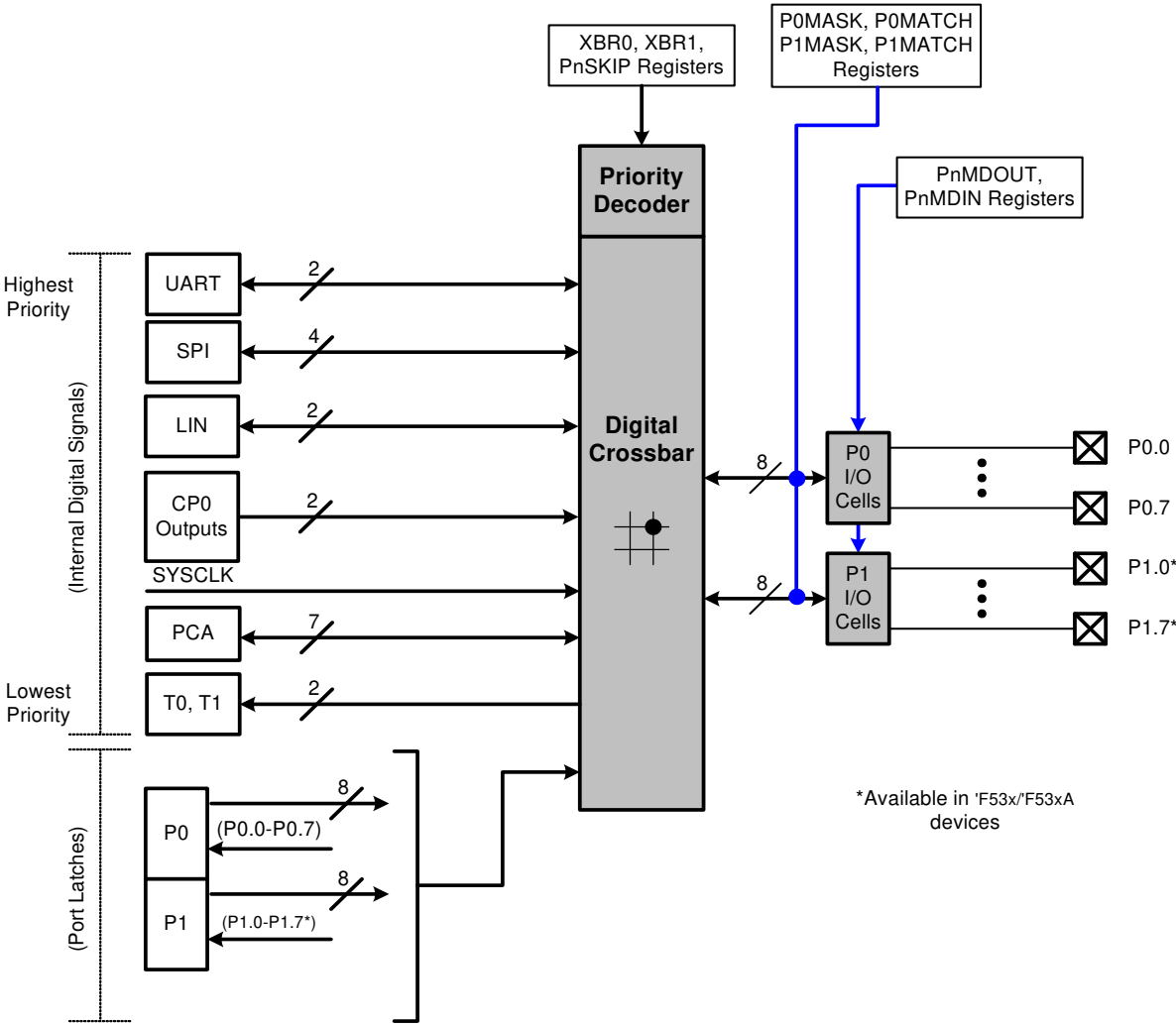


Figure 1.9. Port I/O Functional Block Diagram

## 2. Electrical Characteristics

### 2.1. Absolute Maximum Ratings

**Table 2.1. Absolute Maximum Ratings**

| Parameter  | Conditions | Min  | Typ | Max               | Units |
|--|------------|------|-----|-------------------|-------|
| Ambient temperature under Bias   |            | -55  | —   | 135               | °C    |
| Storage Temperature  |            | -65  | —   | 150               | °C    |
| Voltage on $V_{REGIN}$ with Respect to GND   |            | -0.3 | —   | 5.5               | V     |
| Voltage on $V_{DD}$ with Respect to GND  |            | -0.3 | —   | 2.8               | V     |
| Voltage on XTAL1 with Respect to GND   |            | -0.3 | —   | $V_{REGIN} + 0.3$ | V     |
| Voltage on XTAL2 with Respect to GND   |            | -0.3 | —   | $V_{REGIN} + 0.3$ | V     |
| Voltage on any Port I/O Pin or $\overline{RST}$ with Respect to GND  |            | -0.3 | —   | $V_{REGIN} + 0.3$ | V     |
| Maximum Output Current Sunk by any Port Pin  |            | —    | —   | 100               | mA    |
| Maximum Output Current Sourced by any Port Pin   |            | —    | —   | 100               | mA    |
| Maximum Total Current through $V_{REGIN}$ , and GND  |            | —    | —   | 500               | mA    |
| <p><b>Note:</b> Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.</p> |            |      |     |                   |       |