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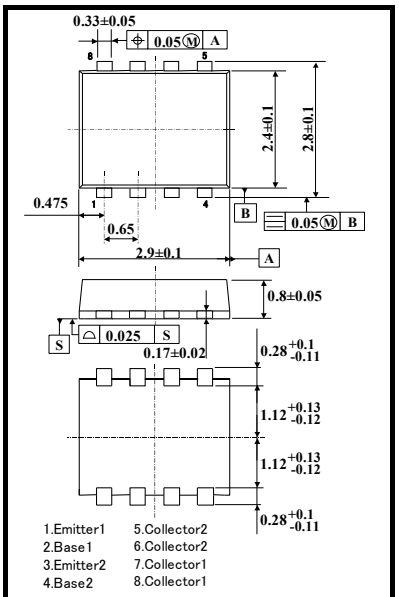
TOSHIBA Transistor Silicon NPN / PNP Epitaxial Type (PCT Process)

TPCP8901

Portable Equipment Applications

Switching Applications

Unit: mm



JEDEC	—
JEITA	—
TOSHIBA	2-3V1C

Weight: 0.017 g (typ.)

- Small footprint due to small and thin package
- High DC current gain : PNP h_{FE} = 200 to 500 (I_C = –0.1 A)
  :NPN h_{FE} = 400 to 1000 (I_C = 0.1 A)
- Low collector-emitter saturation : PNP $V_{CE\ (sat)}$ = –0.20 V (max)
  : NPN $V_{CE\ (sat)}$ = 0.17 V (max)
- High-speed switching : PNP t_f = 70 ns (typ.)
  : NPN t_f = 85 ns (typ.)

Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating		Unit
			PNP	NPN	
Collector-base voltage		V_{CBO}	–50	100	V
Collector-emitter voltage		V_{CEO}	–50	50	V
Emitter-base voltage		V_{EBO}	–7	7	V
Collector current	DC (Note 1)	I_C	–0.8	1.0	A
	Pulse (Note 1)	I_{CP}	–5.0	5.0	
Base current		I_B	–100	100	mA
Collector power dissipation (t = 10s)	Single-device operation	P_C (Note 2)	1.48		W
	Single-device value at dual operation		0.80		
Collector power dissipation (DC)	Single-device operation	P_C (Note 2)	0.83		W
	Single-device value at dual operation		0.48		
Junction temperature		T_j	150		°C
Storage temperature range		T_{stg}	–55 to 150		°C

Note 1: Please use devices on condition that the junction temperature is below 150℃.
Icp=±5A (@ t≦100 μ s)

Note 2: Mounted on FR4 board (glass epoxy, 1.6 mm thick, Cu area: 645 mm^2)

Note 3: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Start of commercial production
2004-01

Figure 1. Circuit configuration (top view)

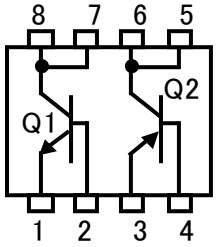
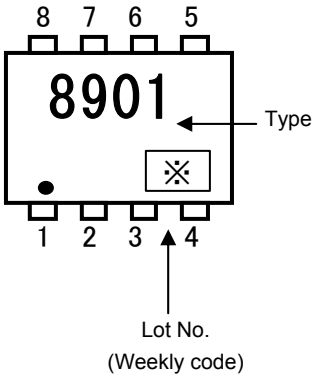
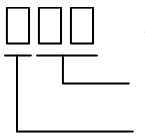


Figure 2. Marking (Note 4)



Note 4: ● on lower left on the marking indicates Pin 1.

※ Weekly code: (Three digits)



Week of manufacture

(01 for first week of year, continues up to 52 or 53)

Year of manufacture

(One low-order digits of calendar year)

Electrical Characteristics (Ta = 25°C)

PNP

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Collector cut-off current		I_{CBO}	V_{CB} = –50 V, I_E = 0	—	—	–100	nA
Emitter cut-off current		I_{EBO}	V_{EB} = –7 V, I_C = 0	—	—	–100	nA
Collector-emitter breakdown voltage		$V_{(BR)\ CEO}$	I_C = –10 mA, I_B = 0	–50	—	—	V
DC current gain		h_{FE} (1)	V_{CE} = –2 V, I_C = –0.1 A	200	—	500	
		h_{FE} (2)	V_{CE} = –2 V, I_C = –0.3 A	125	—	—	
Collector-emitter saturation voltage		$V_{CE\ (sat)}$	I_C = –0.3 A, I_B = –0.01 A	—	—	–0.20	V
Base-emitter saturation voltage		$V_{BE\ (sat)}$	I_C = –0.3 A, I_B = –0.01 A	—	—	–1.10	V
Collector output capacitance		C_{ob}	V_{CB} = –10 V, I_E = 0, f = 1MHz	—	8	—	pF
Switching time	Rise time	t_r	See Figure 3 circuit diagram V_{CC} ≃ –30 V, R_L = 100 Ω $-I_{B1} = I_{B2}$ = –10 mA	—	60	—	ns
	Storage time	t_{stg}		—	280	—	
	Fall time	t_f		—	70	—	

NPN

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Collector cut-off current		I_{CBO}	V_{CB} = 100 V, I_E = 0	—	—	100	nA
Emitter cut-off current		I_{EBO}	V_{EB} = 7 V, I_C = 0	—	—	100	nA
Collector-emitter breakdown voltage		$V_{(BR)\ CEO}$	I_C = 10 mA, I_B = 0	50	—	—	V
DC current gain		h_{FE} (1)	V_{CE} = 2 V, I_C = 0.1 A	400	—	1000	
		h_{FE} (2)	V_{CE} = 2 V, I_C = 0.3 A	200	—	—	
Collector-emitter saturation voltage		$V_{CE\ (sat)}$	I_C = 300 mA, I_B = 6 mA	—	—	0.17	V
Base-emitter saturation voltage		$V_{BE\ (sat)}$	I_C = 300 mA, I_B = 6 mA	—	—	1.10	V
Collector output capacitance		C_{ob}	V_{CB} = 10 V, I_E = 0, f = 1MHz	—	5	—	pF
Switching time	Rise time	t_r	See Figure 4 circuit diagram V_{CC} ≃ 30 V, R_L = 100 Ω $I_{B1} = -I_{B2}$ = 10 mA	—	35	—	ns
	Storage time	t_{stg}		—	680	—	
	Fall time	t_f		—	85	—	

Figure 3. Switching Time Test Circuit & Timing Chart

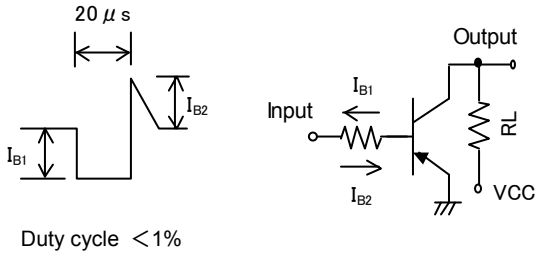
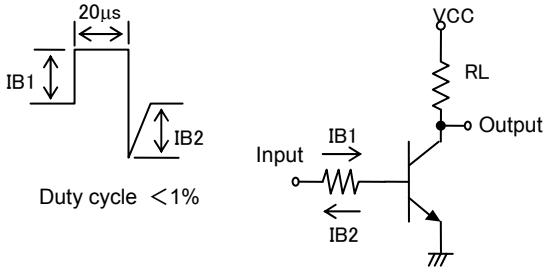
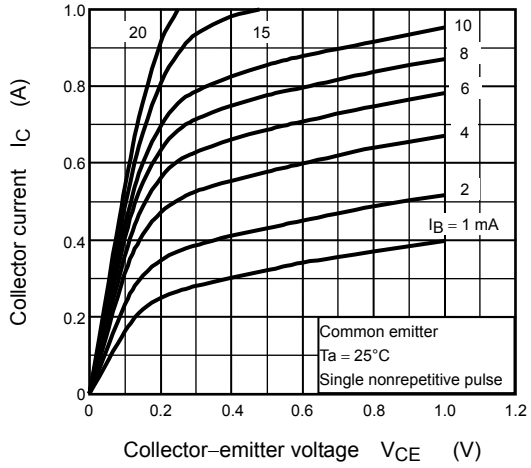


Figure 4. Switching Time Test Circuit & Timing Chart

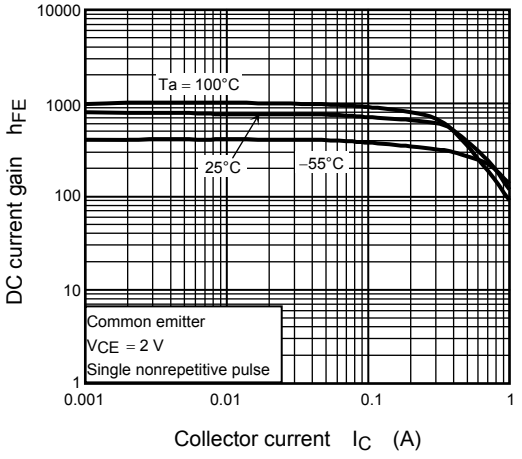


NPN

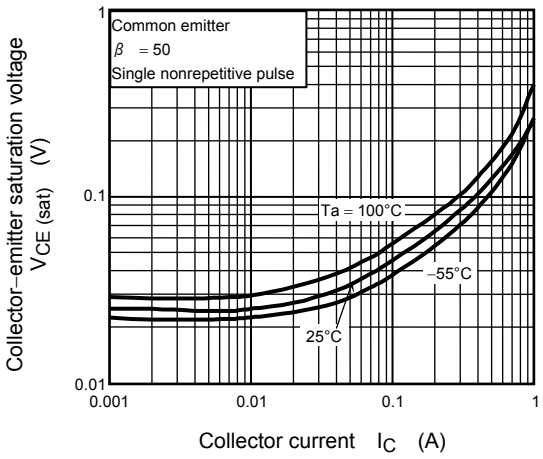
$I_C - V_{CE}$



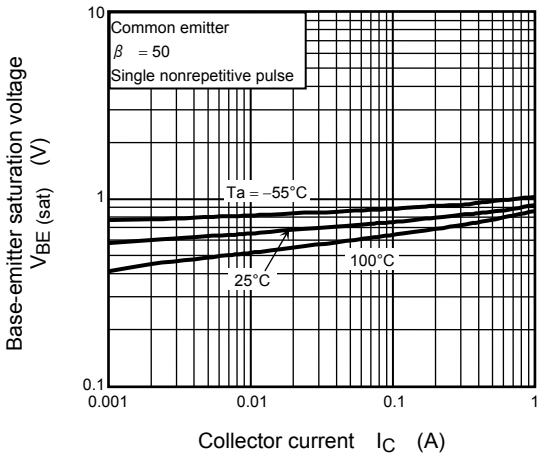
$h_{FE} - I_C$



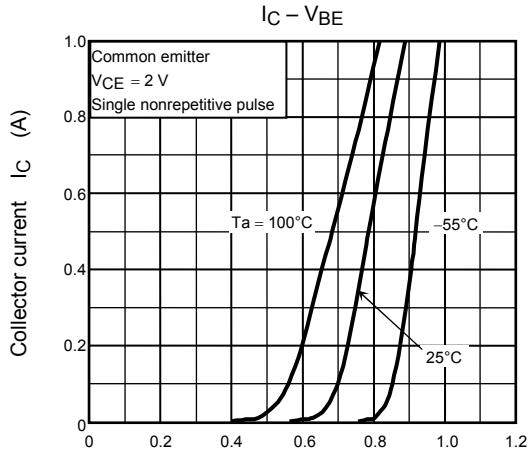
$V_{CE\ (sat)} - I_C$



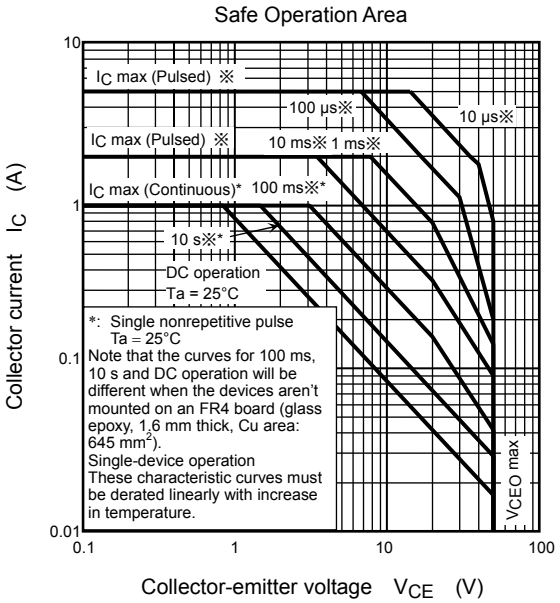
$V_{BE\ (sat)} - I_C$



$I_C - V_{BE}$

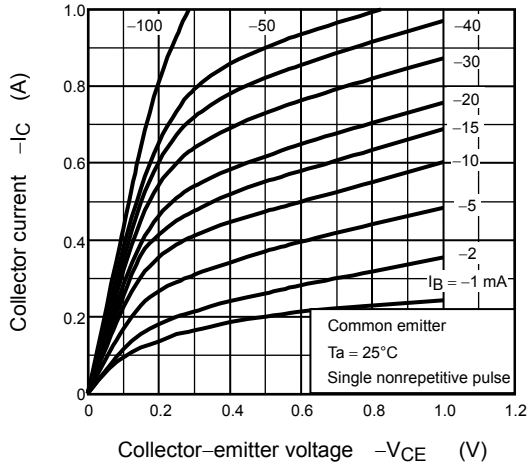


Safe Operation Area

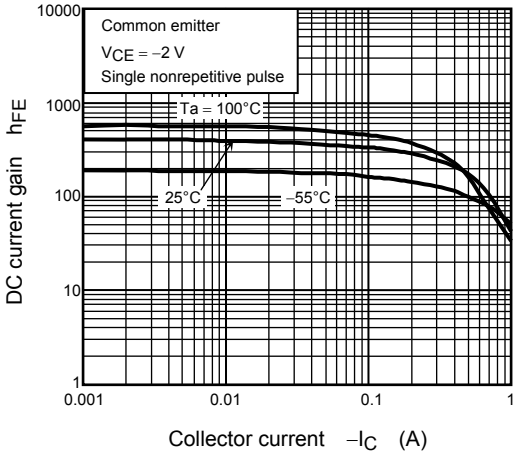


PNP

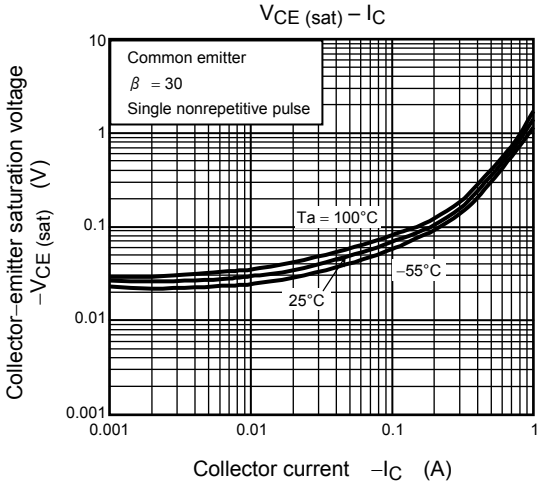
$I_C - V_{CE}$



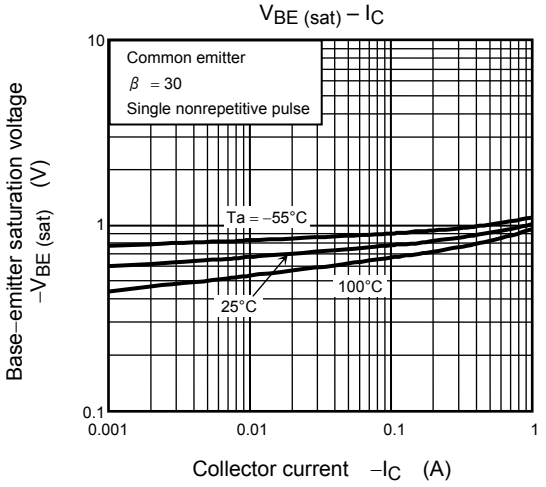
$h_{FE} - I_C$



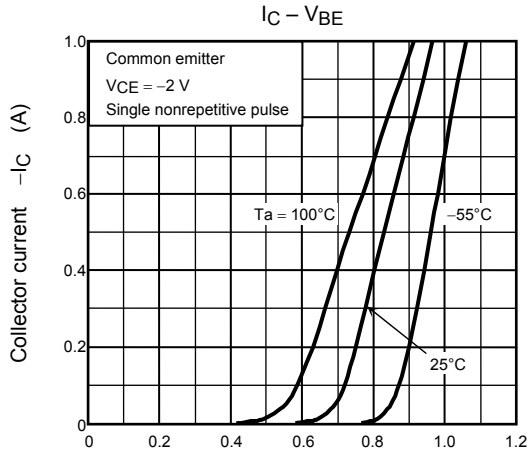
$V_{CE\ (sat)} - I_C$



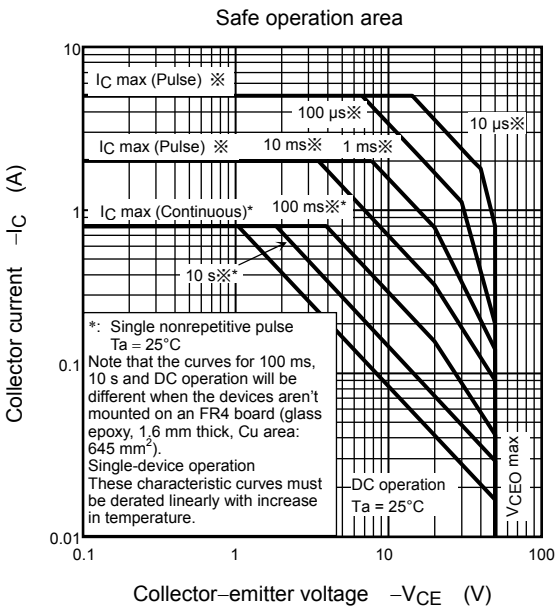
$V_{BE\ (sat)} - I_C$



$I_C - V_{BE}$

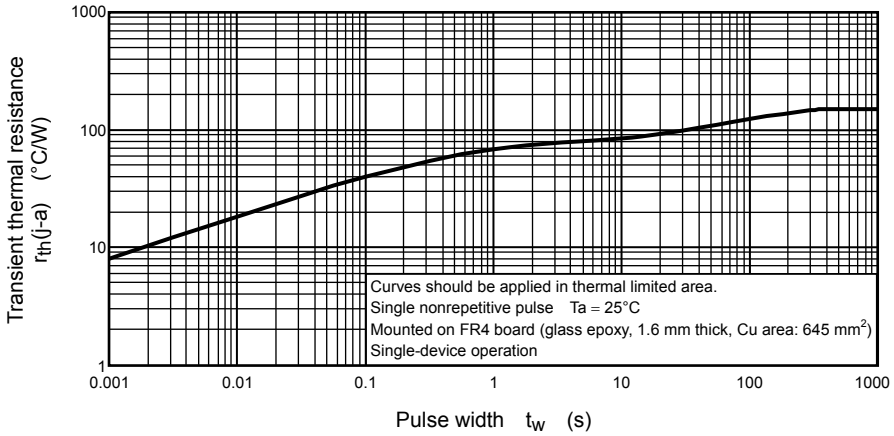


Safe operation area

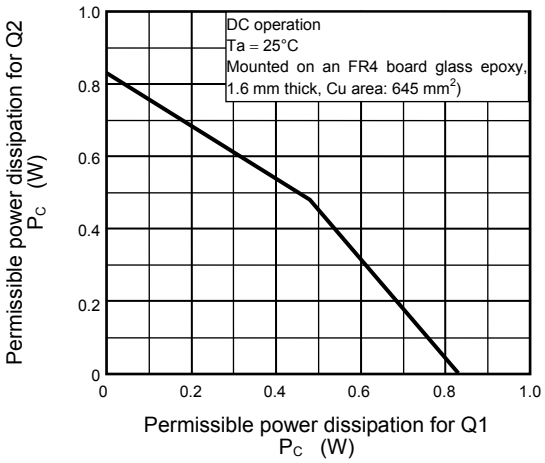


Common

$r_{th} - t_w$



Permissible Power Dissipation for Simultaneous Operation



Collector power dissipation at the single-device operation is 0.83W.
Collector power dissipation at the single-device value at dual operation is 0.48W.
Collector power dissipation at the dual operation is set to 0.96W.

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